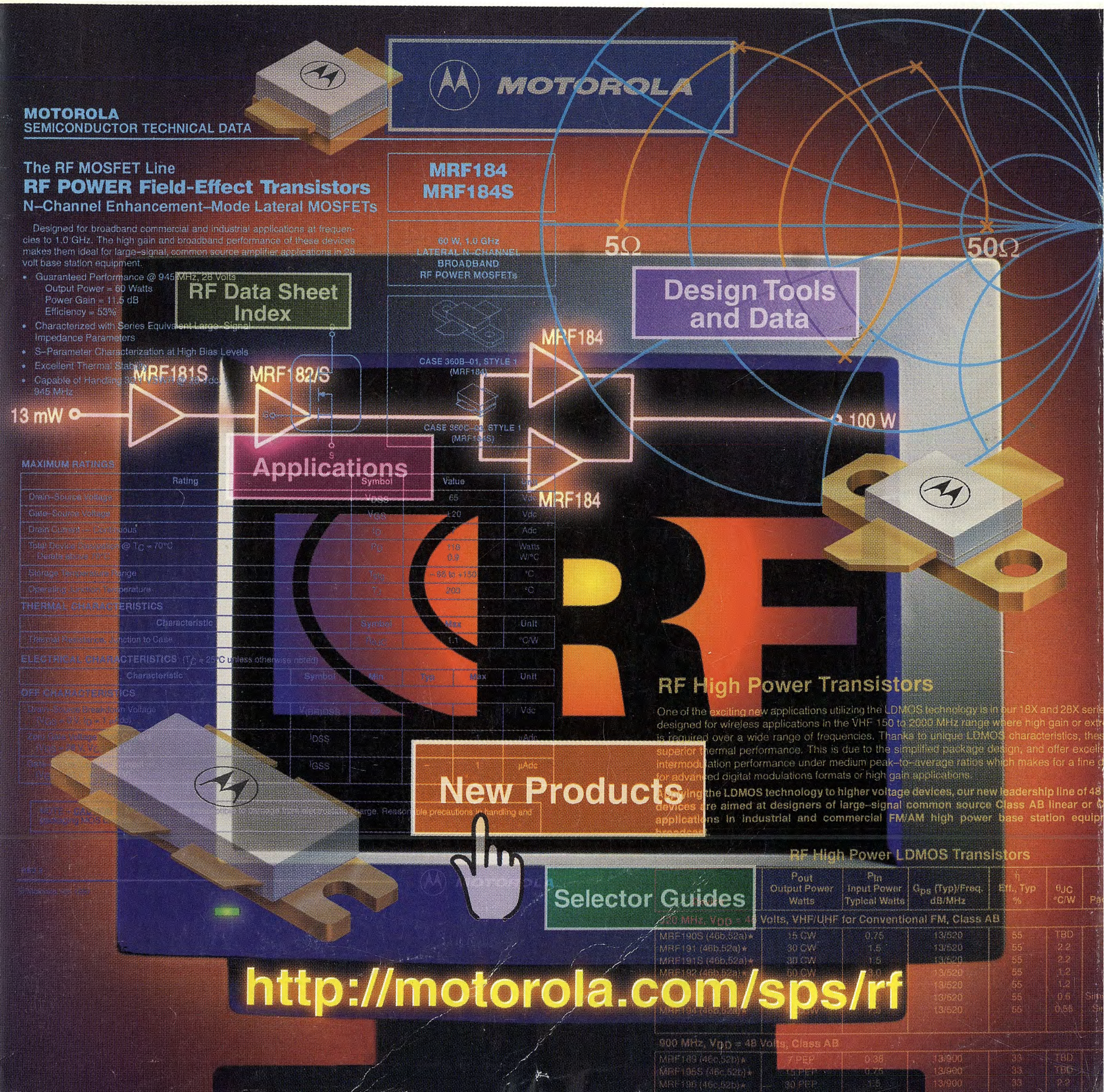
MOTOROLA

DL110/D
REV 8

RF
Device Data



MOTOROLA

RF Device Data

Table of Contents

In Brief . . .

This publication presents technical information for the several product families that comprise the Motorola portfolio of RF Products. The product families include bipolar, LDMOS, MOSFET RF Power, and gallium arsenide chip technologies in a variety of ceramic and plastic surface mount packages. Discrete components, hybrid modules, and integrated circuits provide different levels of complexity in an effort to provide RF solutions to our customers' RF needs.

This edition encompasses a considerable number of changes that have occurred since our last printing. Some devices have been removed from this book due to package changes or new technology replacements and many new devices have been added.

All devices are in alphanumeric order in the **Device Index** of this book. Just turn to the appropriate page for technical details of the known device. If you need to identify a device that meets your functional performance requirements of frequency, output power, gain, or other parameters, then utilize the **Selector Guide** section of the book.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. Please consult your nearest Motorola Semiconductor sales office for further assistance regarding any aspect of Motorola RF Products.

Remember

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274.

Printed in U.S.A.

ABOUT THIS REVISION

- The RF Device Data Book is contained in one volume. Application notes are contained in the RF Application Reports handbook which is available through the Motorola Literature Distribution Center by ordering HB215/D. Phone and fax numbers for ordering literature are listed on the back cover of this book.

- New Products introduced since our last printing have been added to the portfolio.

- Some devices have been removed due to package changes and newer technology.

- The Tuning, Hot Carrier, and PIN Diode Data Sheet information can be obtained by contacting the Signal Products Division's Product Marketing organization.

- For Cross Reference information on Motorola replacement devices, please consult your local Distributor or Motorola Sales Office. See Section Six in this data book for a complete listing of Motorola Distributor and Worldwide Sales Offices.

DATA CLASSIFICATION

ADVANCE INFORMATION

Data sheets herein contain information on new products. Specifications and information are subject to change without notice.

FORMAL

For a fully characterized device, there must be devices in the warehouse and price authorization.

MOTOROLA

How to Access RF Data On–line!

Use Motorola's M*fax*™

M*fax* offers access to over 30,000 Motorola documents for faxing to customers worldwide. With menus and voice instruction, customers can request the documents needed using their own touch–tone telephones from any location 7 days a week and 24 hours a day.

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Or access RF information directly on the Internet and use the following URL to stay current with Motorola RF new product data, up–to–date selector guides, applications information, data sheets and much more.

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And use the Motorola SPS World Marketing Internet Server to access other Motorola Semiconductor Product data.

Motorola SPS's Electronic Data Delivery organization has set up a World Wide Web Server to deliver Motorola SPS's technical data to the global Internet community.

After accessing the Internet, to locate the Motorola SPS World Marketing server, use the following URL:

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The SPS World Marketing Server provides you with instant access to data sheets, selector guide information, package outlines, on–line technical support and much more.

RF DEVICE INDEX

RF DEVICE INDEX — continued

Section One

Selector Guide

While Motorola is considered to be the supermarket for semiconductor products, there is not a category in which the selection is more diverse, or more complete, than in products designed for RF system applications. From MOS, bipolar power and signal transistors to integrated circuits, Motorola's RF components cover the entire spectrum from HF to microwave to personal communications. Yet, product expansion continues — not only to keep pace with the progressive needs of the industry, but to better serve the needs of designers for a reliable and comprehensive source of supply.

How to Use This Selector Guide

The products in this guide are separated FIRST into major categories such as Power FETs, Power Bipolar, Medium Power Transistors, Small Signal, Monolithic Integrated Circuits, Power Amplifier Modules and CATV Distribution Amplifiers. SECOND, within each category parts are listed by frequency band, except for medium power transistors, small signal transistors and monolithic integrated circuits, which are divided by application. Small signal transistor applications are low noise, linear amplifiers, switches, and oscillators. Monolithic integrated circuit application groupings are switching, receiver functions and transmitter functions. THIRD, within a frequency band, transistors are further grouped by operating voltage and, finally, output power.

To Replace Devices in an Existing Design

Call your local Motorola Sales Office or Distributor to determine Motorola's closest replacement device.

Remember

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274.

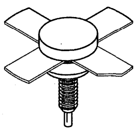
Page

Motorola RF Discrete Transistors

In the following pages, the reader will find the most extensive group of RF Discrete Transistors offered by any semiconductor manufacturer anywhere in the world today.

From Bipolar to FET, from Low Power to High Power, the user can choose from a variety of packages. They include plastic, metal can and ceramic that are microstrip circuit compatible or surface mountable. Many are designed for automated assembly equipment.

Major sub–headings are MOSFETs, Power Bipolar and Small Signal.



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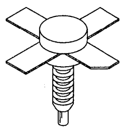

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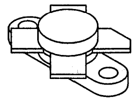

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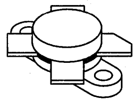

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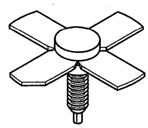

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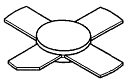

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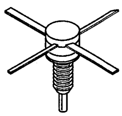

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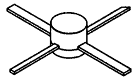

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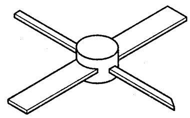

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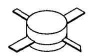

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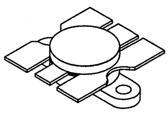

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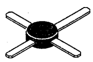

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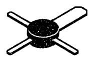

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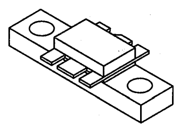

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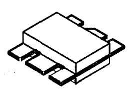
(CS–12)



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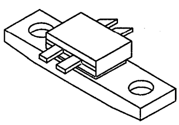

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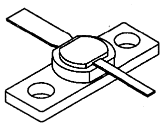

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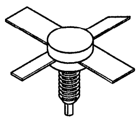

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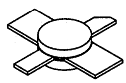

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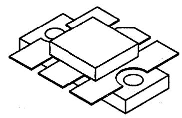

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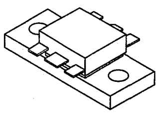

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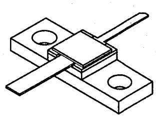

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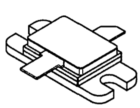

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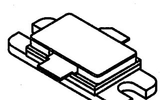

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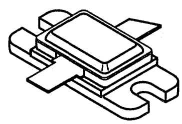

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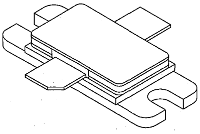

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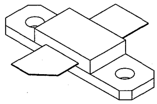

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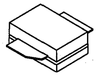

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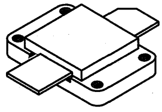

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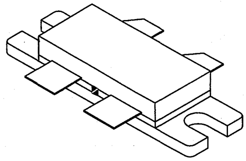
(HOG PAC)



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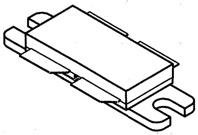

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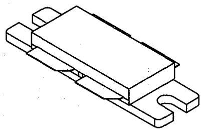

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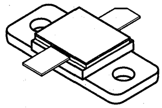

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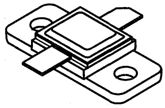

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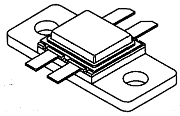

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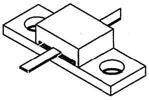

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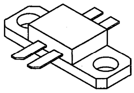

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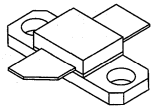

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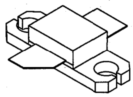

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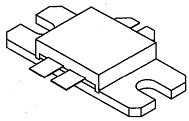

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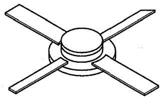

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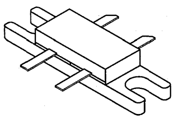

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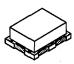

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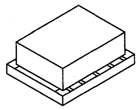

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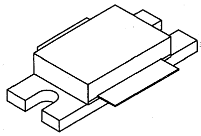

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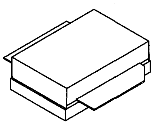

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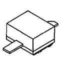

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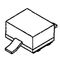

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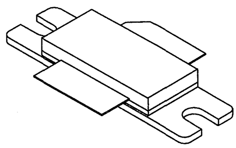

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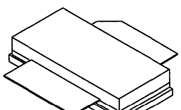

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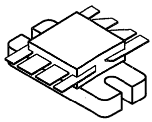

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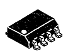


CASE 751
STYLE 1
(SO–8)

RF Power MOSFETs

Motorola RF Power MOSFETs are constructed using a planar process to enhance manufacturing repeatability. They are *N–channel field effect transistors* with an oxide insulated gate which controls vertical current flow.

Compared with bipolar transistors, RF Power FETs exhibit higher gain, higher input impedance, enhanced thermal stability and lower noise. The FETs listed in this section are specified for operation in RF Power Amplifiers and are grouped by frequency range of operation and type of application. Arrangement within each group is first by order of voltage then by increasing output power.

Table 1. To 54 MHz

Designed for broadband HF/SSB commercial and industrial applications. The high gain, broadband performance and linear characterization of this device makes it ideal for large–signal, common–source amplifier applications in 12.5 volt mobile and amateur radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	Typical IMD d_3 dB	d_5 dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 Volts, Class AB								
MRF255	55	0.8	16/54	45	–30	–30	1.0	211–11/2

Table 2. To 150 MHz HF/SSB

For military and commercial HF/SSB fixed, mobile and marine transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} Typical Gain dB @ 30 MHz	Typical IMD d_3 dB	d_{11} dB	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB							
MRF140	150	4.7	15	–30	–60	0.6	211–11/2
MRF171A(46a)	30	0.45	19	–32	—	1.52	211–07/2
V_{DD} = 50 Volts, Class AB							
MRF148	30	0.5	18	–35	–60	1.5	211–07/2
MRF150	150	3	17	–32	–60	0.6	211–11/2
MRF154	600	12	17	–25	—	0.13	368/2
MRF157	600	6	20	–25	—	0.13	368/2

(46)To be introduced: a) 4Q97; b) 1Q98

RF Power MOSFETs (continued)

Table 3. To 225 MHz VHF AM/FM

For VHF military and commercial aircraft radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Efficiency Typical %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB						
MRF134	5	0.2	14/150	55	10	211–07/2
MRF136	15	0.38	16/150	60	3.2	211–07/2
MRF136Y	30	1.2	14/150	54	1.8	319B/1
MRF137	30	0.75	16/150	60	1.8	211–07/2
MRF171A[46a]	45	0.56	19/150	65	1.52	211–07/2
MRF173	80	4	13/150	65	0.8	211–11/2
MRF173CQ	80	4	13/150	65	0.8	316–01/2
MRF175LV	100	4	14/225	65	0.65	333/1
MRF174	125	8.3	11.8/150	60	0.65	211–11/2
MRF141	150	15	10/175	55	0.6	211–11/2
MRF175GV	200	8	14/225	65	0.44	375/2
MRF141G	300	30	10/175	55	0.35	375/2
V_{DD} = 50 Volts, Class AB						
MRF151	150	7.5	13/175	45	0.6	211–11/2
MRF176GV	200	4	17/225	55	0.44	375/2
MRF151G	300	7.5	16/175	55	0.35	375/2

Table 4. To 500 MHz VHF/UHF AM/FM

For VHF/UHF military and commercial aircraft radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB						
MRF158	2	0.02	20/400	55	13.2	305A/2
MRF160	4	0.08	17/400	50	7.2	249/3
MRF166C	20	0.4	17/400	55	2.5	319/3
MRF166W	40	2	13/400	50	1.0	412/1
MRF175LU	100	10	10/400	55	0.65	333/1
MRF177	100	6.4	12/400	60	0.65	744A/2
MRF175GU	150	9.5	12/400	55	0.44	375/2
MRF275L[46a]	100	12.5	9/500	55	0.65	333/2
MRF275G★	150	11.9	11/500	55	0.44	375/2
V_{DD} = 50 Volts, Class AB						
MRF176GU	150	6	14/400	50	0.44	375/2

[46]To be introduced: a) 4Q97; b) 1Q98

★New Product

RF Power MOSFETs (continued)

Table 5. To 520 MHz

Designed for broadband VHF & UHF commercial and industrial applications. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 12.5/7.5 volt mobile, portable and base station operation.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	$θ_{JC}$ °C/W	Package/Style
V_{CC} = 7.5 Volts, Class AB						
MRF5003,R1[18a]	3	0.27	10.5/512	50	14	430/2
MRF5007,R1[18a]	7	0.5	11.5/512	55	5	430B/1
V_{CC} = 12.5 Volts, Class AB						
MRF5015	15	1.1	11.5/512	55	3.5	319/3
MRF5035	35	6.3	7.5/512	55	1.8	316–01/3
520 MHz, V_{DD} = 48 Volts, VHF/UHF for Conventional FM, Class AB – LDMOS Die						
MRF190S[46a,52b]	15 CW	0.75	13/520	55	TBD	TBD
MRF191[46a,52b]	30 CW	1.5	13/520	55	2.2	360B/1
MRF191S[46a,52b]	30 CW	1.5	13/520	55	2.2	360C/1
MRF192[46a,52b]	60 CW	3.0	13/520	55	1.2	360B/1
MRF192S[46a,52b]	60 CW	3.0	13/520	55	1.2	360B/1
MRF193[46a,52b]	120 CW	6.0	13/520	55	0.6	Similar to 375B/2
MRF194[46a,52b]	150 CW	7.5	10/520	50	0.55	Single–ended Device

Table 6. To 900 MHz

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	$θ_{JC}$ °C/W	Package/Style
900 MHz, V_{DD} = 48 Volts, Class AB – LDMOS Die						
MRF189[46a,52b]	7 PEP	0.38	13/900	33	TBD	TBD
MRF195S[46a,52c]	15 PEP	0.75	13/900	33	2.5	458/1
MRF196[46a,52c]	30 PEP	1.5	13/900	33	2.2	360B/1
MRF196S[46a,52c]	30 PEP	1.5	13/900	33	2.2	360C/1
MRF197[46a,52c]	60 PEP	3.0	13/900	33	1.2	360B/1
MRF197S[46a,52c]	60 PEP	3.0	13/900	33	1.2	360C/1
MRF198[46a,52c]	90 PEP	4.5	13/900	33	1.0	Single–ended Device
MRF199[46a,52c]	150 PEP	15	10/900	33	0.55	Single–ended Device

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.

(46)To be introduced: a) 4Q97; b) 1Q98

(52)Engineering samples available: a) 3Q97; b) 4Q97; c) 1Q98

Table 7. To 1.0 GHz

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	$θ_{JC}$ °C/W	Package/Style
1.0 GHz, V_{DD} = 26 Volts, Class AB – LDMOS Die						
MRF6522–5(46a)	5	0.06	19/960	55	15	458A/1
MRF6522–10(46a)	10	0.16	18/960	55	6.0	458A/1
1.0 GHz, V_{DD} = 28 Volts, Class AB – LDMOS Die						
MRF181S(46a)	4	0.16	14/1000	40	3.6	458/1
MRF181Z(46b)	4	0.16	14/1000	40	3.6	458A/1
MRF182	30	1.2	14/1000	60	1.75	360B/1
MRF182S★	30	1.2	14/1000	60	1.75	360C/1
MRF183	45	1.8	14/1000	60	1.5	360B/1
MRF183S★	45	1.8	14/1000	60	1.5	360C/1
MRF184★	60	1.9	15/1000	60	1.1	360B/1
MRF184S★	60	1.9	15/1000	60	1.1	360C/1
MRF185 (3)★	85	3.4	14/1000	55	0.7	375B/2
MRF186(3,46a)	120	7.6	12/1000	55	0.6	375B/2

Table 8. To 1.6 GHz

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	$θ_{JC}$ °C/W	Package/Style
1.6 GHz, V_{DD} = 28 Volts, Class AB, Characterized for INMARSAT Uplinks–LDMOS Die						
MRF3010(46b)	10	0.9	10.5/1600	55	3.6	360B/1

(3)Internal Impedance Matched Push-Pull Transistors

(46)To be introduced: a) 4Q97; b) 1Q98

★New Product

RF Power Bipolar Transistors

Motorola's broad line of bipolar RF power transistors are characterized for operation in RF power amplifiers. Typical applications are in base stations, military and commercial landmobile, avionics and marine radio transmitters. Groupings are by frequency band and type of application. Within each group, the arrangement of devices is by major supply voltage rating, then in the order of increasing output power. All devices are NPN polarity except where otherwise noted.

HF Transistors

Table 1. 1.5 – 30 MHz, HF/SSB

Designed for broadband operation, these devices feature specified Intermodulation Distortion at rated power output. Applications include mobile, marine, fixed station, and amateur HF/SSB equipment, operating from 12.5, 13.6, 28, or 50 volt supplies.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 30 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 or 13.6 Volts, Class AB					
MRF421	100 PEP/CW	10	10	0.6	211–11/1
V_{CC} = 28 Volts, Class AB					
MRF426	25 PEP/CW	0.16	22	2.5	211–07/1
MRF422	150 PEP/CW	15	10	0.6	211–11/1
V_{CC} = 50 Volts, Class AB					
MRF429	150 PEP/CW	7.5	13	0.8	211–11/1
MRF448	250 PEP/CW	15.7	12	0.6	211–11/1

Table 2. 14 – 30 MHz, CB/Amateur Band

These HF transistors are designed for economical, high–volume use in CW, AM and SSB applications.

V_{CC} = 12.5 or 13.6 Volts, Class AB

MRF455	60	3	13	1	211–07/1
MRF454	80	5	12	0.7	211–11/1

Table 3. 27 – 50 MHz, Low–Band FM Band

For use in the FM "Low–Band," for Mobile communications.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 50 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 or 13.6 Volts, Class AB					
MRF492	70	5.6	11	0.7	211–11/1

VHF Transistors

Table 4. 30 – 200 MHz Band

Designed for Military Radio and Commercial Aircraft VHF bands, these 28–volt devices include the all–gold metallized MRF314/16/17 high–reliability series.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class AB					
MRF314	30	3	10/150	2.2	211–07/1
MRF316(2)	80	8	10/150	0.8	316–01/1
MRF317(2)	100	12.5	9/150	0.65	316–01/1

(2)Internal Impedance Matched

VHF Transistors (continued)

Table 5. 136 – 174 MHz High Band

The "workhorse" VHF FM High–Band is served by Motorola with the broadest range of devices and package combinations in the industry.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 175 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 Volts, Class C					
MRF4427R2(18b)	1	0.016	18(19)	125(1)	751/1
MRF553	1.5	0.11	11.5	25	317D/2
MRF2628	15	0.95	12	4	244/1
MRF1946	30	3	10	1.6	211–07/1
MRF1946A	30	3	10	1.8	145A–09/1
MRF240	40	5	9	2.2	145A–09/1
MRF247(2)	75	15	7	0.7	316–01/1

UHF Transistors

Table 6. 100 – 400 MHz Band

Stringent requirements of the UHF Military band are met by MRF325, 326, 327, 329 and 2N6439 types, with all–gold metal systems, specified ruggedness and programmed wirebond construction, to assure consistent input impedances for internally matched parts.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min) Gain @ 400 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class C					
MRF325(2)	30	4.3	8.5	2.2	316–01/1
MRF326(2)	40	5	9	1.6	316–01/1
2N6439(2)	60	10	7.8	1.2	316–01/1
MRF327(2)	80	14.9	7.3	0.7	316–01/1
MRF329(2)	100	20	7	0.7	333/1
MRF392(3)	125	19.8	8	0.7	744A/1

Table 7. 400 – 500 MHz Band

Similar to the 100–400 MHz transistors, these devices have bandwidth capabilities operating up to 500 MHz. All have nitride passivated die, gold metal systems, specified ruggedness and controlled wirebond construction to meet the stringent requirements of military space applications.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class C					
MRF313	1	0.03	15/400	28.5	305A/1
MRF321	10	0.62	12/400	6.4	244/1
MRF323	20	2	10/400	3.2	244/1
MRF338(2)	80	15	7.3/470	0.7	333/1
MRF393(3)	100	18	7.5/500	0.7	744A/1

(1) $R_{\theta JA}$. Thermal Resistance Junction to Ambient.

(2) Internal Impedance Matched

(3) Internal Impedance Matched Push-Pull Transistors

(18) Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.

(19) Typical

Table 8. 470 – 512 MHz Band

Higher power output devices in this UHF power transistor series feature internally input–matched construction, are designed for broadband operation, and have guaranteed ruggedness under output mismatch and RF overdrive conditions. Devices are specified for handheld, mobile and base station operation.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 Volts, Class C					
MRF581(4)	0.6	0.03	13/500	40	317/2
MRF555	1.5	0.15	10/470	25	317D/2
MRF652	5	0.5	10/512	7	244/1
MRF652S	5	0.5	10/512	7	249/1
MRF653	10	2	7/512	4	244/1
MRF641(2)	15	2.5	7.8/470	4	316–01/1
MRF654(2)	15	2.5	7.8/512	4	244/1
MRF644(2)	25	5.9	6.2/470	1.7	316–01/1
MRF650(2)	50	15.8	5.0/512	1.3	316–01/1
MRF658(2)	65	25	4.15/512	1	316–01/1

900 MHz Transistors

Table 9. 870 – 960 MHz Band

Designed specifically for the 900 MHz mobile radio band, MRF840 through MRF847 devices offer superior gain and ruggedness, using the unique CS–12 package, which minimizes common–element impedance, and thus maximizes gain and stability. Devices are listed for mobile and base station applications.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 12.5 Volts — Class C — Si Bipolar					
MRF559(5)	0.5	0.08	8/870	50	317/2
MRF581(5)	0.6	0.06	10(19)/870	40	317/2
MRF8372R1,R2(5,18a,b)	0.75	0.11	8/870	45	751/1
MRF557(5)	1.5	0.23	8/870	25	317D/2
MRF840(2,6)	10	2.5	6/870	3.1	319/1
MRF842(2,6)	20	5	6/870	1.5	319/1
MRF847(2,6)	45	16	4.5/870	1	319/1

(2)Internal Impedance Matched
(4)Small signal gain. P_o is Typ.
(5)Common Emitter Configuration
(6)Common Base Configuration
(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.
(19)Typical

900 MHz Transistors (continued)

Table 9. 870 – 960 MHz Band (continued)

Device	P_{out} Output Power Watts	Class	P_{in}(Max) Input Power Watts	Gp (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 24 Volts — Si Bipolar						
MRF891	5	AB	0.63	9/900	7	319/2
MRF891S	5	AB	0.63	9/900	7	319A/2
MRF894(2)	30	C	6	7/900	1.5	319/1
MRF897(3)	30	AB	3	10/900	1.7	395B/1
MRF897R(3)	30	AB	3	10.5/900	1.7	395B/1
MRF898(2)	60	C	12	7/900	1	333A/1
V_{CC} = 26 Volts — Si Bipolar						
MRF6409★	20	AB	26/50	10/960	3.8	319/2
MRF6414	50	AB	26/200	8.5/960	1.3	333A/2
MRF899(3)	150	AB	24	8/900	0.8	375A/1

1.5 GHz Transistors

Table 10. 1600 – 1640 MHz Band

Device	P_{out} Output Power Watts	Class	η Eff. (Min) %	Gp (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
MRA1600–002	2	C	40	8.4/1600	15	394/1
MRF16006	6	C	40	7.4/1600	6.8	395C/2
MRF16030	30	C	40	7.5/1600	1.7	395C/2

Microwave Transistors

Table 11. L–Band Pulse Power

These products are designed to operate in short pulse width, 10 µs, low duty cycle, 1%, power amplifiers operating in the 960–1215 MHz band. All devices have internal impedance matching. The prime application is avionics equipment for distance measuring (DME), area navigation (TACAN) and interrogation (IFF).

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_P (Min) Gain @ 1090 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 18 Volts — Class A & AB Common Emitter					
MRF1000MB	0.2	0.02	10	25	332A/2
V_{CC} = 35 Volts — Class B & C Common Base					
MRF1004MB	4	0.4	10	25	332A/1

(2)Internal Impedance Matched
(3)Internal Impedance Matched Push-Pull Transistors
★New Product

Table 11. L–Band Pulse Power (continued)

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_P (Min) Gain @ 1090 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 50 Volts — Class C Common Base					
MRF1015MB	15	1.5	10	10	332A/1
MRF1035MB	35	3.5	10	5	332A/1
MRF1090MA	90	9	10	0.6	332–04/1
MRF1090MB	90	9	10	0.6	332A/1
MRF1150MA	150	25	7.8	0.3	332–04/1
MRF1150MB	150	25	7.8	0.3	332A/1

Table 12. L–Band Long Pulse Power

These products are designed for pulse power amplifier applications in the 960–1215 MHz frequency range. They are capable of handling up to 10 µs pulses in long pulse trains resulting in up to a 50% duty cycle over a 3.5 millisecond interval. Overall duty cycle is limited to 25% maximum. The primary applications for devices of this type are military systems, specifically JTIDS and commercial systems, specifically Mode S. Package types are hermetic.

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_{PB} (Min) Gain @ 1215 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts — Class C Common Base					
MRF10005	5	0.71	8.5	8	336E/1
V_{CC} = 36 Volts — Class C Common Base					
MRF10031	30	3	10	3	376B/1
MRF10120	120	19	8	0.6	355C/1
V_{CC} = 50 Volts					
MRF10070	70	7	10(7)	0.4	376C/1
MRF10150	150	15	10(7)	0.25	376B/1
MRF10350	350	44	9(7)	0.11	355E/1
MRF10500	500	63	9(7)	0.12	355D/1
MRF10501	500	63	9(7)	0.12	355H/1

Table 13. 2 GHz Narrowband CW

The MRW2000 Series of NPN Silicon microwave power transistors are designed for common base service in amplifier or oscillator applications in the 1–2.3 GHz frequency range.

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_{PB} (Min) Gain @ 2 GHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts — Class B & C Common Base					
MRW2001	1	0.13	9	35	328A/1
MRW2003	3	0.48	8	15	328A/1

Table 14. 3 GHz Narrowband CW, Class B & C Common Base

The MRW3000 Series are the industry's first 100% VSWR tolerant 3 GHz devices. They are common–base configured in hermetic packages and rated for 28 volt operation.

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_{PB} (Min) Gain @ 3.0 GHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts					
MRW3001	1	0.2	7	35	328A/1
MRW3003	3	0.75	6	17	328A/1
MRW3005	5	1.6	5	8.5	328A/1

(7)Typical @ 1090 MHz

Linear Transistors

The following sections describe a wide variety of devices specifically characterized for linear amplification. Included are medium power and high power parts covering frequencies from 100 MHz–4 GHz.

Table 15. To 1 GHz, Class A

These devices offer a selection of performance and price for linear amplification to 1 GHz. The "MRA" prefix parts are input matched and feature high overdrive and extreme ruggedness capability.

Device	P_o @ 1 dB Comp. Point Watts	G_{SS} (Min)/Freq. Small Signal Gain dB/MHz	Bias Point (Vdc/A)	θ_{JC} °C/W	Package/Style
V_{CC} = 19 Volts					
MRA1000–3.5L	3.5	10/1000	19/0.6	8	145A–09/1
MRA1000–7L	7	9/1000	19/1.2	4	145D–02/1
MRA1000–14L	14	8/1000	19/2.4	2.1	145D–02/1

Device	P_{out} Output Power Watts	Gp (Min)/Freq. Power Gain dB/MHz	Bias Point Per Side (Vdc/MA)	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts					
MRA0510–50H	50	7/1000	28/120	1.4	391–01/1

Table 16. To 2 GHz, Class A

These parts offer low cost alternatives to matched devices used primarily as pre–drivers to 2 GHz.

Device	P_o @ 1 dB Comp. Point Watts	G_{SS} (Min)/Freq. Small Signal Gain dB/MHz	Bias Point (Vdc/A)	θ_{JC} °C/W	Package/Style
V_{CC} = 20 Volts					
MRF3094(9)	0.5	10.5/2000	20/0.12	40	328A/2
MRF3095(9)	0.8	9/2000	20/0.12	35	328A/2

Table 17. UHF Ultra Linear For TV Applications

The following devices have been characterized for ultra–linear applications such as low–power TV transmitters in Band IV and Band V. Each features diffused ballast resistors and an all–gold metal system to provide enhanced reliability and ruggedness.

Device	P_{ref}(Min) Watts	G_P (Min)/Freq. Small Signal Gain dB/MHz	3 Tone IMD(8) dB	θ_{JC} °C/W	Package/Style
V_{CC} = 20 Volts, Class A					
TPV596A	0.5	11.5/860	–58	20	244/1
TPV597	1	10.5/860	–58	9	244/1
TPV598	4	7/860	–60	5	244/1

Device	P_{out} Output Power Watts	Class	P_{in}(Max) Input Power Watts	Gp (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CE} = 24 Volts — Class A						
MRF857S	2.1 (CW)	A	0.4	12.5/900	8.4	305D/1
MRF858	3.6 (CW)	A	0.29	11/900	6.9	319/2
MRF858S	3.6 (CW)	A	0.29	11/900	6.9	319A/2
MRF859	6.5 W (CW)	A	0.46	11.5/900	3.9	319/2
MRF859S	6.5 W (CW)	A	0.46	11.5/900	3.9	319A/2

(8)Vision Carrier: – 8 dB; Sound Carrier: – 7 dB; Sideband Carrier: – 16 dB
(9)Former Prefix was "RF"

Linear Transistors (continued)

Table 17. UHF Ultra Linear For TV Applications (continued)

Device	P_{ref}(Min) Watts	G_P (Min)/Freq. Small Signal Gain dB/MHz	3 Tone IMD[8] dB	θ_{JC} °C/W	Package/Style
V_{CC} = 25 Volts, Class A					
TPV695A	14	9.5/860	–47	2.5	395B/1
TPV7025	25	8.5/860	–45	1.5	398/1
V_{CC} = 28 Volts, Class AB					
TPV8100B	100[11]	8.5/860	—	0.7	398/1

Table 18. Microwave Linear for PCN Applications

The following devices have been developed for linear amplifiers in the 1.5–2 GHz region and have characteristics particularly suitable for PDC, PCS or DCS1800 base station applications.

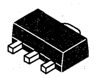
Device	P_{out} Watts	Class	Bias Point Vdc/mA	Gain (Typ)/Freq dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 20 Volts–Bipolar Die						
MRF6401[12]	0.5	A	20/80	10/1880	30	305C/1
V_{CC} = 26 Volts–Bipolar Die						
MRF6402[13]	4.5	AB	26/40	10/1880	5	319/2
MRF6404[16]	30	AB	26/150	8.5/1880	1.4	395C/1
MRF6408	12	AB	26/100	8.8/1880	2.8	395C/1
MRF15030	30	A, AB	26/125	9/1490	1.4	395C/1
MRF15060★	60	A, AB	26/200	10/1490	0.7	451/1
MRF15060S★	60	A, AB	26/200	10/1490	0.7	451A/1
MRF15090	90	A, AB	26/250	7.5/1490	0.7	375A/1
MRF20030★	30	A, AB	26/120	10.5/2000	1.4	395D/1
MRF20060★	60	A, AB	26/200	9.4/2000	0.7	451/1
MRF20060S★	60	A, AB	26/200	9.4/2000	0.7	451A/1
MRF20120[46b]	120	AB	26/500	9.5/2000	0.35	TBD
V_{DD} = 26 Volts–LDMOS Die						
MRF280S[46b]	2	A, AB	26/15	16/2000	10	458/1
MRF280Z[46b]	2	A, AB	26/15	16/2000	10	458A/1
MRF281S[46b]	4	A, AB	26/25	13.6/2000	8.75	458/1
MRF281Z[46b]	4	A, AB	26/25	13.6/2000	8.75	458A/1
MRF6525–5[46a]	5	AB	26/70	11.5/2000	15	458A/1
MRF6525–10[46a]	10	AB	26/130	10/2000	6.0	458A/1
MRF282S★	10	A, AB	26/75	13/2000	2.9	458/1
MRF282Z★	10	A, AB	26/75	13/2000	2.9	458A/1
MRF284 ★	30	A, AB	26/200	11.5/2000	2.0	360B/1
MRF284S★	30	A, AB	26/200	11.5/2000	2.0	360C/1
MRF286[46a]	60	A, AB	26/500	11.4/2000	.73	465/1
MRF286S[46a]	60	A, AB	26/500	11.4/2000	.73	465A/1

(8)Vision Carrier: – 8 dB; Sound Carrier: – 7 dB; Sideband Carrier: – 16 dB
(11)Output power at 1 dB compression in Class AB
(12)Formerly known as "TP4001S"
(13)Formerly known as "TP4004"
(16)Formerly known as "TP4035"
(46)To be introduced: a) 4Q97; b) 1Q98
★New Product

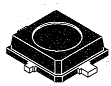
Motorola RF Medium Power Transistors

RF Medium Power Transistors are used in portable transmitter applications and low voltage drivers for higher power devices. They can be used for analog cellular, GSM and the newer digital handheld cellular phones. GaAs, LDMOS and Bipolar devices are available. RF Medium Power Transistors are supplied in industry standard SOT packages as well as Motorola's high performance PLD line of surface mount power RF packages. Other applications include talkback pagers, wireless modems and LANs, cable modems, highspeed drivers and instrumentation.

CASE 318A
STYLE 7, 8
(SOT–143)



CASE 345–03
STYLE 8, 9
(SOT–89)



CASE 449
(PLD–1)

RF Medium Power Transistors

Discrete Wireless Transmitter Devices

Device	Freq. MHz	V_{DD} V	Typical Output Power dBm	Typical Drain Eff. %	Typical Gain dB	Semiconductor Technology	Package
3.5 V Applications							
MRF9822T1(18f)★	850	3.5	31.0	70	11	GaAs PHEMT	PLD–1
4.8 V Applications							
MRF9242T1(18f,46a)	900	4.8	31.5	65	9.5	LDMOS	PLD–1
MRF9282T1(18f,46a)	900	4.8	34.0	60	8	LDMOS	PLD–1
5.8 V Applications							
MXR9745T1(18f)★	850	5.8	31.5	60	8.5	LDMOS	SOT–89
MXR9745RT1(18f)★	850	5.8	31.5	60	8.5	LDMOS	SOT–89
MRF9251T1(18c,46a)	900	5.8	23.5	60	10.5	LDMOS	SOT–143
MRF9811T1(18c)★	900	5.8	22	60	15	GaAs MAFET	SOT–143
MRF9745T1(18f)★	900	5.8	30	55	10	LDMOS	PLD–1

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.

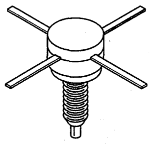
(46)To be introduced: a) 4Q97; b) 1Q98

★New Product

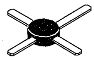
Motorola RF Small Signal Transistors

Motorola's broad line of RF Small Signal Transistors includes NPN and PNP Silicon Bipolar Transistors characterized for low noise amplifiers, mixers, oscillators, multipliers, non–saturated switches and low–power drivers.

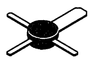
These devices are available in a wide variety of package types: plastic Macro–X, ceramic and surface mounted. Most of these transistors are fully characterized with s–parameters.



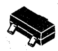
CASE 244A
STYLE 1



CASE 317
STYLE 2
(MACRO–X)



CASE 317D
STYLE 2
(POWER MACRO)

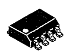


CASE 318–08
STYLE 6
(SOT–23)

CASE 318A
STYLE 1, 11
LOW PROFILE
(SOT–143)

CASE 419
STYLE 3
(SC–70/SOT–323)

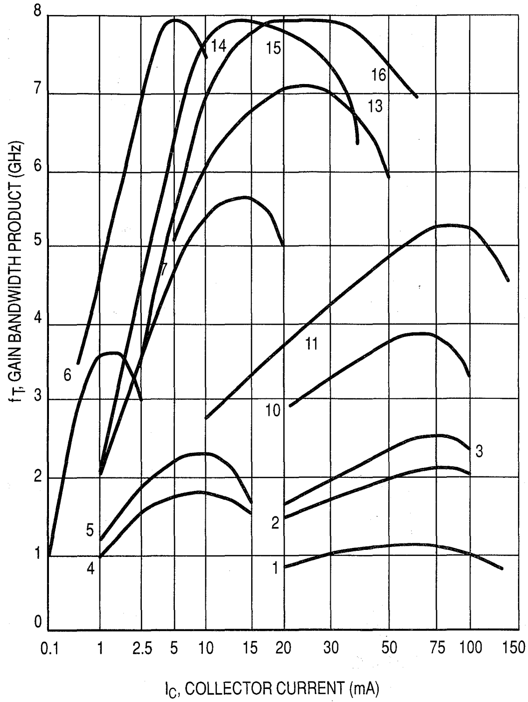
CASE 419B
STYLE 16, 17
(SC–70ML/SOT–323)



CASE 751
STYLE 1
(SO–8)

RF Small Signal Transistors

RF Small Signal Transistor Gain Characteristics



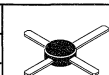
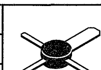
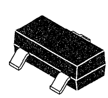
Curve numbers apply to transistors listed in the subsequent tables.

Selection by Package

In small–signal RF applications, the package style is often determined by the end application or circuit construction technique. To aid the circuit designer in device selection, the Motorola broad range of RF small–signal amplifier transistors is organized by package. Devices for other applications such as oscillators or switches are shown in the appropriate preceding tables. **These devices are NPN polarity unless otherwise designated.**

Plastic Packages

Table 1. Plastic

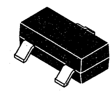
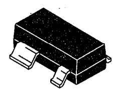
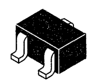
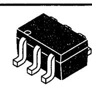
Device	Gain–Bandwidth @ f_T Typ GHz	I_C mA	Curve No. Page 1–18	NF_{min} @ f Typ dB	MHz	Gain @ f Typ dB	MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	Package
Case 317/2 — MACRO–X										
MRF571	8	50	12	1.5	1000	12	1000	10	70	
MRF559	3	100	10	—	—	13	512	18	150	
MRF581	5	75	11	2	500	15.5	500	18	200	
Case 317D/2										
MRF553	—	—	—	—	—	13	175	16	500	
MRF555	—	—	—	—	—	12.5	470	16	400	
MRF557	—	—	—	—	—	9	870	16	400	
Case 318–08/6 — SOT–23										
MMBR521LT1(17,18c)	3.4	–35	—	1.5	500	15	500	–10	–70	
MMBR5031LT1(18c)	1	5	—	2.5	450	17	450	10	20	
BFS17LT1(18c)	1.3	25	—	—	—	—	—	15	—	
BFR92ALT1(18c)	4.5	14	—	—	—	15	—	15	25	
MMBR901LT1(18c)	4	15	7	1.9	1000	12	1000	15	30	
BFR93ALT1(18c)	3.4	30	—	2.5	30	—	—	12	35	

(17)PNP

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.

Selection by Package (continued)

Table 1. Plastic (continued)

Device	Gain–Bandwidth @		Curve No. Page 1–18	NF_{min} @ f		Gain @ f		Maximum Ratings		Package
	f_T Typ GHz	I_C mA		Typ dB	MHz	Typ dB	MHz	$V_{(BR)CEO}$ Volts	I_C mA	
Case 318–08/6 — SOT–23 (continued)										
MMBR5179LT1(18c)	1.4	5	4	—	—	15	200	12	50	
MMBR941LT1(18c)	8	15	15	2.1	2000	8.5	2000	10	50	
MMBR941LT3(18d)	8	15	15	2.1	2000	8.5	2000	10	50	
MMBR941BLT1(18c)	8	15	15	2.1	2000	8.5	2000	10	50	
MMBR911LT1(18c)	6	30	8	2	500	17	500	12	60	
MMBR571LT1(18c)	8	50	12	2	500	16.5	500	10	80	
MMBR951LT1(18c)	8	30	16	2.1	2000	7.5	2000	10	100	
MMBR951ALT1(18c)	8	30	16	2.1	2000	7.5	2000	10	100	
Case 318A/1 — SOT–143										
MRF5711LT1(18c)	8	50	12	1.6	1000	13.5	1000	10	70	
MRF5211LT1(17,18c)	4.2	–50	—	2.8	1000	11	1000	–10	–70	
MRF9411LT1(18c)	8	15	15	2.1	2000	9.5	2000	10	50	
MRF5811LT1(18c)	5	75	11	2.0	500	18.4	500	18	200	
MRF9511LT1(18c)	8	30	16	2.1	2000	9	2000	10	100	
Case 419/3 — SC–70/SOT–323										
MRF917T1(18c)★	6	20	8	2.3	1000	10	1000	12	60	
MRF577T1(18c)★	7	40	12	1.5	1000	10	1000	10	80	
MRF927T1(18c)	8	5	14	1.7	1000	9.8	1000	10	10	
MRF927T3(18d)	8	5	14	1.7	1000	9.8	1000	10	10	
MRF947T1(18c,d)	8	15	15	2.1	2000	10.5	1500	10	50	
MRF947AT1(18c)	8	15	15	2.1	2000	10.5	1500	10	50	
MRF947BT1(18c,d)	8	15	15	2.1	2000	10.5	1500	10	50	
MRF957T1(18c)	8	30	16	2.0	2000	9	1500	10	100	
Case 419B–01 — SC–70ML/SOT–363										
MRF2947AT1(18c)★	8	15	15	1.5	1000	14	1000	10	50	
MRF2947RAT1(18c)★	8	15	15	1.5	1000	14	1000	10	50	

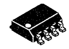
(17)PNP

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.

★New Product

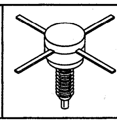
Selection by Package (continued)

Table 1. Plastic (continued)

Device	Gain–Bandwidth @ f_T Typ GHz	I_C mA	Curve No. Page 1–18	NF_{min} @ f Typ dB	MHz	Gain @ f Typ dB	MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	Package
Case 751/1 — SO–8										
MRF3866R2[18b]	0.8	50	1	—	—	10.5	400	30	400	
MRF5812R1,R2[18a,b]	5.5	75	11	2	500	15.5	500	15	200	
MRF8372R1,R2[18a,b]	5	75	11	—	—	10	870	16	200	

Ceramic SOE Case

Table 2. Ceramic SOE Case

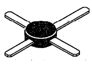
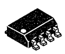
Device	Gain–Bandwidth @ f_T Typ GHz	I_C mA	Curve No. Page 1–18	N @ f Typ dB	MHz	Gain @ f Typ dB	MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	Package
Case 244A/1										
MRF587	5.5	90	11	3	500	13	500	15	200	

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.

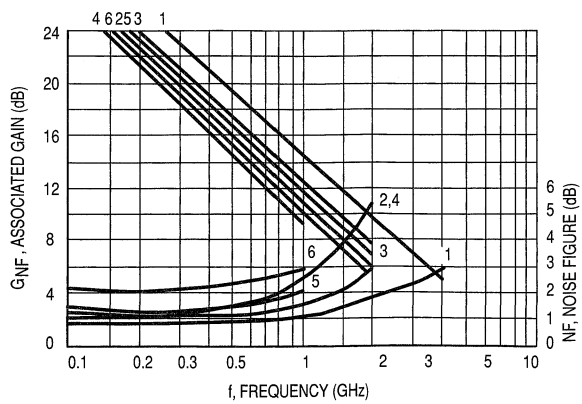
Selection by Application

Table 3. Low Noise

The Small–Signal devices listed are designed for low noise and high gain amplifier mixer, and multiplier applications. Each transistor type is available in various packages. **Polarity is NPN unless otherwise noted.**

Package	Name	Case Number	Curve Number (See figure below)					
			1	2[17]	3	4	5	6
	MACRO–X	317/2	—	—	MRF571	MRF581	—	—
	SOT–23	318–08/6	MMBR941LT1 MMBR941LT3 MMBR941BLT1 MMBR951LT1[20]	MMBR521LT1	MMBR571LT1	—	MMBR901LT1	MMBR911LT1
	SC–70/ SOT–323	419/3	MRF917T1 MRF577T1 MRF927T1 MRF927T3 MRF947AT1 MRF947T1 MRF947BT1 MRF957T1[20]	—	—	—	—	—
	SC–70ML/ SOT–363	419B/ 16, 17	MRF2947AT1 MRF2947RAT1	—	—	—	—	—
	SOT–143	318A/1	MRF9411LT1 MRF9511LT1[20]	MRF5211LT1	MRF5711LT1	MRF5811LT1	—	—
	SO–8	751/1	—	—	—	MRF5812R1,R2	—	—

(17)PNP
(20)Higher Current Version



Gain and Noise Figure versus Frequency

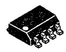
Table 4. CATV, MATV and Class A Linear

For Class A linear CATV/MATV applications. Listed according to increasing gain bandwidth (f_T).

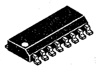
Device	Nominal Test Conditions V_{CE}/I_C Volts/mA	f_T Typ MHz	Noise Figure Typ/Freq. dB/MHz	Distortion Specifications 3rd Order IMD dBc	Distortion Specifications Output Level dBmV	$V_{(BR)CEO}$ V	Package/ Style
MMBR5179LT1[18c]	6/5	1500	4/450			12	318–08/6
MMBR5031LT1[18c,d]	6/5	2000	1.9/450			10	318–08/6
MRF5812R1,R2[18a,b]	10/75	5000	1.8/500	−65	+50	15	751/1
MRF581	10/75	5000	2.7/300	−65	+50	18	317/2
MRF587	15/90	5500	3/500	−72	+50	17	244A/1

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.

CASE 318A–05
(SOT–143)

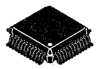


CASE 751
(SO–8)

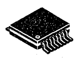


CASE 751B
(SO–16)

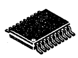
CASE 846A
(MICRO–8)



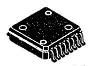
CASE 932
(TQFP–48)



CASE 948C
(TSSOP–16)



CASE 948D
(TSSOP–20)



CASE 978
(PFP–16)

Motorola RF Monolithic Integrated Circuits

Motorola's RF monolithic integrated circuit devices provide an integrated solution for the personal communications market. These devices are available in plastic SOIC–8, SOIC–16, SOT–143, TSSOP–16, Micro–8, TSSOP–20, TQFP–48 or PFP–16 packages.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

RF Monolithic Integrated Circuits

Switching

Antenna Switches/Local Oscillator Switches

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current µA (Typ)	P_{in}, 1 dB Compression dBm (Typ)	TX Insertion Loss dB (Typ)	Isolation dB (Typ)	Package	System Applicability
MRFIC1801(18b)	1500–2500	2.7–5.5	300	29	0.6	20	SO–8	DECT, PHS, PCS, ISM
MRFIC0903(18b)★	100–2000	2.7–5.0	60	35.5	0.65	21	SO–8	AMPS, Class 4 & 5 GSM, DCS1800, PHS, PCS
MRFIC0921(18a,46a)	100–1000	2.7–5.5	300	16	0.6	22	Micro–8	AMPS, CT1, CT2, GSM, IS–54, ISM, DECT, PHS, PDC

Receiver Functions

General Purpose Integrated Circuits

General Purpose Cascode Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain @ 900 MHz dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC0915(18c,46a)	100–2000	2.7–5.0	2.2	16.5	1.9	38	SOT–143	AMPS, CT1, CT2, GSM, IS–54, ISM, DECT, PHS, PCS
MRFIC0916(18c)★	100–2000	2.7–5.0	4.7	18.5	1.9	44	SOT–143	AMPS, CT1, CT2, GSM, IS–54, ISM, DECT, PHS, PCS

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	Input Third Order Intercept	Package	System Applicability
MRF9820T1(18c)★	100–1500	2–5	1.0	16	–3	SOT–143	AMPS, CT1, CT2, GSM, IS–54, ISM, DECT, PHS, PCS

900 MHz Front End

LNA + Mixer

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	Output Level, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC2001(18b)	500–1000	0–250	2.7–5.0	4.7	23	–10	SO–8	CT2, ISM

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.

(46)To be introduced 2nd half of 1996.

★New Product

1.5 – 2.2 GHz Front End

Integrated LNA

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC1501(18b)★	1000–2000	3–5	5.7	18	1.1	26	SO–8	GPS
MRFIC1808(18b)★	1700–2100	2.7–4.5	5.0	17	1.6	37	SO–8	DECT, PHS, PCS
MRFIC1808DM(18b,46a)	1700–2100	2.7–4.5	5.0	17	1.6	32	Micro–8	DECT, PHS, PCS

GPS Receiver

MRFIC1502★	1570–1580	4.5–5.5	50	65	9.5	—	TQFP–48	GPS

Integrated LNA/Downconverter

Device	RF Freq. Range GHz	IF Freq. Range GHz	Supply Volt. Range Vdc	Supply Current RX Mode mA (Typ)	Mixer Conv. Gain dB (Typ)	LNA Gain dB (Typ)	LNA Noise Figure dB (Typ)	Package	System Applicability
MRFIC1804(18b)	1.8–2.0	70–325	2.7–3.3	10	4	14	2.3	SO–16	DECT,PHS,PCS
MRFIC1814(18b,46a)	1.8–2.0	70–325	2.7–4.5	10	5	17	2.5	TSSOP–16	DECT,PHS,PCS

2.4 GHz Front End

Integrated LNA/Downconverter

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Conv. Gain dB (Typ)	LNA Noise Figure dB (Typ)	Isolation Lo to RF, Lo to IF dB (Typ)	Package	System Applicability
MRFIC2401(18b)	2400–2500	100–350	4.75–5.25	9.5	21	1.9	20	SO–16	WLAN, MMDS, ISM

Transmitter Functions

General Purpose Integrated Circuits

Quadrature Modulator

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Gain Control dB (Typ)	Lo Leakage dBm (Typ)	SSB P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC0001(18b)	50–260	2.7–5.5	10	30	–55	–10	TSSOP–20	DCS1800, GSM, NADC PDC, PHS, PCS1900

General Purpose Cascode Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain @ 900 MHz dB (Typ)	Noise Figure dB (Typ)	Reverse Isolation dB (Typ)	Package	System Applicability
MRFIC0915(18c,46a)	100–2000	2.7–5.0	2.2	16.5	1.9	38	SOT–143	AMPS,CT1,CT2,GSM,IS–54, ISM,DECT,PHS,PCS
MRFIC0916(18c)★	100–2000	2.7–5.0	4.7	18.5	1.9	44	SOT–143	AMPS,CT1,CT2,GSM,IS–54, ISM,DECT,PHS,PCS

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.
(46)To be introduced: a) 4Q97; b) 1Q98
★New Product

900 MHz Transmit Chain

Transmit Mixer

Device	RF Freq. Range MHz	IF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current µA (Typ)	Conv. Gain dB (Typ)	Output Level, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC2002(18b)	500–1000	0–250	2.7–5.0	5.5	0.1	10	–18	SO–8	AMPS,CT1,CT2, GSM, IS–54, ISM
MRFIC2101(18b)	800–1000	0–250	3–4.75	45	2	26.5	4.5	SO–16	AMPS,CT1,CT2, GSM, IS–54, ISM, USPCS, CDMA
MRFIC0931(18b)★	500–2000	0–250	2.7–4.8	38	—	25	1.0	SO–8	AMPS,CT1,CT2, GSM, IS–54, ISM, USPCS, CDMA

Driver Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	Gain Control dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2004(18b)	800–1000	2.7–4.0	11	0.7	21.5	34	–1	SO–16	AMPS,CT1,CT2, GSM,ISM
MRFIC2006(18b)	500–1000	1.8–4.0	46	—	23	—	15.5	SO–8	AMPS,CT1,CT2, GSM,ISM
MRFIC0904(18b)★	800–1000	2.7–5.0(47)	280	0.05	27	24.5	25.5	SO–16	AMPS,GSM,ISM

Integrated Power Amplifiers

Low Power 900 MHz Power Amplifiers

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Return Loss Input/Output dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	Semiconductor Technology
MRFIC2006(18b)	500–1000	1.8–4.0	46	23	15	15.5	SO–8	Silicon

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	Semiconductor Technology
MRFIC2101(18b)	800–1000	3 – 4.75	38	2	16	18	SO–16	Silicon

Analog Cellular

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC0910(18e,46a)	824–905	4.8	50	17.8	–40	30.8/13	PFP–16	LDMOS
MRFIC0912(18e)★	824–905	4.6(47)	55	23.8	–25	30.8/7	PFP–16	GaAs
MRFIC0923(18e,46b,52b)	824–905	3.6	50	17.8	–40	30.8/13	PFP–16	LDMOS

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.
(46)To be introduced: a) 4Q97; b) 1Q98
(47) Negative supply required
(52)Engineering samples available: a) 3Q97; b) 4Q97; c) 1Q98
★New Product

GSM Cellular

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC0913(18e)★	880–915	4.8(47)	48	24.5	–30	34.5/10	PFP–16	GaAs
MRFIC0917(18e,46a)	880–915	3.6(47)	43	22	–30	34/12	PFP–16	GaAs

DCS1800, PCS1900

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Min)	Package	Semiconductor Technology
MRFIC1818(18e)★	1.7–1.9	4.8(47)	35	30	–30	33/3	PFP–16	GaAs
MRFIC1817(18e,46a)	1.7–1.9	3.6(47)	35	27	–30	32/5	PFP–16	GaAs

Two–way Paging, ISM

Device	Freq. Range MHz	Supply Volt. Vdc	Power Added Efficiency % (Min)	Power Gain dB (Min)	Harmonic Output 2fo dBc	P_{out}/P_{in} dBm (Typ)	Package	Semiconductor Technology
MRFIC0914(18b)★	890–950	4.8	35	28	–45	30.5/2.5	SO–16	LDMOS

1.5 – 2.2 GHz Transmit Chain

Upconverter

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	Supply Current TX Mode mA (Typ)	Standby Current µA (Typ)	Conv. Gain dB (Typ)	Recommended IF Input MHz (Typ)	P_{out}, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC1803(18b)	1.7–2.5	2.7–3.3	28	100	10	70–350	–2	SO–16	DECT,PHS, PCS
MRFIC1813(18b)★	1.7–2.5	2.7–4.5	25	100	15	70–350	3	TSSOP–16	CDMA,PCS
MRFIC0931(18b)★	500–2000	2.7–4.8	38	—	20	0–250	–2	SO–8	CDMA,PCS

Power Amplifier

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc(47)	Supply Current mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	P_{out}/P_{in} dBm (Typ)	1 dB Comp. dBm (Typ)	Pkg	System Applicability
MRFIC1805(18b)★	1.7–2.5	2.7–5.0	170	—	21	21.5/2	24	TSSOP–16	DECT,PHS, PCS
MRFIC1806(18b)	1.5–2.5	3.0–5.0	115	0.25	23	19.5/–3	21	SO–16	DECT,PHS, PCS
MRFIC1807(18b)	1.5–2.2	3.0–5.0	325	0.06	8	26.8/20	25	SO–16	DECT,PHS, PCS

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.

(46)To be introduced: a) 4Q97; b) 1Q98

(47) Negative supply required

★New Product

Power Amplifier

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	PA Supply Current TX Mode mA (Typ)	Standby Current mA (Typ)	Small Signal Gain dB (Typ)	Insertion Loss Rx Mode dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC1807(18b) (Including TX/RX Switch)	1.5–2.2	3.0–5.0	325	0.06	8	1	25	SO–16	DECT, PHS, PCS

2.4 GHz Transmit Chain

Exciter Amplifier

Device	Freq. Range GHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Noise Figure dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2404(18b)	2.0–3.0	4.75–5.25	9	17	4.3	5	SO–8	WLAN, MMDS, ISM

Power Amplifier

Device	Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Small Signal Gain dB (Typ)	Power Control Range dB (Typ)	P_{out}, 1 dB Compression dBm (Typ)	Package	System Applicability
MRFIC2403(18b)	2200–2700	4.75–5.25	95	23	20	19	SO–16	WLAN, MMDS, ISM

Upconverter

Device	RF Output Freq. Range GHz	Supply Volt. Range Vdc	Supply Current TX Mode mA (Typ)	Standby Current µA (Typ)	Conv. Gain dB (Typ)	Recommended IF Input MHz (Typ)	P_{out}, 1 dB Comp. dBm (Typ)	Package	System Applicability
MRFIC1803(18b)	1.7–2.5	2.7–5.0	28	100	10	70–350	–2	SO–16	WLAN, ISM
MRFIC1813(18b)★	1.7–2.5	2.7–4.5	25	100	15	70–350	3	TSSOP–16	WLAN, ISM

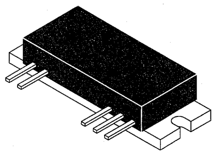
(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.

★New Product

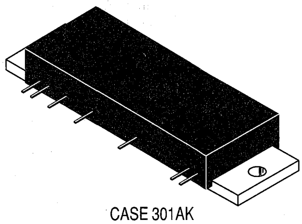
Motorola RF Amplifier Modules

Motorola's line of RF amplifiers designed and specified for use in land mobile radios and general purpose wideband amplification applications. They feature small size, matched inputs and outputs, high stability and guaranteed performance specifications. For the user, they offer the benefits of smaller and less complex system designs in less time and at lower overall cost.

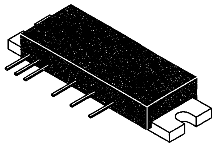
Each amplifier uses modern transistor chips which are gold metallized and have silicon nitride passivation for increased reliability and long life. Chip and wire construction features MOS capacitors and laser trimmed nichrome resistors. Circuit substrates and metallization have been selected for optimum performance cost and reliablity.



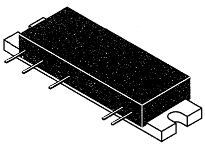
CASE 301AB
STYLE 1



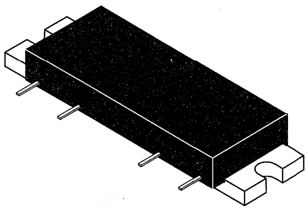
CASE 301AK
STYLE 1



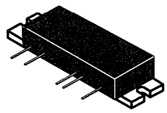
CASE 301AL
STYLE 1



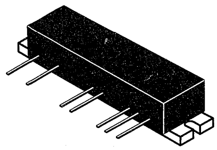
CASE 301AN
STYLE 1



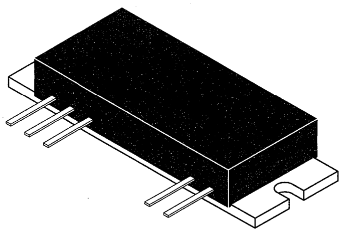
CASE 301AP
STYLE 1



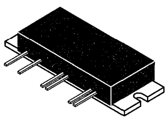
CASE 301E
STYLE 1



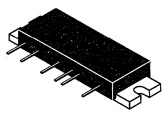
CASE 301F
STYLE 1



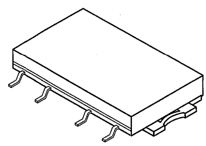
CASE 301G
STYLE 1



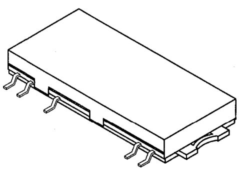
CASE 301K
STYLE 3



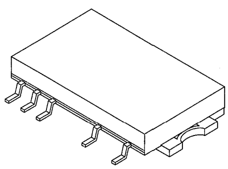
CASE 301V
STYLE 1



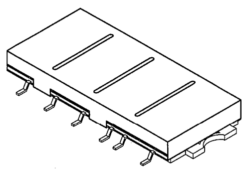
CASE 420AB
STYLE 1



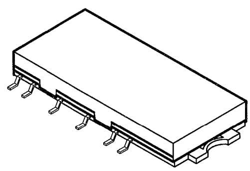
CASE 420AC
STYLE 1



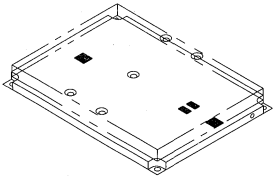
CASE 420J
STYLE 1



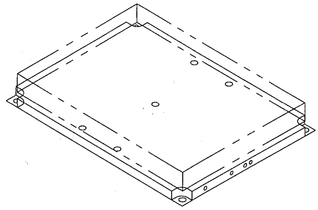
CASE 420L
STYLE 1



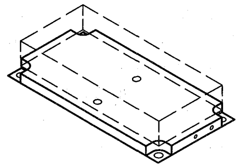
CASE 420Z
STYLE 1



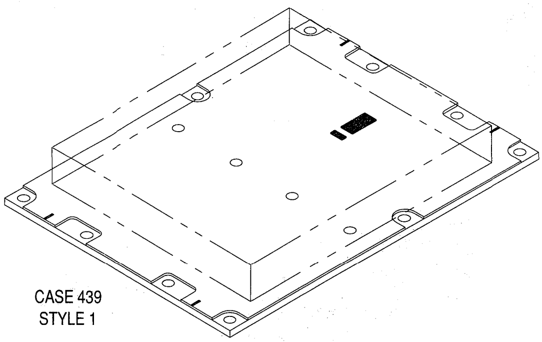
CASE 429A
STYLE 1



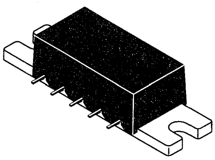
CASE 429C
STYLE 1



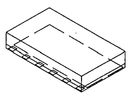
CASE 429E
STYLE 1



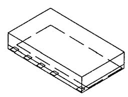
CASE 439
STYLE 1



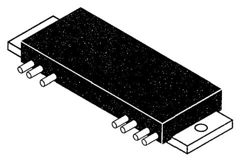
CASE 448
STYLE 1, 2



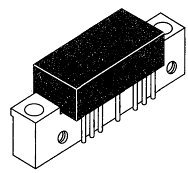
CASE 467
STYLE 1



CASE 467A
STYLE 1



CASE 700
STYLE 2



CASE 714F
STYLE 1

RF Amplifier Modules

Complete amplifiers with 50 ohm in/out impedances are available for a variety of applications including land mobile radios, base stations, TV transmitters and other uses requiring large–signal amplification, both linear and Class C. Frequencies covered range from 68–1990 MHz with power levels extending to 180 watts.

Land Mobile/Portable

The advantages of small size, reproducibility and overall lower cost become more pronounced with increasing frequency of operation. These amplifiers offer a wide range in power levels and gain, with guaranteed performance specifications for bandwidth, stability and ruggedness.

Table 1. VHF/UHF, Class C

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/Style
68–210 MHz, VHF Band — Class C (Silicon Bipolar Die)						
MHW105	5	0.001	68–88	37	7.5	301K/3

136–174 MHz, VHF Band — (LDMOS Die)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
MHW2607–1(46a)	7	0.001	136–174	38.5	7.5	301AN/1
MHW2627–1(46a)	7	0.02	136–174	25.5	7.5	420AC/1
MHW2627–2(46a)	7	0.02	216–234	25.5	7.5	420AC/1

380–470 MHz, Land Mobile Linear (for TransEuropean Trunked Radio – TETRA) — Class AB — (LDMOS Die)

Device	P_{sat} Watts	ACP (P_{out} = 1.6 W @ f_o ±25 kHz, 18 kHz BW) (dBc)	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
MHW2701–1★	4.5	–30	380–430	28	7	420Z/1
MHW2701–2(46b)	4.5	–30	420–470	28	7	420Z/1

380–470 MHz, Land Mobile Linear (for TransEuropean Trunked Radio – TETRA) — Class AB — (LDMOS Die)

Device	P_{sat} Watts	ACP (P_{out} = 5 W @ f_o ±25 kHz, 18 kHz BW) (dBc)	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
MHW2703(46b)	10	–30	380–400	28	7	420Z/1
MHW2723(46b)	12	–30	380–470	30	12.5	420Z/1

400–512 MHz, UHF Band — Class C (Silicon Bipolar Die)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/Style
MHW720A1(22)	20	0.15	400 – 440	21	12.5	700/2
MHW720A2(22)	20	0.15	440 – 470	21	12.5	700/2

(22)Designed for Wide Range P_{out} Level Control
(46)To be introduced: a) 4Q97; b) 1Q98
★New Product

Table 1. VHF/UHF, Class C (continued)

400–520 MHz, UHF Band — Class D – A (Dynamic Bias via Gate Control) — (LDMOS Die)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
MHW2707–1★	7	0.001	400–440	38.5	7.5	301AL/1
MHW2707–2(46a)	7	0.001	440–470	38.5	7.5	301AL/1
MHW2707A1★	7	0.001	400–470	38.5	7.5	301AL/1
MHW2707A2(46a)	7	0.001	470–520	38.5	7.5	301AL/1
MHW2717–1(46a)	7	0.02	400–470	25.5	7.5	420J/1
MHW2717–2(46a)	7	0.02	450–520	25.5	7.5	420J/1
MHW2727–1(46a)	7	0.02	400–470	25.5	7.5	420AC/1
MHW2727–2(46a)	7	0.02	450–520	25.5	7.5	420AC/1
MHW2727–3★	7	0.02	350–400	25.5	7.5	420AC/1

806–821 MHz, UHF Band (for Integrated Digital Enhanced Network – iDEN™)— Class AB — (LDMOS Die)

MHW2801 (46a)	0.8	0.00025	806–821	35	6	420L/1

806–960 MHz, UHF Band — Class C (Silicon Bipolar Die)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/Style
MHW803–2	2	0.001	806–870	33	7.5	301E/1
MHW804–1	4	0.001	800–870	36	7.5	301F/1

806 – 960 MHz, UHF Band — Class AB (LDMOS Die)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
MHW2803(46a)	3.5	0.001	806–824	35.5	6	420L/1
MHW2805–1(46a)	5	0.004	806–870	31	7.5	420AB/1
MHW2805–2(46a)	5	0.004	890–950	31	7.5	420AB/1
MHW2820–1(46b)	20	<0.250	806–870	19	12.5	301G/1(42)
MHW2820–2(46b)	18	<0.300	890–950	17.9	12.5	301G/1(42)
MHW2821–1★	20	<0.250	806–870	19	12.5	301AB/1
MHW2821–2★	18	<0.300	890–950	17.9	12.5	301AB/1

1710 – 1785 MHz, DCS Band — (GaAs FET Die)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/Style
MIM1801(18h,46b,52a)	2.0	0.006	1710–1785	28	3.6	TBD
MIM1802(18h,46b,52a)	2.0	0.006	1710–1785	28	4.8	TBD

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) T1 = 1,500 units.
(42)Drop–in for bipolar MHW820
(46)To be introduced: a) 4Q97; b) 1Q98
(52)Engineering samples available: a) 3Q97; b) 4Q97; c) 1Q98
★New Product

Table 2. UHF, Linear

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/Style
824–849 MHz (for Amps) — Class AB (LDMOS Silicon FET)						
MIM2901(46a)	1.41	0.004	824–849	25.5	3.6	TBD
880–915 MHz (for GSM) — Class AB (Silicon Bipolar Die)						
MHW953(22)	3.5	0.001	890–915	35.4	7.2	301V/1

880–915 MHz (for GSM) — Class AB (LDMOS Silicon FET)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
MIM2906(46a)	3.5	0.316	890–915	30.5	6	467A/1
MIM2908(46a)	3.2	0.002	880–915	32	4.8	467/1

925–960 MHz (for GSM) — Class AB (LDMOS Silicon FET)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/Style
MHW910(46a)	10	0.050	925–960	23	24	301AB/1
MHW913	14	0.1	880–915	21.5	12.5	301AB/1
MHW916	16	0.036	925–960	26.5	26	301AB/1
MHW930(46a)	30	0.060	925–960	27	26	301AB/1

1805–1880 MHz (for DCS1800) — Class AB (Silicon Bipolar Die)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/Style
MHW1815★	15.0	0.015	1805–1880	30	26	301AK/1
1930–1990 MHz (for PCS1900) — Class AB (Silicon Bipolar Die)						
MHW1915★	15.0	0.019	1930–1990	29	26	301AK/1
MHW1916★	15.0	0.013	1930–1990	31	26	301AK/1

(22)Designed for Wide Range P_{out} Level Control
(46)To be introduced: a) 4Q97; b) 1Q98
★New Product

Wideband Linear Amplifiers

Table 1. Cellular Base Station Pre–Drivers

These 50 ohm amplifiers are recommended for modern, multi–tone, CDMA and/or TDMA base–station pre–driver applications. Their high third–order intercept, tight phase control and excellent group delay characteristics make these amplifiers ideal for use in high–power feedforward loops.

Ultra–Linear – Class A (Silicon Bipolar Die)

Device	BW MHz	V_{CC} (Nom.) Volts	I_{CC} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm/MHz	NF (Typ) dB	Case/ Style
MHL9125	800–960	15	700	20	0.5	31	43	7.5	448/2
MHL9128	800–960	28	400	20	0.5	31	43	7.5	448/1

Ultra–Linear – Class A (LDMOS Die)

Device	BW MHz	V_{DD} (Nom.) Volts	I_{DD} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm/MHz	NF (Typ) dB	Case/ Style
MHL9236(46a)	800–960	26	525	30	.1	34	47	4.5	301AP/1

Table 2. Standard 50 Ohm Linear Hybrids

This series of RF linear hybrid amplifiers have been optimized for wideband, 50 ohm applications. These amplifiers were designed for multi–purpose RF applications where linearity, dynamic range and wide bandwidth are of primary concern. Each amplifier is available in various package options. The MHL series utilizes a new case style that provides microstrip input and output connections.

Device	BW MHz	V_{CC} (Nom.) Volts	I_{CC} (Nom.) mA	Gain/Freq. (Typ) dB/MHz	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept Point/Freq. (Typ) dBm/MHz	NF/Freq. (Typ) dB/MHz	Case/ Style
CA2832C	1–200	28	435	35.5/100	0.5	33	47/200	5/200	714F/1
CA2830C	5–200	24	300	34.5/100	0.5	29	46/200	4.7/200	714F/1
CA2818C	.35–400	24	205	18.5/50	0.5	30	45/200	5/200	714F/1
CA2842C	10–400	24	230	22/100	0.5	30	44/300	4/100	714F/1
CA2810C	10–450	24	310	34/50	1.5	30	43/300	5/300	714F/1
MHL8118	40–1000	28	400	17.5/900	1	30	41.5/1000	8.5/1000	448/1
MHL8115	40–1000	15	700	17.5/900	1	30	41.5/1000	8.5/1000	448/2
MHL8018	40–1000	28	210	18.5/900	1	26	38.5/1000	7.5/1000	448/1
MHL8015	40–1000	15	380	18.5/900	1	26	38.5/1000	7.5/1000	448/2

TV Transmitters

Table 3. UHF Ultra Linear for TV Applications

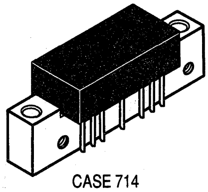
These amplifiers are characterized for ultra–linear applications in Band IV and Band V TV transmitters.

Device	Frequency MHz	P_{ref} Watts	G_P (Min)/Freq. Power Gain dB/MHz	3 Tone(8) IMD 1 dB	3 Tone(25) IMD 2 dB	V_{CC} Volts	Class	Package/Style
MRFA2600(26)	470–860	20	10.5/860	–50	–52.5	26.5	A	429A/1
MRFA2602(28)	470–860	40	9/860	–50	–53	25.5	A	429C/1
RFA8090B	470–860	95(11)	8/860	—	—	28	AB	429E/1
MRFA2604	470–860	180(11)	8/860	—	—	28	AB	439/1

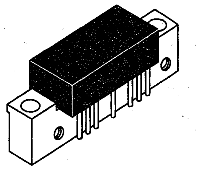
(8)Vision Carrier: – 8 dB; Sound Carrier: – 7 dB; Sideband Carrier: – 16 dB
(11)Output power at 1 dB compression in Class AB
(25)Vision Carrier: – 8 dB; Sound Carrier: – 10 dB; Sideband Carrier: – 16 dB
(26)Formerly known as "RFA6031"
(28)Formerly known as "RFA6060"
(46)To be introduced: a) 4Q97; b) 1Q98

Motorola RF CATV Distribution Amplifiers

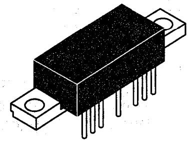
Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.



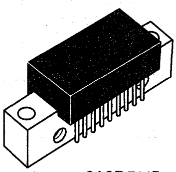
CASE 714
STYLE 1



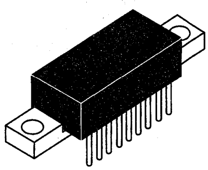
CASE 714F
STYLE 1



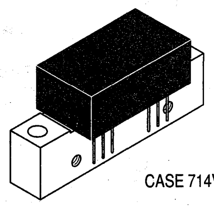
CASE 714G
STYLE 1



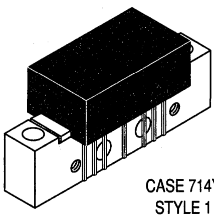
CASE 714P
STYLE 2, 3



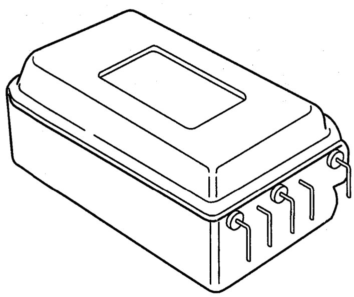
CASE 714T
STYLE 1, 2



CASE 714V



CASE 714Y
STYLE 1



CASE 825A
STYLE 2

CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

Forward Amplifiers

40–1000 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 152 CH	Cross Modulation dB 152 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
MHW9182	18	152	+38	−59[40]	−59	−59	8.0	714/1
MHW9242	24	152	+38	−59[40]	−58	−59	8	714/1

40–860 MHz Hybrids

Device	Gain dB Typ	Frequency MHz	V_{CC} Volts	2nd Order IMD @ V_{out} = 50 dBmV/ch Max	DIN45004B @ f=860 MHz dBμV Min	Noise Figure @ 860 MHz dB Max	Package/ Style
CA901	17	40 – 860	24	−60	120	8	714P/2
CA901A	17	40 – 860	24	−64	120	8	714P/2
Power Doubling Hybrids							
CA912	17	40 – 860	15	−63	123	9.5	714P/3
CA922	17	40 – 860	24	−63	123	9.5	714P/2
CA922A	17	40 – 860	24	−67	123	9.5	714P/2
Hybrid Jumper							
CATHRU	0	1 – 1000	75 Ohm Broadband Hybrid Jumper				714V

(40)Composite 2nd Order; V_{out} = +38 dBmV/ch

CATV Distribution: Forward Amplifiers (continued)

40–860 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation FM = 55.25 MHz dB 128 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
MHW8182	18	128	+38	–60(40)	– 60	– 60	7	714/1
MHW8222	22	128	+38	–60(40)	– 60	– 60	7.5	714/1
MHW8242	24	128	+38	–60(40)	– 60	– 60	7.5	714/1
MHW8272	27	128	+38	–60(40)	– 60	– 60	7.0	714/1
MHW8292	29	128	+38	–56(40)	– 60	– 60	7.0	714/1
Power Doubling Hybrids								
MHW8185★	18.5	128	+40	–62(39)	– 64	– 64	8.0	714Y/1
MHW8205★	20	128	+40	–60(39)	– 63	– 64	8.0	714Y/1
Feedforward Hybrids								
MFF524B	24	128	+44	–68(36)	– 66	—	13.0	825A/2

40–750 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 110 CH	Cross Modulation FM = 55.25 MHz dB 110 CH	Noise Figure @ 750 MHz dB Max	Package/ Style
MHW7142	14	110	+40	–60(39)	– 62	– 66	8.0	714/1
MHW7182	18	110	+40	–62(39)	– 62	– 64	6.5	714/1
MHW7222	22	110	+40	–55(39)	– 60	– 60	7	714/1
MHW7222A★	22	110	+40	–57(39)	– 60	– 60	7	714Y/1
MHW7242	24	110	+40	–60(39)	– 60	– 60	7	714/1
MHW7272	27	110	+40	–60(39)	– 60	– 60	6.5	714/1
MHW7292	29	110	+40	–60(39)	– 60	– 60	6.5	714/1
Power Doubling Hybrids								
MHW7185A	18.5	110	+44	–58(36)	–58	–65	8.5	714/1
MHW7185C★	18.8	110	+44	–64	–62	–63	8.0	714Y/1
MHW7205A	20	110	+44	–56(36)	–57	–64	8.0	714/1
MHW7205C★	20	110	+44	–63	–61	–62	8.0	714Y/1
Feedforward Hybrids								
MFF424B	24	110	+44	–70(36)	–68	—	13	825A/2

(36)Composite 2nd order; V_{out} = +44 dBmV/ch
(39)Composite 2nd order; V_{out} = +40 dBmV/ch
(40)Composite 2nd Order; V_{out} = +38 dBmV/ch
★New Product

CATV Distribution: Forward Amplifiers (continued)

40–600 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.)	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 600 MHz	Package/ Style
			Output Level	2nd Order Test	Composite Triple Beat dB	Cross Modulation dB	dB	
	dB		dBmV	dB	87 CH	87 CH	Max	
MHW6182–6	18	87	+44	–56(36)	–57	–55	6	714/1

Power Doubling Hybrids

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 87 CH	Cross Modulation dB 87 CH	Noise Figure @ 600 MHz dB Max	Package/ Style
MHW6185–6A	18	87	+44	–64(36)	–64	–66	7	714/1
MHW6205–6A	20	87	+44	–63(36)	–63	–65	6.5	714/1

Feedforward Hybrids

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 87 CH	Cross Modulation dB 87 CH	Noise Figure @ 600 MHz dB Max	Package/ Style
MFF324B	24	85	+44	–86(38)	–73	–68	12.5	825A/2

40–550 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.)	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 550 MHz	Package/ Style
			Output Level	2nd Order Test	Composite Triple Beat dB	Cross Modulation dB	dB	
	dB		dBmV	dB	77 CH	77 CH	Max	
MHW6142	14	77	+44	–72(35)	–59	–62	7.5	714/1
MHW6172	17	77	+44	–72(35)	–59	–62	7	714/1
MHW6182	18	77	+44	–72(35)	–58	–62	7	714/1
MHW6222	22	77	+44	–66(35)	–57	–57	6	714/1
MHW6272	27	77	+44	–64(35)	–57	–57	6.5	714/1
MHW6342	34	77	+44	–64(35)	–57	–57	6.5	714/1

Feedforward Hybrids

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 77 CH	Cross Modulation dB 77 CH	Noise Figure @ 550 MHz dB Max	Package/ Style
MFF224B	24	77	+44	–86(35)	–75	–70	11	825A/2

(35)Channels 2 and M30 @ M39
(36)Composite 2nd order; V_{out} = +44 dBmV/ch
(38)Channels 2 and M39 @ M48

CATV Distribution: Forward Amplifiers (continued)

40–450 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 60 CH	Cross Modulation dB 60 CH	Noise Figure @ 450 MHz dB Max	Package/ Style
MHW5182A	18	60	+46	−72(31)	−61	−59	6.5	714/1
MHW5222A	22	60	+46	−72(31)	−60	−59	5.5	714/1
MHW5342A	34	60	+46	−68(31)	−59	−59	6.0	714/1
MHW5382A	38	60	+46	−64(31)	−59	−59	5.0	714/1
Power Doubling Hybrids								
MHW5185B	18	60	+46	−67(32)	−67	−67	7.0	714/1
Feedforward Hybrids								
MFF124B	24	60	+46	−84(31)	−79	−75	10	825A/2

Reverse Amplifiers

5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test(30) dB	Composite Triple Beat dB 22 CH	Composite Triple Beat dB 26 CH	Cross Modulation dB 22 CH	Cross Modulation dB 26 CH	Noise Figure @ 175 MHz dB Max	Package/ Style
MHW1134	13	22	+50	−72	−73	−71(19)	−65	−65(19)	7	714/1
MHW1184	18	22	+50	−72	−70	−70(19)	−64	−64(19)	5.5	714/1
MHW1224	22	22	+50	−72	−69	−68.5(19)	−62	−62(19)	5.5	714/1
MHW1244	24	22	+50	−72	−68	−67.5(19)	−61	−61(19)	5	714/1

Low Current Amplifiers — 5–50 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	I_{DC} mA Max	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test(30) dB	Composite Triple Beat dB 4 CH	Cross Modulation dB 4 CH	Noise Figure @ 50 MHz dB Max	Package/ Style
MHW1304L	30	4	135	+50	−70	−66	−57	4.5	714/1

(19)Typical
(30)Channels 2 and A @ 7
(31)Channels 2 and M13 @ M22
(32)Composite 2nd order; V_{out} = +46 dBmV/ch

Section Two

RF Device Data Sheets

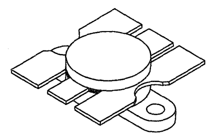
The RF Line
NPN Silicon RF Power Transistor

2N6439

60 W, 225 to 400 MHz CONTROLLED "Q" BROADBAND RF POWER TRANSISTOR NPN SILICON

. . . designed primarily for wideband large–signal output amplifier stages in the 225 to 400 MHz frequency range.

- Guaranteed Performance in 225 to 400 MHz Broadband Amplifier @ 28 Vdc
  Output Power = 60 Watts over 225 to 400 MHz Band
  Minimum Gain = 7.8 dB @ 400 MHz
- Built–In Matching Network for Broadband Operation Using Double Match Technique
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications



CASE 316–01, STYLE 1

MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	33	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	146 0.83	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.2	°C/W

ELECTRICAL CHARACTERISTICS* (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	2.0	mAdc

(continued)

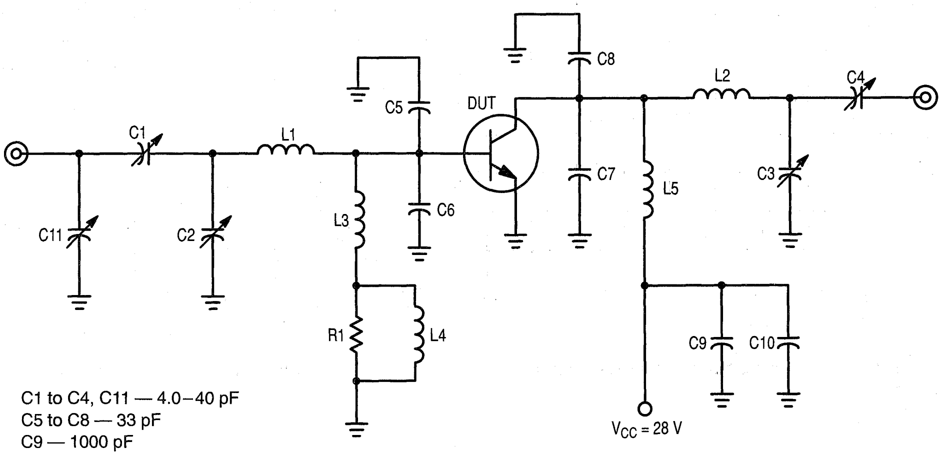
NOTE:
1. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

* Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS* — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	67	75	pF
BROADBAND FUNCTIONAL TESTS (Figure 6)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 60 W, f = 225–400 MHz)	G_{PE}	7.8	8.5	—	dB
Electrical Ruggedness (P_{out} = 60 W, V_{CC} = 28 Vdc, f = 400 MHz, VSWR 30:1 all phase angles)	ψ	No Degradation in Output Power			—
NARROW BAND FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 60 W, f = 400 MHz)	G_{PE}	7.8	10	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 60 W, f = 400 MHz)	η	55	—	—	%

* Indicates JEDEC Registered Data.



C1 to C4, C11 — 4.0–40 pF
C5 to C8 — 33 pF
C9 — 1000 pF
C10 — 5.0 μF
R1 — 15 Ω
L1, L2 — 3/16″ x 1″ Copper Strap
L3 — 1.5 μH
L4 — 10 μH
L5 — 1 Turn #16 AWG, 5/16″ I.D.

Figure 1. 400 MHz Test Amplifier (Narrow Band)

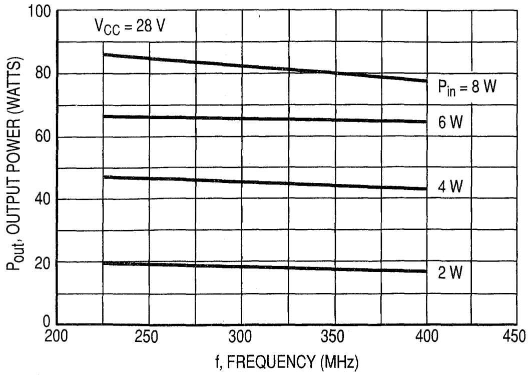


Figure 2. P_{out} versus Frequency

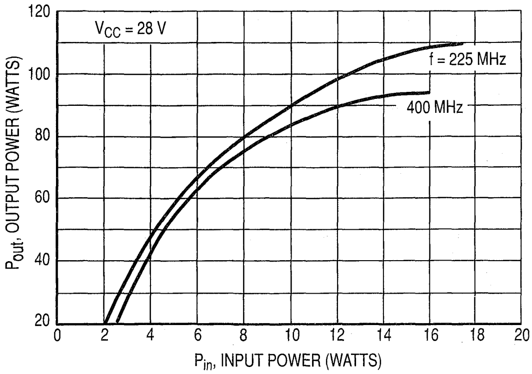


Figure 3. Output Power versus Input Power

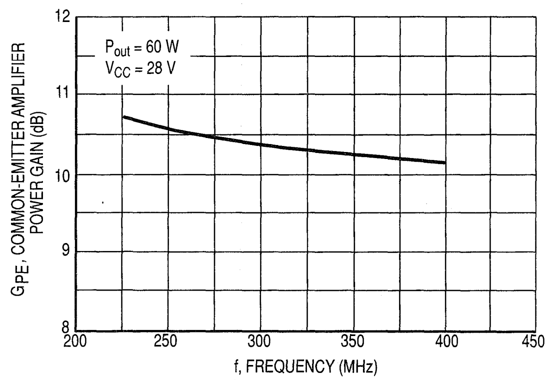


Figure 4. Power Gain versus Frequency

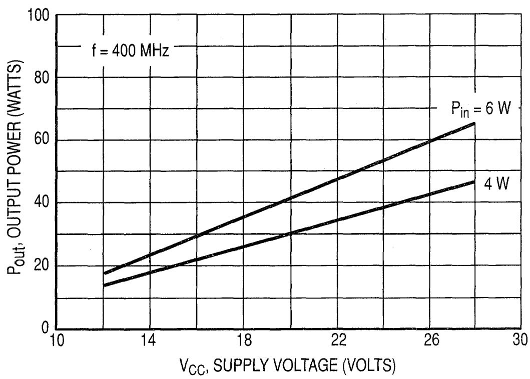


Figure 5. Output Power versus Supply Voltage

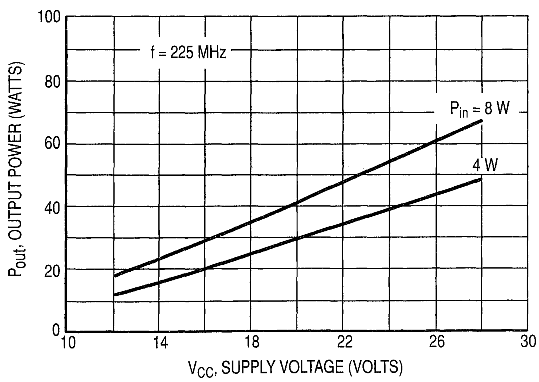
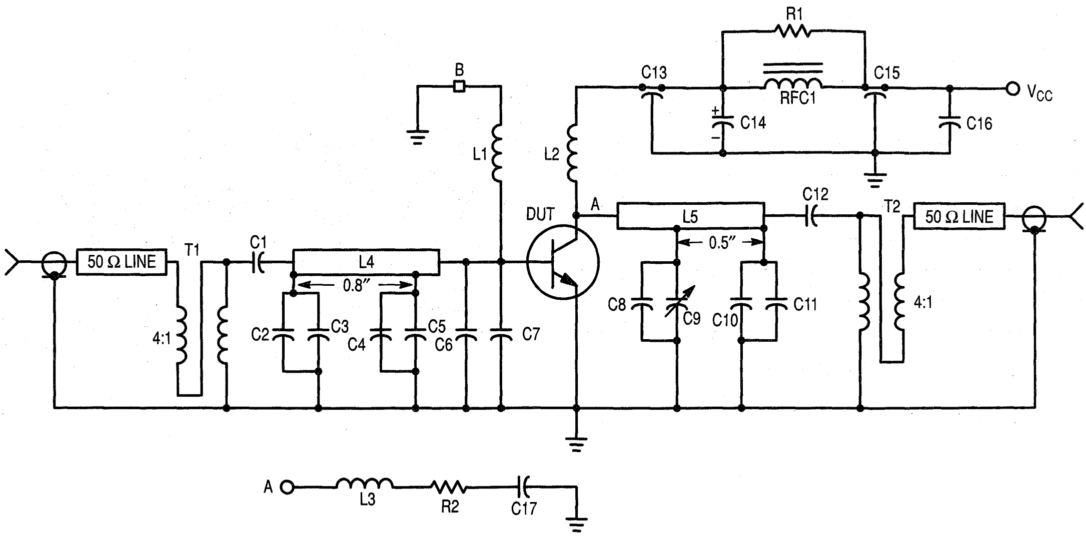


Figure 6. Output Power versus Supply Voltage



C1 — 68 pF
C2, C4, C8, C10 — 27 pF
C3, C5, C11 — 10 pF
C6, C7 — 51 pF
C9 — 1.0–10 pF JOHANSON
C12 — 100 pF
C13, C15 — 680 pF
C14, C16 — 1.0 µF, 35 V Tantalum
C17 — 0.1 µF, ERIE Red Cap

RFC1 — Ferrite Bead Choke, Feroxcube VK200 19/4B
B — Ferroxcube 56-590-65/4B Ferrite Bead
T1, T2 — 25 Ohms (UT25) Miniature Coaxial Cable, 1 turn
R1 — 11 Ω, 1.0 W
R2 — 20 Ω, 1/4 W
L1 — 10 Turns, #22 AWG, 1/8″ I.D.
L2 — 4 Turns, #16 AWG, 1/4″ I.D.
L3 — 6 Turns, #24 AWG, 1/8″ I.D.
L4, L5 — 1″ x 0.25″ Microstrip Line
Board Material 0.031″ Thick Teflon-Fiberglass

Figure 7. 225 to 400 MHz Broadband Test Circuit Schematic

BROADBAND DATA (Circuit, Figure 7)

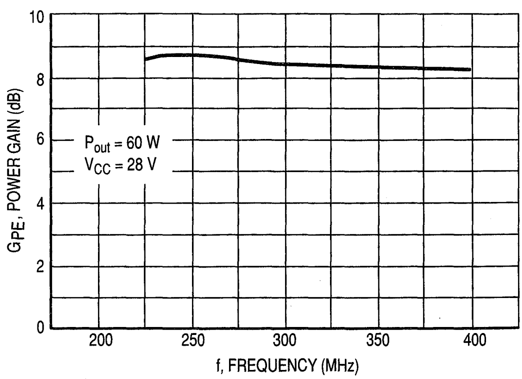


Figure 8. Power Gain versus Frequency

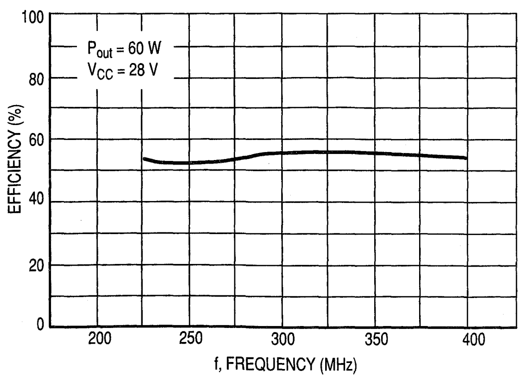


Figure 9. Efficiency versus Frequency

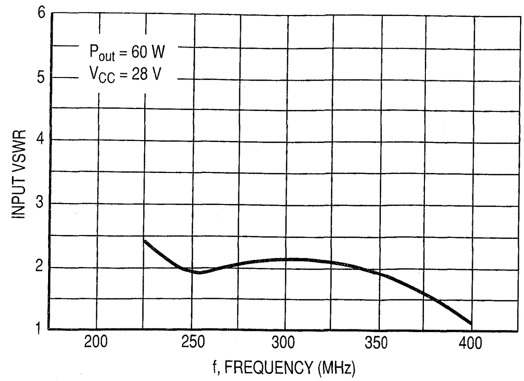
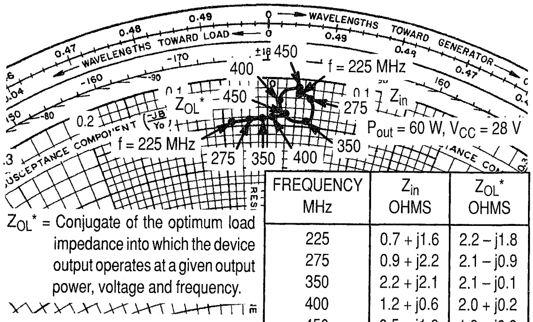


Figure 10. Input VSWR versus Frequency



Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FREQUENCY MHz	Z_{in} OHMS	Z_{OL}* OHMS
225	0.7 + j1.6	2.2 – j1.8
275	0.9 + j2.2	2.1 – j0.9
350	2.2 + j2.1	2.1 – j0.1
400	1.2 + j0.6	2.0 + j0.2
450	0.5 + j1.6	1.9 + j0.9

Figure 11. Series Equivalent Input-Output Impedance

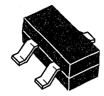
The RF Line
NPN Silicon High-Frequency Transistors

BFR92ALT1

Designed primarily for use in high–gain, low–noise, small–signal UHF and microwave amplifiers constructed with thick and thin–film circuits using surface mount components.

- T1 suffix indicates tape and reel packaging of 3,000 units per reel.

RF TRANSISTORS
NPN SILICON



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	15	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Emitter–Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Continuous	I_C	25	mAdc
Maximum Junction Temperature	T_{Jmax}	150	°C
Power Dissipation, T_{case} = 75°C Derate linearly above T_{case} = 75°C @	$P_{D(max)}$	0.273 3.64	W mW/°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Storage Temperature	T_{stg}	–55 to +150	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	275	°C/W

DEVICE MARKING

BFR92ALT1 = P2

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (1) (I_C = 10 mA)	$V_{(BR)CEO}$	15	—	Vdc
Collector–Base Breakdown Voltage (I_C = 100 μA)	$V_{(BR)CBO}$	20	—	Vdc
Emitter–Base Breakdown Voltage (I_C = 100 μA)	$V_{(BR)EBO}$	2.0	—	Vdc
Collector Cutoff Current (V_{CB} = 10 V)	I_{CBO}	—	50	nA
ON CHARACTERISTICS				
DC Current Gain (I_C = 14 mA, V_{CE} = 10 V)	h_{FE}	40	—	—
Collector–Emitter Saturation Voltage (1) (I_C = 25 mA, I_B = 5.0 mA)	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 25 mA, I_B = 5.0 mA)	$V_{BE(sat)}$	—	1.2	Vdc

NOTE:
1. Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Typ	Unit
SMALL–SIGNAL CHARACTERISTICS			
Current–Gain — Bandwidth Product (I_C = 14 mA, V_{CE} = 10 V, f = 500 MHz)	f_T	4.5	GHz
Noise Figure (V_{CE} = 1.5 V, I_C = 3.0 mA, R_S = 50 Ω, f = 500 MHz)	NF	3.0	dB
Capacitance–Collector to Base (V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{cb}	0.7	pF

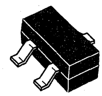
The RF Line
NPN Silicon High-Frequency Transistors

Designed primarily for use in high–gain, low–noise, small–signal UHF and microwave amplifiers constructed with thick and thin–film circuits using surface mount components.

- T1 Suffix Indicates Tape and Reel Packaging of 3,000 Units per Reel.

BFR93ALT1

RF TRANSISTORS
NPN SILICON



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	12	Vdc
Collector–Base Voltage	V_{CBO}	15	Vdc
Emitter–Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Continuous	I_C	35	mAdc
Maximum Junction Temperature	T_{Jmax}	150	°C
Power Dissipation, T_{case} = 75°C (2) Derate linearly above T_{case} = 75°C @	$P_{D(max)}$	0.306 4.08	W mW/°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Storage Temperature	T_{stg}	–55 to +150	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	245	°C/W

DEVICE MARKING

BFR93ALT1 = R2

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (1) (I_C = 10 mA)	$V_{(BR)CEO}$	12	—	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CBO}$	15	—	Vdc
Emitter–Base Breakdown Voltage (I_C = 100 μA)	$V_{(BR)EBO}$	2.0	—	Vdc
Collector Cutoff Current (V_{CE} = 10 V)	I_{CEO}	—	50	nA
Collector Cutoff Current (V_{CB} = 10 V)	I_{CBO}	—	50	nA
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 30 mA, V_{CE} = 5.0 V)	h_{FE}	40	—	—
Collector–Emitter Saturation Voltage (1) (I_C = 35 mA, I_B = 7.0 mA)	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 35 mA, I_B = 7.0 mA)	$V_{BE(sat)}$	—	1.2	Vdc

NOTE:
1. Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. Case temperature measured on collector lead immediately adjacent to body of package.

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
SMALL–SIGNAL CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 30 mA, V_{CE} = 5.0 V, f = 500 MHz)	f_T	3.0	—	GHz
Noise Figure (V_{CE} = 5.0 V, I_C = 2.0 mA, R_S = 50 Ω, f = 30 MHz)	NF	—	3.0	dB

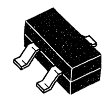
The RF Line
NPN Silicon High-Frequency Transistor

BFS17LT1

Designed primarily for use in high–gain, low–noise amplifier, oscillator and mixer applications. Packaged for thick or thin film circuits using surface mount components.

- T1 suffix indicates tape and reel packaging of 3,000 units per reel.

RF TRANSISTOR
NPN SILICON



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE
(TO–236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	15	Vdc
Collector–Base Voltage	V_{CBO}	25	Vdc
Maximum Junction Temperature	T_{Jmax}	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, T_A = 25°C Derate above 25°C (1)	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	–55 to +150	°C
Thermal Resistance Junction to Ambient (1)	$R_{\theta JA}$	357	°C/W

DEVICE MARKING

BFS17LT1 = E1

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mA)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 100 μA)	$V_{(BR)CBO}$	25	—	—	Vdc
Collector Cutoff Current (V_{CE} = 10 V)	I_{CEO}	—	—	25	nA
Collector Cutoff Current (V_{CB} = 10 V)	I_{CBO}	—	—	25	nA
Emitter Cutoff Current (V_{EB} = 4 V)	I_{EBO}	—	—	100	μA
ON CHARACTERISTICS					
DC Current Gain (I_C = 2 mA, V_{CE} = 1 V) (I_C = 25 mA, V_{CE} = 1 V)	h_{FE}	 20 20	 — —	 150 —	—
Collector–Emitter Saturation Voltage (I_C = 10 mA, I_B = 1 mA)	$V_{CE(sat)}$	—	—	0.4	V
Base–Emitter Saturation Voltage (I_C = 10 mA, I_B = 1 mA)	$V_{BE(sat)}$	—	—	1	V
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 2 mA, V_{CE} = 5 V, f = 500 MHz) (I_C = 25 mA, V_{CE} = 5 V, f = 500 MHz)	f_T	 — —	 1 1.3	 — —	GHz
Output Capacitance (V_{CB} = 10 V, f = 1 MHz)	CCB	—	1	—	pF
Noise Figure (I_C = 2 mA, V_{CE} = 5 V, R_S = 50 Ω, f = 30 MHz)	NF	—	5	—	dB

NOTE:
1. Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

REV 7

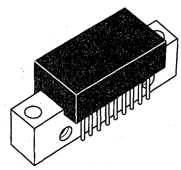
The RF Line
VHF/UHF CATV Amplifiers

CA901
CA901A

. . . designed for broadband applications requiring low–distortion amplification. Specifically intended for CATV/MATV market requirements. These amplifiers feature ion–implanted arsenic emitter transistors and an all gold metal system.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  Frequency Range — 40 to 860 MHz
  Power Gain — 17 dB Typ @ f = 40 MHz
  Noise Figure — 6.5 dB Typ @ f = 500 MHz
  120 dBμV DIN45004B @ 860 MHz
- All Gold Metallization for Improved Reliability
- Superior Gain, Return Loss and DC Current Stability with Temperature

**17 dB
40–860 MHz
VHF/UHF
CATV/MATV
AMPLIFIERS**



**CASE 714P–03, STYLE 2
(CA)**

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+14	dBm
Supply Voltage	V_{CC}	26	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	860	MHz
Power Gain (f = 40 MHz)	P_G	16.5	17	17.5	dB
Slope (40–860 MHz)	S	0.2	0.8	1.5	dB
Gain Flatness	—	—	—	0.6	dB
Input/Output Return Loss f = 40–100 MHz f = 100–800 MHz f = 800–860 MHz	IRL/ORL	20 15 10/15	— 17 12/18	— — —	dB
Second Order Intermodulation Distortion CA901 (V_{out} = +50 dBmV per ch.) CA901A	IMD_2	— —	— —	−60 −64	dB
DIN45004B (See Figure 1) f = 40–400 MHz f = 400–860 MHz	DIN	121 120	— —	— —	dBμV
Noise Figure f = 500 MHz f = 860 MHz	NF	— —	6.5 7.0	7.5 8.0	dB
Supply Current	I_{DC}	—	235	255	mA

REV 6

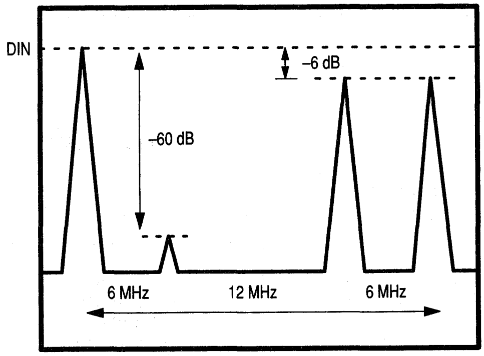


Figure 1. DIN45004B Test

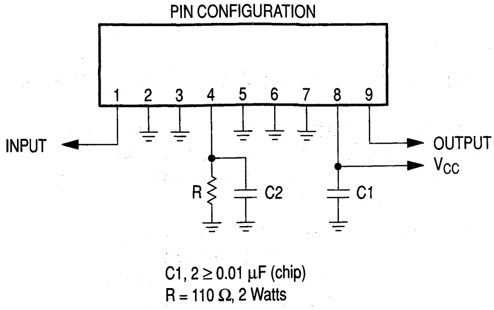


Figure 2. External Connections

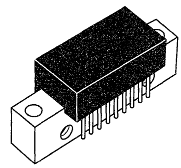
The RF Line
VHF/UHF CATV Amplifier

CA912

. . . designed for broadband applications requiring low–distortion and high output capability. Specifically intended for CATV/MATV market requirements. These amplifiers feature ion–implanted arsenic emitter transistors and an all gold metal system.

- Specified Characteristics at T_C = 25°C; V_{CC} = 15 V
  Frequency Range — 40 to 860 MHz
  Power Gain — 17 dB Typ @ f = 40 MHz
  Noise Figure — 7.0 dB Typ @ f = 500 MHz
  123 dBμV DIN45004B @ 860 MHz
- All Gold Metallization for Improved Reliability
- Superior Gain, Return Loss and DC Current Stability with Temperature

17 dB
40–860 MHz
VHF/UHF
CATV/MATV
AMPLIFIER



CASE 714P–03, STYLES 2, 3

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
RF Input Power Per Tone	P_{in}	+17	dBm
Storage Temperature	T_{stg}	– 40 to +100	°C
Operating Case Temperature Range	T_C	– 20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 15 V, 75 Ohm System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{DC}	640	700	760	mA
Power Gain (f = 40 MHz)	PG	16.5	17	17.5	dB
Bandwidth	BW	40	—	860	MHz
Slope (40–860 MHz)	S	0.2	0.8	1.5	dB
Gain Flatness	FL	—	—	1.0	dB
Input/Output Return Loss f = 40 – 100 MHz f = 100 – 800 MHz f = 800 – 860 MHz	IRL/ORL	20 15 10	— 17 12	— — —	dB
Second Order Intermodulation Distortion (V_o = + 50 dBmV/ch.)	IMD_2	—	—	–67	dB
DIN45004B (See Figure 1) f = 40 – 400 MHz f = 400 – 860 MHz	DIN	124 123	— —	— —	dBμV
Noise Figure f = 500 MHz f = 860 MHz	NF	— —	7.0 8.0	8.5 9.5	dB

REV 7

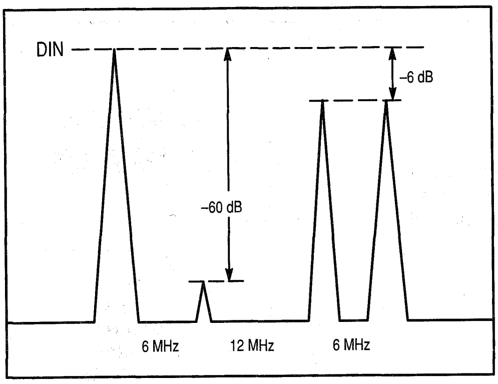


Figure 1. DIN45004B Test

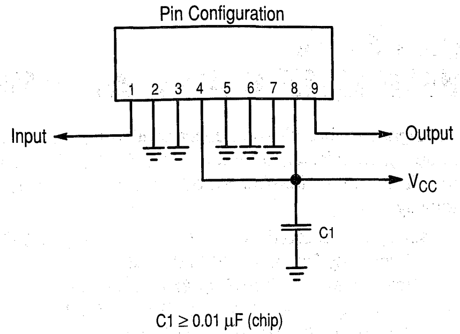


Figure 2. External Connections Case 714P–03, Style 3

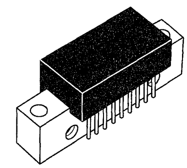
The RF Line
VHF/UHF CATV Amplifiers

CA922
CA922A

Designed for broadband applications requiring low–distortion and high output capability. Specifically intended for CATV/MATV market requirements. These amplifiers feature ion–implanted arsenic emitter transistors and an all gold metal system.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C
  - Frequency Range — 40 to 860 MHz
  - Power Gain — 17 dB Typ @ f = 40 MHz
  - Noise Figure — 7.0 dB Typ @ f = 500 Mhz
  - 123 dBµV DIN45004B @ 860 MHz
- All Gold Metalization for Improved Reliability
- Superior Gain, Return Loss and DC Current Stability with Temperature
- Improved 2nd Order IMD Available (CA922A)

17 dB
40–860 MHz
VHF/UHF
CATV/MATV
AMPLIFIERS



CASE 714P–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	26	V
RF Input Power Per Tone	P_{in}	+16	dBm
Storage Temperature	T_{stg}	– 40 to +100	°C
Operating Case Temperature Range	T_C	– 20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 75 Ohm System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	Idc	—	400	440	mA
Power Gain (f = 40 MHz)	PG	16.5	17	17.5	dB
Bandwidth	BW	40	—	860	MHz
Slope (40 – 860 MHz)	S	0.2	0.8	1.5	dB
Gain Flatness	FL	—	—	1.0	dB
Input/Output Return Loss f = 40–100 MHz f = 100–800 MHz f = 800–860 MHz	IRL/ORL	20 15 10/13	— 17 12/15	— — —	dB
Second Order Intermodulation Distortion CA922 (V_o = +50 dBmV/ch.) CA922A	IMD_2	— —	— —	– 63 – 67	dB dB
DIN45004B (See Figure 1) f = 40–400 MHz f = 400–860 MHz	DIN	124 123	— —	— —	dBµV
Noise Figure f = 500 MHz f = 860 MHz	NF	— —	7.0 8.0	8.5 9.5	dB

REV 6

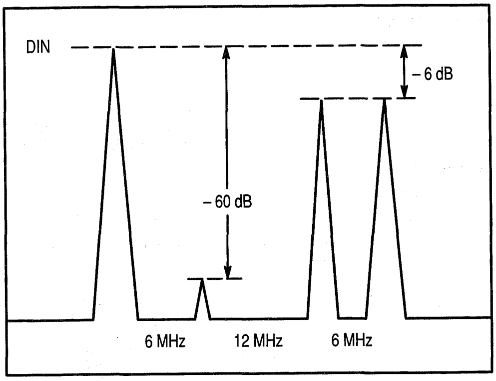


Figure 1. DIN45004B Test

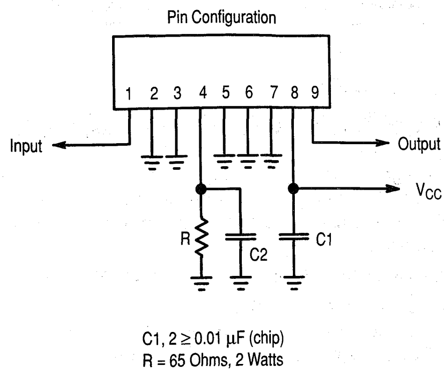


Figure 2. External Connections

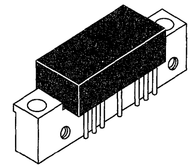
The RF Line
Wideband Linear Amplifier

CA2810C

. . . designed for amplifier applications in 50 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push–pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
- Frequency Range — 10 to 450 MHz
  Output Power — 1 W Typ @ 1 dB Compression, f = 200 MHz
  Power Gain — 34 dB Typ @ f = 50 MHz
  PEP — 400 mW Typ @ –32 dB IMD
  Noise Figure — 5 dB Max @ f = 300 MHz
- All Gold Metallization for Improved Reliability

**34 dB
10–450 MHz
800 mWATT
WIDEBAND
LINEAR AMPLIFIER**



**CASE 714F–03, STYLE 1
[CA (POS. SUPPLY)]**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+5	dBm
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	450	MHz
Gain Flatness (f = 10–450 MHz)	F_L	—	—	±1.5	dB
Power Gain (f = 50 MHz)	P_G	33	34	35	dB
Noise Figure, Boradband (f = 300 MHz)	NF	—	—	5	dB
Power Output — 1 dB Compression (f = 200 MHz)	$P_{o1\ dB}$	800	1000	—	mW
Third Order Intercept (See Figure 10, f_1 = 300 MHz)	ITO	—	43	—	dBm
Input/Output VSWR (f = 10–450 MHz)	VSWR	—	—	2:1	—
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 10–300 MHz)	d_{so}	—	–55	–45	dB
Reverse Isolation (f = 10–450 MHz)	—	—	40	—	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 10) (f = 10–450 MHz @ –32 dB IMD)	PEP	—	400	—	mW
Supply Current	I_{CC}	270	310	330	mA

TYPICAL CHARACTERISTICS

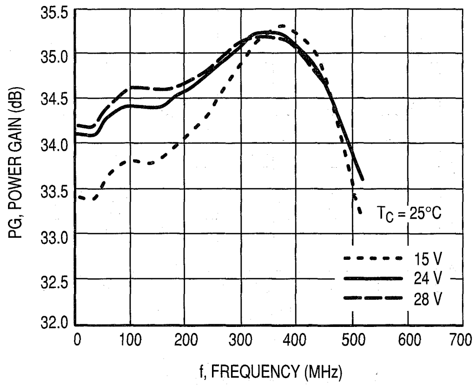


Figure 1. Power Gain versus Voltage

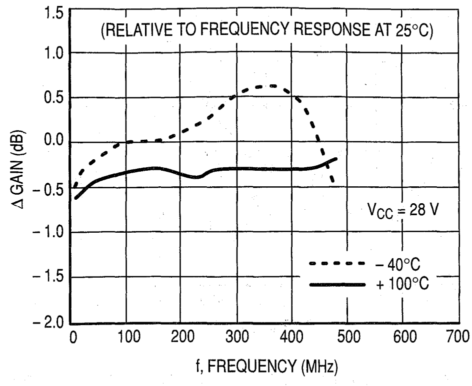


Figure 2. Relative Power Gain versus Temperature

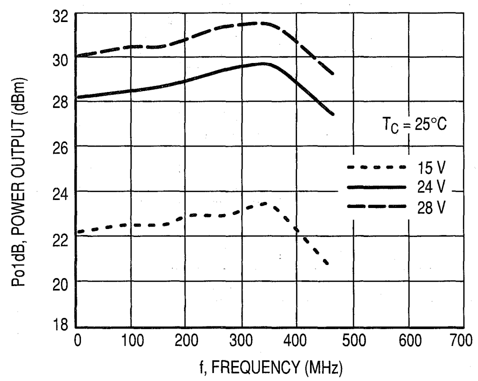


Figure 3. 1 dB Compression versus Voltage

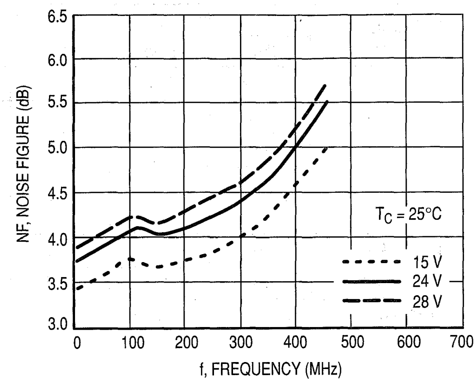


Figure 4. Noise Figure versus Voltage

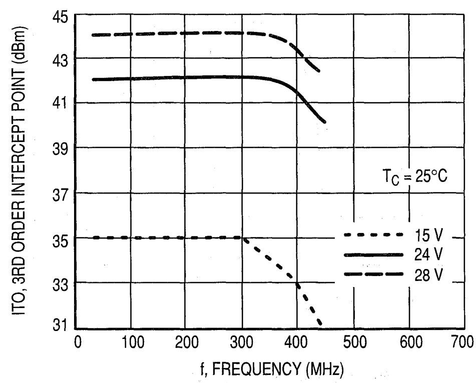


Figure 5. Third Order Intercept versus Voltage

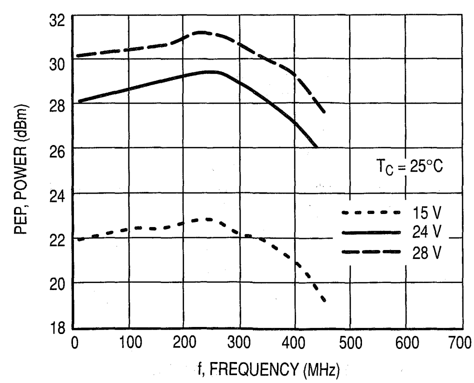


Figure 6. Peak Envelope Power versus Voltage

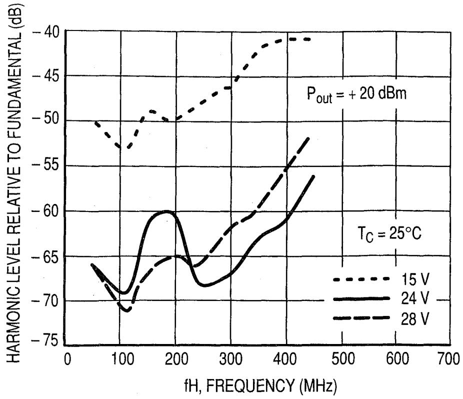


Figure 7. Second Harmonic Distortion versus Voltage

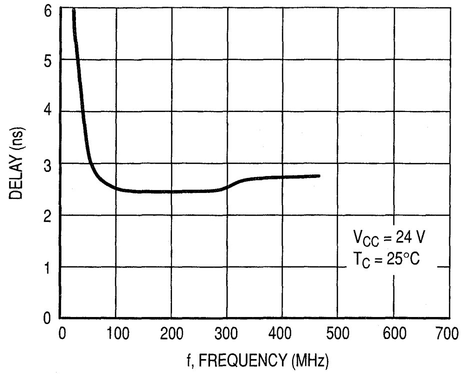


Figure 8. Group Delay versus Frequency

Biased at 24 Volts **T = 25°C Zo = 50Ω**

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
10	–13.8	3.5	34.2	–145	–46	–131	–13.5	8.2
50	–16.0	–3.0	34.2	150	–47	–172	–18.5	4.6
100	–14.4	–14	34.4	88	–48	102	–14.5	–9.2
200	–13.2	–50	34.6	2	–42	35	–13.2	–80
300	–13.9	–79	35.0	–80	–46	65	–16.7	–49
400	–14.1	–115	35.0	–80	–48	–44	–14.2	11
450	–16.2	–122	34.6	120	–53	–82	–13.8	–46

Magnitude in dB, Phase Angle in degrees.

Table 1. S–Parameters

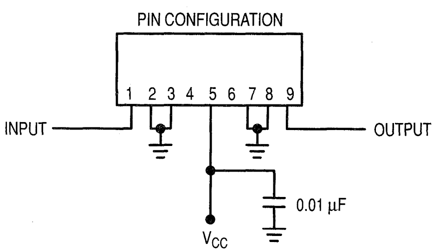
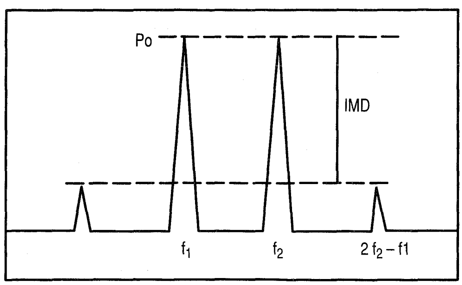


Figure 9. External Connections



ITO = Po + IMD / 2 @ IMD > 60 dB
PEP = 4 x Po @ IMD = – 32 dB

Figure 10. Intermodulation Test

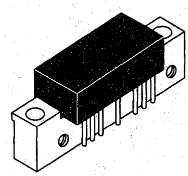
The RF Line
Wideband Linear Amplifier

CA2818C

Designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push–pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  Frequency Range — 0.35 to 400 MHz
  Output Power — 1000 mW Typ @ 1 dB Compression, f = 200 MHz
  Power Gain — 18.5 dB Typ @ f = 50 MHz
  PEP — 1000 mW Typ @ −32 dB IMD, f = 200 MHz
  Noise Figure — 5 dB Typ @ f = 200 MHz
  ITO — 47 dBm Typ @ f = 150 MHz
- All Gold Metallization for Improved Reliability
- Unconditional Stability Under All Load Conditions

18.5 dB
0.35–400 MHz
1000 mWATT
WIDEBAND
LINEAR AMPLIFIER



CASE 714F–03, STYLE 1
[CA (POS. SUPPLY)]

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+14	dBm
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	0.35	—	400	MHz
Gain Flatness (f = 0.35–400 MHz)	F_L	—	±0.5	±1	dB
Power Gain (f = 50 MHz)	P_G	17.75	18.5	19.25	dB
Noise Figure, Broadband (f = 200 MHz)	NF	—	5	6	dB
Power Output — 1 dB Compression (f = 200 MHz)	$P_{o\ 1dB}$	800	1000	—	mW
Third Order Intercept (See Figure 10, f_1 = 200 MHz)	ITO	43	45	—	dBm
Input/Output VSWR (f = 0.35–400 MHz)	VSWR	—	1.7:1	2:1	—
Second Harmonic Distortion (P_o = 100 mW) f_{2H} = 0.35–200 MHz f_{2H} = 200–400 MHz	d_{so}	— —	−65 —	−60 −50	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 10) f = 0.35–200 MHz @ −32 dB IMD f = 200–400 MHz @ −32 dB IMD	PEP	600	800	—	mW
Supply Current	I_{CC}	190	205	220	mA

REV 1

TYPICAL CHARACTERISTICS

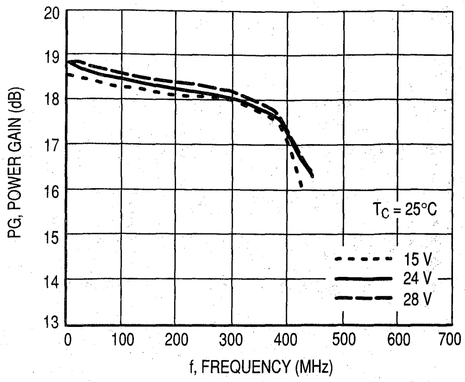


Figure 1. Power Gain versus Voltage

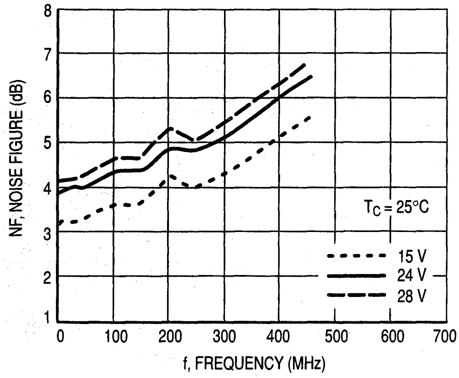


Figure 4. Noise Figure versus Voltage

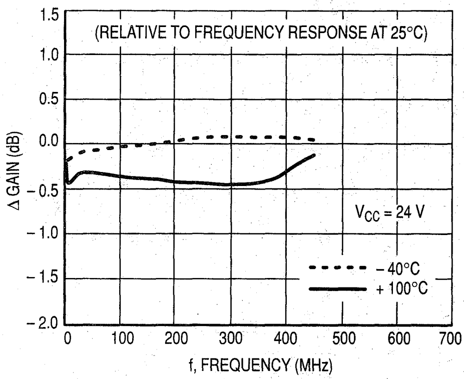


Figure 2. Relative Power Gain versus Temperature

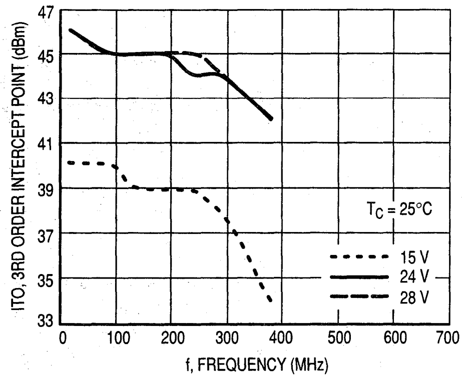


Figure 5. Third Order Intercept versus Voltage

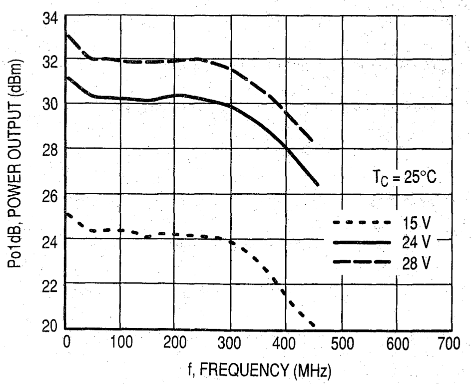


Figure 3. 1 dB Compression versus Voltage

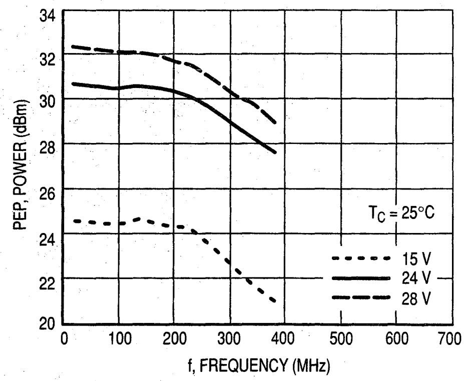


Figure 6. Peak Envelope Power versus Voltage

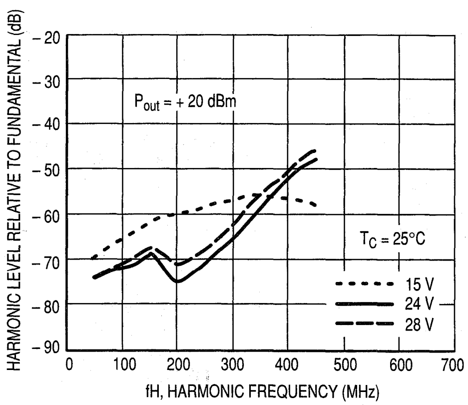


Figure 7. Second Harmonic Distortion versus Voltage

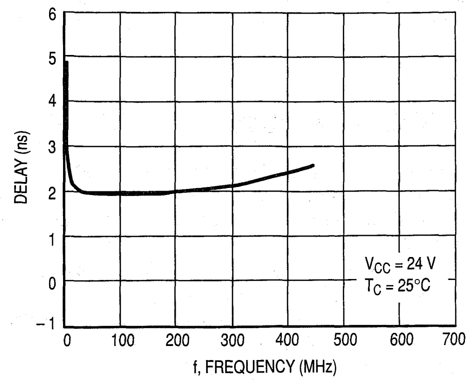


Figure 8. Group Delay versus Frequency

Biased at 24 Volts **T = 25°C Zo = 50Ω**

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.35	−17.0	18.7	18.4	7.4	−24.1	−169	−16.4	11.1
1	−17.3	10.7	18.6	3.4	−24.0	−175	−16.7	6.5
50	−16.3	−7.6	18.7	−38.8	−23.9	145	−17.0	−38.8
100	−15.6	−15.1	18.5	−70.1	−24.1	117	−18.4	−65.9
200	−14.0	−47.3	18.3	−149	−24.8	47.9	−20.6	−101
300	−14.1	−85	18.1	135	−25.3	−15	−16.6	−142
400	−18.0	−137	17.4	58	−25.9	−84.3	−14.2	134

Magnitude in dB, Phase Angle in degrees.

Table 1. S–Parameters

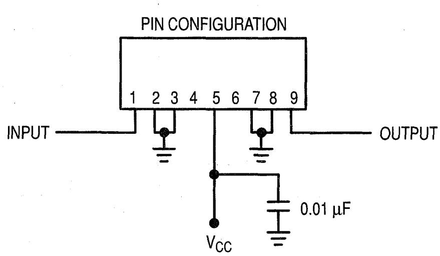
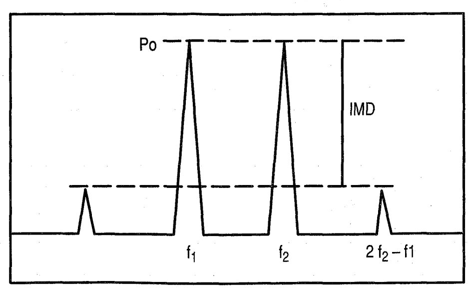


Figure 9. Functional Schematic



ITO = Po + IMD / 2 @ IMD > 60 dB
PEP = 4 x Po @ IMD = – 32 dB

Figure 10. Intermodulation Test

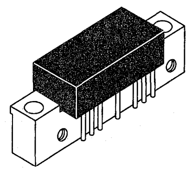
The RF Line
Wideband Linear Amplifiers

CA2830C

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push–pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  - Frequency Range — 5 to 200 MHz
  - Output Power — 800 mW Typ @ 1 dB Compression, f = 200 MHz
  - Power Gain — 34.5 dB Typ @ f = 100 MHz
  - PEP — 800 mW Typ @ –32 dB IMD
  - Noise Figure — 4.7 dB Typ @ f = 200 MHz
  - ITO — 46 dBm @ f = 200 MHz
- All Gold Metallization for Improved Reliability
- Unconditional Stability Under All Load Conditions

34.5 dB
5–200 MHz
800 mWATT
WIDEBAND
LINEAR AMPLIFIERS



CASE 714F–03, STYLE 1
(CA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+5	dBm
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	5	—	200	MHz
Gain Flatness (f = 5–200 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	33.5	34.5	35.5	dB
Noise Figure, Broadband (f = 200 MHz)	NF	—	4.7	5.5	dB
Power Output — 1 dB Compression (f = 5–200 MHz)	$P_{o\ 1dB}$	630	800	—	mW
Power Output — 1 dB Compression (f = 5–200 MHz, V_{CC} = 28 V)	$P_{o\ 1dB}$	1000	1260	—	mW
Third Order Intercept (See Figure 10, f_1 = 200 MHz)	ITO	44	46	—	dBm
Input/Output VSWR (f = 5–200 MHz)	VSWR	—	1.5:1	2:1	—
Second Harmonic Distortion (Tone at 100 mW, f_{2H} = 150 MHz)	d_{so}	—	–60	–50	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 10) (f = 5–200 MHz @ –32 dB IMD)	PEP	600	800	—	mW
Supply Current	I_{CC}	270	300	330	mA

REV 1

TYPICAL CHARACTERISTICS

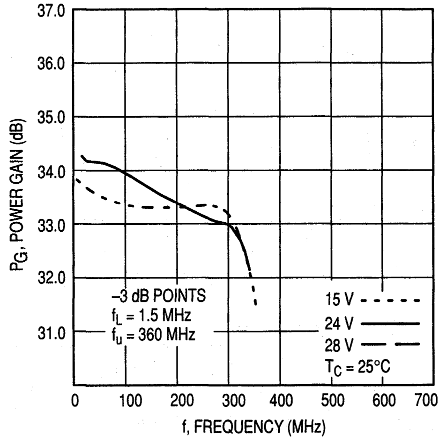


Figure 1. Power Gain versus Frequency

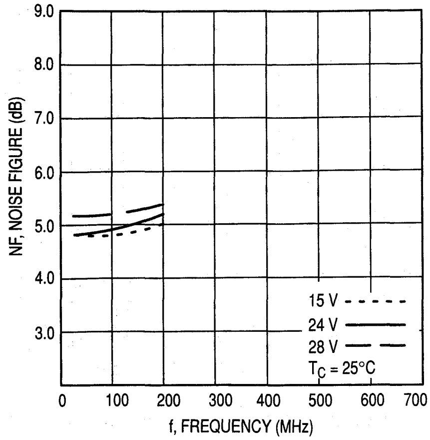


Figure 4. Noise Figure versus Voltage

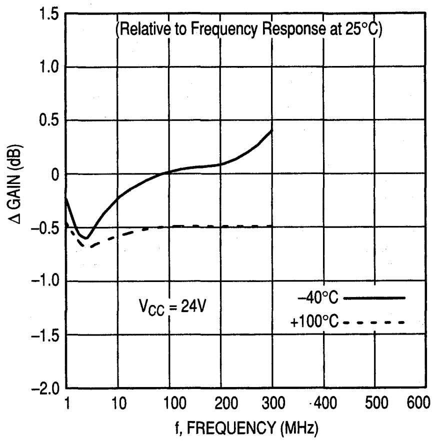


Figure 2. Relative Power Gain versus Temperature

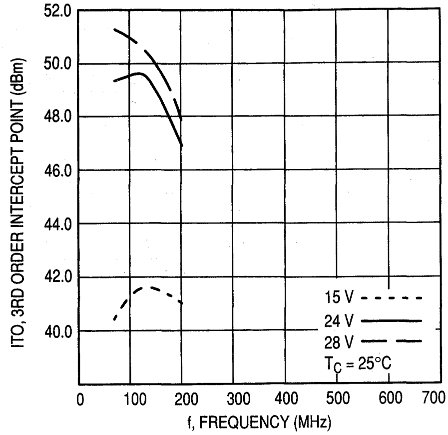


Figure 5. Third Order Intercept versus Voltage

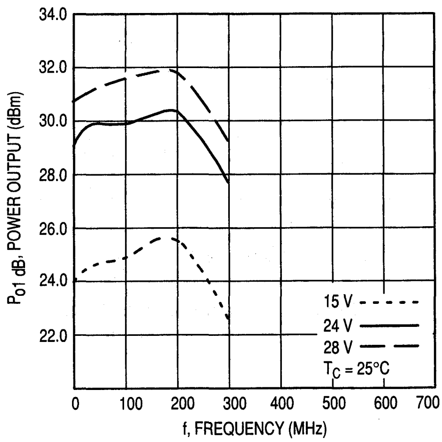


Figure 3. 1 dB Gain Compression versus Voltage

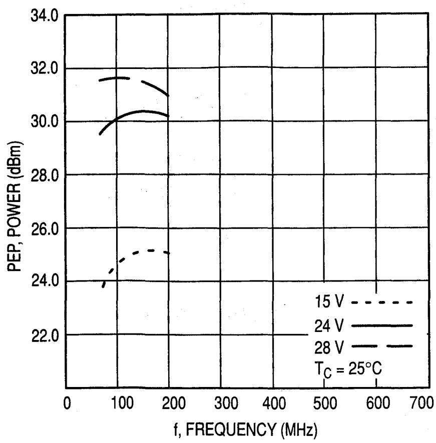


Figure 6. Peak Envelope Power versus Voltage

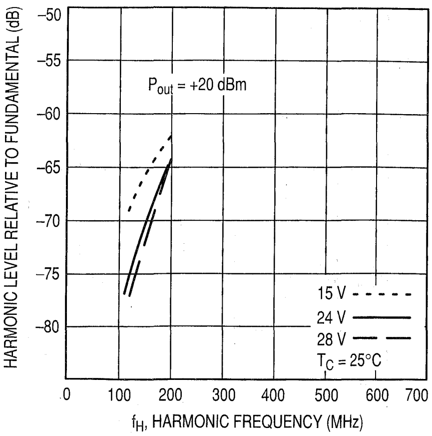


Figure 7. Second Harmonic Distortion versus Voltage

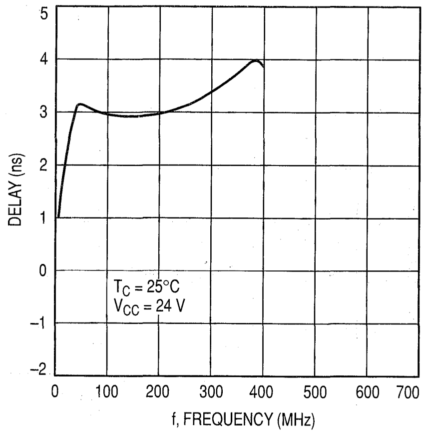


Figure 8. Group Delay versus Frequency

Biased at 24 Volts **T = 25°C Zo = 50Ω**

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
5	–18.3	66.2	34.6	15.2	–47.0	17.7	–9.8	87.4
10	–19.3	45.5	34.6	–0.6	–47.0	2.3	–14.5	76.8
50	–15.6	35.0	34.2	–56.7	–47.5	–30.3	–12.6	45.0
100	–13.2	34.4	33.9	–114	–47.9	–62.9	–10.8	10.7
200	–11.1	30.1	33.5	134	–48.3	–128	–14.9	–42.6

Magnitude in dB, Phase Angle in degrees.

Table 1. S–Parameters

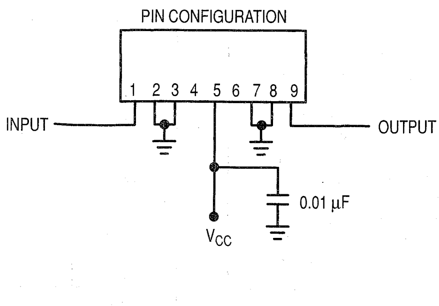
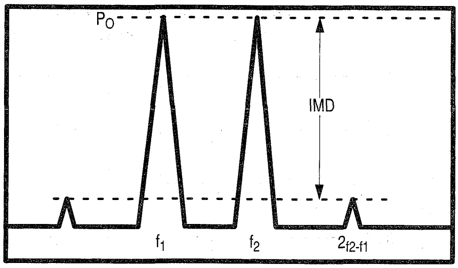


Figure 9. External Connections



$ITO = P_O + \frac{IMD}{2}$ @ IMD > 60dB

PEP = 4X P_O @ IMD = –32dB

Figure 10. Intermodulation Test

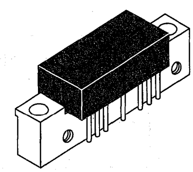
The RF Line
Wideband Linear Amplifier

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push–pull circuit design.

- Specified Characteristics at V_{CC} = 28 V, T_C = 25°C:
  Frequency Range — 1 to 200 MHz
  Output Power — 1580 mW Typ @ 1 dB Compression, f = 200 MHz
  Power Gain — 35.5 dB Typ @ f = 100 MHz
  PEP — 900 mW Typ @ –32 dB IMD
  Noise Figure — 5 dB Typ @ f = 200 MHz
  ITO — 47 dBm @ f = 200 MHz
- All Gold Metallization for Improved Reliability
- Unconditional Stability Under All Load Conditions

CA2832C

**35.5 dB
1–200 MHz
1.6 WATT
WIDEBAND
LINEAR AMPLIFIER**



**CASE 714F–03, STYLE 1
[CA (POS. SUPPLY)]**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	30	Vdc
RF Power Input	P_{in}	+5	dBm
Operating Case Temperature Range	T_C	–20 to +90	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1	—	200	MHz
Gain Flatness (f = 1–200 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	34	35.5	37	dB
Noise Figure, Broadband (f = 200 MHz)	NF	—	5	6	dB
Power Output — 1 dB Compression (f = 1–200 MHz)	$P_{o\ 1dB}$	1260	1580	—	mW
Power Output — 1 dB Compression (f = 150 MHz)	$P_{o\ 1dB}$	—	2000	—	mW
Third Order Intercept (See Figure 10, f_1 = 200 MHz)	ITO	45	47	—	dBm
Input/Output VSWR (f = 1–200 MHz)	VSWR	—	1.5:1	2:1	—
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 150 MHz)	d_{so}	—	–70	–60	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 10) (f = 1–200 MHz @ –32 dB IMD)	PEP	—	900	—	mW
Supply Current	I_{CC}	400	435	470	mA

TYPICAL CHARACTERISTICS

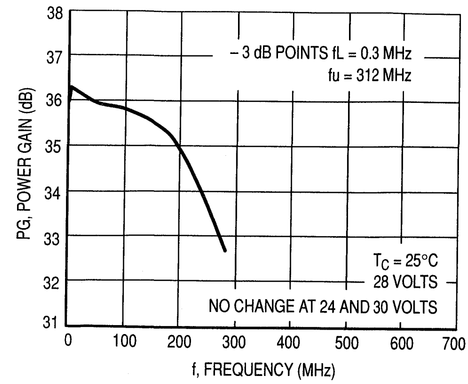


Figure 1. Power Gain versus Voltage

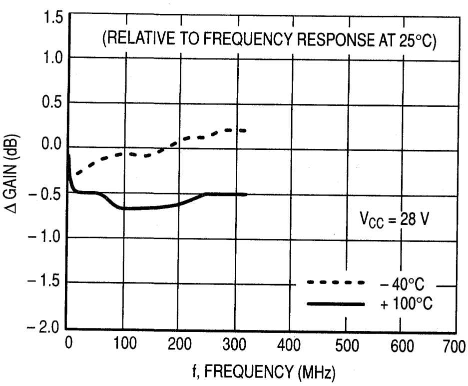


Figure 2. Relative Power Gain versus Temperature

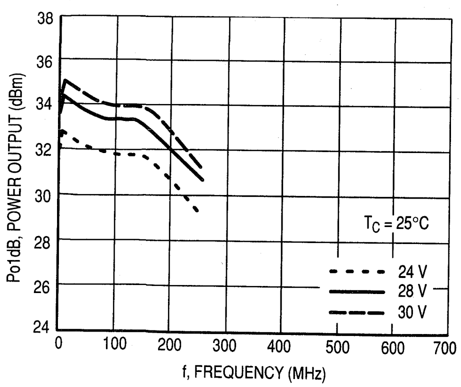


Figure 3. 1 dB Compression versus Voltage

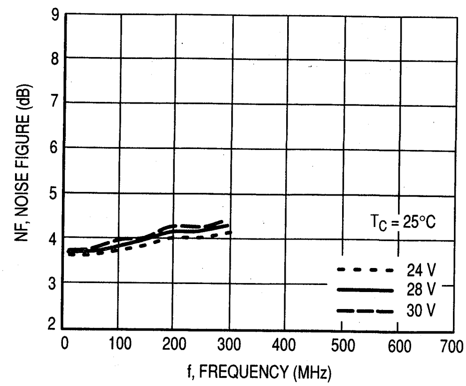


Figure 4. Noise Figure versus Voltage

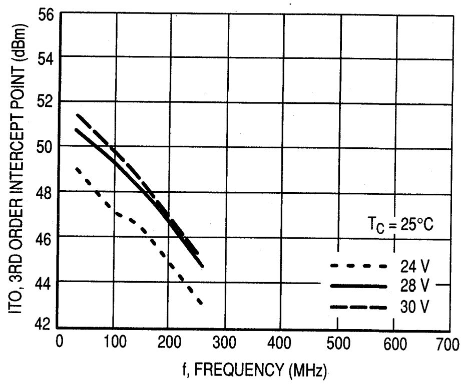


Figure 5. Third Order Intercept versus Voltage

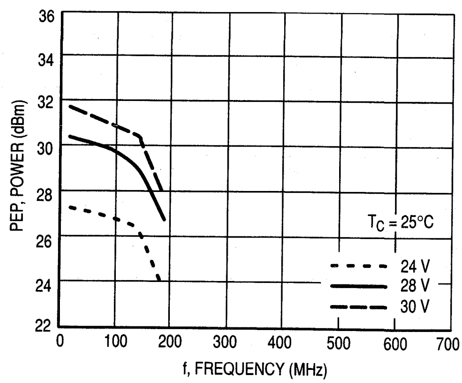


Figure 6. Peak Envelope Power versus Voltage

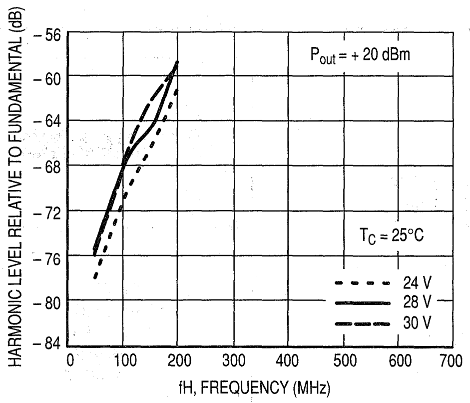


Figure 7. Second Harmonic Distortion versus Voltage

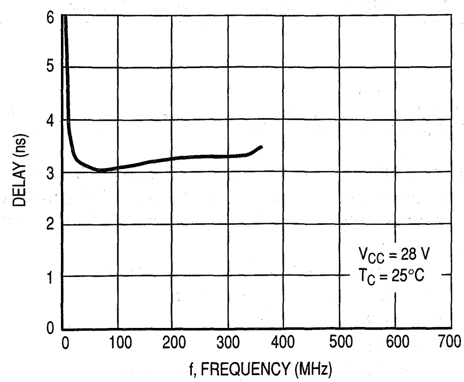


Figure 8. Group Delay versus Frequency

Biased at 28 Volts **T_C = 25°C Zo = 50Ω**

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
1	−16.7	64	36.0	23.3	−42	−5.2	−12.9	73
10	−21.5	21	36.2	−8.4	−47	−1.4	−21.9	28
50	−18.5	6.8	35.9	−56	−44	2.8	−17.9	−10
100	−16.9	−1.8	35.7	−103	−46	−68	−15.7	−48
200	−12.9	−18	34.7	145	−49	−98	−14.9	115

Magnitude in dB, Phase Angle in degrees.

Table 1. S–Parameters

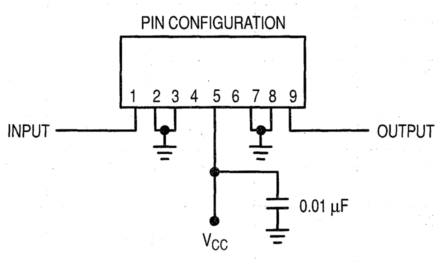
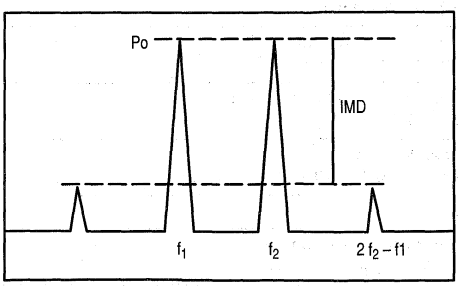


Figure 9. External Connections



ITO = Po + IMD / 2 @ IMD > 60 dB
PEP = 4 x Po @ IMD = – 32 dB

Figure 10. Intermodulation Test

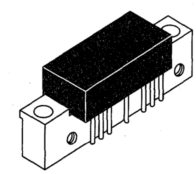
The RF Line
Wideband Linear Amplifier

CA2842C

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push–pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  Frequency Range — 10–400 MHz
  Output Power — 1580 mW Typ @ 1 dB Compression, f = 200 MHz, V_{CC} = 28 V
  Power Gain — 22 dB Typ @ f = 100 MHz
  PEP — 650 mW Min @ –32 dB IMD
  Noise Figure — 4 dB Typ @ f = 100 MHz
  ITO — 46 dBm @ f = 300 MHz
- All Gold Metallization for Improved Reliability
- Unconditional Stability Under All Load Conditions

22 dB
10–400 MHz
1.2 WATTS
WIDEBAND
LINEAR AMPLIFIER



CASE 714F–03, STYLE 1
[CA (POS. SUPPLY)]

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+14	dBm
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	400	MHz
Gain Flatness (f = 10–400 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	21	22	23	dB
Noise Figure, Broadband (f = 100 MHz)	NF	—	4	5	dB
Power Output — 1 dB Compression (f = 10–200 MHz, V_{CC} = 28 V)	$P_{o1\ dB}$	1260	1580	—	mW
Power Output — 1 dB Compression (f = 200–400 MHz, V_{CC} = 28 V)	$P_{o1\ dB}$	630	—	—	mW
Third Order Intercept (See Figure 10, f_1 = 10–400 MHz, See Fig. 10)	ITO	42	44	—	dBm
Input/Output VSWR (f = 10–400 MHz)	VSWR	—	1.3:1	1.5:1	—
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 300 MHz)	d_{so}	—	—	–50	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 10) (f = 200 MHz @ –32 dB IMD)	PEP	650	1000	—	mW
Supply Current	I_{CC}	200	230	250	mA

TYPICAL CHARACTERISTICS

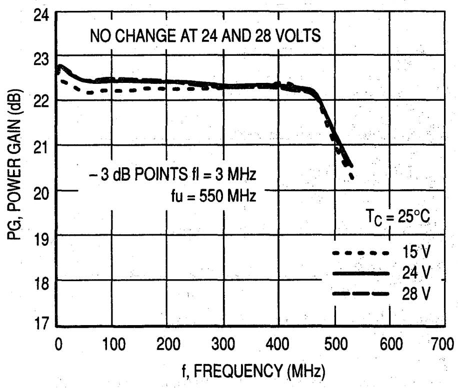


Figure 1. Power Gain versus Voltage

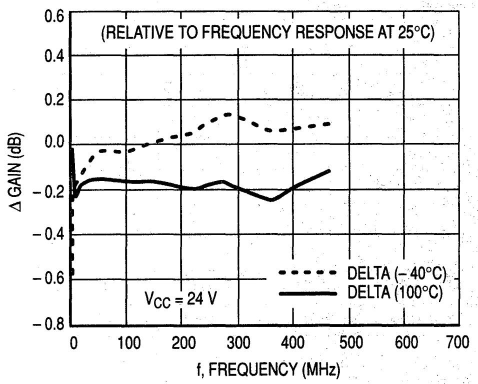


Figure 2. Relative Power Gain versus Temperature

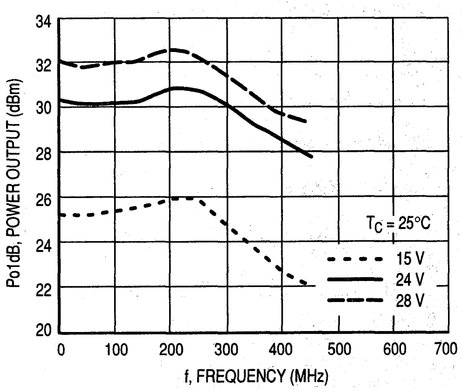


Figure 3. 1 dB Compression versus Voltage

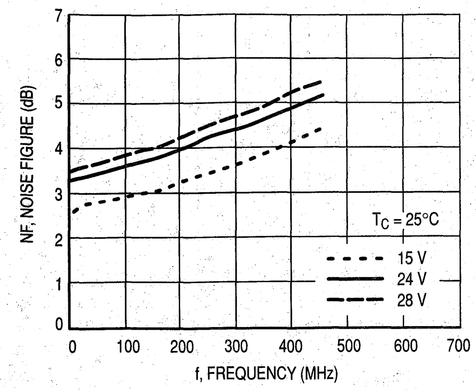


Figure 4. Noise Figure versus Voltage

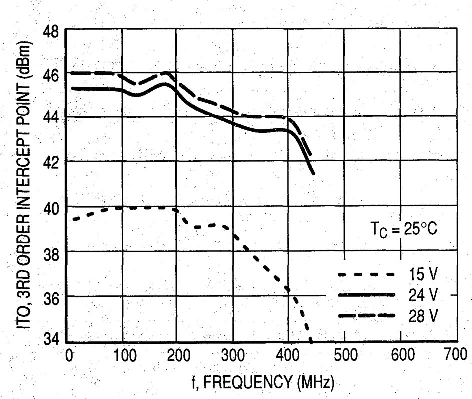


Figure 5. Third Order Intercept versus Voltage

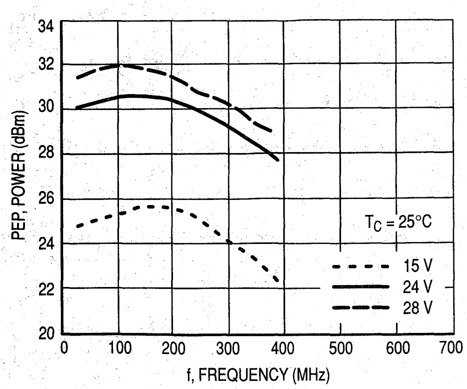


Figure 6. Peak Envelope Power versus Voltage

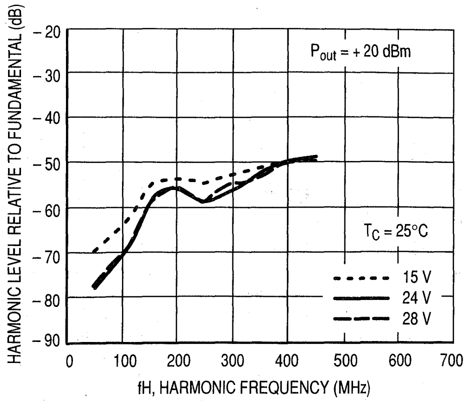


Figure 7. Second Harmonic Distortion versus Voltage

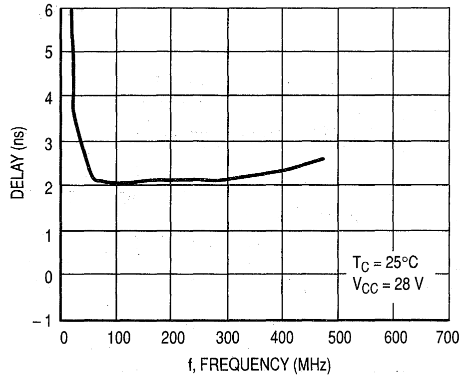


Figure 8. Group Delay versus Frequency

Biased at 24 Volts **T_C = 25°C Zo = 50Ω**

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
10	−15.8	62	22.8	−168	−27	15	−20.2	29
50	−26.5	20	22.5	146	−27	−25	−24	15
100	−25.5	25	22.5	111	−27.5	−56	−22.5	−16
200	−20.5	−7	22.5	26	−27.9	−117	−18.1	−73
300	−17.2	−48	22.5	−51	−28.5	−170	−16.5	−125
400	−18.8	−129	22.4	−126	−28.3	114	−22.5	156

Magnitude in dB, Phase Angle in degrees.

Table 1. S–Parameters

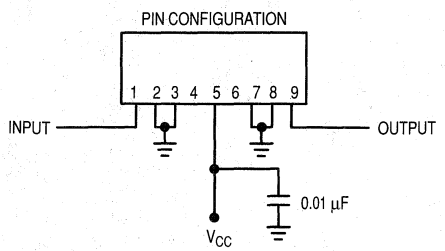
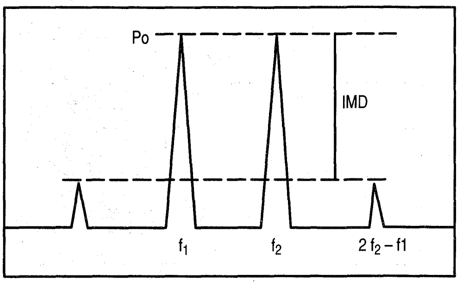


Figure 9. External Connections



ITO = Po + IMD / 2 @ IMD > 60 dB
PEP = 4 x Po @ IMD = – 32 dB

Figure 10. Intermodulation Test

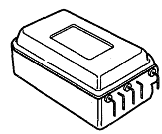
The RF Line
450 MHz CATV Feedforward Amplifier

MFF124B

Designed for broadband applications requiring low–distortion amplification. Specifically intended for CATV market requirements. Two hybrid amplifiers along with couplers and delay lines are packaged together to provide extremely low distortion products at conventional CATV amplifier output levels.

- Specifically Designed to Provide Improved Performance in 450 MHz CATV Applications
- Distortion Components Reduced more than 20 dB from Conventional CATV Hybrid Amplifiers
- Specified for 60–Channel Performance
- Fully Shielded Metal Package

**24 dB
40–450 MHz
60–CHANNEL
CATV
FEEDFORWARD
AMPLIFIER**



CASE 825A–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, T_C = 50°C, 75 Ω system unless otherwise noted)

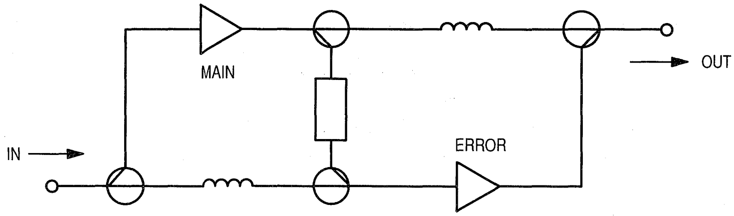
Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	550	MHz
Power Gain — 50 MHz	G_P	23.4	24	24.6	dB
Slope	S	+0.2	—	+1.4	dB
Gain Flatness	—	—	—	±0.2	dB
Return Loss — Input (f = 40–450 MHz)	IRL	18	—	—	dB
Return Loss — Output (f = 40–450 MHz)	ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch., ch. A, H2, H22)	IMD	—	—	–80	dB
Cross Modulation Distortion	XMD_{60}				dB
(V_{out} = 46 dBmV per ch., ch. 2, 60–channels)		—	–80	—	
(V_{out} = 46 dBmV per ch., ch. 2, —, H22)		—	—	–75	
Composite Triple Beat	CTB				dB
(V_{out} = 46 dBmV per ch., ch. 2, 60–channels)		—	–85	—	
(V_{out} = 46 dBmV per ch., ch. 2, —, H22)		—	—	–79	
Noise Figure (f = 50 MHz)	NF	—	—	9	dB
(f = 450 MHz)		—	—	10	
DC Current	I_{DC}	—	660	725	mA

REV 1

PERFORMANCE DERATE versus TEMPERATURE (TYP)

Symbol	Characteristics	Test Conditions	–20 +80°C	–20 +100°C
G	Gain	50 MHz	±0.5 dB	±0.6 dB

CIRCUITRY BLOCK DIAGRAM



PERFORMANCE MEASUREMENT
Motorola test fixture: P/N FF124BTF is necessary for accurate measurement.

The RF Line

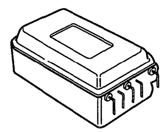
550 MHz CATV Feedforward Amplifier

MFF224B

Designed for broadband applications requiring low–distortion amplification. Specifically intended for CATV market requirements. Two hybrid amplifiers along with couplers and delay lines are packaged together to provide extremely low distortion products at conventional CATV amplifier output levels.

- Specifically Designed to Provide Improved Performance in 550 MHz CATV Applications
- Distortion Components Reduced more than 20 dB from Conventional CATV Hybrid Amplifiers
- Specified for 77–Channel Performance
- Fully Shielded Metal Package

24 dB
40–550 MHz
77–CHANNEL
CATV
FEEDFORWARD
AMPLIFIER



CASE 825A–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, T_C = 50°C, 75 Ω system unless otherwise noted)

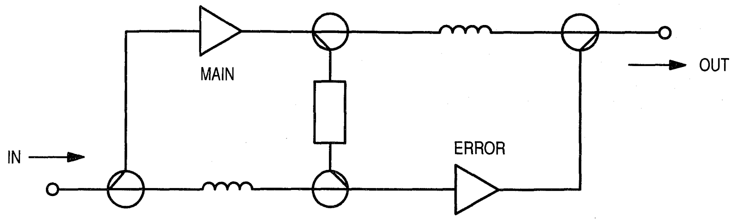
Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	550	MHz
Power Gain — 50 MHz	G_P	23.4	24	24.6	dB
Slope	S	+0.2	—	+1.8	dB
Gain Flatness	—	—	—	±0.25	dB
Return Loss — Input (f = 40−550 MHz)	IRL	18	—	—	dB
Return Loss — Output (f = 40−550 MHz)	ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch., ch. A, H2, H22)	IMD	—	—	–80	dB
Cross Modulation Distortion (V_{out} = 44 dBmV per ch., ch. 2, 77–channels) (V_{out} = 44 dBmV per ch., ch. 2, —, H39)	XMD_{77}	 — —	 −80 —	 — −70	dB
Composite Triple Beat (V_{out} = 44 dBmV per ch., ch. 2, 77–channels) (V_{out} = 44 dBmV per ch., ch. 2, —, H39)	CTB	 — —	 −85 —	 — −75	dB
Noise Figure (f = 50 MHz) (f = 550 MHz)	NF	— —	— —	9 11	dB
DC Current	I_{DC}	—	660	725	mA

REV 1

PERFORMANCE DERATE versus TEMPERATURE (TYP)

Symbol	Characteristics	Test Conditions	–20 +80°C	–20 +100°C
G	Gain	50 MHz	±0.5 dB	±0.6 dB

CIRCUITRY BLOCK DIAGRAM



PERFORMANCE MEASUREMENT
Motorola test fixture: P/N FF124BTF is necessary for accurate measurement.

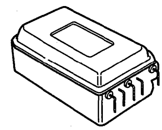
The RF Line
600 MHz CATV Feedforward Amplifier

MFF324B

Designed for broadband applications requiring low–distortion amplification. Specifically intended for CATV market requirements. Two hybrid amplifiers along with couplers and delay lines are packaged together to provide extremely low distortion products at conventional CATV amplifier output levels.

- Specifically Designed to Provide Improved Performance in 600 MHz CATV Applications
- Distortion Components Reduced more than 20 dB from Conventional CATV Hybrid Amplifiers
- Specified for 85–Channel Performance
- Fully Shielded Metal Package

24 dB
40–600 MHz
85–CHANNEL
CATV
FEEDFORWARD
AMPLIFIER



CASE 825A–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	28	V
RF Input Power	P_{in}	+55	dBmV
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

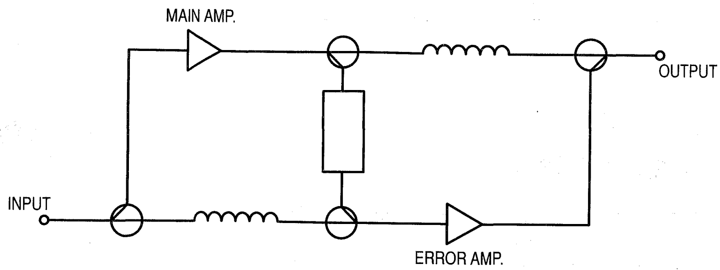
ELECTRICAL CHARACTERISTICS (T_C = 50°C, V_{CC} = 24 V, 75 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	600	MHz
Power Gain — 50 MHz	G_p	23.4	24	24.6	dB
Slope	S	+0.4	—	+2.0	dB
Gain Flatness	—	—	—	±0.25	dB
Return Loss — Input	IRL	18	—	—	dB
Return Loss — Output	ORL	18	—	—	dB
Cross Modulation Distortion (V_{out} = +44 dBmV per ch., ch. 2, —, H47)	XMD_{85}	—	—	–68	dB
Composite Triple Beat (V_{out} = +44 dBmV per ch., ch. 2, —, H47)	CTB_{85}	—	—	–73	dB
Noise Figure (f = 50 MHz) (f = 600 MHz)	NF	— —	— —	9.0 12.5	dB
DC Current	I_{DC}	—	660	725	mA

PERFORMANCE DERATE versus TEMPERATURE (TYP)

Symbol	Characteristics	Test Conditions	–20 + 80°C	–20 + 100°C
ΔG_p	Change in Gain w/Temp.	50 MHz	±0.5 dB	±0.6 dB

REV 1



PERFORMANCE MEASUREMENT

Motorola test fixture: P/N FF124BTF is necessary for accurate measurement.

Figure 1. Block Diagram of Circuit

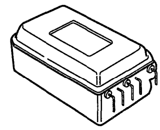
The RF Line
750 MHz CATV Feedforward Amplifier

MFF424B

Designed for broadband applications requiring low–distortion amplification. Specifically intended for CATV market requirements. Two hybrid amplifiers along with couplers and delay lines are packaged together to provide extremely low distortion products at conventional CATV amplifier output levels.

- Specifically Designed to Provide Improved Performance in 750 MHz CATV Applications
- Distortion Components Reduced more than 20 dB from Conventional CATV Hybrid Amplifiers
- Specified for 110 Channel Performance
- Fully Shielded Metal Package

**24 dB
40–750 MHz
110 CHANNEL
CATV FEEDFORWARD
AMPLIFIER**



CASE 825A–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	28	V
RF Input Power	P_{in}	+55	dBmV
Storage Temperature Range	T_{stg}	−40 to +100	°C
Operating Case Temperature Range	T_C	−20 to +100	°C

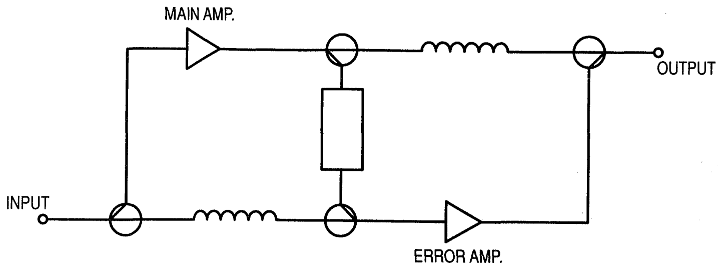
ELECTRICAL CHARACTERISTICS (T_C = 50°C, V_{CC} = 24 V, 75 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	750	MHz
Power Gain — 50 MHz	G_p	23.4	24	24.6	dB
Slope	S	+0.4	+0.9	+1.4	dB
Gain Flatness	—	—	—	±0.3	dB
Return Loss — Input	IRL	18	—	—	dB
Return Loss — Output	ORL	18	—	—	dB
Composite Triple Beat (V_{out} = +44 dBmV at ch. 2 to ch. M73) (9 dB Up slope, V_{out} = +46 dBmV at ch. M73)	 CTB_{110} flat CTB_{110} slope	 — —	 — −70	 −68 —	dB
Composite Second Order Beat (V_{out} = +44 dBmV at ch. 2 to ch. M73) (9 dB Up slope, V_{out} = +46 dBmV at ch. M73)	 CSO_{110} flat CSO_{110} slope	 — —	 — −72	 −70 —	dB
Noise Figure (f = 50 MHz) (f = 750 MHz)	NF	—	—	9.0 13.0	dB
DC Current	I_{DC}	—	660	725	mA

PERFORMANCE DERATE versus TEMPERATURE (TYP)

Symbol	Characteristic	Test Conditions	−20 + 80°C	−20 + 100°C
ΔG_p	Change in Gain w/Temp.	50 MHz	±0.5 dB	±0.6 dB

REV 2



PERFORMANCE MEASUREMENT

Motorola test fixture: P/N FF124BTF is necessary for accurate measurement.

Figure 1. Block Diagram of Circuit

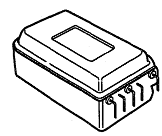
The RF Line
860 MHz CATV Feedforward Amplifier

MFF524B

Designed for broadband applications requiring low–distortion amplification. Specifically intended for CATV market requirements. Two hybrid amplifiers along with couplers and delay lines are packaged together to provide extremely low distortion products at conventional CATV amplifier output levels.

- Specifically Designed to Provide Improved Performance in 860 MHz CATV Applications
- Distortion Components Reduced more than 20 dB from Conventional CATV Hybrid Amplifiers
- Specified for 128 Channel Performance
- Fully Shielded Metal Package

**24 dB
40–860 MHz
128 CHANNEL
CATV FEEDFORWARD
AMPLIFIER**



CASE 825A–03, STYLE 2

MAXIMUM RATINGS

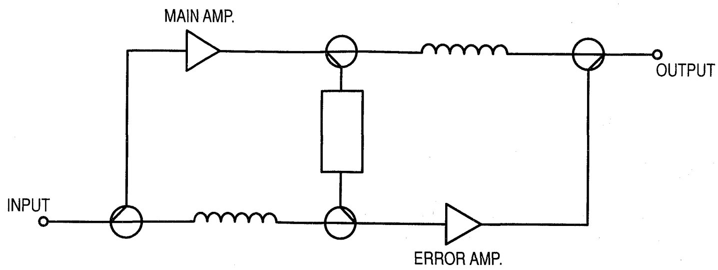
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	28	V
RF Input Power	P_{in}	+55	dBmV
Storage Temperature Range	T_{stg}	−40 to +100	°C
Operating Case Temperature Range	T_C	−20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 50°C, V_{CC} = 24 V, 75 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	860	MHz
Power Gain — 50 MHz	G_p	23.4	24	24.6	dB
Slope	S	+0.4	+1	+1.6	dB
Gain Flatness	—	—	—	±0.3	dB
Return Loss — Input f = 50 – 750 MHz f = 750 – 860 MHz	IRL	18 16	— —	— —	dB
Return Loss — Output f = 50 – 750 MHz f = 750 – 860 MHz	ORL	18 16	— —	— —	dB
Composite Triple Beat (1) (V_{out} = +44 dBmV at ch. 2, 55.25 MHz to ch. M90, 853.25 MHz)	CTB_{128} flat	—	−70	−66	dB
Composite Second Order Beat (1) (V_{out} = +44 dBmV at ch. 2, 55.25 MHz to ch. M90, 853.25 MHz)	CSO_{128} flat	—	−73	−68	dB
DIN45004B (See Figure 2)	DIN	—	130	—	dBμV
Noise Figure (f = 50 MHz) (f = 860 MHz)	NF	—	—	9.0 13.0	dB
DC Current	I_{DC}	—	660	725	mA

PERFORMANCE DERATE versus TEMPERATURE (TYP)

Symbol	Characteristic	Test Conditions	−20 + 80°C	−20 + 100°C
ΔG_p	Change in Gain w/Temp.	50 MHz	±0.5 dB	±0.6 dB



PERFORMANCE MEASUREMENT

Motorola test fixture: P/N FF124BTF is necessary for accurate measurement.

Figure 1. Block Diagram of Circuit

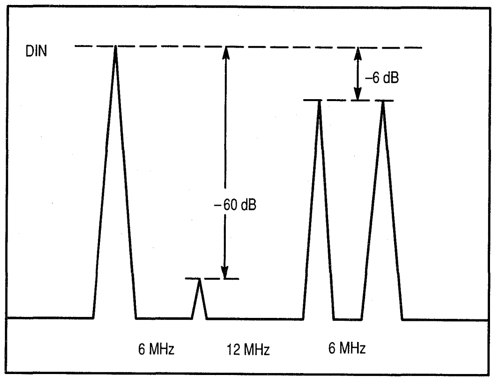


Figure 2. DIN45004B Test

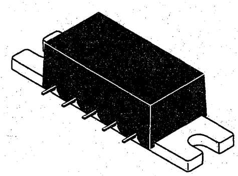
The RF Line
UHF Linear Amplifier

MHL8015
MHL8018

Designed for linear amplifier applications in 50 ohm systems requiring wide bandwidth, low noise, and low distortion. Internal DC blocking on RF ports reduces external component count and related circuit area. This hybrid utilizes push–pull circuit design.

- Supply Voltage: 15 Vdc (MHL8015)
  28 Vdc (MHL8018)
- Third Order Intercept: 38 dBm Typ
- Power Gain: 18.5 dB Typ (@ f = 900 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- 50 Ohm Input/Output Impedances

400 mW, 18.5 dB
40–1000 MHz
LINEAR AMPLIFIERS



CASE 448–02
MHL8015, STYLE 2
MHL8018, STYLE 1

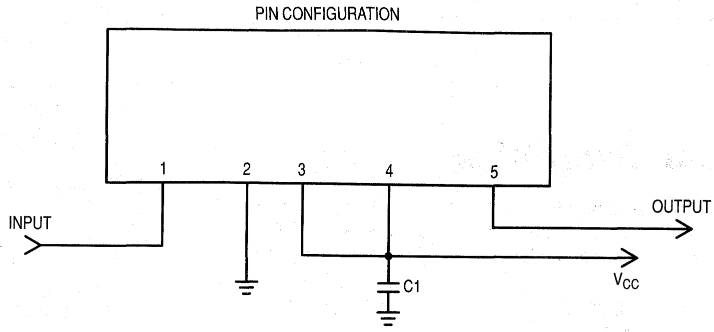
ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
DC Supply Voltage	MHL8015 MHL8018	V_{CC}	18 32	Vdc
RF Input Power		P_{in}	+14	dBm
Storage Temperature Range		T_{stg}	–40 to +100	°C
Operating Case Temperature Range		T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C; V_{CC} = 15 Vdc (MHL8015), 28 Vdc (MHL8018); 50 Ω System)

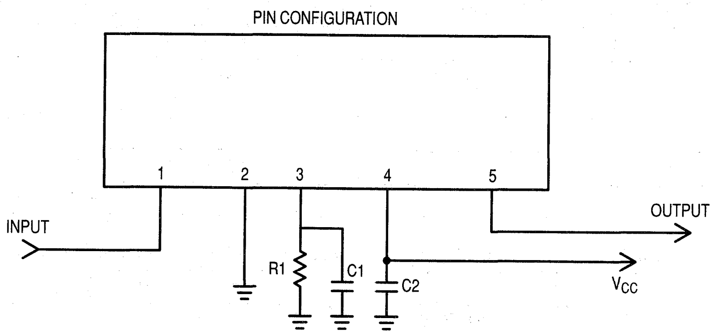
Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current	MHL8015 MHL8018	I_{DC}	— —	380 210	410 240	mA
Power Gain	(f = 900 MHz)	P_G	17.5	18.5	19.5	dB
Gain Flatness	(f = 40–1000 MHz)	FL	—	1.0	2.0	dB
Power Output @ 1 dB Comp.	(f = 900 MHz)	P_{out} 1 dB	25	26	—	dBm
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	37	38	—	dBm
Input/Output VSWR	(f = 40–900 MHz) (f = 900–1000 MHz)	VSWR	— —	— —	2.0:1 2.6:1	
Noise Figure, Broadband	(f = 500 MHz) (f = 1000 MHz)	NF	— —	6.5 7.5	8.0 9.0	dB
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1000 MHz)		dso	—	–50	–40	dB
Second Order Intermodulation Distortion (P_o = 2.75 dBm, f_1 = 373 MHz, f_2 = 450 MHz)		IM2	—	—	–60	dB
Intermodulation Distortion, 3 Tone (f = 860 MHz, P_{sync} = 200 mW)		IM3	—	–60	—	dB

REV 1



C1 ≥ 0.01 μF (CHIP)

Figure 1. MHL8015 External Connections
(Case 448–02, Style 2)



C1, C2 ≥ 0.01 μF (CHIP)
R1 = 200 Ω, 1 WATT

Figure 2. MHL8018 External Connections
(Case 448–02, Style 1)

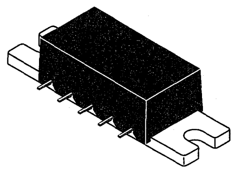
The RF Line
UHF Linear Amplifier

MHL8115
MHL8118

Designed for linear amplifier applications in 50 Ohm systems requiring wide bandwidth, low noise, and low distortion. Internal DC blocking on RF ports reduces external component count and related circuit area. This hybrid utilizes push–pull circuit design.

- Supply Voltage: 15 Vdc (MHL8115)
  28 Vdc (MHL8118)
- Third Order Intercept: 41.5 dBm Typ
- Power Gain: 17.5 dB Typ (@ 900 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- 50 Ohm Input/Output Impedances

1 W, 17.5 dB
50–1000 MHz
LINEAR AMPLIFIERS



CASE 448–02
MHL8115, STYLE 2
MHL8118, STYLE 1

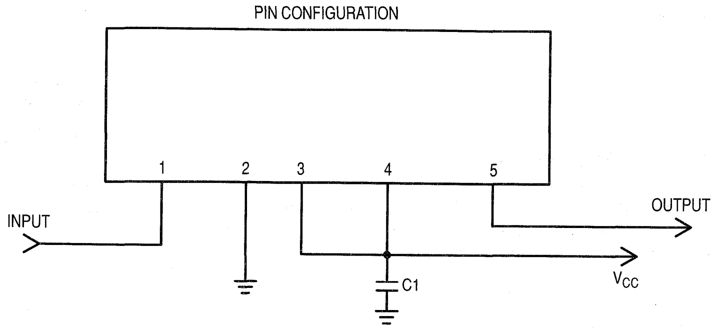
ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
DC Supply Voltage	MHL8115 MHL8118	V_{CC}	18 32	Vdc
RF Input Power		P_{in}	+20	dBm
Storage Temperature Range		T_{stg}	–40 to +100	°C
Operating Case Temperature Range		T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = +25°C; V_{CC} = 15 Vdc (MHL8115), 28 Vdc (MHL8118); 50 Ω System)

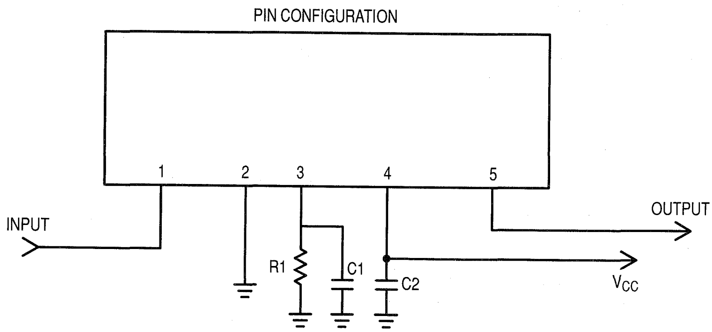
Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current	MHL8115 MHL8118	I_{DC}	— —	700 400	760 440	mA
Power Gain	(f = 900 MHz)	P_G	16.5	17.5	—	dB
Gain Flatness	(f = 50–1000 MHz)	FL	—	1.0	2.0	dB
Power Output @ 1 dB Comp.	(f = 900 MHz)	P_{out} 1 dB	29	30	—	dBm
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	40.5	41.5	—	dBm
Input/Output VSWR	(f = 50–900 MHz) (f = 900–1000 MHz)	VSWR	— —	— —	2.0:1 2.6:1	
Noise Figure, Broadband	(f = 500 MHz) (f = 1000 MHz)	NF	— —	7.5 8.5	8.5 9.5	dB
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1000 MHz)		dso	—	–55	–45	dB
Second Order Intermodulation Distortion (P_o = 2.75 dBm, f_1 = 373 MHz, f_2 = 450 MHz)		IM2	—	–65	–60	dB
Intermodulation Distortion, 3 Tone (f = 860 MHz, P_{sync} = 200 mW)		IM3	—	–60	—	dB

REV 1



C1 ≥ 0.01 µF (CHIP)

Figure 1. MHL8115 External Connections (Case 448–02, Style 2)



C1, C2 ≥ 0.01 µF (CHIP)
R1 = 90 Ω, 3 WATTS

Figure 2. MHL8118 External Connections (Case 448–02, Style 1)

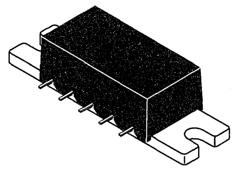
The RF Line
UHF Linear Amplifier

MHL9125
MHL9128

1.3 W, 20 dB
800–960 MHz
LINEAR AMPLIFIERS

Designed specifically for linear amplifier applications in the cellular frequency band. Internal DC blocking on RF ports reduces external component count and related circuit area. These devices can be easily combined for higher power applications.

- Supply Voltage: 15 Vdc (MHL9125)
  28 Vdc (MHL9128)
- Third Order Intercept: 43 dBm Typ
- Power Gain: 20 dB Typ (@ f = 900 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- 50 Ohm Input/Output Impedances



CASE 448–02
MHL9125, Style 2
MHL9128, Style 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise stated)

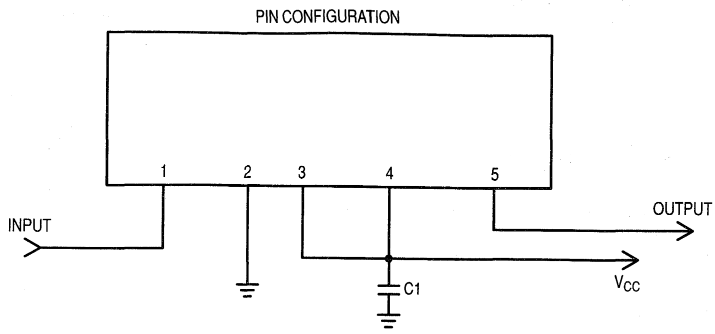
Rating		Symbol	Value	Unit
DC Supply Voltage	MHL9125 MHL9128	V_{CC}	18 32	Vdc
RF Input Power		P_{in}	+20	dBm
Operating Case Temperature Range		T_C	–20 to +100	°C
Storage Temperature Range		T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 Vdc (MHL9125), 28 Vdc (MHL9128); T_C = 25°C; 50 Ω System, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current	MHL9128 MHL9125	I_{DC}	400 700	— —	440 760	mA
Power Gain (1)	(f = 900 MHz)	P_G	19	20	21	dB
Absolute Phase Variation (1)	(f = 900 MHz)	$\Delta\phi$		±8	±18	Deg.
Gain Flatness	(f = 800–960 MHz)	G_F	—	0.5	0.75	dB
Power Output @ 1 dB Comp.	(f = 900 MHz)	P_{out} 1 dB	30	31	—	dBm
Input VSWR	(f = 800–920 MHz) (f = 920–960 MHz)	$VSWR_{in}$	— —	1.25:1 1.50:1	1.5:1 1.9:1	
Output VSWR	(f = 800–960 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	42	43	—	dBm
Noise Figure	(f = 960 MHz)	NF	—	7.5	9.5	dB

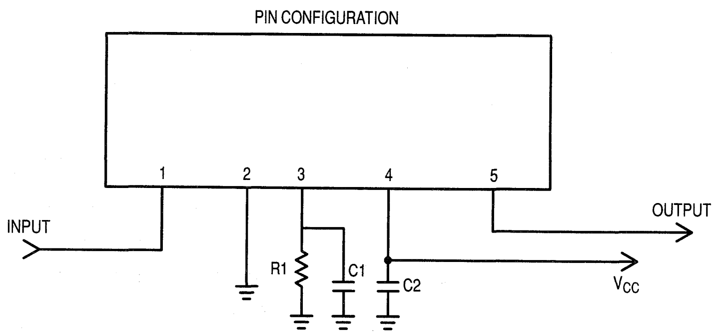
(1) Consult factory for tighter gain and/or phase windows.

REV 1



C1 ≥ 0.01 μF (CHIP)

Figure 1. MHL9125 External Connections (Case 448–02, Style 2)



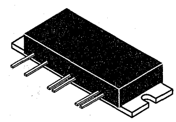
C1, C2 ≥ 0.01 μF (CHIP)
R1 = 90 Ω, 3 WATTS

Figure 2. MHL9128 External Connections (Case 448–02, Style 1)

The RF Line
VHF Power Amplifier

MHW105

**5.0 W
68 to 88 MHz
VHF POWER
AMPLIFIER**



CASE 301K–02, STYLE 3

The MHW105 is designed specifically for portable radio applications. The MHW105 is capable of 5.0 watts power output, operates from a 7.5 volt supply and requires only 1.0 mW of RF input power.

- Specified 7.5 Volt Characteristics:
  RF Input Power — 1.0 mW (0 dBm)
  RF Output Power — 5.0 W
  Minimum Gain — 37 dB
  Harmonics — −40 dBc Max @ 2 f_0
- 50 Ohm Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability

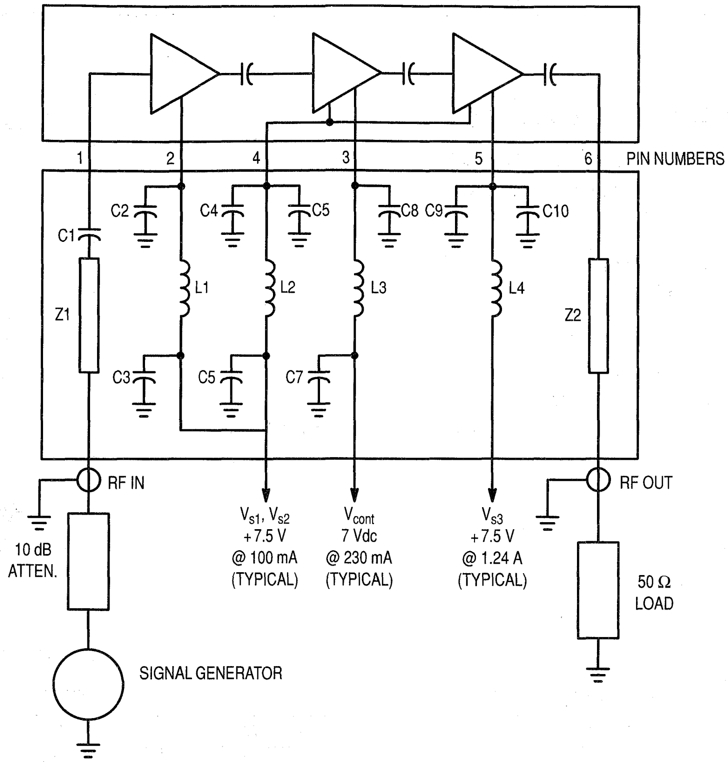
MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{s3}	9.0	Vdc
DC Control & Bias Voltage	$V_{s1,2}$	9.0	Vdc
DC Control Voltage	V_{cont}	9.0	Vdc
RF Input Power	P_{in}	5.0	mW
RF Output Power (V_{cont} = 9.0 Vdc)	P_{out}	7.0	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−30 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{s1} = V_{s2} = V_{s3} = 7.5 Vdc; V_{cont} ≤ 7.0 Vdc; T_C = +25°C, 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range	BW	68	88	MHz
Power Gain (P_{out} = 5.0 W) (1)	G_P	37	—	dB
Control Voltage (P_{in} = 1.0 mW; P_{out} = 5.0 W) (1)	V_{cont}	—	7.0	Vdc
Efficiency (P_{out} = 5.0 W) (1)	η	40	—	%
Harmonics (P_{out} = 5.0 W) (1) 2 f_0, 3 f_0	—	—	−40	dBc
Input VSWR (P_{out} = 5.0 W) (1)	$VSWR_{in}$	—	2.0:1	—
Load Mismatch (V_{s1} = V_{s2} = V_{s3} = 9.0 Vdc; Load VSWR = 20:1; P_{out} = 5.0 W) (1)	ψ	No Degradation in Power Output Before and After Test		
Stability (P_{in} = 1.0 to 3.0 mW; V_{s1} = V_{s2} = V_{s3} = 6.0 to 9.0 Vdc; P_{out} = 1.0 W to 5.0 W; Load VSWR = 8:1, All Phase Angles) (1)	—	All Spurious Outputs More Than 60 dB Below Desired Signal		
Quiescent Current (V_{s1} = V_{s2} = V_{s3} = 7.5 Vdc; V_{cont} = 7.0 Vdc; P_{in} = 0)	I_Q	—	200	mA

NOTE:
1. Adjust V_{cont} for specified P_{out}



C1, C2, C3, C4, C6, C7, C8, C9 — 18,000 pF CHIP
C5, C10 — 3.3 μF TANTALUM CHIP
L1, L2, L3, L4 — 0.2 μH
Z1, Z2 — 50 Ω MICROSTRIP LINE

Figure 1. VHF Power Module Test Circuit Diagram

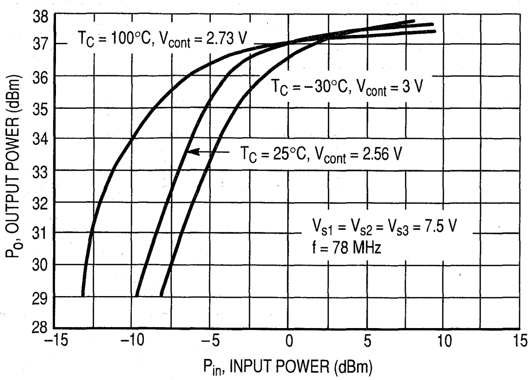


Figure 2. Output Power versus Input Power

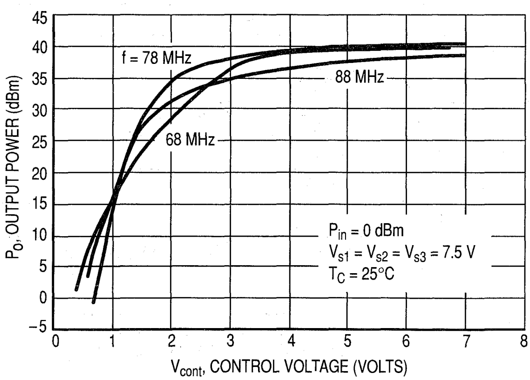


Figure 3. Output Power versus Control Voltage

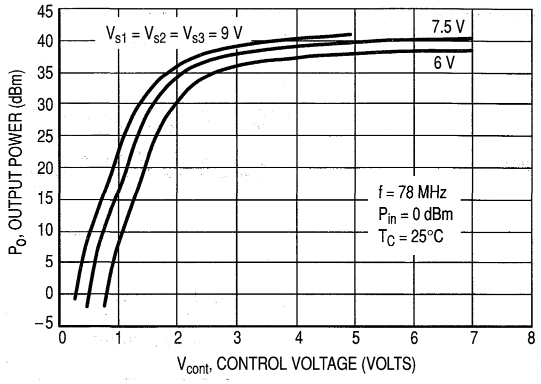


Figure 4. Output Power versus Control Voltage

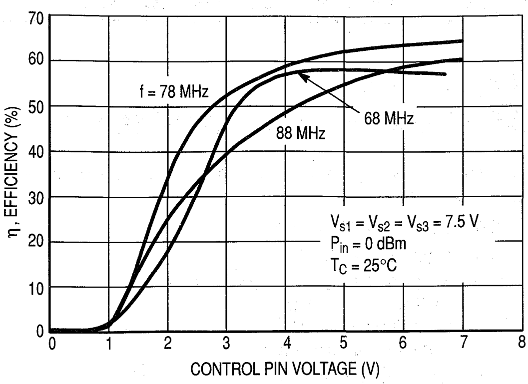


Figure 5. Efficiency versus Control Voltage

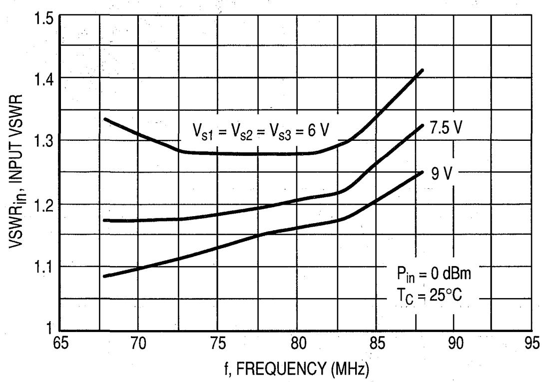


Figure 6. Input VSWR versus Frequency

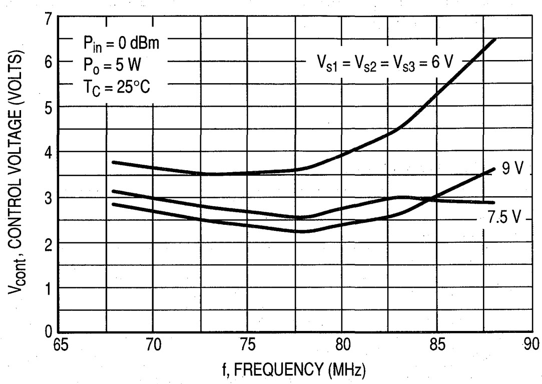


Figure 7. Control Voltage versus Frequency

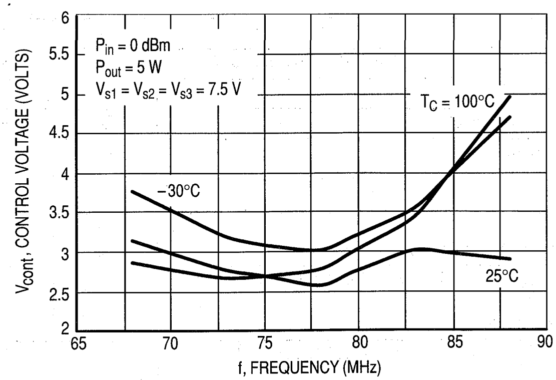


Figure 8. Control Voltage versus Frequency

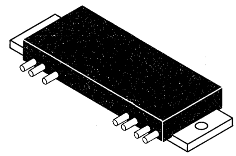
The RF Line
UHF Power Amplifiers

MHW720A1
MHW720A2

Capable of wide power range control as encountered in UHF cellular telephone applications.

- MHW720A1 400–440 MHz
- MHW720A2 440–470 MHz
- Specified 12.5 Volt, UHF Characteristics —
  Output Power = 20 Watts
  Minimum Gain = 21 dB
  Harmonics = –40 dB (Max)
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

20 W, 400 to 470 MHz
RF POWER
AMPLIFIERS



CASE 700–04, STYLE 2

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating		Symbol	Value	Unit
DC Supply Voltages		V_{s1}, V_{s2}	15.5	Vdc
RF Input Power		P_{in}	250	mW
RF Output Power (@ V_{s1} = V_{s2} = 12.5 V)		P_{out}	25	W
Operating Case Temperature Range		T_C	−30 to +100	°C
Storage Temperature Range	MHW720A1, MHW720A2	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{s1} and V_{s2} set at 12.5 Vdc, T_C = 25°C, 50 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Frequency Range	MHW720A1 MHW720A2	—	400 440	440 470	MHz
Input Power (P_{out} = 20 W)		P_{in}	—	150	mW
Power Gain (P_{out} = 20 W)		G_p	21	—	dB
Efficiency (P_{out} = 20 W)	MHW720A1, MHW720A2	η	35	—	%
Harmonics (P_{out} = 20 W, Reference)		—	—	–40	dB
Input Impedance (P_{out} = 20 W, 50 Ω Reference)		Z_{in}	—	2:1	VSWR
Gain Degradation (1) (P_{out} = 20 W, Reference Gain @ T_C = + 25°C)	T_C = –30°C T_C = +80°C	—	— —	–0.7 –0.7	dB
Load Mismatch (VSWR = 30:1, V_{s1} = V_{s2} = 15.5 Vdc, P_{out} = 30 W)		—	No degradation in P_{out}		
Stability (P_{in} = 0 to 250 mW, V_{s1} = V_{s2} = 10 to 15.5 Vdc) 1. Load VSWR = 4:1, 50 Ω Reference 2. Source VSWR = 2:1, 50 Ω Refernece	MHW720A1, MHW720A2	—	All spurious outputs more than 60 dB below desired signal		
Quiescent Current (I_{s1} No RF Drive Applied)	MHW720A1, MHW720A2	$I_{s1\ (q)}$	—	200	mA

NOTE:
1. See Figure 5, Input Power versus Case Temperature

REV 7

APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the nominal conditions of Vs_1 (Pin 5) and V_{s2} (Pin 3) equal to 12.5 Vdc and with output power equaling 20 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100° base plate temperature is 165°. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use has been made with the factory representative.

Gain Control

This module is designed for wide range P_{out} level control. The recommended method of power output control, as shown in Figure 3, is to fix V_{s1} and V_{s2} at 12.5 Vdc and vary the input RF drive level at Pin 7.

In all applications, the module output power should be limited to 20 watts.

Decoupling

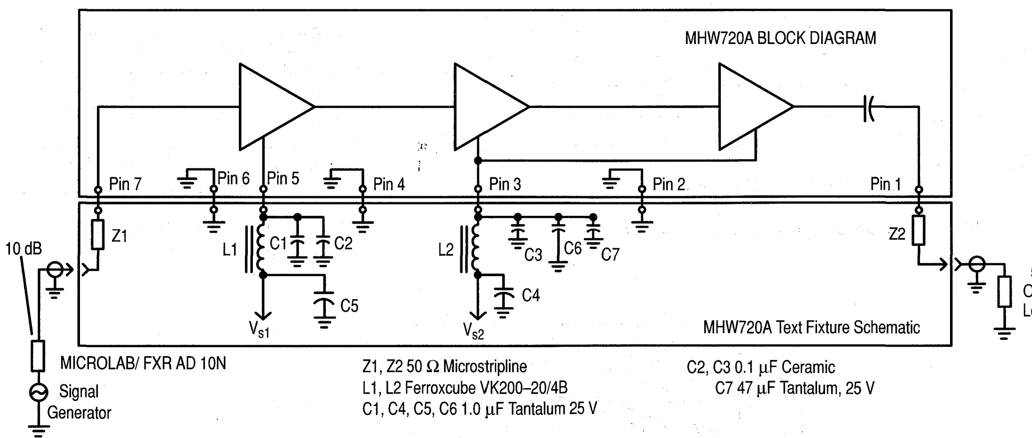
Due to the high gain of the three stages and the module size limitation, the external decoupling network requires careful consideration. Both Pins 3 and 5 are internally bypassed with a 0.018 µF chip capacitor effective for frequencies from 5 through 470 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test fixture schematic are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR less than 4:1.

Load Mismatch

During final test, each module is load mismatch tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_{s1} and V_{s2} equal 15.5 V, load VSWR infinite, and output power equal to 30 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.005 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB–107.



NOTE: No Internal D.C. blocking on input pin.

Figure 1. UHF Power Amplifier Test Setup

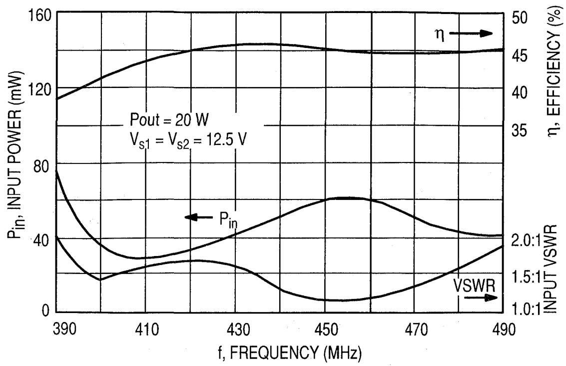


Figure 2. Input Power, Efficiency, and VSWR versus Frequency

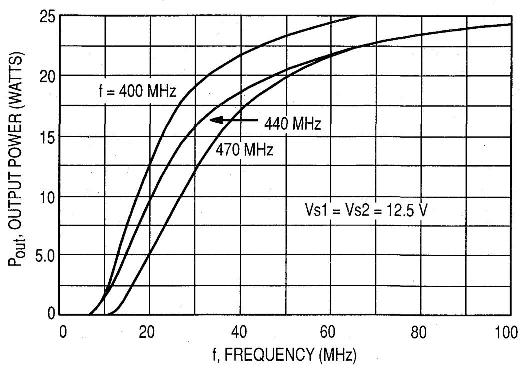


Figure 3. Output Power versus Input Power

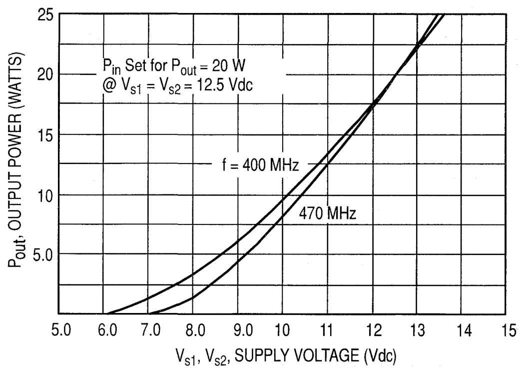


Figure 4. Output Power versus Voltage

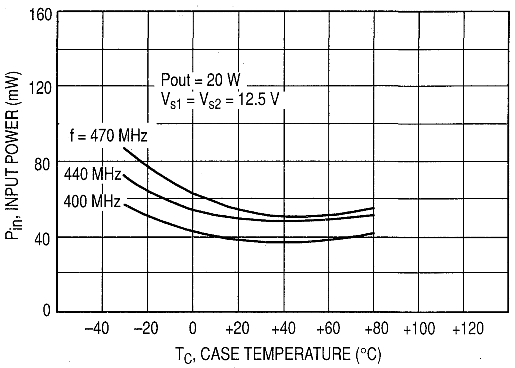


Figure 5. Input Power versus Case Temperature

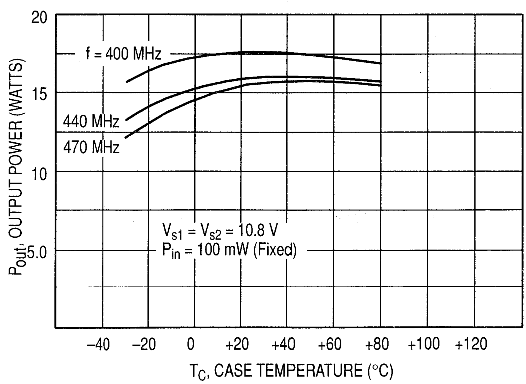


Figure 6. Output Power versus Case Temperature @ 10.8 V Supply

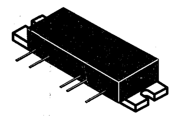
The RF Line
UHF Power Amplifiers

MHW803-2

Capable of wide power range control as encountered in portable cellular radio applications (30 dB typical).

- MHW803–2 806–870 MHz
- Specified 7.5 Volt Characteristics
  RF Input Power = 1 mW (0 dBm)
  RF Output Power = 2 Watts
  Minimum Gain ($V_{Control}$ = 4 V) = 33 dB
  Harmonics = −45 dBc Max @ 2 f_o
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**2 W, 806 to 905 MHz
UHF POWER
AMPLIFIERS**



CASE 301E–04, STYLE 1

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 2,3,4)	$V_{s1,2,3}$	10	Vdc
DC Control Voltage (Pin 1)	V_{Cont}	4	Vdc
RF Input Power	P_{in}	3	mW
RF Output Power (V_{s1} = V_{s2} = V_{s3} = 10 V)	P_{out}	3	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−30 to +100	°C

ELECTRICAL CHARACTERISTICS V_{s1} = V_{s2} = V_{s3} = 7.5 Vdc, (Pins 2,3,4), T_C = 25°C, 50 Ω System

Characteristic	Symbol	Min	Max	Unit
Frequency Range	—	806	870	MHz
Control Voltage (P_{out} = 2 W, P_{in} = 1 mW) (1)	V_{Cont}	0	4	Vdc
Quiescent Current (V_{s1}, Pin 2 = 7.5 Vdc) (2)	$I_{s1(q)}$	—	65	mA
Power Gain (P_{out} = 2 W, V_{Cont} = 4 Vdc)	G_p	33	—	dB
Efficiency (P_{out} = 2 W, P_{in} = 1 mW) (1)	η	37	—	%
Harmonics (P_{out} = 2 W) (1) 2 f_o (P_{in} = 1 mW) 3 f_o	—	—	−45 −55	dBc
Input VSWR (P_{out} = 2 W, P_{in} = 1 mW), 50 Ω Ref. (1)	—	—	2.0:1	—
Noise power 30 kHz Bandwidth, 45 MHz above fo (P_{out} = 2 W (1) T_C = +25°C (P_{in} = 1 mW) T_C = +100°C	 — —	 — —	 −85 −82	 dBm dBm
Load Mismatch (V_{s1} = V_{s2} = V_{s3} = 10 Vdc) VSWR = 10:1, P_{out} = 3 W, P_{in} = 3 mW (1)		No Degradation in Power Output		
Stability (P_{in} = 0.5–2 mW, V_{s1} = V_{s2} = V_{s3} = 6–9 Vdc) P_{out} between 0 mW and 2 W (1) Load VSWR = 6:1, Source VSWR = 3:1)		All spurious outputs more than 60 dB below desired signal		

NOTES:
1. Adjust V_{cont} for specified P_{out}.
2. V_{Cont} = 0 Vdc.

REV 7

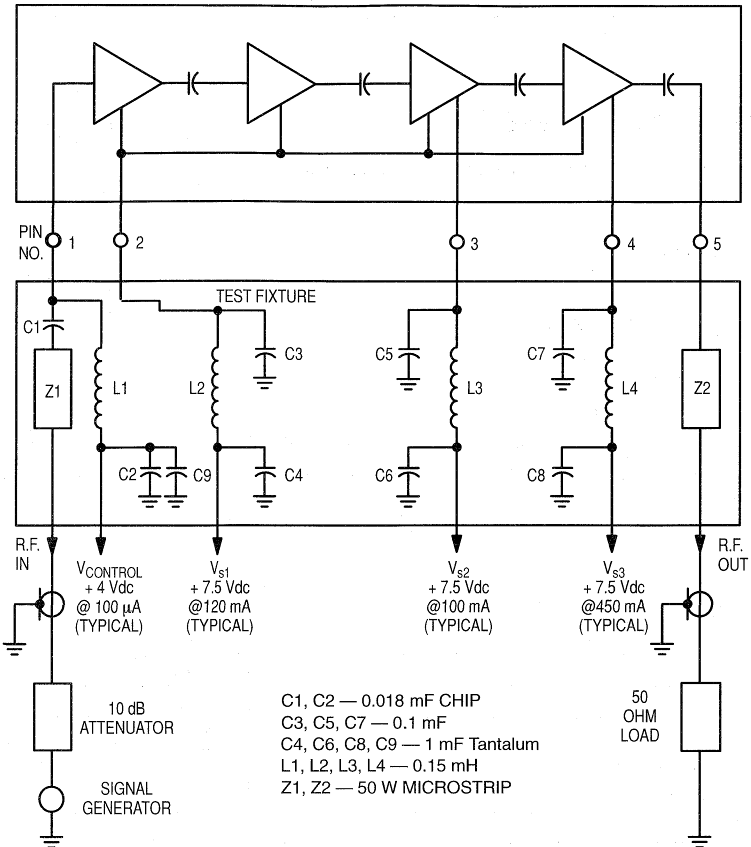


Figure 1. Power Module Test System Block Diagram

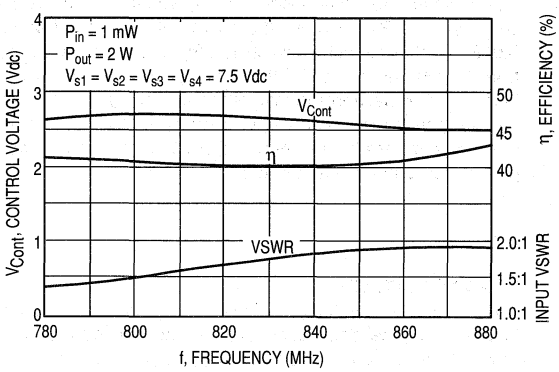


Figure 2. Control Voltage, Efficiency and VSWR versus Frequency

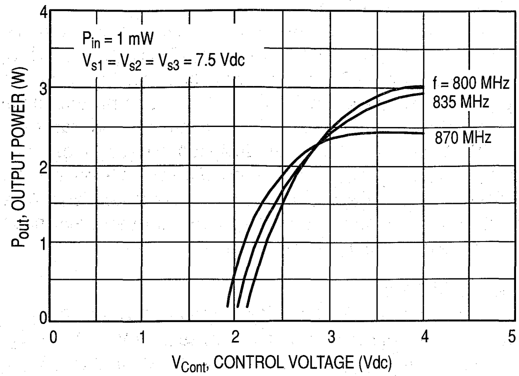


Figure 3. Output Power versus Control Voltage

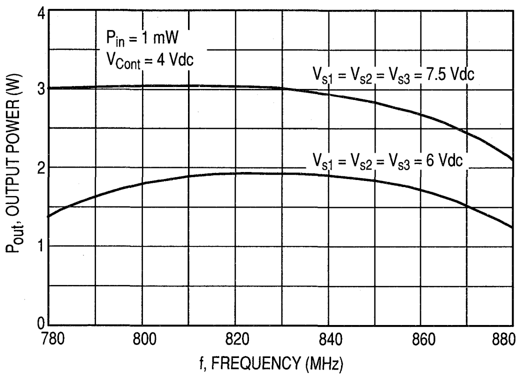


Figure 4. Output Power versus Frequency

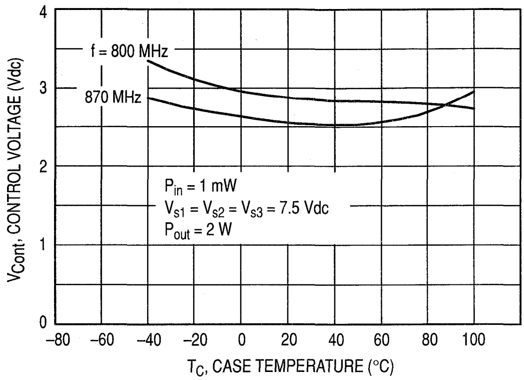


Figure 5. Control Voltage versus Case Temperature

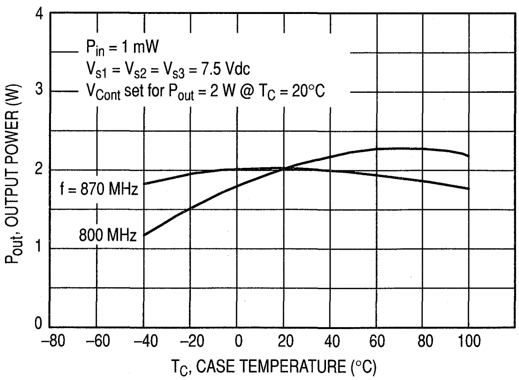


Figure 6. Output Power versus Case Temperature

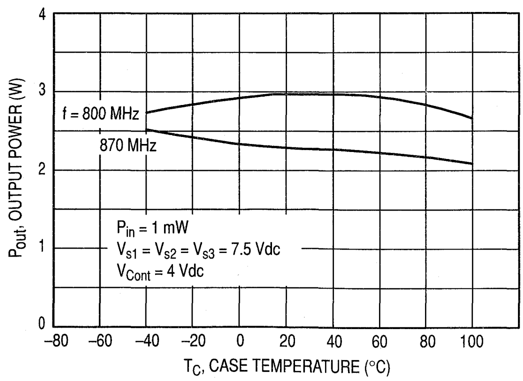


Figure 7. Output Power versus Case Temperature at Maximum Control Voltage

APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of $V_{s1} = V_{s2} = V_{s3} = 7.5$ Vdc (Pins 2, 3, 4) and P_{out} equal to 2 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100°C case operating temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

GAIN CONTROL

The module output should be limited to 2 watts. The preferred method of power output control is to fix $V_{s1} = V_{s2} = V_{s3} = 7.5$ Vdc (Pins 2, 3, 4), P_{in} (Pin 1) at 1 mW, and vary V_{Cont} (Pin 1) voltage.

DECOUPLING

Due to the high gain of the three stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 4 are internally bypassed with a 0.018 µF chip capacitor which is effective for frequencies from 5 MHz through 905 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are $V_{s1} = V_{s2} = V_{s3}$ equal to 10 Vdc, VSWR equal to 10:1, and output power equal to 3 watts.

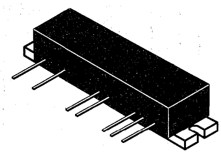
The RF Line
UHF Power Amplifiers

MHW804-1

Designed specifically for portable radio applications. The MHW804 is capable of wide power range control, operates from a 7.5 volt supply and requires only 1.0 mW of RF input power.

- Specified 7.5 Volt Characteristics:
  - RF Input Power — 1.0 mW (0 dBm)
  - RF Output Power — 4.0 W
  - Minimum Gain — 36 dB
  - Harmonics — –45 dBc Max @ 2.0 f_o
- 50 Ohm Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

4.0 WATTS
800 to 870 MHz
RF POWER
AMPLIFIERS



CASE 301F–03, STYLE 1

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_s	10	Vdc
DC Control Voltage	V_{cont}	4.0	Vdc
RF Input Power	P_{in}	5.0	mW
RF Output Power	P_{out}	6.0	W
Operating Case Temperature Range	T_C	– 30 to +100	°C
Storage Temperature Range	T_{stg}	– 30 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = + 25°C, 50 ohm system, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range	BW	800	870	MHz
Power Gain ($V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5}$ = 7.5 V; V_{cont} = 3.75 V)	G_p	36	—	dB
Control Voltage (P_{in} = 0 dBm, P_{out} = 4.0 W, $V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5}$ = 7.5 V, Adjust V_{cont} for specified P_{out})	V_{cont}	—	3.75	Vdc
Efficiency (Same condition as for V_{cont})	η	32	—	%
Current Drain (Same conditions as for V_{cont}) IS1 + IS4 (Pins 2, 5) IS2 + IS3 + IS5 (Pins 3, 4, 6) $I_{control}$ (Pin 1)	I_D	— — —	210 1430 0.2	mA
Input VSWR (Same conditions as for V_{cont})	$VSWR_{in}$	—	2.0:1	—
Harmonic Content (Same conditions as for V_{cont}) 2.0 f_o 3.0 f_o	—	— —	– 45 – 50	dBc
Leakage Current — $I_{s2} + I_{s3} + I_{s5}$ ($V_{s2} = V_{s3} = V_{s5}$ = 7.5 V; $V_{s1} = V_{s4}$ = 0 V V_{cont} = 0 V; P_{in} = 0 mW)	I_L	—	0.3	mA
Standby Current — $I_{s1} + I_{s4}$ ($V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5}$ = 7.5 V V_{cont} = 4.0 V; P_{in} = 0 mW)	I_S	—	220	mA
Load Mismatch Stress ($V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5}$ = 9.0 V; P_{in} = 2.0 mW; P_{out} = 6.0 W; Load VSWR = 20:1, All Phase Angles. Adjust V_{cont} for Specified P_{out})	ψ	No Degradation in Output Power		
Stability ($V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5}$ = 6.0 to 9.0 V; P_{IN} = – 1.0 dBm to + 3.0 dBm; P_{out} = 1.0 W to 4.0 W; Load VSWR = 6:1, All Phase Angles; Adjust V_{cont} for Specified P_{out})	—	All Spurious Outputs More Than 60 dB Below Desired Signal		

REV 7

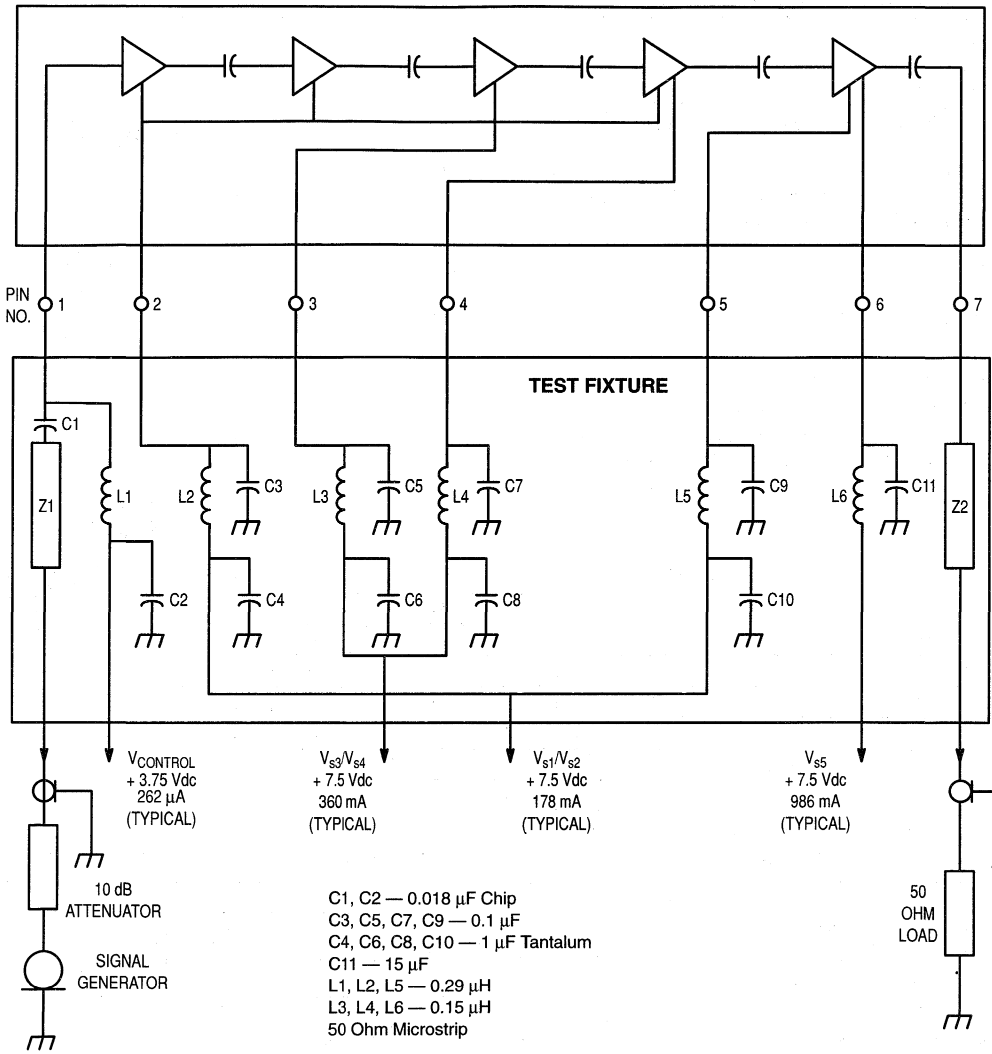


Figure 1. Power Module Test System Block Diagram

TYPICAL CHARACTERISTICS

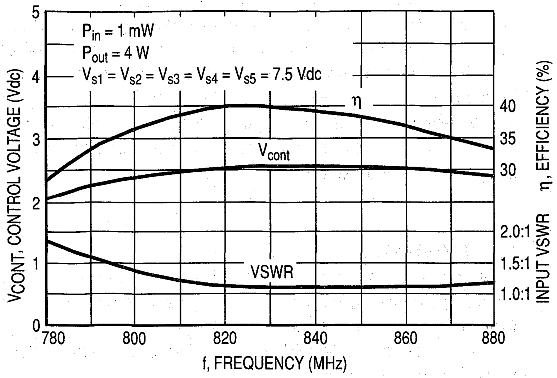


Figure 2. Control Voltage, Efficiency and VSWR versus Frequency

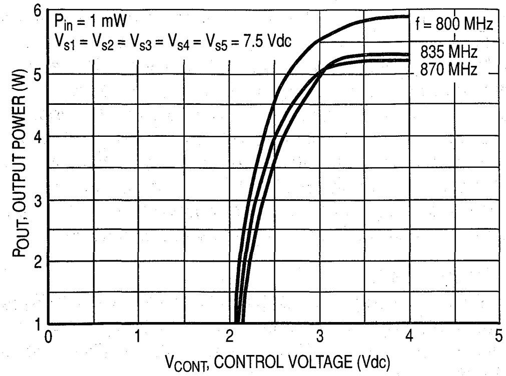


Figure 3. Output Power versus Control Voltage

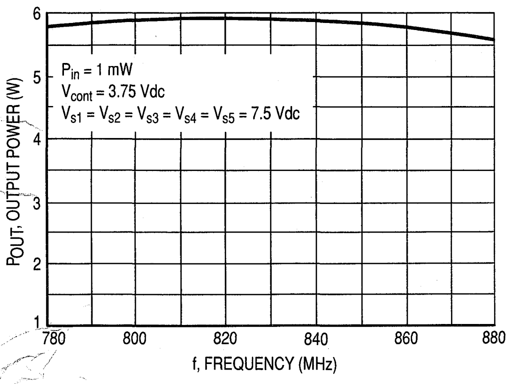


Figure 4. Output Power versus Frequency

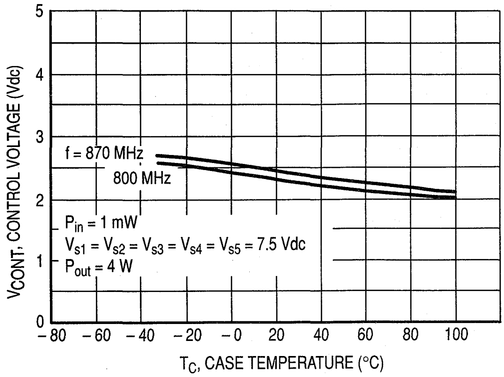


Figure 5. Control Voltage Case Temperature

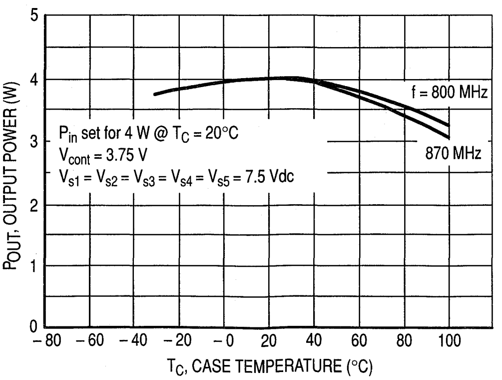


Figure 6. Output Power versus Case Temperature

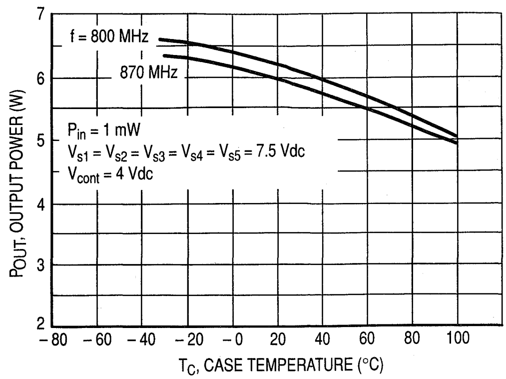


Figure 7. Output Power versus Case Temperature at Maximum Control Voltage

APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of $V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5} = 7.5$ Vdc (Pins 2, 3, 4, 5, 6) and P_{out} equal to 4.0 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100°C case operating temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

GAIN CONTROL

The module output should be limited to 4.0 watts. The preferred method of power output control is to fix $V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5} = 7.5$ Vdc (Pins 2, 3, 4, 5, 6), P_{in} (Pin 1) at 1.0 mW, and vary V_{cont} (Pin 1) voltage.

DECOUPLING

Due to the high gain of the four stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3, 4, and 6 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5.0 MHz through 925 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

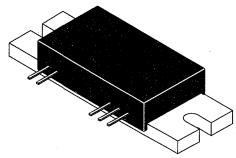
LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are $V_{s1} = V_{s2} = V_{s3} = V_{s4} = V_{s5}$ equal to 9.0 V, VSWR equal to 20:1, and output power equal to 6.0 watts.

UHF Silicon FET Power Amplifier

MHW913

14 WATT
880–915 MHz
RF POWER AMPLIFIER



CASE 301AB–02, STYLE 1

Designed specifically for the Pan European digital 8.0 watt, GSM mobile radio. The MHW913 is capable of wide power range control, operates from a 12.5 volt supply and requires less than 100 mW of RF input power.

- Specified 12.5 V Characteristics
  RF Input Power ≤ 100 mW (20 dBm)
  RF Output Power = 14 W
  Minimum Gain = 21.5 dB
  Minimum Efficiency = 35%
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass Substrate Eliminates Possibility of Substrate Fracture
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{bias}, V_{S2}, V_{S3}	5.0 15.6	Volt
RF Input Power	P_{in}	200	mW
RF Output Power	P_{out}	15	Watt
Storage Temperature	T_C	– 30 to +100	°C
Operating Case Temperature	T_{stg}	– 30 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{S2} = V_{S3} = 12.5 Vdc, V_{bias} = 4.8 Vdc, T_C = 25°C, 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range	BW	880	915	MHz
Efficiency (P_{out} = 14 W) (1)	η	35	—	%
Power Gain (P_{out} = 14 W) (1)	G_p	21.5	—	dB
Harmonic Output (P_{out} = 14 W Reference) (1)	$2f_o$ $3f_o$	— —	– 30 – 35	dBc
Input VSWR (P_{out} = 14 W) (1)	$VSWR_{in}$	—	3:1	
Linearity — % AM in Output P_{out} = 0.02 to 14 W; 135 kHz, 1.0% AM on Input (1)	—		6.0	%
Output Power at Decreased Voltage (P_{in} = 100 mW, V_{S2} = V_{S3} = 10.8 Vdc) (1)	P_{out}	10	—	Watt

(1) Adjust P_{in} for specified P_{out}.

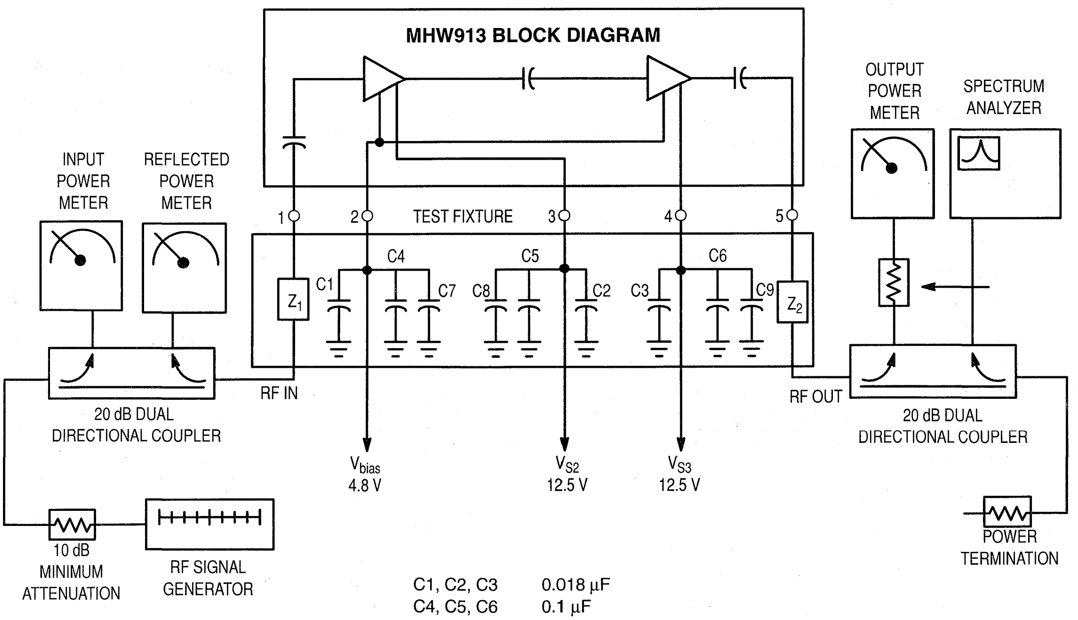
(continued)

REV 3

ELECTRICAL CHARACTERISTICS (continued) (V_{S2} = V_{S3} = 12.5 V, V_{bias} = 4.8 V, T_C = 25°C, 50 Ω system, unless otherwise noted)

Load Mismatch Stress (V_{supply} = 15.6 Vdc, P_{out} = 15 W; Load VSWR = 10:1, All Phase Angles) (1)	—	No degradation in output power		
Stability (V_{supply} = 10.8 to 16 Vdc; P_{out} = 0.03 to 14 W; Load VSWR = 6:1, All Phase Angles) (1)	—	All spurious outputs more than 60 dB below desired signal		
Quiescent Current (With No RF Applied) (V_{S2} = V_{S3} = 12.5 Vdc, V_{bias} = 4.8 Vdc)	I_{sq}	—	500	mA
Leakage Current (P_{in} = 0 mW, V_{S2} = V_{S3} = 12.5 Vdc, V_b = 0 Vdc)	I_L	—	0.6	mA
Bias P_{in} Current (P_{out} = 14 W) (1)	I_{bias}	—	0.8	mA
Noise Power (In 30 kHz Bandwidth, 20 MHz above f_o) (P_{out} = 0.03 to 14 W, V_{S2} = V_{S3} = 10.8 to 15.6 Vdc; V_{bias}= 4.8 Vdc) (1)	—	—	–70	dBm

(1) Adjust P_{in} for specified P_{out}.



C1, C2, C3	0.018 µF
C4, C5, C6	0.1 µF
C7, C8, C9	1.0 µF
Z1, Z2	50 Ω Microstrip

Figure 1. MHW913 Test Circuit Diagram

Typical Characteristics

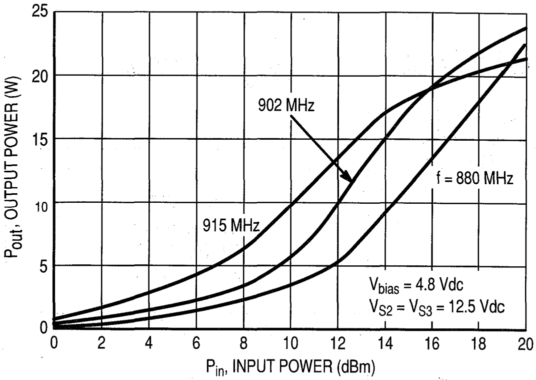


Figure 2. Output Power versus Input Power

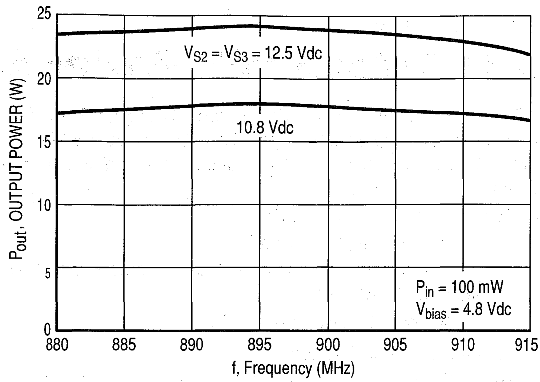


Figure 3. Output Power versus Frequency

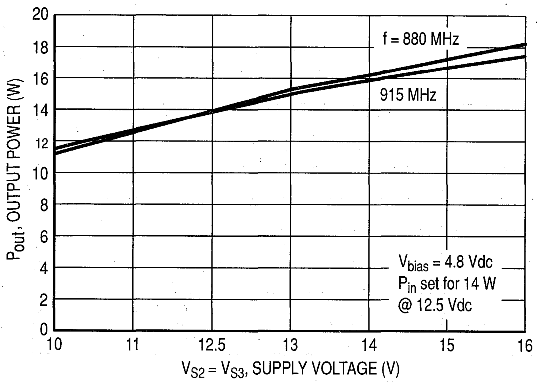


Figure 4. Output Power versus Supply Voltage

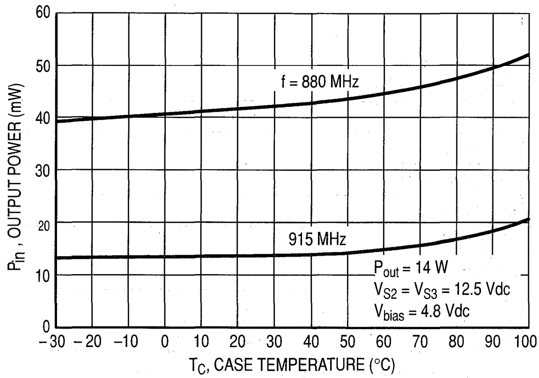


Figure 5. Input Power versus Case Temperature for P_{out} = 14 W

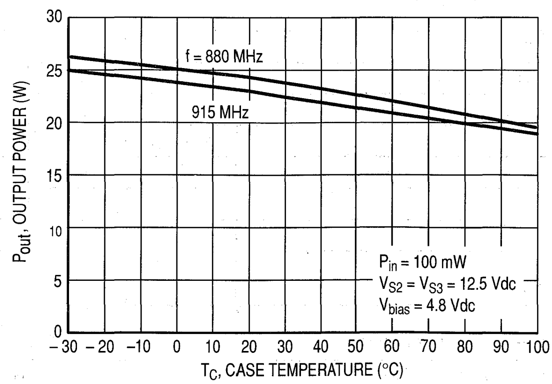


Figure 6. Output Power versus Case Temperature for Maximum Input Power

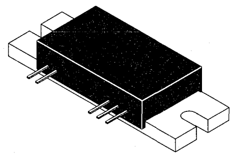
The RF Line
UHF Silicon FET Power Amplifier

MHW916

Designed specifically for the European Digital Extended Group Special Mobile (GSM) Base Station applications in the 925–960 MHz frequency range. MHW916 operates from a 26 Volt supply and requires 15.5 dBm of RF input power.

- Specified 26 Volt Characteristics
  RF Input Power: 15.5 dBm Max
  RF Output Power: 16 Watts at 1.0 dB Compression Point
  Minimum Gain: 26.5 dB
  Harmonics: –35 dBc Max at 2Fo
- 50 Ω Input/Output System
- Meet GSM Linearity Specification for Base Station up to 12.5 Watts

**16 WATT
925–960 MHz
RF POWER
AMPLIFIER**



CASE 301AB–02, STYLE 1

MAXIMUM RATINGS

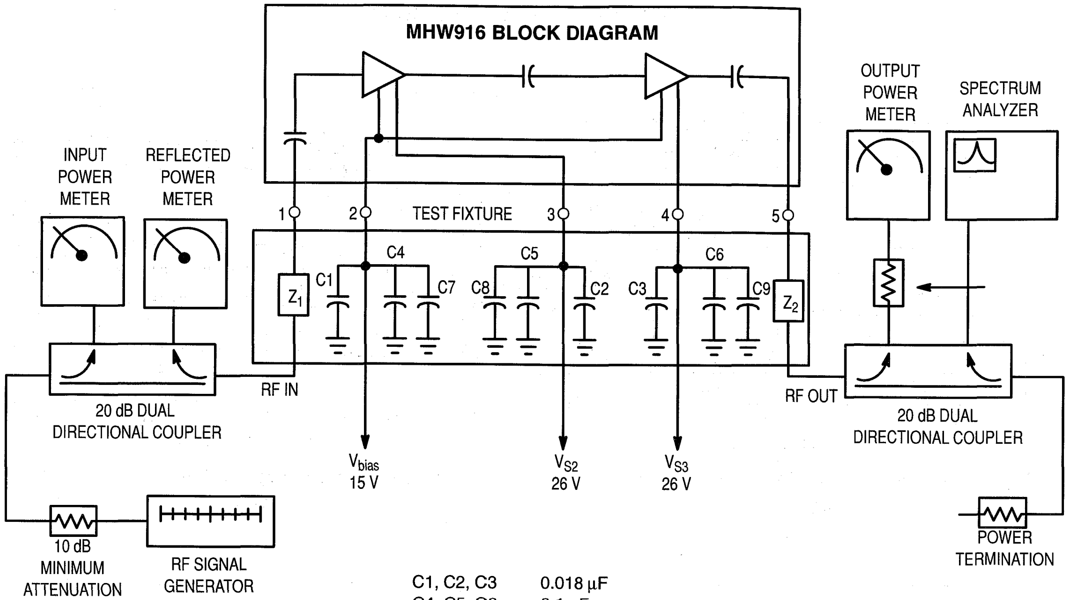
Parameter	Symbol	Value	Unit
DC Supply Voltage	V_S	28	Vdc
DC Bias Voltage	V_B	16	Vdc
RF Input Power	P_{in}	19	dBm
RF Output Voltage	P_{out}	25	W
Operating Case Temperature Range	T_C	– 5.0 to +85	°C
Storage Temperature Range	T_{stg}	– 30 to +100	°C
Standby Current (Pin Removed, $I_{stdby} = I_{S1} + I_{S2}$)	I_{stdby}	400	mA

ELECTRICAL CHARACTERISTICS (T_C = 25°C, $V_{S1} = V_{S2}$ = 26 Vdc, V_{bias} = 15 Vdc, 50 ohm system)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	925	—	960	MHz
Quiescent Current (P_{in} = 0 mW)	Idq1 + Idq2	—	400	—	mA
Power Gain (P_{out} = 16 W) (1)	Gp	26.5	30	32.5	dB
Output Power at 1.0 dB Compression	P1dB	16	—	—	W
Efficiency (1.0 dB Compression Power)	η_1	37	44	—	%
Efficiency (P_{out} = 16 W) (1)	η_2	33	39	—	%
Input VSWR (P_{out} = 16 W) (1)	$VSWR_{in}$	—	—	2:1	—
Harmonic 2 f_o (P_{out} = 16 W) (1)	H_2	—	–40	–35	dBc
Harmonic 3 f_o (P_{out} = 16 W) (1)	H_3	—	–60	–45	dBc
Ripple (P_{out} = 16 W) (1)	Rp	—	1.0	—	dB
Load Mismatch Stress (P_{out} = 16 W) Load VSWR = 5:1, All Phase Angles	Ψ	No Degradation in Output Power			
Stability (P_{out} = 10 mW to 16 W) Load VSWR = 3:1, All Phase Angles (Except Harmonics)	—	All Spurious Outputs More Than 60 dB Below Desired Signal			
Stability (P_{out} = –5.0 dBm to 42 dBm, f = 925 to 960 MHz) Load VSWR = 2:1, All Phase Angles	—	All Spurious Outputs Lower Than –46 dBm or –85 dBc (Whichever the Higher)			

(1) Adjust P_{in} for Specified P_{out}.

REV 2



C1, C2, C3	0.018 μF
C4, C5, C6	0.1 μF
C7, C8, C9	1.0 μF
Z1, Z2	50 Ω Microstrip

Figure 1. MHW916 Test Circuit Diagram

TYPICAL CHARACTERISTICS

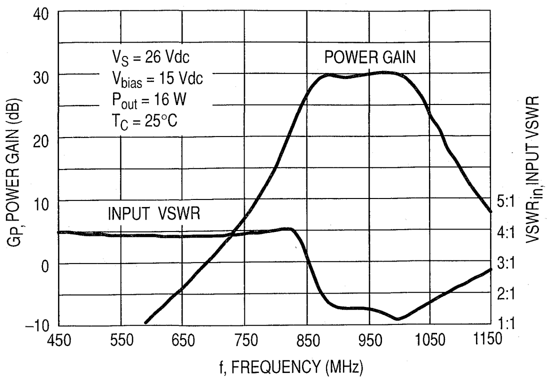


Figure 2. Power Gain and Input VSWR versus Frequency

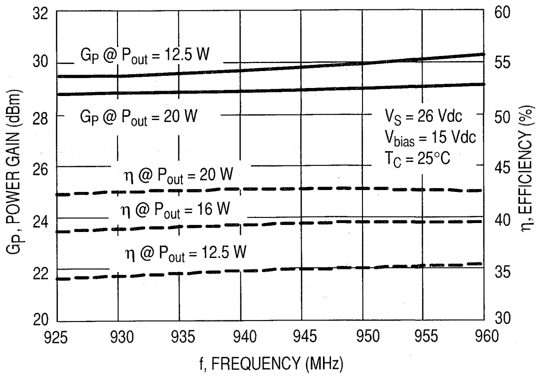


Figure 3. Power Gain and Efficiency versus Frequency

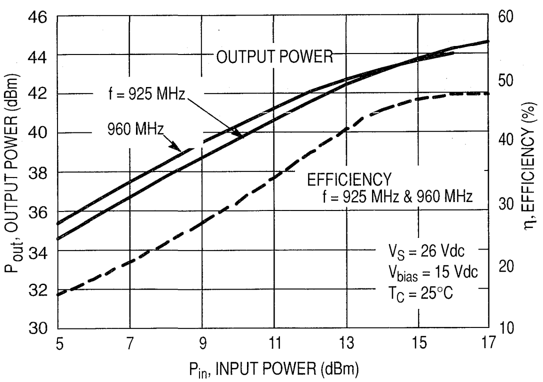


Figure 4. Output Power and Efficiency versus Input Power

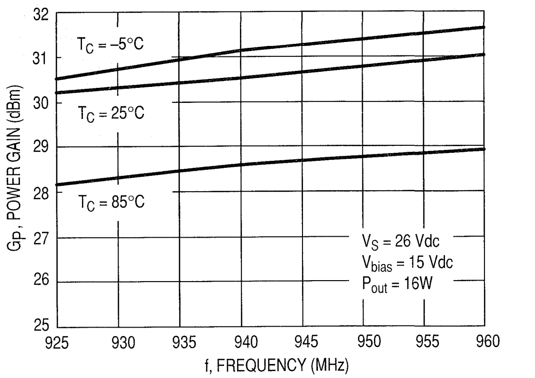


Figure 5. Power Gain versus Frequency

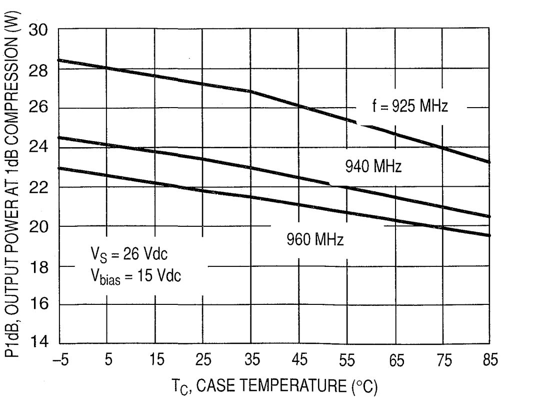


Figure 6. Output Power at 1 dB Compression versus Temperature

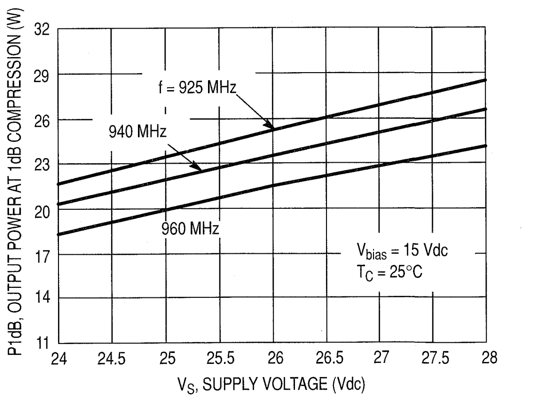


Figure 7. Output Power at 1dB Compression versus Supply Voltage

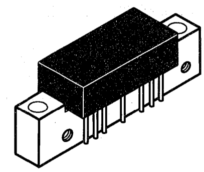
The RF Line
Low Distortion Wideband Amplifiers

MHW1134
MHW1184
MHW1224
MHW1244

. . . designed specifically for broadband applications requiring low distortion characteristics. Specified for use as return amplifiers for mid–split and high–split 2–way cable TV systems. Features all gold metallization system.

- Guaranteed Broadband Power Gain @ f = 5.0–200 MHz
- Guaranteed Broadband Noise Figure @ f = 5.0–175 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- All Ion–Implanted Arsenic Emitter Transistor Chips with 6.0 GHz f_T's
- Circuit Design Optimized for Good RF Stability Under High VSWR Load Conditions
- Transformers Designed to Insure Good Low Frequency Gain Stability versus Temperature

13.0 dB
18.0 dB
22.0 dB
24.0 dB
5.0–200 MHz
CATV HIGH–SPLIT
REVERSE AMPLIFIERS



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system)

Characteristic	Symbol	MHW1134	MHW1184	MHW1224	MHW1244	Units
Power Gain @ 10 MHz	G_P	13.0 ± 0.5	18.5 ± 0.5	22.0 ± 0.5	24.0 ± 0.5	dB
Frequency Range (Response/Return Loss) Note 1	BW	5.0–200				MHz
Cable Slope Equivalent (5.0–200 MHz)	S	–0.2 Min/+0.8 Max				dB
Gain Flatness (5.0–200 MHz)	F	±0.2 Max				dB
Input/Output Return Loss (5.0–200 MHz) Note 1	IRL/ORL	18.0 Min				dB
Cross Modulation Distortion @ +50 dBmV per ch. 12–Channel FLAT (5.0–120 MHz) 22–Channel FLAT (5.0–175 MHz) (2) (3) 26–Channel FLAT (5.0–200 MHz)	 XM_{12} XM_{22} XM_{26}	 –70 Typ –65 Max –65 Typ	 –68 Typ –64 Max –64 Typ	 –67 Typ –62 Max –62 Typ	 –66 Typ –61 Max –61 Typ	 dB dB dB

NOTES:
1. Response and return loss characteristics are tested and guaranteed for the full 5.0–200 MHz frequency range.
2. Motorola 100% distortion and noise figure testing is performed over the 5.0–175 MHz frequency range. Cross modulation and composite triple beat testing are with 22–channel loading; Video carriers used are:

T7–T13	7.0–43.0 MHz	7–Channels
2–6	55.25–83.25 MHz	5–Channels
A–7	121.25–175.25 MHz	10–Channels

3. Video carriers used for 12–Channel typical performances are T7–6; For 26–Channel typical performance, Channels 8, 9, 10 and 11 are added to the 22–Channel carriers listed above.

REV 6

ELECTRICAL CHARACTERISTICS — continued (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system)

Characteristic	Symbol	MHW1134	MHW1184	MHW1224	MHW1244	Units
Composite Triple Beat Distortion @ +50 dBmV per ch. 22–Channel FLAT (5.0–175 MHz) Notes 2 and 3 26–Channel FLAT (5.0–200 MHz)	CTB_{22} CTB_{26}	–73 Max –71 Typ	–72 Max –70 Typ	–69 Max –68.5 Typ	–68 Max –67.5 Typ	dB dB
Individual Triple Beat Distortion @ +50 dBmV per ch. Mid–Split (5.0–120 MHz) T11, T12 and CH2 @ 123.25 MHz High–Split (5.0–175 MHz) T13, CH2 and CH5 @ 175.5 MHz	TB_3 TB_3	–90 Typ –87 Typ	–88 Typ –85 Typ	–88 Typ –85 Typ	–87 Typ –84 Typ	dB dB
Second Order Distortion @ +50 dBmV per ch. High–Split (5.0–175 MHz) CH2, CHA @ 176.5 MHz	IMD	–72 Max	–72 Max	–72 Max	–72 Max	dB
Noise Figure High–Split (5.0–175 MHz) Note 2	NF	7.0 Max	5.5 Max	5.5 Max	5.0 Max	dB
DC Current	I_{DC}	210 Typ/240 Max				mAdc

NOTES:

1. Response and return loss characteristics are tested and guaranteed for the full 5.0–200 MHz frequency range.
2. Motorola 100% distortion and noise figure testing is performed over the 5.0–175 MHz frequency range. Cross modulation and composite triple beat testing are with 22–channel loading; Video carriers used are:

T7–T13	7.0–43.0 MHz	7–Channels
2–6	55.25–83.25 MHz	5–Channels
A–7	121.25–175.25 MHz	10–Channels

3. Video carriers used for 12–Channel typical performances are T7–6; For 26–Channel typical performance, Channels 8, 9, 10 and 11 are added to the 22–Channel carriers listed above.

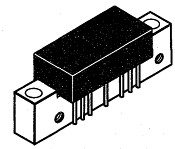
The RF Line
Low Distortion Wideband Reverse Amplifier Modules

MHW1304L

24 Vdc
50 MHz
30 dB
CATV LOW CURRENT AMPLIFIER

Designed specifically for broadband applications requiring low distortion characteristics. Specified for use as return amplifiers for low–split 2–way cable TV systems. Features all gold metallization system.

- Guaranteed Broadband Power Gain
- Guaranteed Broadband Noise Figure
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- Circuit Design Optimized for Good RF Stability Under High VSWR Load Conditions
- Transformers Designed to Insure Good Low Frequency Gain Stability versus Temperature



CASE 714–06, STYLE 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{IN}	+70	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 ohm system, unless otherwise noted)

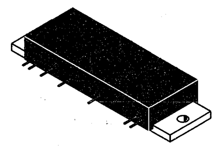
Characteristic		Symbol	Min	Max	Unit
Bandwidth	All	BW	5.0	50	MHz
Power Gain	(f = 5.0 MHz)	Gp	29.2	30.8	dB
Return Loss	(@ f = 5.0–50 MHz)	RL	18	—	dB
Second Order Distortion	(V_{out} = +50 dBmV/ch)	IMD	—	–70	dBc
Cross Modulation	(V_{out} = +50 dBmV/ch)	XMD_4	—	–57	dBc
Triple Beat Distortion	(V_{out} = +50 dBmV/ch)	TB_3	—	–66	dBc
Noise Figure	(f = 50 MHz)	NF	—	4.5	dB
DC Current		I_{DC}	100	135	mA

The RF Line
Microwave Bipolar Power Amplifier

MHW1815

15 W
1805–1880 MHz
RF POWER AMPLIFIER

- Specified 26 Volt Characteristics:
  RF Output Power: 15 Watts
  RF Power Gain: 32 dB Typ
  Efficiency: 25% Min
- 50 Ohm Input/Output System



CASE 301AK–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_S	28	Vdc
DC Bias Voltage	V_B	5.5	Vdc
RF Input Power	P_{in}	17	dBm
RF Output Power	P_{out}	23	W
Operating Case Temperature Range	T_C	–30 to +85	°C
Storage Temperature Range	T_{stg}	–30 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C; V_S = 26 Vdc; V_{BIAS} = 5 Vdc; 50 Ω system)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1805	—	1880	MHz
Total Quiescent Current (P_{in} = 0 mW)	I_q	—	300	—	mA
Power Gain (P_{out} = 15 W) (1)	G_p	30	32	—	dB
Output Power at 1 dB Compression	P1dB	15	—	—	Watts
Efficiency (1 dB Compression Power)	η	25	—	—	%
Input VSWR (P_{out} = 15 W)	$VSWR_{IN}$	—	—	2:1	—
Ripple (P_{out} = 15 W)	Rp	—	1	—	dB
Load Mismatch Stress (P_{out} = 15 W; Load VSWR = 3:1; at All Phase Angles)	ψ	No Degradation in Output Power			
Stability (P_{out} = 1 mW – 15 W; Load VSWR = 2:1; at All Phase Angles except Harmonics)	—	All Spurious Outputs More than 60 dB Below Desired Signal			
Stability (P_{out} = 1 mW – 15 W; Load VSWR = 2:1; f = 1805 – 1880 MHz; at All Phase Angles)	—	All Spurious Typically Lower than –36 dBm			

(1) Adjust P_{in} for specified P_{out}.

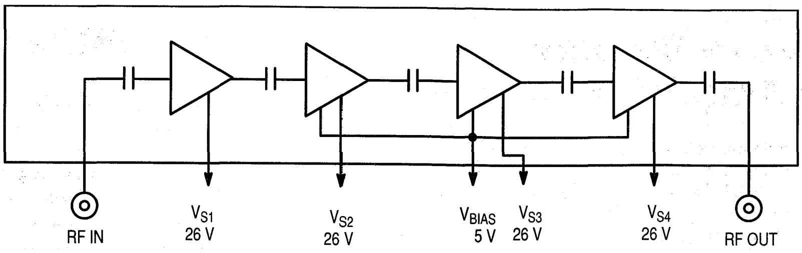


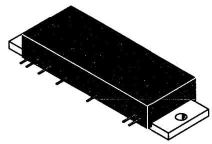
Figure 1. Internal Diagram

The RF Line
Microwave Bipolar Power Amplifier

MHW1915

15 W
1930–1990 MHz
RF POWER AMPLIFIER

- Specified 26 Volt Characteristics:
  RF Output Power: 15 Watts
  RF Power Gain: 31 dB Typ
  Efficiency: 25% Min
- 50 Ohm Input/Output System



CASE 301AK–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_S	28	Vdc
DC Bias Voltage	V_B	5.5	Vdc
RF Input Power	P_{in}	17	dBm
RF Output Power	P_{out}	23	W
Operating Case Temperature Range	T_C	−30 to +85	°C
Storage Temperature Range	T_{stg}	−30 to +100	°C

ELECTRICAL CHARACTERISTICS (V_S = 26 Vdc; V_{BIAS} = 5 Vdc; T_C = +25°C; 50 Ω system)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1930	—	1990	MHz
Total Quiescent Current ($P_{in = 0\ mW}$)	I_q	—	300	—	mA
Power Gain (P_{out} = 15 W) (1)	G_p	29	31	—	dB
Output Power at 1 dB Compression	P1dB	15	—	—	Watts
Efficiency (1 dB Compression Power)	η	25	—	—	%
Input VSWR (P_{out} = 15 W)	$VSWR_{IN}$	—	—	2:1	—
Ripple (P_{out} = 15 W)	Rp	—	1	—	dB
Load Mismatch Stress (P_{out} = 15 W; Load VSWR = 2:1; at All Phase Angles)	ψ	No Degradation in Output Power			
Stability (P_{out} = 1 mW – 15 W; Load VSWR = 2:1; at All Phase Angles except Harmonics)	—	All Spurious Outputs More than 60 dB Below Desired Signal			
Stability (P_{out} = 1 mW – 15 W; Load VSWR = 2:1; f = 1930 – 1990 MHz; at All Phase Angles)	—	All Spurious Outputs Typically Lower than −36 dBm			

(1) Adjust P_{in} for specified P_{out}.

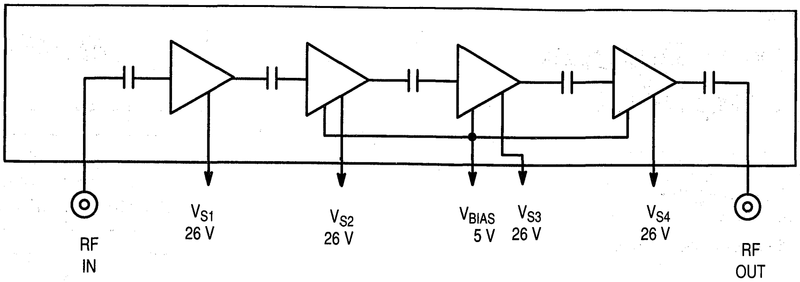


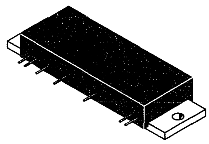
Figure 1. Internal Diagram

The RF Line
Microwave Bipolar Power Amplifier

MHW1916

15 W
1930–1990 MHz
RF POWER AMPLIFIER

- Specified 26 Volt Characteristics:
  RF Output Power: 15 Watts
  RF Power Gain: 34 dB Typ
  Efficiency: 24% Min
- 50 Ohm Input/Output Impedances



CASE 301AK–01, STYLE 1

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_S	28	Vdc
DC Bias Voltage	V_B	5.5	Vdc
RF Input Power	P_{in}	17	dBm
RF Output Power	P_{out}	23	W
Operating Case Temperature Range	T_C	−30 to +95	°C
Storage Temperature Range	T_{stg}	−30 to +100	°C

ELECTRICAL CHARACTERISTICS (V_S = 26 Vdc; V_{BIAS} = 5 Vdc; T_C = +25°C; 50 Ω system)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1930	—	1990	MHz
Total Quiescent Current ($P_{in = 0\ mW}$)	I_q	—	300	—	mA
Power Gain (P_{out} = 15 W) (1)	G_p	31	34	38	dB
Output Power at 1 dB Compression	P1dB	15	—	—	Watts
Efficiency (1 dB Compression Power)	η	24	27	—	%
Input VSWR (P_{out} = 15 W)	$VSWR_{IN}$	—	—	2:1	
Ripple (P_{out} = 15 W)	Rp	—	1	2	dB
Gain Variation at any given Frequency over Output Power (1 mW ≤ P_{out} ≤ 15 W)	ΔG_p	—	1	2.4	dB
Load Mismatch Stress (P_{out} = 15 W; Load VSWR = 3:1; at All Phase Angles)	ψ	No Degradation in Output Power			
Stability (P_{out} = 1 mW – 15 W; Load VSWR = 2:1; at All Phase Angles except Harmonics)		All Spurious Outputs More than 60 dB Below Desired Signal			
Stability (P_{out} = 1 mW – 15 W; Load VSWR = 2:1; f = 1930 – 1990 MHz; at All Phase Angles)		All Spurious Outputs Typically Lower than −36 dBm			

(1) Adjust P_{in} for specified P_{out}.

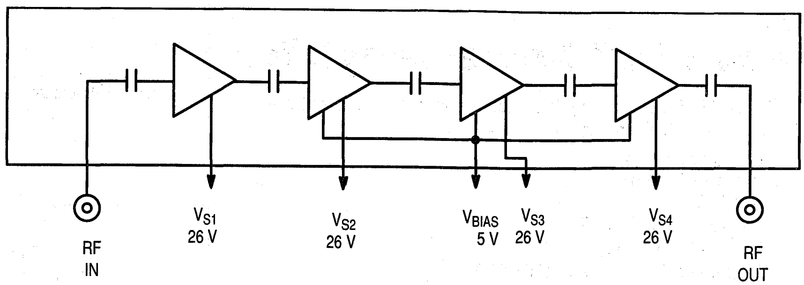


Figure 1. Internal Diagram

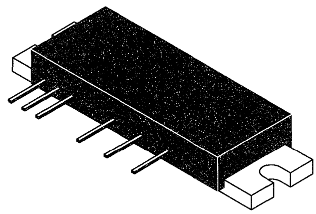
The RF Line
UHF Silicon FET Power Amplifier

Designed for 7.5 volt UHF power amplifier applications in industrial and commercial equipment primarily for hand portable radios.

- Specified 7.5 Volt Characteristics:
  RF Input Power: 1 mW (0 dBm)
  RF Output Power: 7 W
  Minimum Gain (V_{cont} = 7 V): 38.5 dB
  Harmonics: −40 dBc Max @ 2 f_o
- Meets European Transient Specification (ETS 300 113)
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness

MHW2707-1

**7 W
403–440 MHz
UHF POWER AMPLIFIER**



CASE 301AL–01, STYLE 1

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 2, 4, 5)	$V_{DD1, 2, 3}$	9	Vdc
DC Control Voltage (Pin 3)	V_{cont}	7	Vdc
RF Input Power	P_{in}	2	mW
RF Output Power ($V_{DD1, 2, 3}$ = 9 V)	P_{out}	9	W
Operating Case Temperature Range	T_C	−30 to +80	°C
Storage Temperature Range	T_{stg}	−30 to +80	°C

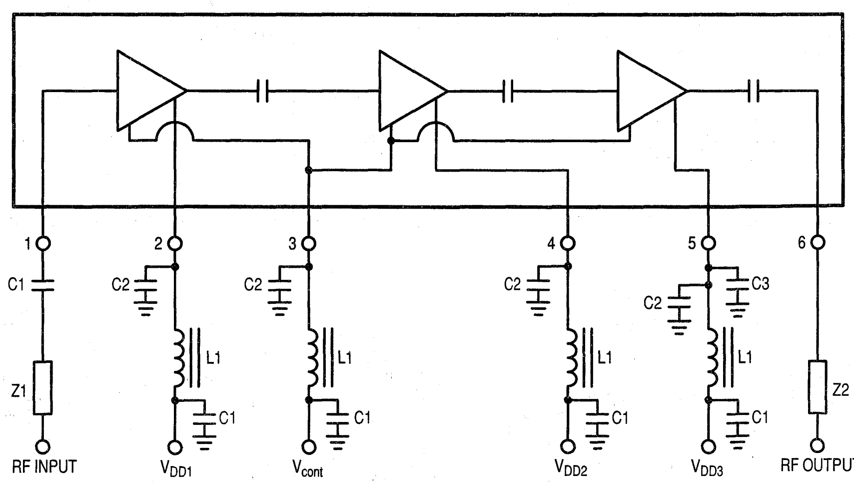
REV 1

ELECTRICAL CHARACTERISTICS ($V_{DD1} = V_{DD2} = V_{DD3}$ = 7.5 Vdc (Pins 2, 4, 5); T_C = +25°C, 50 ohm system unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range	BW	403	440	MHz
Control Voltage (P_{out} = 7 W; P_{in} = 1 mW) (1)	V_{cont}	0	7	Vdc
Quiescent Current ($V_{DD1} = V_{DD2} = V_{DD3}$ = 7.5 Vdc; P_{in} = 0 mW, V_{cont} = 0 Vdc)	—	—	1	mA
Power Gain (P_{out} = 7 W, V_{cont} = 7 Vdc)	G_p	38.5	—	dB
Efficiency (P_{out} = 7 W; P_{in} = 1 mW) (1)	η	40	—	%
Harmonics (P_{out} = 7 W; P_{in} = 1 mW) (1) 2 f_o	—	—	–40	dBc
Input VSWR (P_{out} = 7 W; P_{in} = 1 mW, 50 Ω Ref.) (1)	$VSWR_{in}$	—	2:1	—
Control Current ($V_{DD1} = V_{DD2} = V_{DD3}$ = 7.5 Vdc; P_{in} = 1 mW) (1)	I_{cont}	—	2	mA
Load Mismatch Stress ($V_{DD1} = V_{DD2} = V_{DD3}$ = 9 Vdc; P_{in} = 2 mW; P_{out} = 9 W; Load VSWR = 10:1, All Phase Angles at Frequency of Test) (1)	ψ	No Degradation in Output Power Before & After Test		
Stability (P_{in} = 1–2 mW; $V_{DD1} = V_{DD2} = V_{DD3}$ = 6–9 Vdc; P_{out} = between 0.1 mW and 9 W; Load VSWR = 8:1, All Phase Angles at Frequency of Test) (1)	—	All Spurious Outputs More Than 60 dB Below Desired Signal		

(1) Adjust V_{cont} for Specified P_{out}.

MHW2707–1 CIRCUIT BLOCK DIAGRAM



Pin Designations:

Pin 1 — RF Input Power (0 dBm)
Pin 2 — V_{DD1} (7.5 Vdc)
Pin 3 — V_{cont} (0 – 7 Vdc)
Pin 4 — V_{DD2} (7.5 Vdc)
Pin 5 — V_{DD3} (7.5 Vdc)
Pin 6 — RF OUT (7 Watts nom.)

Element Values:

C1 = 0.018 μF
C2 = 0.1 μF
C3 = 3.3 μF
L1 = 0.22 μH CHOKE
Z1 = Z2 = 50 Ω Microstrip Line

Figure 1. UHF Power Module Test Circuit Schematic and Device Block Diagram

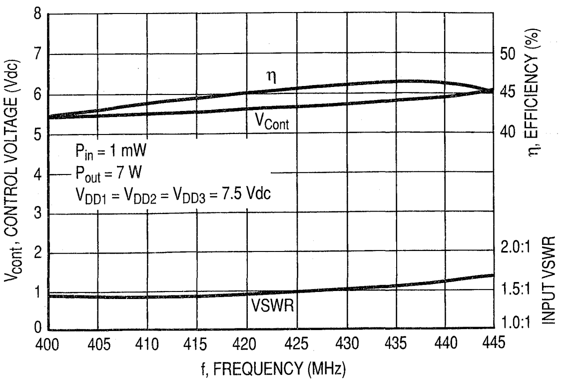


Figure 2. Control Voltage, Efficiency and VSWR versus Frequency

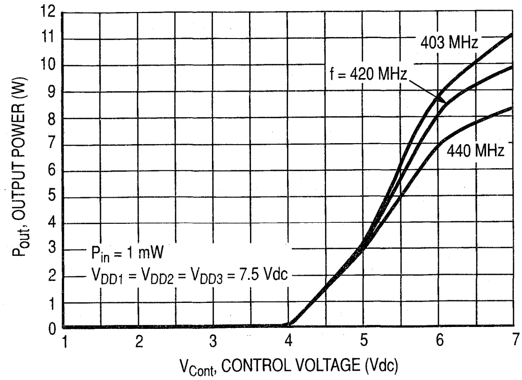


Figure 3. Output Power versus Control Voltage

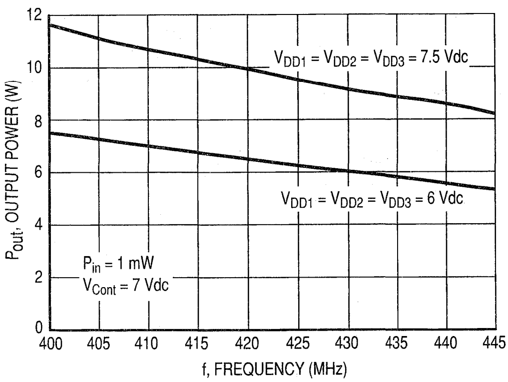


Figure 4. Output Power versus Frequency

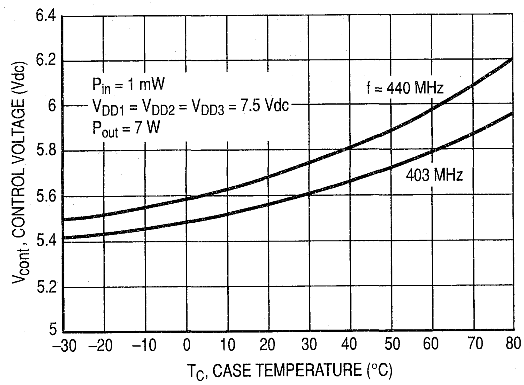


Figure 5. Control Voltage versus Case Temperature

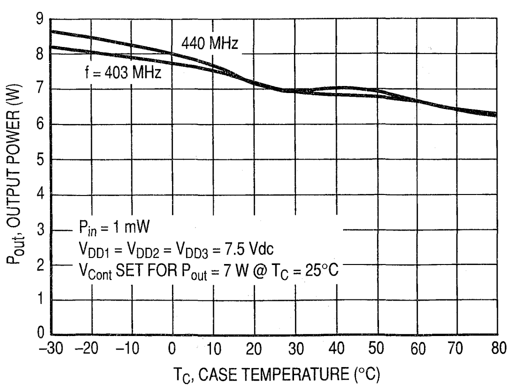


Figure 6. Output Power versus Case Temperature

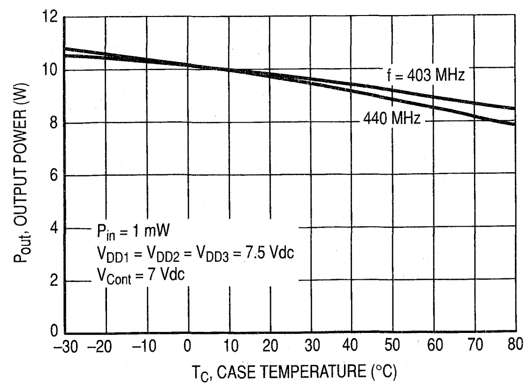


Figure 7. Output Power versus Case Temperature at Maximum Control Voltage

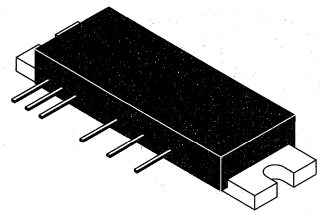
The RF Line
UHF Silicon FET Power Amplifier

Designed for 7.5 volt UHF power amplifier applications in industrial and commercial equipment primarily for hand portable radios.

- Specified 7.5 Volt Characteristics:
  RF Input Power: 1 mW (0 dBm)
  RF Output Power: 7 W
  Minimum Gain (V_{cont} = 7 V): 38.5 dB
  Harmonics: −35 dBc Max @ 2 f_o
- Provides Wideband Performance
- Meets European Transient Specification (ETS 300 113)
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness

MHW2707A1

7 W
400–470 MHz
UHF POWER AMPLIFIER



CASE 301AL–01, STYLE 1

MAXIMUM RATINGS (Flange Temperature = 25°C)

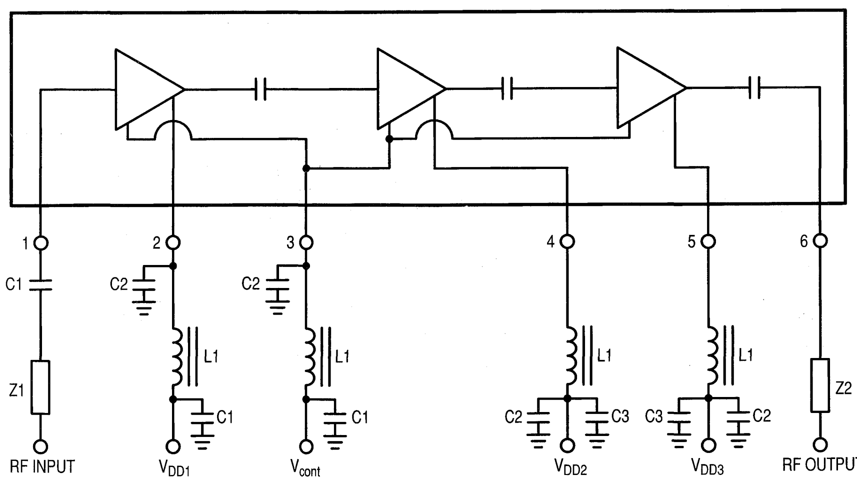
Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 2, 4, 5)	$V_{DD1, 2, 3}$	9	Vdc
DC Control Voltage (Pin 3)	V_{cont}	7	Vdc
RF Input Power	P_{in}	2	mW
RF Output Power ($V_{DD1, 2, 3}$ = 9 V)	P_{out}	9	W
Operating Case Temperature Range	T_C	−30 to +80	°C
Storage Temperature Range	T_{stg}	−30 to +80	°C

ELECTRICAL CHARACTERISTICS (V_{DD1} = V_{DD2} = V_{DD3} = 7.5 Vdc (Pins 2, 4, 5); T_C = +25°C, 50 ohm system unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range	BW	400	470	MHz
Control Voltage (P_{out} = 7 W; P_{in} = 1 mW) (1)	V_{cont}	0	7	Vdc
Quiescent Current (V_{DD1} = V_{DD2} = V_{DD3} = 7.5 Vdc; P_{in} = 0 mW, V_{cont} = 0 Vdc)	—	—	1	mA
Power Gain (P_{out} = 7 W, V_{cont} = 7 Vdc)	G_p	38.5	—	dB
Efficiency (P_{out} = 7 W; P_{in} = 1 mW) (1)	η	45	—	%
Harmonics (P_{out} = 7 W; P_{in} = 1 mW) (1) 2 f_o	—	—	–35	dBc
Input VSWR (P_{out} = 7 W; P_{in} = 1 mW, 50 Ω Ref.) (1)	$VSWR_{in}$	—	3	—
Control Current (V_{DD1}= V_{DD2} = V_{DD3} = 7.5 Vdc; P_{in} = 1 mW) (1)	I_{cont}	—	2	mA
Load Mismatch Stress (V_{DD1} = V_{DD2} = V_{DD3} = 9 Vdc; P_{in} = 2 mW; P_{out} = 9 W; Load VSWR = 10:1, All Phase Angles at Frequency of Test) (1)	ψ	No Degradation in Output Power Before & After Test		
Stability (P_{in} = 1–2 mW; V_{DD1} = V_{DD2} = V_{DD3} = 6–9 Vdc; P_{out} = between 0.1 mW and 9 W; Load VSWR = 8:1, All Phase Angles at Frequency of Test) (1)	—	All Spurious Outputs More Than 60 dB Below Desired Signal		

(1) Adjust V_{cont} for Specified P_{out}.

MHW2707A1 CIRCUIT BLOCK DIAGRAM



Pin Designations:

Pin 1 — RF Input Power (0 dBm)
Pin 2 — V_{DD1} (7.5 Vdc)
Pin 3 — V_{cont} (0 – 7 Vdc)
Pin 4 — V_{DD2} (7.5 Vdc)
Pin 5 — V_{DD3} (7.5 Vdc)
Pin 6 — RF OUT (7 Watts nom.)

Element Values:

C1 = 0.018 μF
C2 = 0.1 μF
C3 = 3.3 μF
L1 = 0.22 μH CHOKE
Z1 = Z2 = 50 Ω Microstrip Line

Figure 1. UHF Power Module Test Circuit Schematic and Device Block Diagram

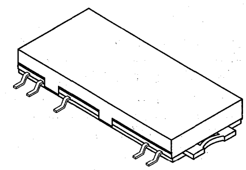
The RF Line
UHF Silicon FET Power Amplifiers

MHW2727-3

Designed for 7.5 volt UHF power amplifier applications in industrial and commercial equipment primarily for hand portable radios.

- Specified 7.5 Volt Characteristics:
  RF Input Power: 20 mW (13 dBm)
  RF Output Power: 7 W
  Minimum Gain (V_{cont} = 7 V): 25.5 dB
  Harmonics: – 35 dBc Max @ 2.0 f_o 350 – 360 MHz
  – 40 dBc Max @ 2.0 f_o 360 – 400 MHz
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness

7 W,
350 – 400 MHZ
UHF POWER AMPLIFIERS



CASE 420AC–01 , STYLE 1

MAXIMUM RATINGS (Flange Temperature = 25°C)

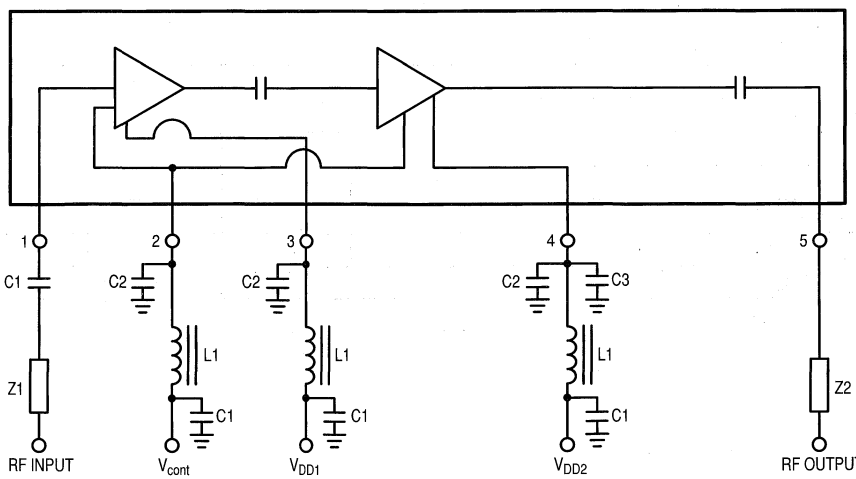
Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 3, 4)	$V_{DD1,2}$	9	Vdc
DC Control Voltage (Pin 2)	V_{cont}	9	Vdc
RF Input Power	P_{in}	40	mW
RF Output Power ($V_{DD1,2}$ = 9 V)	P_{out}	9	W
Operating Case Temperature Range	T_C	–30 to +100	°C
Storage Temperature Range	T_{stg}	–30 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD1}, V_{DD2} = 7.5 Vdc (Pins 3, 4); T_C = +25°C, 50 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Frequency Range		BW	350	400	MHz
Control Voltage (P_{out} = 7 W; P_{in} = 20 mW) (1)		V_{cont}	0	7	Vdc
Quiescent Current (V_{DD1}, V_{DD2} = 7.5 Vdc; P_{in} = 0 mW, V_{cont} = 0 Vdc)		—	—	1	mA
Power Gain (P_{out} = 7 W) (1)		G_p	25.5	—	dB
Efficiency (P_{out} = 7 W; P_{in} = 20 mW) (1)		η	40	—	%
Harmonics (P_{out} = 7 W; P_{in} = 20 mW) (1)	2.0 f_o 350 – 360 MHz 2.0 f_o 360 – 400 MHz	—	—	– 35 – 40	dBc
Input VSWR (P_{out} = 7 W; P_{in} = 20 mW, 50 Ω Ref.) (1)		$VSWR_{in}$	—	2.3:1	—
Control Current (V_{DD1}, V_{DD2} = 7.5 Vdc; P_{in} = 20 mW, P_{out} = 7 W) (1)		I_{cont}	—	2	mA
Load Mismatch Stress (V_{DD1}, V_{DD2} = 9 Vdc; P_{in} = 40 mW; P_{out} = 9 W; Load VSWR = 10:1, at All Phase Angles) (1)		ψ	No Degradation in Output		
Stability (P_{in} = 20–40 mW; V_{DD1}, V_{DD2} = 6–9 Vdc; P_{out} = between 0.1 W and 9 W; Load VSWR = 8:1, at All Phase Angles) (1)		—	All Spurious Outputs More Than 60 dB Below Desired Signal		

(1) Adjust V_{cont} for Specified P_{out}.

MHW2727 CIRCUIT BLOCK DIAGRAM



Pin Designations:

Pin 1 — RF Input Power (13 dBm)
Pin 2 — V_{cont} (0 – 9 Vdc)
Pin 3 — V_{DD1} (7.5 Vdc)
Pin 4 — V_{DD2} (7.5 Vdc)
Pin 5 — RF OUT (7 Watts nom.)

Element Values:

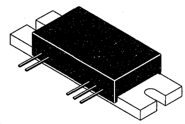
C1 = 0.018 μF
C2 = 0.1 μF
C3 = 3.3 μF
L1 = 0.22 μH CHOKE
Z1, Z2 = 50 Ω Microstrip Line

Figure 1. UHF Power Module Test Circuit Schematic and Device Block Diagram

The RF Line
UHF Silicon FET Power Amplifiers

MHW2821-1
MHW2821-2

–1: 20 W, 806–870 MHz
–2: 18 W, 890–950 MHz
RF POWER AMPLIFIER



CASE 301AB–02, STYLE 1

Designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 806 to 950 MHz.

- Specified 12.5 Volt Characteristics:
  RF Input Power: ≤ 250 mW (MHW2821–1)
  ≤ 300 mW (MHW2821–2)
  RF Output Power: 20 W (MHW2821–1)
  18 W (MHW2821–2)
- LDMOS FET Technology
- Epoxy Glass Substrate Eliminates Possibility of Substrate Fracture
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Cost Effective

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{bias}, V_{S2}, V_{S3}	12.5 16	Vdc
RF Input Power	P_{in}	400	mW
RF Output Power	P_{out}	23	W
Operating Case Temperature Range	T_C	– 30 to +100	°C
Storage Temperature Range	T_{stg}	– 30 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{S2} = V_{S3} = 12.5 Vdc; V_{bias} = 12.5 Vdc; T_C = +25°C, 50 Ω system, unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Frequency Range	MHW2821–1 MHW2821–2	BW	806 890	870 950	MHz
Input Power (P_{out} = 20 W) (1) (P_{out} = 18 W) (1)	MHW2821–1 MHW2821–2	P_{in}	— —	250 300	mW
Power Gain (P_{out} = 20 W) (1) (P_{out} = 18 W) (1)	MHW2821–1 MHW2821–2	G_P	19 17.9	— —	dB
Efficiency (Rated P_{out})		η	35	—	%
Harmonics (Rated P_{out} Reference) (1)		$2f_o$ $3f_o$	— —	– 40 – 45	dBc
Input VSWR (Rated P_{out}) (1)		$VSWR_{in}$	—	3:1	dB

(1) Adjust P_{in} for specified P_{out}.

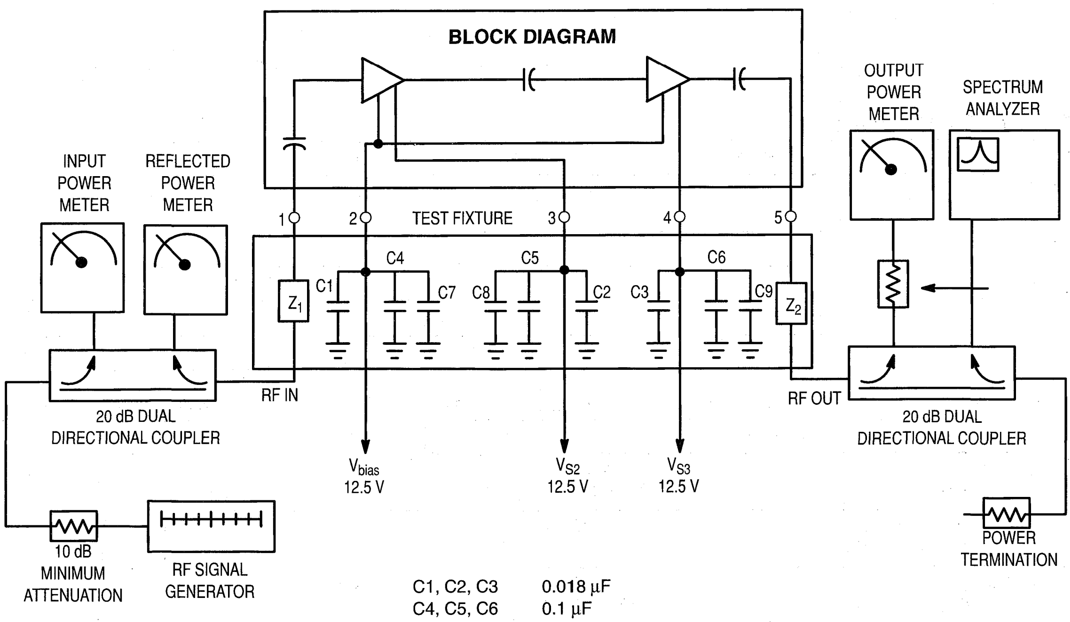
(continued)

REV 1

ELECTRICAL CHARACTERISTICS (continued) (V_{S2} = V_{S3} = 12.5 Vdc, V_{bias} = 12.5 Vdc, T_C = +25°C, 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Load Mismatch Stress (V_{supply} = 16 Vdc; P_{out} = 20 W for MHW2821–1; P_{out} = 18 W for MHW2821–2; Load VSWR = 20:1, All Phase Angles at Frequency of Test) (1)	ψ	No Degradation in Output Power Before and After Test		
Stability (V_{supply} = 10.8 to 16 Vdc; P_{in} = 0 to 250 mW for MHW2821–1; P_{in} = 0 to 300 mW for MHW2821–2; Load VSWR = 4:1, All Phase Angles at Frequency of Test	—	All Spurious Outputs More than 60 dB Below Desired Signal		
Quiescent Current (With No RF Applied) (V_{S2} = V_{S3} = 12.5 Vdc; V_{bias} = 12.5 Vdc)	I_{sq}	—	500	mA
Leakage Current (With No RF Applied) (V_{S2} = V_{S3} = 12.5 Vdc; V_{bias} = 0 Vdc)	I_L	—	0.6	mA
Bias P_{in} Current (Rated P_{out}) (1)	I_{bias}	—	3	mA

(1) Adjust P_{in} for specified P_{out}.



C1, C2, C3	0.018 µF
C4, C5, C6	0.1 µF
C7, C8, C9	1.0 µF
Z1, Z2	50 Ω Microstrip

Figure 1. Test Circuit Diagram

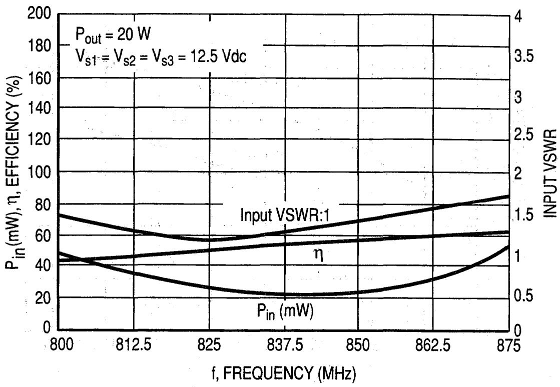


Figure 2. Input Power, Efficiency and VSWR versus Frequency

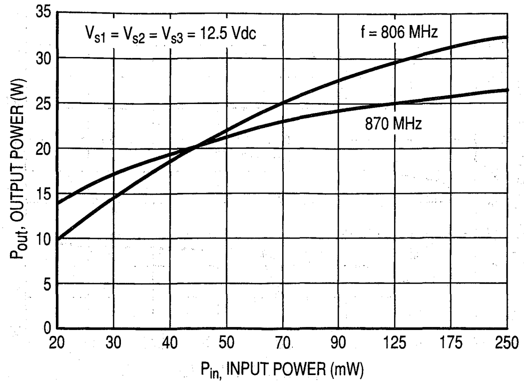


Figure 3. Output Power versus Input Power

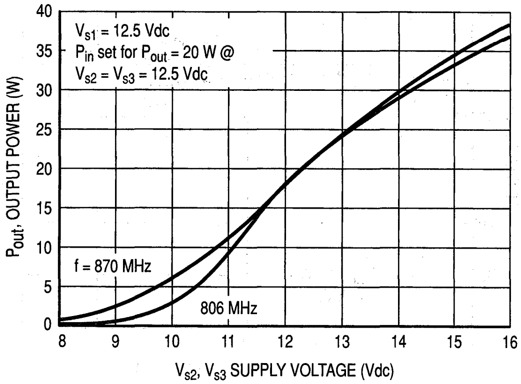


Figure 4. Output Power versus Supply Voltage

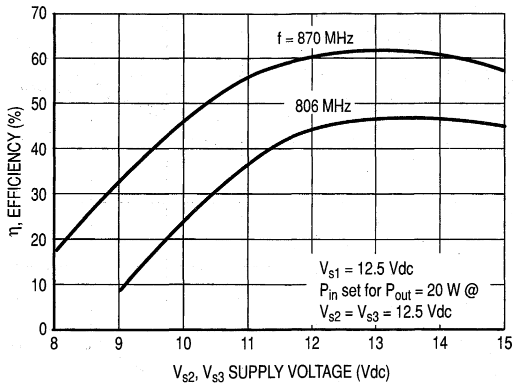


Figure 5. Efficiency versus Supply Voltage

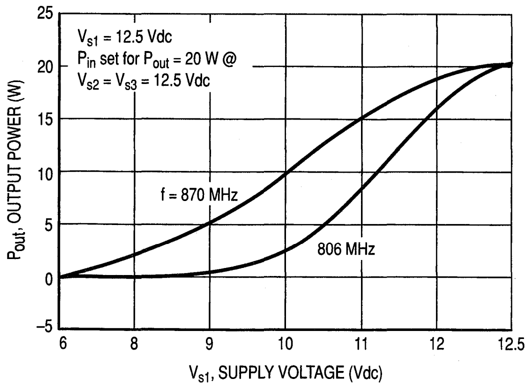


Figure 6. Output Power versus Supply Voltage to First Stage (V_{s1})

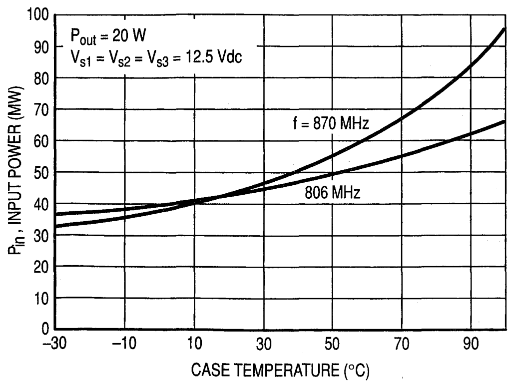


Figure 7. Input Power versus Case Temperature

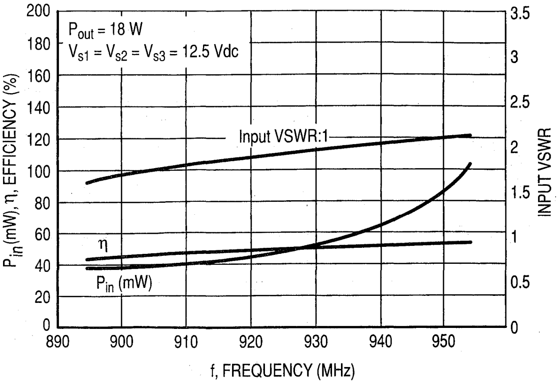


Figure 8. P_{in} VSWR, and Efficiency versus Frequency

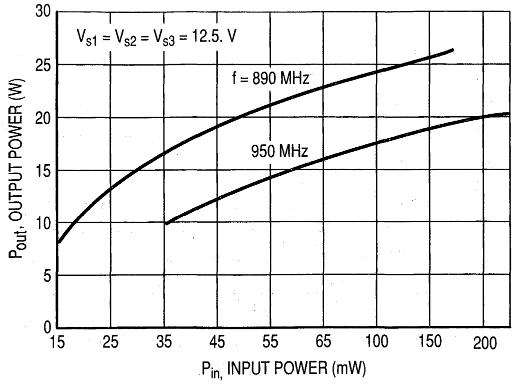


Figure 9. Output Power versus Input Power

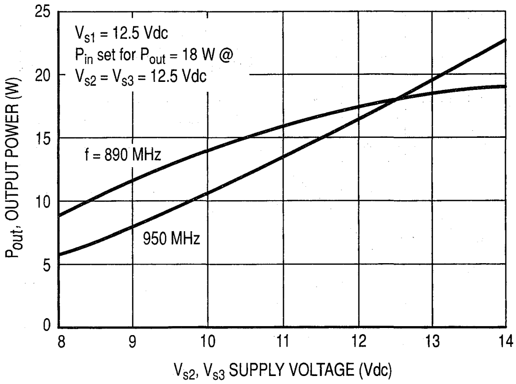


Figure 10. P_{out} versus Supply Voltage

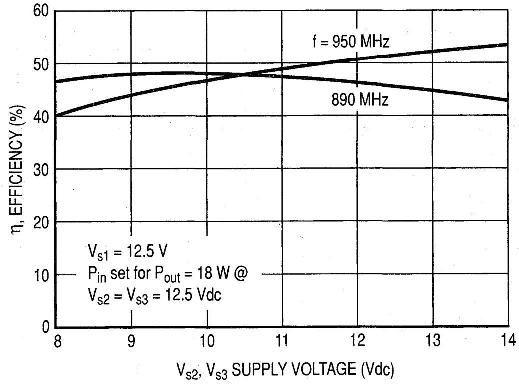


Figure 11. Efficiency versus Supply Voltage

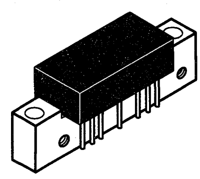
The RF Line
450 MHz CATV Amplifier

. . . designed specifically for 450 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53– and 60–Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 18.2 dB (Typ) @ 50 MHz
  19.0 dB (Typ) @ 450 MHz
- Broadband Noise Figure
  NF = 6.5 dB (Max)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion–Implanted Transistors

MHW5182A

**18 dB GAIN
450 MHz
60–CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIER**



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	17.8	18.2	18.8	dB
Power Gain — 450 MHz		G_p	18.5	19	20	dB
Slope		S	0.3	—	1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	–85	—	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	–80	–72	
Cross Modulation Distortion	53–Channel FLAT	XMD_{53}	—	–62	—	dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	XMD_{60}	—	–61	–59	
Composite Triple Beat	53–Channel FLAT	CTB_{53}	—	–64	—	dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	CTB_{60}	—	–62	–61	
DIN (European Applications Only)*						dBμV**
300 MHz — (CH V + Q – P @ W)		DIN1	—	126	—	
400 MHz— (CH M8 + M15 – M9 @ M14)		DIN2	—	126	—	
450 MHz — (CH M20 + M23 – M22 @ M21)		DIN3	—	125	—	
Noise Figure (f = 450 MHz)		NF	—	5.5	6.5	dB
DC Current		I_{DC}	—	210	240	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ)	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+60	≤−60
Q	259.25	+60	
V	289.25	+66	
W (Ref.)	295.25	+66	
M8	361.25	+60	≤−60
M9	367.25	+60	
M14 (Ref.)	397.25	+66	
M15	403.25	+66	
M20	433.25	+65	≤−60
M21 (Ref.)	439.25	+65	
M22	445.25	+59	
M23	451.25	+59	

** DIN (dBμV) = Reference Channel Level (dBmV) +60 dB

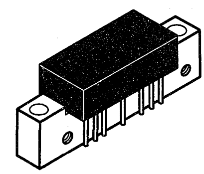
The RF Line
High Output Doubler 450/550 MHz CATV Amplifier Modules

MHW5185B
MHW6185B

The MHW5185B and MHW6185B are designed specifically for 450/550 MHz CATV applications. Features ion–implanted arsenic emitter transistors and an all gold metallization system.

- 5th Generation Die Technology
- Specified for 60/77–Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 18.5 dB Typ @ 50 MHz
  19.2 dB Typ @ 450 MHz
  19.5 dB Typ @ 550 MHz
- Broadband Noise Figure
  NF = 4.5 dB Typ @ 50 MHz
- Improvement in Distortion Over Conventional Hybrids
- Allows Higher Output Level Operation

18 dB GAIN
450/550 MHz
60/77–CHANNEL
CATV AMPLIFIERS



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
Frequency Range		MHW5185B MHW6185B	BW	40 40	— —	450 550	MHz
Power Gain	50 MHz 450 MHz 550 MHz	All MHW5185B MHW6185B	G_p	18 18.5 18.8	18.5 19.2 19.5	19 20 20.5	dB
Slope	40–450 MHz 40–550 MHz	MHW5185B MHW6185B	S	0.3 0.3	— —	1.8 2.0	dB
Gain Flatness (Peak To Valley)		MHW5185B MHW6185B	—	— —	— —	0.4 0.5	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz 40–550 MHz	MHW5185B MHW6185B	IRL/ORL	18 18	— —	— —	dB
Composite Second Order 60 ch, (V_{out} = +46 dBmV) 77 ch, (V_{out} = +44 dBmV)		 MHW5185B MHW6185B	$CSO_{60/77}$	 — —	 −70 −68	 −67 −65	dB

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion			$XMD_{60/77}$				dB
(60 ch, V_{out} = +46 dBmV @ Fm = 55 MHz)		MHW5185B		—	−70	−67	
(77 ch, V_{out} = +44 dBmV @ Fm = 55 MHz)		MHW6185B		—	−78	−68	
Signal–to–Triple Beat Noise			$CTB_{60/77}$				dB
(60 ch, V_{out} = +46 dBmV)		MHW5185B		—	−68	−67	
(77 ch, V_{out} = +44 dBmV)		MHW6185B		—	−66	−65	
Noise Figure	450 MHz	MHW5185B	NF	—	5.5	7.0	dB
	550 MHz	MHW6185B		—	6.0	7.5	
DC Current (V_{DC} = 24 Vdc, T_C = 30°C)			I_{DC}	380	415	440	mA

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

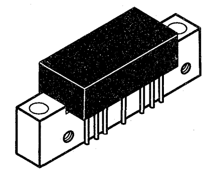
The RF Line
450 MHz CATV Amplifier

... designed for broadband applications requiring low distortion characteristics. Specifically intended for CATV market requirements. Features ion–implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 22 dB (Typ)
- Broadband Noise Figure — @ f = 40–450 MHz
  NF = 4.5 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion–Implanted Transistors

MHW5222A

22 dB GAIN
450 MHz
60–CHANNEL
CATV TRUNK AMPLIFIER



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	21.4	22	22.6	dB
Power Gain — 450 MHz		G_p	22.0	22.9	23.5	dB
Slope		S	0.2	0.5	1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV, Ch 2, M6, M15)			—	−80	—	
(V_{out} = +44 dBmV, Ch 2, M13, M22)			—	−78	−72	
Cross Modulation Distortion (V_{out} = +46 dBmV)	53–Channel FLAT	XMD_{53}	—	−60	—	dB
	60–Channel FLAT	XMD_{60}		−60	−59	
Composite Triple Beat (V_{out} = +46 dBmV)	53–Channel FLAT	CTB_{53}	—	−63	—	dB
	60–Channel FLAT	CTB_{60}	—	−61	−60	
DIN (European Applications Only)						dBμV
300 MHz — (CH V + Q – P @ W)		DIN1	—	125.5	—	
400 MHz — (CH M8 + M15 – M9 @ M14)		DIN2	—	125	—	
450 MHz — (CH M20 + M23 – M22 @ M21)		DIN3	—	124	—	
Noise Figure (f = 450 MHz)		NF	—	4.5	5.0	dB
DC Current		I_{DC}	—	210	240	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ)	DIN Beat Level dB Relative to Ref. Ch.
P Q V W (Ref.)	253.25 259.25 289.25 295.25	+59.5 +59.5 +65.5 +65.5	⩽–60
M8 M9 M14 (Ref.) M15	361.25 367.25 397.25 403.25	+59 +59 +65 +65	⩽–60
M20 M21 (Ref.) M22 M23	433.25 439.25 445.25 451.25	+64 +64 +58 +58	⩽–60

**DIN (dBμV) = Reference Channel Level (dBmV) +60 dB

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

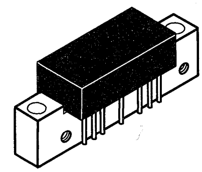
The RF Line
450 MHz CATV Amplifier

MHW5342A

. . . designed specifically for 450 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53– and 60–Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 34.5 dB Typ @ 50 MHz
  35.5 dB Typ @ 450 MHz
- Broadband Noise Figure
  NF = 5.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion–Implanted Transistors

34 dB GAIN
450 MHz
60–CHANNEL
CATV LINE EXTENDER
AMPLIFIER



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	33.5	34.5	35.5	dB
Power Gain — 450 MHz		G_p	34.5	35.5	37	dB
Slope		S	0	+1.0	+2.5	dB
Gain Flatness (Peak To Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	−78	—	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	−74	−68	
Cross Modulation Distortion (V_{out} = +46 dBmV)	53–Channel FLAT	XMD_{53}	—	−63	—	dB
	60–Channel FLAT	XMD_{60}		−63	−59	
Composite Triple Beat (V_{out} = +46 dBmV)	53–Channel FLAT	CTB_{53}	—	−63	—	dB
	60–Channel FLAT	CTB_{60}	—	−62	−59	
DIN (European Applications Only)						dBμV
300 MHz — (CH V + Q − P @ W)		DIN1	—	126	—	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	125	—	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	124	—	
Noise Figure (f = 450 MHz)		NF	—	5.0	6.0	dB
DC Current		I_{DC}	—	310	340	mA

REV 6

*DIN (European Applications Only)

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ)	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+60	≤−60
Q	259.25	+60	
V	289.25	+66	
W (Ref.)	295.25	+66	
M8	361.25	+59	≤−60
M9	367.25	+59	
M14 (Ref.)	397.25	+65	
M15	403.25	+65	
M20	433.25	+64	≤−60
M21 (Ref.)	439.25	+64	
M22	445.25	+58	
M23	451.25	+58	

**DIN (dBμV) = Reference Channel Level (dBmV) +60 dB

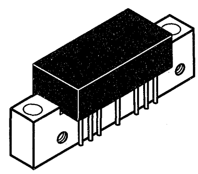
The RF Line
450 MHz CATV AMPLIFIER

MHW5382A

38 dB GAIN
450 MHz
60–CHANNEL
CATV LINE EXTENDER
AMPLIFIER

. . . designed specifically for 450 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53– and 60–Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 38 dB (Typ)
- Broadband Noise Figure
  NF = 4.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion–Implanted Transistors



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	37	38	39.5	dB
Power Gain — 450 MHz		G_p	38	39	40	dB
Slope		S	0	+1.0	+2.5	dB
Gain Flatness (Peak To Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	–78	—	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	–72	–64	
Cross Modulation Distortion	53–Channel FLAT	XMD_{53}	—	–63	—	dB
(V_{out} = +46 dBmV)	60–Channel FLAT	XMD_{60}		–61	–59	
Composite Triple Beat	53–Channel FLAT	CTB_{53}	—	–63	—	dB
(V_{out} = +46 dBmV)	60–Channel FLAT	CTB_{60}	—	–60	–59	
DIN (European Applications Only)						dBμV
300 MHz — (CH V + Q – P @ W)		DIN1	—	125	—	
400 MHz— (CH M8 + M15 – M9 @ M14)		DIN2	—	124	—	
450 MHz — (CH M20 + M23 – M22 @ M21)		DIN3	—	123	—	
Noise Figure (f = 450 MHz)		NF	—	4.0	5.0	dB
DC Current		I_{DC}	—	310	340	mA

***DIN (European Applications Only)**

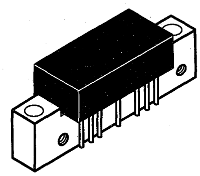
NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ)	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+59	≤−60
Q	259.25	+59	
V	289.25	+65	
W (Ref.)	295.25	+65	
M8	361.25	+58	≤−60
M9	367.25	+58	
M14 (Ref.)	397.25	+64	
M15	403.25	+64	
M20	433.25	+57	≤−60
M21 (Ref.)	439.25	+57	
M22	445.25	+63	
M23	451.25	+63	

**DIN (dBμV) = Reference Channel Level (dBmV) +60 dB

The RF Line
550 MHz CATV Amplifier

MHW6142

14 dB GAIN
550 MHz
77–CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIER



CASE 714–06, STYLE 1

. . . designed specifically for 550 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 77 Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 14 dB (Typ) @ 50 MHz
  14.5 dB (Min) @ 550 MHz
- Broadband Noise Figure
  NF = 7.5 dB (Max)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion–Implanted Transistors

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain — 50 MHz		G_p	13.5	14	14.5	dB
Power Gain — 550 MHz		G_p	14.5	—	—	dB
Slope		S	0.2	—	1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.5	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	−78	—	
(V_{out} = +44 dBmV per ch., Ch 2, M30, M39)			—	−75	−72	
Cross Modulation Distortion						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	XMD_{60}	—	−64	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	XMD_{77}	—	−65	−62	
Composite Triple Beat						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	CTB_{60}	—	−62	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	CTB_{77}	—	−65	−59	
Noise Figure (f = 550 MHz)		NF	—	6.5	7.5	dB
DC Current		I_{DC}	—	210	240	mA

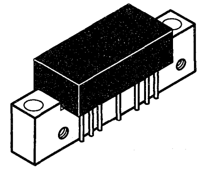
The RF Line
77-Channel (550 MHz) CATV Input/Output Trunk Amplifier

MHW6172

. . . designed specifically for 550 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7 GHz f_T and an all gold metallization system.

- Specified for 77–Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 17.2 dB (Typ)
- Broadband Noise Figure — @ f = 550 MHz
  NF = 6 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz Ion–Implanted Transistors

**17 dB GAIN
550 MHz
77–CHANNEL
CATV AMPLIFIER**



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz	G_p	16.8	17.2	17.8	dB
Slope		S	0	+0.5	2.0	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	−80	—	
(V_{out} = +44 dBmV per ch., Ch 2, M30, M39)			—	−78	−70	
Cross Modulation Distortion						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	XMD_{60}	—	−63	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	XMD_{77}	—	−65	−62	
Composite Triple Beat Noise						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	CTB_{60}	—	−62	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	CTB_{77}	—	−60	−59	
Noise Figure	450 MHz	NF	—	5.5	—	dB
	550 MHz		—	6	7	
DC Current		I_{DC}	—	210	240	mA

REV 6

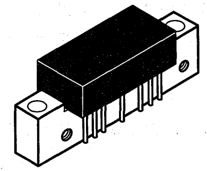
The RF Line
550 MHz CATV Amplifier

MHW6182

. . . designed specifically for 550 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 77 Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 18.2 dB (Typ) @ 50 MHz
  18.8 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 7.0 dB (Max)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion–Implanted Transistors

**18 dB GAIN
550 MHz
77–CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIER**



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain — 50 MHz		G_p	17.7	18.2	18.7	dB
Power Gain — 550 MHz		G_p	18.8	19.2	20	dB
Slope		S	0.5	—	2.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.5	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	−85	—	
(V_{out} = +44 dBmV per ch., Ch 2, M30, M39)			—	−80	−72	
Cross Modulation Distortion						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	XMD_{60}	—	−61	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	XMD_{77}	—	−64	−62	
Composite Triple Beat						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	CTB_{60}	—	−62	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	CTB_{77}	—	−60	−58	
Noise Figure (f = 550 MHz)		NF	—	—	7.0	dB
DC Current		I_{DC}	—	210	240	mA

REV 6

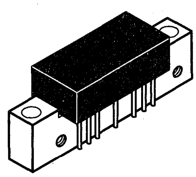
The RF Line
600 MHz CATV Amplifier Module

MHW6182-6

This module is designed specifically for 600 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7 GHz f_T and an all gold metallization system.

- Specified for 87–Channel Performance
- Broadband Power Gain — @ f = 40–600 MHz
  G_p = 17.6 dB (Min) @ 50 MHz
  18.2 dB (Min) @ 600 MHz
- Broadband Noise Figure @ 600 MHz
  NF = 6 dB (Max)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz Ion–Implanted Transistors

5TH GENERATION
18 dB GAIN
600 MHz
87–CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIERS



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input	V_{in}	+60	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	600	MHz
Power Gain	f = 50 MHz	G_p	17.6	18.2	18.8	dB
Power Gain	f = 600 MHz	G_p	18.2	19.2	20	dB
Slope	f = 40–600 MHz	S	0	—	1.8	dB
Gain Flatness (Peak to Valley)	f = 40–600 MHz	—	—	0.2	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	f = 40–600 MHz	IRL/ORL	18	—	—	dB
Composite Second Order (V_{out} = +44 dBmV/Ch)	87–Channel FLAT	CSO_{87}	—	—	−56	dB
Cross Modulation Distortion (V_{out} = +44 dBmV/Ch, Fm = 55 MHz)	87–Channel FLAT	XMD_{87}	—	—	−55	dB
Composite Triple Beat (V_{out} = +44 dBmV/Ch)	87–Channel FLAT	CTB_{87}	—	—	−57	dB
Noise Figure	f = 50 MHz f = 600 MHz	NF	— —	— —	5 6	dB
DC Current (V_{DC} = 24 Vdc, T_C = 30°C)		I_{DC}	180	210	240	mA

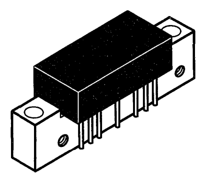
REV 1

The RF Line
High Output Doubler 600 MHz CATV Amplifier

MHW6185-6A

**18.5 dB GAIN
600 MHz
87–CHANNEL
CATV AMPLIFIER**

- 24 V Supply Voltage
- Specified for 87–Channel Performance
- 6th Generation Die Technology
- Improvement in Distortion Over Conventional Hybrids
- Allows Higher Output Level Operation
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	600	MHz
Power Gain	50 MHz 600 MHz	G_p	18 18.5	18.5 18.8	19 20	dB
Slope	40–600 MHz	S	0	0.3	1.5	dB
Gain Flatness (40–600 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–600 MHz	IRL/ORL	18	—	—	dB
Composite Second Order (V_{out} = +44 dBmV/ch., Worst Case)	87–Channel FLAT	CSO_{87}	—	−70	−64	dBc
Cross Modulation Distortion (V_{out} = +44 dBmV/ch., FM = 55 MHz)	87–Channel FLAT	XMD_{87}	—	−70	−66	dBc
Composite Triple Beat (V_{out} = +44 dBmV/ch., Worst Case)	87–Channel FLAT	CTB_{87}	—	−66	−64	dBc
Noise Figure	50 MHz 600 MHz	NF	— —	5 6	6 7	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	380	435	460	mA

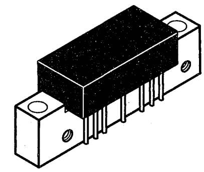
REV 1

The RF Line
High Output Doubler 600 MHz CATV Amplifier

- 24 V Supply Voltage
- Specified for 87–Channel Performance
- 6th Generation Die Technology
- Improvement in Distortion Over Conventional Hybrids
- Allows Higher Output Level Operation
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

MHW6205-6A

**20 dB GAIN
600 MHz
87–CHANNEL
CATV AMPLIFIER**



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	600	MHz
Power Gain	50 MHz 600 MHz	G_p	19.5 19.8	20 20.1	20.5 21.5	dB
Slope	40 – 600 MHz	S	0	0.2	1.5	dB
Gain Flatness (40 – 600 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40 – 600 MHz	IRL/ORL	18	—	—	dB
Composite Second Order — Intermodulation Distortion (V_{out} = +44 dBmV/ch., Worst Case)	87–Channel FLAT	CSO_{87}	—	−65	−63	dBc
Cross Modulation Distortion (V_{out} = +44 dBmV/ch., FM = 55 MHz)	87–Channel FLAT	XMD_{87}	—	−67	−65	dBc
Composite Triple Beat (V_{out} = +44 dBmV/ch., Worst Case)	87–Channel FLAT	CTB_{87}	—	−68	−63	dBc
Noise Figure	50 MHz 600 MHz	NF	— —	4.5 5.5	5.5 6.5	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	380	435	460	mA

REV 1

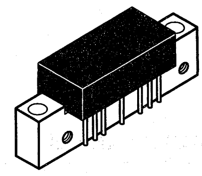
The RF Line
550 MHz CATV Amplifier

MHW6222

. . . designed specifically for 550 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 77–Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 22 dB (Typ) @ 50 MHz
  22 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 6.0 dB (Max)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion–Implanted Transistors

22 dB GAIN
550 MHz
77–CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIER



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+60	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain — 50 MHz		G_p	21.4	22	22.6	dB
Power Gain — 550 MHz		G_p	22	—	—	dB
Slope		S	0.2	—	1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	−80	—	
(V_{out} = +44 dBmV per ch., Ch 2, M30, M39)			—	−72	−66	
Cross Modulation Distortion						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	XMD_{60}	—	−60	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	XMD_{77}	—	−60	−57	
Composite Triple Beat						dB
(V_{out} = +46 dBmV per ch.)	60–Channel FLAT	CTB_{60}	—	−61	—	
(V_{out} = +44 dBmV per ch.)	77–Channel FLAT	CTB_{77}	—	−59	−57	
Noise Figure (f = 550 MHz)		NF	—	5.0	6.0	dB
DC Current		I_{DC}	—	210	240	mA

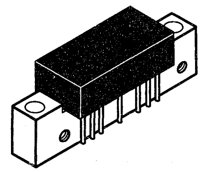
REV 6

MHW6272

The RF Line
77-Channel (550 MHz) CATV Line Extender Amplifier

- Specified for 60– and 77–Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 27 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 550 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

27 dB GAIN
550 MHz
77–CHANNEL
CATV AMPLIFIER



CASE 714–06, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz 550 MHz	G_p	26.2 27	27 —	27.8 29.2	dB
Slope		S	0	1	2	dB
Gain Flatness (Peak To Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz 450–550 MHz	IRL/ORL	18 16	— —	— —	dB
Second Order Intermodulation Distortion (V_{out} = +48 dBmV per ch., Ch 2, 13, R) (V_{out} = +46 dBmV per ch., Ch 2, M6, M15) (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		IMD	 — — — —	 –80 –78 –76 –69	 — — — –64	dB
Cross Modulation Distortion @ Ch 2 (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 53–Channel FLAT 60–Channel FLAT 70–Channel FLAT 77–Channel FLAT	 XMD_{53} XMD_{60} XMD_{70} XMD_{77}	 — — — —	 –63 –62 –61 –59	 — — — –57	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 53–Channel FLAT 60–Channel FLAT 70–Channel FLAT 77–Channel FLAT	 TB_{53} TB_{60} TB_{70} TB_{77}	 — — — —	 –63 –62 –61 –59	 — — — –57	dB
Noise Figure	550 MHz	NF	—	6.0	6.5	dB
DC Current		I_{DC}	—	310	340	mA

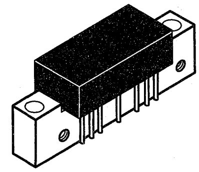
The RF Line
77-Channel (550 MHz) CATV Amplifier

MHW6342

. . . designed specifically for 550 MHz CATV applications. Features ion–implanted arsenic emitter transistors with 7 GHz f_T and an all gold metallization system.

- Specified for 77–Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 34.5 dB (Typ) @ 50 MHz
  35 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 5.5 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz Ion–Implanted Transistors

34 dB GAIN
550 MHz
77–CHANNEL
CATV AMPLIFIER



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz	G_p	33.5	34.5	35.5	dB
Power Gain	550 MHz	G_p	34.5	—	—	dB
Slope		S	0	1	2	dB
Gain Flatness (Peak To Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz 450–550 MHz	IRL/ORL	18 16	— —	— —	dB
Second Order Intermodulation Distortion (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		IMD	 — —	 −75 −70	 — −64	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60–Channel FLAT 77–Channel FLAT	 XMD_{60} XMD_{77}	 — —	 −61 −59	 — −57	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60–Channel FLAT 77–Channel FLAT	 CTB_{60} CTB_{77}	 — —	 −60 −58	 — −57	dB
Noise Figure	550 MHz	NF	—	5.5	6.5	dB
DC Current		I_{DC}	—	310	340	mA

REV 6

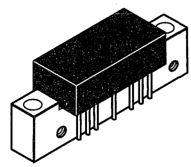
The RF Line
750 MHz CATV Conventional Hybrid Amplifier

MHW7142

Designed specifically for 750 MHz CATV applications. Features ion–implanted arsenic emitter transistors with an all gold metallization system.

- Supply Voltage = 24 Vdc
- 5th Generation Die Technology
- Specified for 110 Channel Performance
- Power Gain = 14.5 dB max @ f = 50 MHz
- Superior Gain, Return Loss and DC Current Stability
- All Gold Metallization

24 Vdc
750 MHz
110 – CHANNEL
CATV AMPLIFIER



CASE 714–06, Style 1

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{IN}	+70	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24Vdc, T_C = 25°C, 75 ohm system, unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Frequency		BW	40	750	MHz
Power Gain	(f = 50 MHz)	Gp1	13.5	14.5	dB
Power Gain	(f = 750 MHz)	Gp2	14.2	15.2	dB
Slope	(f = 40 – 750 MHz)	S	0.3	1.5	dB
Gain Flatness	(f = 40 – 750 MHz, Peak to Valley)	G_f	—	0.6	dB
Return Loss	(@ f = 40 MHz)	RL	20	—	dB
Return Loss Derate	(@ f > 40 MHz)	RLD	—	.006	dB/MHz
Composite Second Order	(V_{out} = +40 dBmV/ch)	CSO_{110}	—	–60	dBc

(continued)

REV 1

ELECTRICAL CHARACTERISTICS — continued (V_{CC} = 24Vdc, T_C = 25°C, 75 ohm system, unless otherwise noted)

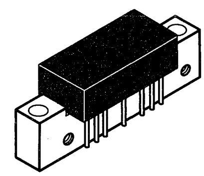
Characteristic		Symbol	Min	Max	Unit
Cross Modulation	(V_{out} = +40 dBmV/ch, FM = 55.25 MHz)	XMD_{110}	—	–66	dBc
Composite Triple Beat	(V_{out} = +40 dBmV/ch)	CTB_{110}	—	–62	dBc
Noise Figure	(f = 50 MHz)	NF_1	—	6.0	dB
Noise Figure	(f = 750 MHz)	NF_2	—	7.5	dB
DC Current		IDC	180	240	mA

The RF Line

110-Channel (750 MHz), 128-Channel (860 MHz) & 152-Channel (1000 MHz) CATV Amplifiers

MHW7182
MHW8182
MHW9182

18 dB GAIN
750/860/1000 MHz
110/128/152 CHANNEL
CATV AMPLIFIERS



CASE 714–06, STYLE 1

The MHW7182, MHW8182, and MHW9182 are designed specifically for up to 1000 MHz CATV systems as output amplifiers in trunk and line extender applications. These amplifiers feature ion–implanted, arsenic emitter transistors and an all gold metallization system.

- Specified for 110/128/152–Channel Performance
- Broadband Power Gain — @ f = 40–1000 MHz
  G_p = 18.2 dB Min @ 750, 860 & 1000 MHz
- Broadband Noise Figure
  NF = 5.5 dB Typ — MHW7182
  6.0 dB Typ — MHW8182
  6.5 dB Typ — MHW9182
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+70	dBmV
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc; T_C = +30°C, 75 ohm system, unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
Frequency Range		MHW7182	BW	40	—	750	MHz
		MHW8182		40	—	860	
		MHW9182		40	—	1000	
Power Gain	50 MHz	All	G_p	17.6	18.2	18.8	dB
	750 MHz	MHW7182		18.2	18.9	20.5	
	860 MHz	MHW8182		18.2	19.0	20.5	
	1000 MHz	MHW9182		18.2	19.2	20.7	
Slope		MHW7182, MHW8182, MHW9182	S	0	1.0	2.5	—
Gain Flatness (Peak To Valley)			G_f	—	0.4	0.6	—
		MHW7182, MHW8182		—	0.4	0.8	
		MHW9182					
Input/Output Return Loss @ f = 40 MHz		MHW7182, MHW8182, MHW9182	IRL/ORL	20	24	—	dB
Derate Return Loss @ f > 40 MHz		MHW7182	RLD	—	—	0.007	dB/MHz
		MHW8182		—	—	0.008	
(Ref = 20 dB @ 40 MHz)		MHW9182		—	—	0.009	
Composite Second Order							dB
(V_{out} = +40 dBmV/ch; 110 Channels)		MHW7182	CSO_{110}	—	−67	−62	
(V_{out} = +38 dBmV/ch; 128 Channels)		MHW8182	CSO_{128}	—	−67	−60	
(V_{out} = +38 dBmV/ch; 152 Channels)		MHW9182	CSO_{152}	—	−67	−59	

(continued)

REV 6

ELECTRICAL CHARACTERISTICS — continued (V_{CC} = 24 Vdc; T_C = +30°C, 75 ohm system, unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion							dBc
(V_{out} = +40 dBmV/ch, 110–Channel @ Fm = 55.25 MHz)		MHW7182	XMD_{110}	—	−68	−64	
(V_{out} = +38 dBmV/ch, 128–Channel @ Fm = 55.25 MHz)		MHW8182	XMD_{128}	—	−68	−60	
(V_{out} = +38 dBmV/ch, 152–Channel @ Fm = 55.25 MHz)		MHW9182	XMD_{152}	—	−68	−59	
Composite Triple Beat							dBc
(V_{out} = +40 dBmV/ch, 110–Channels, Worst Case)		MHW7182	CTB_{110}	—	−64	−62	
(V_{out} = +38 dBmV/ch, 128–Channels, Worst Case)		MHW8182	CTB_{128}	—	−62	−60	
(V_{out} = +38 dBmV/ch, 152–Channels, Worst Case)		MHW9182	CTB_{152}	—	−61	−59	
Noise Figure	f = 50 MHz		NF	—	3.6	5.0	dB
	f = 750 MHz	MHW7182		—	5.5	6.5	
	f = 860 MHz	MHW8182		—	6.0	7.0	
	f = 1000 MHz	MHW9182		—	6.5	8.0	
DC Current			I_{DC}	180	210	240	mA

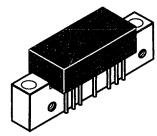
The RF Line
High Output Power Doubler 750 MHz CATV Amplifiers

MHW7185A
MHW7205A

Designed specifically for 750 MHz CATV applications. Features ion–implanted, arsenic emitter transistors with an all gold metallization system.

- Supply Voltage = 24 Vdc
- 6th Generation Die Technology
- Specified for 110 Channel Performance
- Broadband Power Gain @ f = 50 MHz
  Gp = 18 dB Min (MHW7185A)
  Gp = 19.5 dB Min (MHW7205A)
- Broadband Noise Figure @ f = 50 MHz
  NF = 6 dB Max
- Improvement in Distortion Over Conventional Hybrids
- Allows Higher Output Level Operation

750 MHz, 24 Vdc
110 CHANNEL
CATV AMPLIFIERS



CASE 714–06, Style 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{IN}	+70	dBmV
Operating Case Temperature Range	T_C	– 20 to +100	°C
Storage Temperature Range	T_{stg}	– 40 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = 30°C, 75 Ω system, unless otherwise noted)

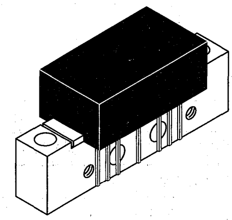
Characteristic			Symbol	Min	Max	Unit
Bandwidth			BW	40	750	MHz
Power Gain	(f = 50 MHz)	MHW7185A MHW7205A	Gp1	18.0 19.5	19.0 20.5	dB
Power Gain	(f = 750 MHz)	MHW7185A MHW7205A	Gp2	18.5 20.0	20.5 21.5	dB
Slope	(f = 40 – 750 MHz)		S	0	2	dB
Gain Flatness	(f = 40 – 750 MHz, Peak to Valley)		G_f	—	1	dB
Return Loss	(f = 40 MHz)		RL	18	—	dB
Return Loss Derate	(f > 40 MHz)		RLD	—	0.007	dB/MHz
Composite Triple Beat	(V_{out} = +44 dBmV/ch, 110 Channels, Worst Case)	MHW7185A MHW7205A	CTB_{110}	— —	–58 –57	dBc
Cross Modulation	(V_{out} = +44 dBmV/ch, 110 Channels, FM = 55 MHz)	MHW7185A MHW7205A	XMD_{110}	—	–65 –64	dBc
Composite Second Order	(V_{out} = +44 dBmV/ch, 110 Channels, Worst Case)	MHW7185A MHW7205A	CSO_{110}	— —	–58 –56	dBc
Noise Figure	(f = 50 MHz)		NF_1	—	6	dB
Noise Figure	(f = 750 MHz)		NF_2	—	8.5	dB
DC Current			IDC	380	460	mA

The RF Line

High Output Power Doubler 750 MHz CATV Amplifier

MHW7185C

19.4 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–02, STYLE 1

- Specified for 77 and 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 19.4 dB (Typ)
- Broadband Noise Figure
  NF = 5.8 dB (Typ) @ 750 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

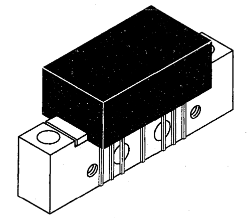
ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	18.3 19	18.8 19.4	19.3 20	dB
Slope	40–750 MHz	S	0	0.4	1.0	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	19 —	— —	— 0.006	dB dB/MHz
Composite Second Order (V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT 77–Channel FLAT	CSO_{110} CSO_{77}	— —	–72 –80	–64 —	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +44 dBmV/ch., FM = 55 MHz)	110–Channel FLAT 77–Channel FLAT	XMD_{110} XMD_{77}	— —	–66 –69	–63 —	dBc
Composite Triple Beat (V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT 77–Channel FLAT	CTB_{110} CTB_{77}	— —	–64 –70	–62 —	dBc
Noise Figure	50 MHz 550 MHz 750 MHz	NF	— — —	4.0 4.8 5.8	5.0 — 7.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

The RF Line
High Output Power Doubler 750 MHz CATV Amplifier

MHW7205C

20.2 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714Y–02, STYLE 1

- Specified for 77 and 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 20.2 dB (Typ)
- Broadband Noise Figure
  NF = 5.8 dB (Typ) @ 750 MHz
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors
- Composite Triple Beat — @ 110–Channel Loading
  CTB = –63 dB (Typ)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	19.3 20	19.8 20.2	20.3 21	dB
Slope	40–750 MHz	S	0	0.4	1.0	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	19 —	— —	— 0.006	dB dB/MHz
Composite Second Order (V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT 77–Channel FLAT	CSO_{110} CSO_{77}	— —	–70 –80	–63 —	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +44 dBmV/ch., FM = 55 MHz)	110–Channel FLAT 77–Channel FLAT	XMD_{110} XMD_{77}	— —	–65 –69	–62 —	dBc
Composite Triple Beat (V_{out} = +44 dBmV/ch., Worst Case)	110–Channel FLAT 77–Channel FLAT	CTB_{110} CTB_{77}	— —	–63 –70	–61 —	dBc
Noise Figure	50 MHz 550 MHz 750 MHz	NF	— — —	4.0 4.8 5.8	5.0 — 7.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

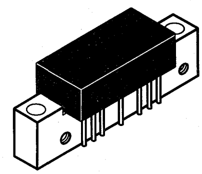
The RF Line
110-Channel (750 MHz) and 128-Channel (860 MHz) CATV Amplifiers

MHW7222
MHW8222

22 dB GAIN
750/860 MHz
110/128 CHANNEL
CATV AMPLIFIERS

The MHW7222 and MHW8222 are designed specifically for up to 860 MHz CATV systems as amplifiers in trunk and line extender applications. These amplifiers feature ion–implanted, arsenic emitter transistors and an all gold metallization system.

- Specified for 110/128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 22 dB Typ @ 750 and 860 MHz
- Broadband Noise Figure
  NF = 5.5 dB Typ — MHW7222
  6.4 dB Typ — MHW8222
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization



CASE 714–06, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+70	dBmV
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
Frequency Range		MHW7222 MHW8222	BW	40 40	— —	750 860	MHz
Power Gain	f = 50 MHz f = 750 MHz f = 860 MHz	All MHW7222 MHW8222	G_p	20.8 22 21.8	21.5 22.3 22.3	22.2 24 24	dB
Slope (f = 40–750 MHz)		MHW7222, MHW8222	S	0	1	2	—
Gain Flatness (Peak To Valley) (f = 40–750 MHz)		MHW7222 MHW8222	G_f	— —	0.4 0.4	0.6 0.8	—
Input/Output Return Loss @ f = 40 MHz		MHW7222, MHW8222	IRL/ORL	20	24	—	dB
Derate Return Loss @ f > 40 MHz		MHW7222 MHW8222	RLD	— —	— —	0.008 0.009	dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch; 110 Channels) (V_{out} = +38 dBmV/ch; 128 Channels)		 MHW7222 MHW8222	 CSO_{110} CSO_{128}	 — —	 −63 −63	 −55 −56	dB

(continued)

REV 1

ELECTRICAL CHARACTERISTICS — continued

Characteristic			Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion							dBc
(V_{out} = +40 dBmV/ch, 110–Channel @ Fm = 55.25 MHz)		MHW7222	XMD_{110}	—	−64	−60	
(V_{out} = +38 dBmV/ch, 128–Channel @ Fm = 55.25 MHz)		MHW8222	XMD_{128}	—	−68	−60	
Composite Triple Beat							dBc
(V_{out} = +40 dBmV/ch, 110–Channels, Worst Case)		MHW7222	CTB_{110}	—	−62	−60	
(V_{out} = +38 dBmV/ch, 128–Channels, Worst Case)		MHW8222	CTB_{128}	—	−62	−60	
Noise Figure	f = 50 MHz	All	NF	—	3.6	5	dB
	f = 750 MHz	MHW7222		—	5.5	7	
	f = 860 MHz	MHW8222		—	6.4	7.5	
DC Current			I_{DC}	180	220	240	mA

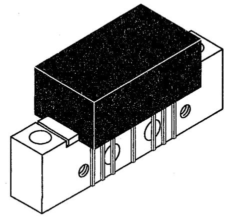
The RF Line
110-Channel (750 MHz) CATV Amplifier

MHW7222A

22 dB GAIN
750 MHz
110 CHANNEL
CATV AMPLIFIER

The MHW7222A is designed specifically for up to 750 MHz CATV systems as amplifiers in trunk and line extender applications. This amplifier features ion–implanted, arsenic emitter transistors, an all gold metallization system and offers improved ruggedness and distortion performance.

- Specified for 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 22.3 dB Typ @ 750 MHz
- Broadband Noise Figure
  NF = 5.5 dB Typ
- All Gold Metallization



CASE 714Y–02, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+28	Vdc
RF Input Voltage (Single Tone)	V_{in}	+70	dBmV
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	f = 50 MHz f = 750 MH	G_p	20.8 22	21.5 22.3	22.2 24	dB
Slope (f = 40–750 MHz)		S	0	1	2	—
Gain Flatness (Peak To Valley)	(f = 40–750 MHz)	G_f	—	0.4	0.6	—
Input/Output Return Loss @ f = 40 MHz		IRL/ORL	20	24	—	dB
Derate Return Loss @ f > 40 MHz		RLD	—	—	0.008	dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch; 110 Channels) (V_{out} = +44 dBmV/ch; 77 Channels)		 CSO_{110} CSO_{77}	 — —	 −65 −65	 −57 —	dB

(continued)

ELECTRICAL CHARACTERISTICS — continued

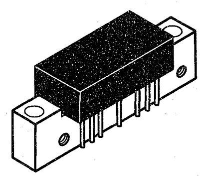
Characteristic		Symbol	Min	Typ	Max	Unit
Cross Modulation Distortion						dBc
(V_{out} = +40 dBmV/ch, 110–Channel @ Fm = 55.25 MHz)		XMD_{110}	—	−64	−60	
(V_{out} = +44 dBmV/ch, 77–Channel @ Fm = 55.25 MHz)		XMD_{77}	—	−60	—	
Composite Triple Beat						dBc
(V_{out} = +40 dBmV/ch, 110–Channels, Worst Case)		CTB_{110}	—	−63	−60	
(V_{out} = +44 dBmV/ch, 77–Channels, Worst Case)		CTB_{77}	—	−62	—	
Noise Figure	f = 50 MHz	NF	—	3.6	5	dB
	f = 750 MHz		—	5.5	7	
DC Current		I_{DC}	180	220	240	mA

The RF Line
110-Channel (750 MHz) CATV Line Extender Amplifier

MHW7242

- Specified for 110–Channel Performance
- Broadband Power Gain — @ f = 40–750 MHz
  G_p = 24 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Max) @ 750 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

24 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER



CASE 714–06, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

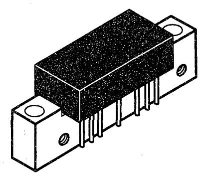
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	23.2 24	24 24.7	24.8 26	dB
Slope	40–750 MHz	S	0	0.7	2	dB
Gain Flatness (40–750 MHz, Peak To Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case)		CSO_{110}	—	–65	–60	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–63	–60	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–63	–60	dBc
Noise Figure	50 MHz 750 MHz	NF	— —	— —	5.5 7	dB
DC Current		I_{DC}	280	—	350	mA

The RF Line
110-Channel (750 MHz) CATV Line Extender Amplifier

MHW7272

27 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER

- 24 V Supply Voltage
- Specified for 110–Channel Performance
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors



CASE 714–06, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	26.2 27	27 27.8	27.8 29	dB
Slope	40–750 MHz	S	0	0.7	2	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	–70	–60	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	–63	–60	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	–63	–60	dBc
Noise Figure	50 MHz 750 MHz	NF	— —	— 5.5	5.5 6.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	280	310	350	mA

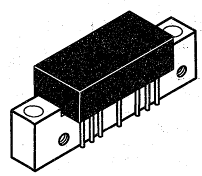
REV 1

The RF Line
110-Channel (750 MHz) CATV Line Extender Amplifier

- 24 V Supply Voltage
- Specified for 110–Channel Performance
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

MHW7292

**29 dB GAIN
750 MHz
110–CHANNEL
CATV AMPLIFIER**



CASE 714–06, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	750	MHz
Power Gain	50 MHz 750 MHz	G_p	28.2 29	29 29.8	29.8 31	dB
Slope	40–750 MHz	S	0	0.7	2	dB
Gain Flatness (40–750 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CSO_{110}	—	−70	−60	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz)	110–Channel FLAT	XMD_{110}	—	−62	−60	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case)	110–Channel FLAT	CTB_{110}	—	−62	−60	dBc
Noise Figure	50 MHz 750 MHz	NF	— —	— 5.5	5.5 6.5	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	280	310	350	mA

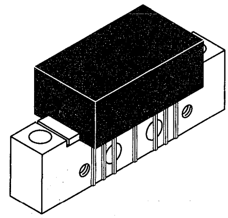
REV 1

The RF Line
High Output Power Doubler 860 MHz CATV Amplifier

MHW8185

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 19.4 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Typ) @ 860 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

19.4 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714Y–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

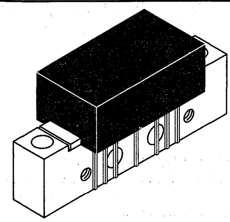
ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	18.3 19	18.8 19.4	19.3 20.5	dB
Slope	40–860 MHz	S	0	.5	1.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.3	1.0	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	19 —	— —	— 0.006	dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	CSO_{128} CSO_{110} CSO_{77}	— — —	–70 –72 –80	–62 — —	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	XMD_{128} XMD_{110} XMD_{77}	— — —	–72 –66 –69	–64 — —	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	CTB_{128} CTB_{110} CTB_{77}	— — —	–67 –64 –70	–64 — —	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 860 MHz	NF	— — — —	4.0 4.8 5.8 7.0	5.0 — — 8.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

The RF Line
High Output Power Doubler 860 MHz CATV Amplifier

MHW8205

**20.2 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER**



CASE 714Y–02, STYLE 1

- Specified for 77, 110 and 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 20.2 dB (Typ)
- Broadband Noise Figure
  NF = 7 dB (Typ) @ 860 MHz
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors
- Composite Triple Beat — @ 128–Channel Loading
  CTB = –66 dB (Typ)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

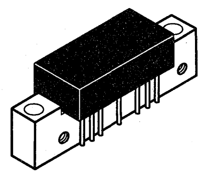
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	19.3 20	19.8 20.2	20.3 21.5	dB
Slope	40–860 MHz	S	0	.4	1.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.3	1.0	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	19 —	— —	— 0.006	dB dB/MHz
Composite Second Order (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	CSO_{128} CSO_{110} CSO_{77}	— — —	–69 –70 –80	–60 — —	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +40 dBmV/ch., FM = 55 MHz) (V_{out} = +44 dBmV/ch., FM = 55 MHz)	128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	XMD_{128} XMD_{110} XMD_{77}	— — —	–72 –65 –69	–64 — —	dBc
Composite Triple Beat (V_{out} = +40 dBmV/ch., Worst Case) (V_{out} = +44 dBmV/ch., Worst Case)	128–Channel FLAT 110–Channel FLAT 77–Channel FLAT	CTB_{128} CTB_{110} CTB_{77}	— — —	–66 –63 –70	–63 — —	dBc
Noise Figure	50 MHz 550 MHz 750 MHz 860 MHz	NF	— — — —	4.0 4.8 5.8 7.0	5.0 — — 8.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	365	400	435	mA

The RF Line
128-Channel (860 MHz) CATV Line Extender Amplifier

MHW8242

- Specified for 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 24 dB (Typ)
- Broadband Noise Figure
  NF = 7.5 dB (Max) @ 860 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors

24 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER



CASE 714–06, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

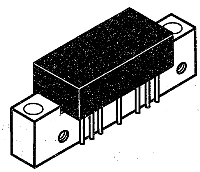
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	23.2 24	24 25	24.8 26.5	dB
Slope	40–860 MHz	S	0	1	2.5	dB
Gain Flatness (40–860 MHz, Peak To Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch., Worst Case)		CSO_{128}	—	−65	−60	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +38 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	−65	−60	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	−63	−60	dBc
Noise Figure	50 MHz 860 MHz	NF	— —	— —	5.5 7.5	dB
DC Current		I_{DC}	280	—	350	mA

The RF Line
128-Channel (860 MHz) CATV Line Extender Amplifier

MHW8272

27 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER

- Specified for 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 27 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 860 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors



CASE 714–06, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

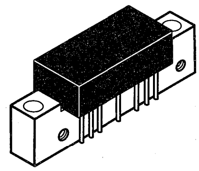
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	26.2 27	27 —	27.8 29.5	dB
Slope	40–860 MHz	S	0	1.0	2.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	—	–58	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +38 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	—	–60	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	—	–60	dBc
Noise Figure	50 MHz 860 MHz	NF	— —	— 6.0	5.5 7.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	280	310	350	mA

The RF Line
128-Channel (860 MHz) CATV Line Extender Amplifier

MHW8292

**29 dB GAIN
860 MHz
128–CHANNEL
CATV AMPLIFIER**

- Specified for 128–Channel Performance
- Broadband Power Gain — @ f = 40–860 MHz
  G_p = 29 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 860 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors



CASE 714–06, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	–20 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

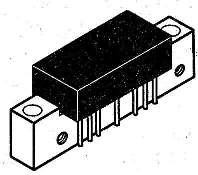
Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	860	MHz
Power Gain	50 MHz 860 MHz	G_p	28.2 29	29 —	29.8 31.5	dB
Slope	40–860 MHz	S	0	1.0	2.5	dB
Gain Flatness (40–860 MHz, Peak to Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.007	dB dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CSO_{128}	—	—	–56	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +38 dBmV/ch., FM = 55 MHz)	128–Channel FLAT	XMD_{128}	—	—	–60	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch., Worst Case)	128–Channel FLAT	CTB_{128}	—	—	–60	dBc
Noise Figure	50 MHz 860 MHz	NF	— —	— 6.0	5.5 7.0	dB
DC Current (V_{DC} = 24 V, T_C = 30°C)		I_{DC}	280	310	350	mA

The RF Line
152-Channel (1000 MHz) CATV Line Extender Amplifier

MHW9242

24 dB GAIN
1000 MHz
152–CHANNEL
CATV AMPLIFIER

- Specified for 152–Channel Performance
- Broadband Power Gain — @ f = 40–1000 MHz
  G_p = 24 dB (Typ)
- Broadband Noise Figure
  NF = 8 dB (Max) @ 1000 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion–Implanted Transistors



CASE 714–06, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	1000	MHz
Power Gain	50 MHz 1000 MHz	G_p	23.2 24	24 25	24.8 27	dB
Slope	40–1000 MHz	S	0	1	2.5	dB
Gain Flatness (40–1000 MHz, Peak–to–Valley)		—	—	0.5	1.0	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	@ 40 MHz @ f > 40 MHz (Derate)	IRL/ORL	20 —	— —	— 0.01	dB dB/MHz
Composite Second Order (V_{out} = +38 dBmV/ch., Worst Case)		CSO_{152}	—	−65	−59	dBc
Cross Modulation Distortion @ Ch 2 (V_{out} = +38 dBmV/ch., FM = 55 MHz)	152–Channel FLAT	XMD_{152}	—	−64	−59	dBc
Composite Triple Beat (V_{out} = +38 dBmV/ch., Worst Case)	152–Channel FLAT	CTB_{152}	—	−61	−58	dBc
Noise Figure	50 MHz 1000 MHz	NF	— —	−5.0 −7.0	5.5 8.0	dB
DC Current		I_{DC}	280	320	350	mA

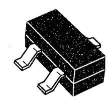
The RF Line
PNP Silicon High-Frequency Transistor

MMBR521LT1
MRF5211LT1

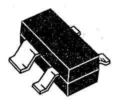
Designed primarily for use in the high–gain, low–noise small–signal amplifiers for operation up to 3.5 GHz. Also usable in applications requiring fast switching times.

- High Current Gain–Bandwidth Product —
  f_T = 3.4 GHz (Typ) @ I_C = −35 mAdc (MMBR521LT1)
  f_T = 4.2 GHz (Typ) @ I_C = −50 mAdc (MRF5211LT1)
- Low Noise Figure @ f = 1.0 GHz —
  $NF_{(matched)}$ = 2.5 dB (Typ) (MMBR521LT1)
  $NF_{(matched)}$ = 2.8 dB (Typ) (MRF5211LT1)
- High Power Gain — $G_{pe\ (matched)}$ = 11 dB (Typ)
- Guaranteed RF Parameters
- Surface Mounted SOT–23 (MMBR521LT1) & SOT–143 (MRF5211LT1) Offer Improved RF Performance
  Lower Package Parasitics
  Higher Gain
- Available in tape and reel packaging options:
  T1 suffix = 3,000 units per reel

I_C = −70 mA
HIGH–FREQUENCY TRANSISTOR
PNP SILICON



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE
(TO–236AA/AB)
MMBR521LT1



CASE 318A–05, STYLE 1
SOT–143
LOW PROFILE
MRF5211LT1

MAXIMUM RATINGS

Ratings		Symbol	Value	Unit
Collector–Emitter Voltage		V_{CEO}	−10	Vdc
Collector–Base Voltage		V_{CBO}	−20	Vdc
Emitter–Base Voltage		V_{EBO}	−2.5	Vdc
Power Dissipation (1) T_C = 75°C, Derate linearly above T_C = 75°C @	All	$P_{D(max)}$	0.333 4.44	W mW/°C
Collector Current — Continuous		I_C	−70	mA
Maximum Junction Temperature		T_{Jmax}	150	°C
Storage Temperature	All	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Ratings	Symbol	Value	Unit
Thermal Resistance, Junction to Case (MMBR521LT1, MRF5211LT1)	$R_{\theta JC}$	225	°C/W

DEVICE MARKING

MMBR521LT1 = 7M	MRF5211LT1 = 04

NOTE:
1. Case Temperature is measured on the collector lead closest to the package. For case temperatures above +75°C: $P_{DISP(max)} = (T_{Jmax} - T_C) / R_{\theta JC}$

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = –1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	–10	–12	—	Vdc
Collector–Base Breakdown Voltage (I_C = –0.1 mAdc, I_E = 0)		$V_{(BR)CBO}$	–20	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = –50 μAdc, I_C = 0)		$V_{(BR)EBO}$	–2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = –8.0 Vdc, I_E = 0)		I_{CBO}	—	—	–10	μAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = –30 mAdc, V_{CE} = –5.0 Vdc)		h_{FE}	25	—	125	—
DYNAMIC CHARACTERISTICS						
Collector–Base Capacitance (V_{CB} = –6.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	—	1.0	1.5	pF
Current Gain — Bandwidth Product		f_T				GHz
(V_{CE} = –8.0 V, I_C = –35 mA, f = 1.0 GHz)	MMBR521LT1		—	3.4	—	
(V_{CE} = –8.0 V, I_C = –50 mA, f = 1.0 GHz)	MRF5211LT1		—	4.2	—	
FUNCTIONAL TESTS						
Power Gain at Minimum Noise Figure		G_{NFmin}				dB
(V_{CE} = –6.0 V, I_C = –5.0 mA, f = 500 MHz)	MMBR521LT1		13	15	—	
(V_{CE} = –6.0 V, I_C = –5.0 mA, f = 1.0 GHz)	MMBR521LT1		8.0	10	—	
(V_{CE} = –6.0 V, I_C = –5.0 mA, f = 1.0 GHz)	MRF5211LT1		10	11	—	
Noise Figure — Minimum		NF_{min}				dB
(V_{CE} = –6.0 V, I_C = –5.0 mA, f = 500 MHz)	MMBR521LT1		—	1.5	2.5	
(V_{CE} = –6.0 V, I_C = –5.0 mA, f = 1.0 GHz)	MMBR521LT1		—	2.5	3.5	
(V_{CE} = –6.0 V, I_C = –5.0 mA, f = 1.0 GHz)	MRF5211LT1		—	2.8	3.5	

TYPICAL CHARACTERISTICS

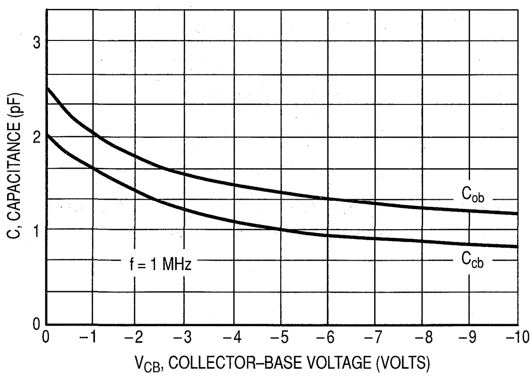


Figure 1. Junction Capacitance versus Voltage

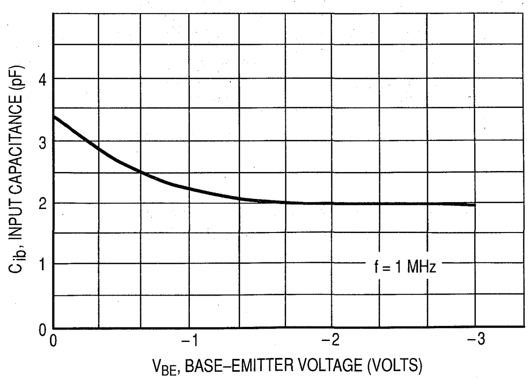


Figure 2. Input Capacitance versus Voltage

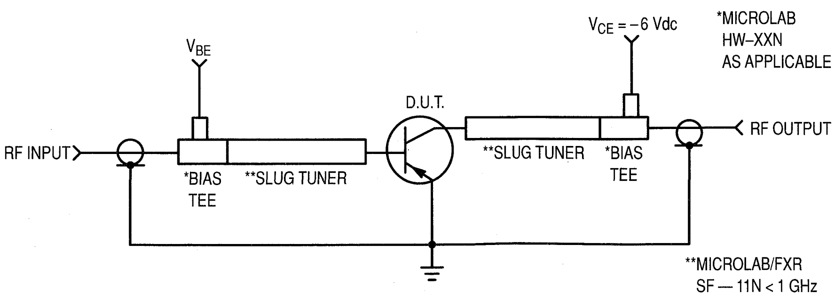


Figure 3. Functional Circuit Schematic

TYPICAL CHARACTERISTICS
MMBR521LT1

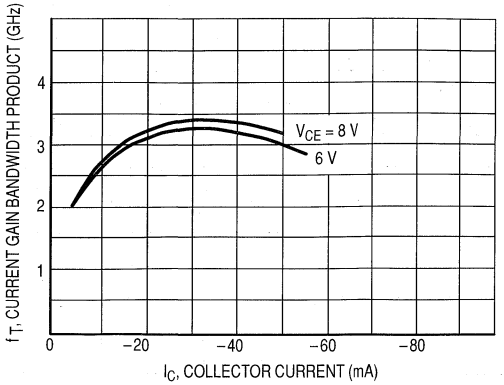


Figure 4. Current Gain Bandwidth Product versus Collector Current

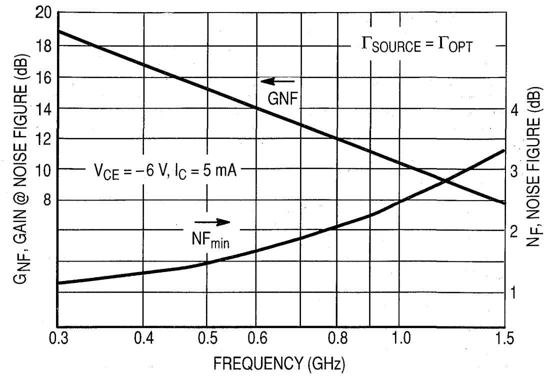


Figure 5. Minimum Noise Figure & Gain @ Noise Figure versus Frequency

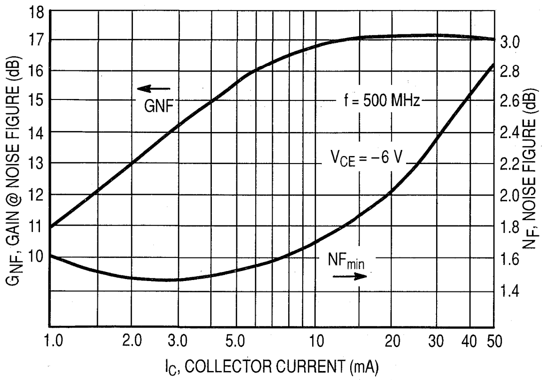


Figure 6. Minimum Noise Figure & Gain @ Noise Figure versus Collector Current

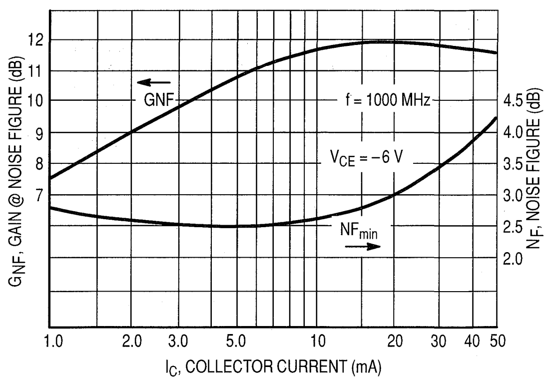


Figure 7. Minimum Noise Figure & Gain @ Noise Figure versus Collector Current

TYPICAL CHARACTERISTICS
MRF5211LT1

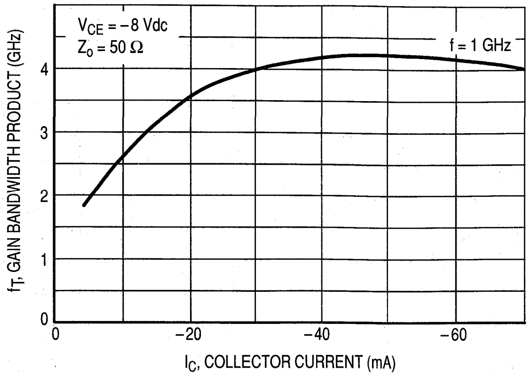


Figure 8. Gain–Bandwidth Product versus Current

GAIN AND NOISE FIGURE versus FREQUENCY

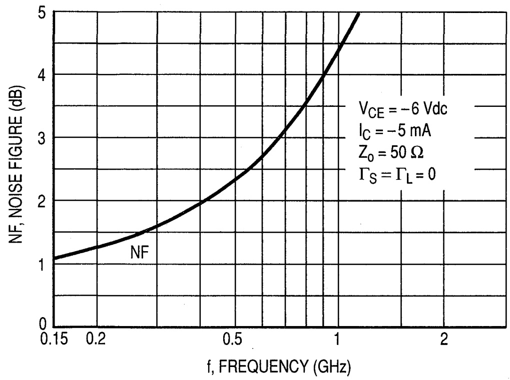


Figure 9. 50 Ohm Noise Figure

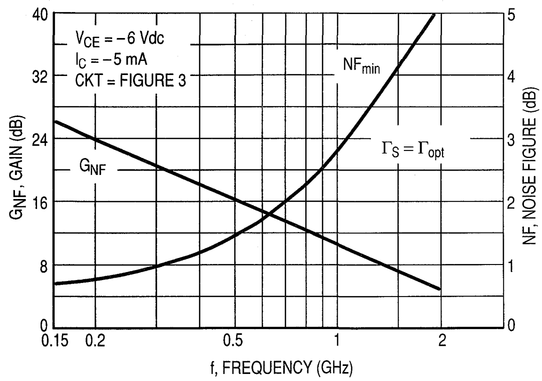


Figure 10. Tuned Circuit

GAIN AND NOISE FIGURE versus CURRENT

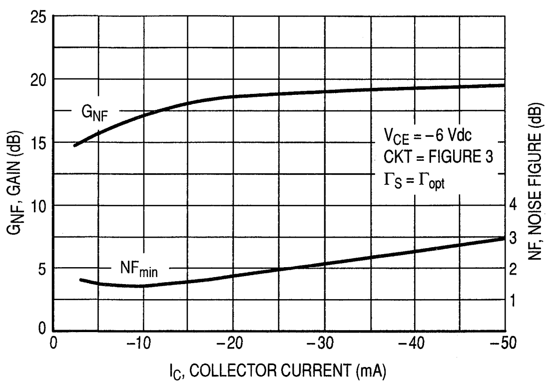


Figure 11. Tuned Circuit — Frequency 500 MHz

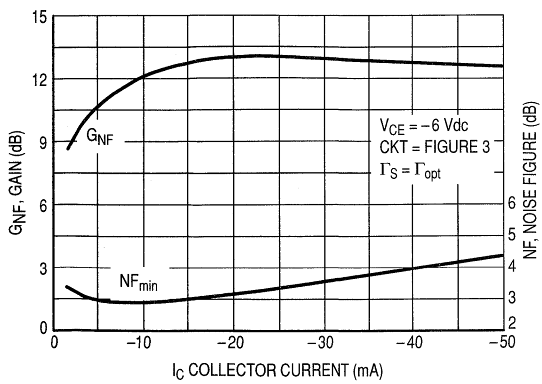


Figure 12. Tuned Circuit — Frequency 1.0 GHz

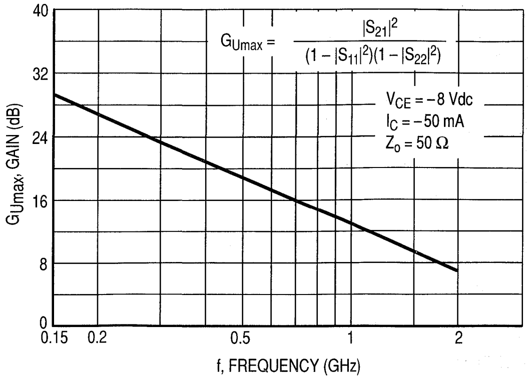


Figure 13. G_{Umax} versus Current

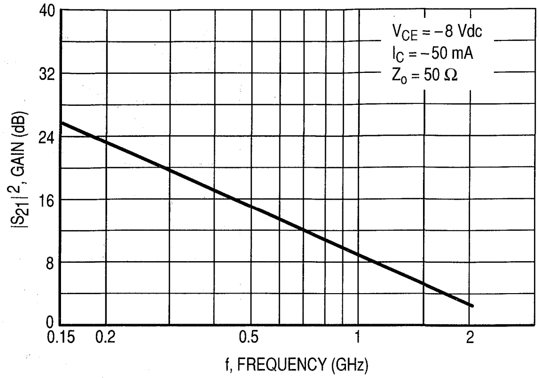


Figure 14. Insertion Gain versus Frequency

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
6	5	100	0.754	–67	11.453	141	0.040	59	0.818	–24
		300	0.683	–132	6.106	105	0.065	39	0.549	–37
		500	0.667	–157	3.954	89	0.071	39	0.472	–40
		700	0.660	–171	2.890	78	0.078	44	0.452	–44
		900	0.656	179	2.294	69	0.085	50	0.449	–49
		1000	0.654	175	2.086	65	0.091	53	0.451	–52
		1500	0.641	158	1.442	48	0.130	64	0.480	–66
		2000	0.672	140	1.108	36	0.188	69	0.466	–79
		2500	0.681	124	0.917	26	0.261	66	0.483	–94
		3000	0.681	110	0.793	18	0.343	60	0.493	–110
		3500	0.686	96	0.716	13	0.426	52	0.500	–126
		4000	0.683	84	0.674	9	0.503	43	0.502	–143
		4500	0.678	73	0.653	6	0.568	34	0.503	–160
		5000	0.669	64	0.653	3	0.620	24	0.507	–176
	10	100	0.632	–92	16.621	131	0.032	55	0.694	–33
		300	0.618	–149	7.460	98	0.050	47	0.417	–41
		500	0.618	–168	4.671	85	0.061	53	0.358	–44
		700	0.616	–178	3.392	76	0.076	58	0.346	–47
		900	0.615	173	2.672	68	0.092	62	0.347	–52
		1000	0.613	170	2.429	64	0.100	63	0.352	–55
		1500	0.601	155	1.677	48	0.150	66	0.382	–68
		2000	0.633	138	1.294	36	0.208	66	0.371	–80
		2500	0.642	124	1.078	25	0.273	62	0.391	–94
		3000	0.646	110	0.929	16	0.346	56	0.408	–109
		3500	0.656	98	0.827	10	0.422	49	0.421	–124
		4000	0.662	86	0.756	4	0.494	41	0.431	–141
		4500	0.664	75	0.709	1	0.554	32	0.442	–158
		5000	0.664	66	0.683	–3	0.609	24	0.455	–174
	50	100	0.547	–149	21.107	115	0.017	63	0.441	–43
		300	0.606	–174	7.891	90	0.037	68	0.260	–42
		500	0.616	177	4.811	80	0.058	73	0.239	–44
		700	0.616	171	3.480	72	0.080	73	0.242	–48
		900	0.616	165	2.746	65	0.102	73	0.248	–54
		1000	0.615	163	2.479	61	0.113	72	0.255	–57
		1500	0.606	150	1.717	46	0.169	69	0.293	–71
		2000	0.643	135	1.327	33	0.229	65	0.289	–82
		2500	0.654	122	1.097	22	0.292	60	0.315	–96
		3000	0.662	108	0.940	13	0.359	54	0.337	–110
		3500	0.672	96	0.825	6	0.427	47	0.356	–126
		4000	0.680	84	0.743	1	0.493	39	0.373	–142
		4500	0.682	74	0.688	–2	0.551	31	0.391	–159
		5000	0.679	64	0.658	–5	0.601	22	0.409	–175
10	5	100	0.792	–59	11.498	144	0.036	62	0.848	–21
		300	0.681	–123	6.513	108	0.061	41	0.598	–32
		500	0.652	–150	4.278	91	0.068	40	0.518	–36
		700	0.639	–166	3.142	80	0.073	44	0.496	–39
		900	0.631	–177	2.491	71	0.081	49	0.489	–44
		1000	0.628	179	2.264	67	0.086	53	0.492	–46
		1500	0.616	161	1.560	50	0.120	64	0.514	–58
		2000	0.644	142	1.199	37	0.171	69	0.500	–70
		2500	0.654	126	0.985	26	0.238	68	0.516	–83
		3000	0.661	111	0.843	18	0.314	63	0.523	–98
		3500	0.670	98	0.749	12	0.399	56	0.529	–113
		4000	0.672	85	0.690	8	0.479	47	0.528	–129
		4500	0.671	73	0.656	5	0.549	38	0.524	–146
		5000	0.665	63	0.649	3	0.609	28	0.523	–162
10	10	100	0.666	–80	17.255	135	0.030	58	0.738	–28
		300	0.596	–141	8.143	101	0.047	48	0.465	–37
		500	0.587	–162	5.139	87	0.059	53	0.404	–38
		700	0.581	–174	3.741	78	0.072	58	0.388	–41
		900	0.578	177	2.947	70	0.086	61	0.387	–45
		1000	0.577	174	2.670	66	0.095	63	0.389	–48
		1500	0.565	158	1.856	50	0.139	66	0.413	–60
		2000	0.596	140	1.431	38	0.191	66	0.402	–70
		2500	0.608	126	1.177	26	0.253	64	0.420	–82
		3000	0.619	112	1.008	17	0.319	59	0.434	–96
		3500	0.632	99	0.886	9	0.393	52	0.444	–110
		4000	0.644	87	0.797	3	0.465	44	0.453	–126
		4500	0.652	75	0.732	–1	0.532	36	0.457	–143
		5000	0.654	65	0.694	–4	0.589	28	0.465	–159

Table 1. MMBR521LT1 Common Emitter S–Parameters

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
−6.0	−5.0	200	0.82	−114	7.9	118	0.07	35	0.59	−46
		500	0.81	−158	4.0	88	0.08	21	0.40	−54
		1000	0.79	175	2.0	67	0.08	21	0.37	−68
		1500	0.76	158	1.3	50	0.07	30	0.43	−82
		2000	0.74	143	1.0	38	0.08	47	0.47	−95
	−10	200	0.78	−137	10.6	109	0.05	32	0.43	−63
		500	0.79	−168	4.9	84	0.06	28	0.26	−75
		1000	0.77	169	2.5	66	0.06	39	0.24	−87
		1500	0.74	155	1.6	50	0.08	49	0.29	−97
		2000	0.71	140	1.2	39	0.10	55	0.32	−106
	−50	200	0.77	−167	13.1	99	0.02	45	0.26	−108
		500	0.77	176	5.7	80	0.04	57	0.18	−132
		1000	0.76	161	2.8	65	0.06	65	0.17	−142
		1500	0.73	149	1.9	51	0.08	67	0.19	−137
		2000	0.70	136	1.4	40	0.12	65	0.20	−137
−8.0	−5.0	200	0.82	−109	8.1	119	0.07	36	0.62	−43
		500	0.80	−154	4.2	90	0.08	22	0.42	−52
		1000	0.78	175	2.2	67	0.08	22	0.38	−65
		1500	0.75	159	1.4	50	0.07	31	0.43	−78
		2000	0.72	143	1.0	37	0.09	43	0.46	−89
	−10	200	0.77	−132	11.2	110	0.05	33	0.45	−61
		500	0.77	−167	5.2	86	0.06	29	0.27	−70
		1000	0.76	169	2.6	67	0.06	39	0.25	−81
		1500	0.73	155	1.7	51	0.07	49	0.29	−90
		2000	0.70	140	1.3	39	0.10	54	0.31	−98
	−50	200	0.75	−164	14.2	100	0.02	43	0.26	−101
		500	0.76	178	6.1	82	0.04	55	0.17	−121
		1000	0.75	163	3.1	67	0.06	64	0.15	−131
		1500	0.72	151	2.0	53	0.08	67	0.18	−126
		2000	0.70	139	1.5	42	0.11	68	0.19	−127

Table 2. MRF5211LT1 Common Emitter S–Parameters

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

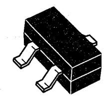
The RF Line
NPN Silicon High-Frequency Transistors

MMBR571LT1
MRF571
MRF5711LT1

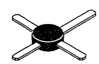
Designed for low noise, wide dynamic range front–end amplifiers and low–noise VCO's. Available in a surface–mountable plastic packages. This Motorola series of small–signal plastic transistors offers superior quality and performance at low cost.

- High Gain–Bandwidth Product
  f_T = 8.0 GHz (Typ) @ 50 mA
- Low Noise Figure
  NF_{min} = 1.6 dB (Typ) @ f = 1.0 GHz (MRF5711LT1, MRF571)
- High Gain
  G_{NF} = 17 dB (Typ) @ 30 mA/500 MHz (MMBR571LT1)
- High Power Gain
  $G_{pe\ (matched)}$ = 13.5 dB (Typ) (MRF5711LT1)
- State–of–the–Art Technology
  Fine Line Geometry
  Ion–Implanted Arsenic Emitters
  Gold Top Metallization and Wires
  Silicon Nitride Passivation
- Available in tape and reel packaging options:
  T1 suffix = 3,000 units per reel

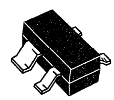
I_C = 80 mA
LOW NOISE
HIGH–FREQUENCY
TRANSISTORS



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE
MMBR571LT1



CASE 317–01, STYLE 2
MACRO–X
MRF571



CASE 318A–05, STYLE 1
SOT–143
LOW PROFILE
MRF5711LT1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	10	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Emitter–Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	80	mA
Total Device Dissipation @ T_{case} = 75°C MMBR571LT1, MRF5711LT1 Derate linearly above T_{case} = 75°C @	$P_{D(max)}$	0.33 4.44	W mW/°C
Total Device Dissipation (1) @ T_C = 75°C Derate above 75°C MRF571	P_D	0.58 7.73	Watts mW/°C
Operating and Storage Temperature	T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance, Junction to Case MRF5711LT1, MMBR571LT1	$R_{\theta JC}$	225	°C/W
Thermal Resistance, Junction to Case MRF571	$R_{\theta JC}$	130	°C/W
Maximum Junction Temperature	T_{Jmax}	150	°C

DEVICE MARKING

MMBR571LT1 = 7X	MRF5711LT1 = 02

NOTE:
1. Case temperature measured on collector lead immediately adjacent to body of package.

REV 8

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector–Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0)			$V_{(BR)CEO}$	10	12	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)			$V_{(BR)CBO}$	20	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 50 μAdc, I_C = 0)			$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 8.0 Vdc, I_E = 0)			I_{CBO}	—	—	10	μAdc
ON CHARACTERISTICS							
DC Current Gain (I_C = 30 mAdc, V_{CE} = 5.0 Vdc)			h_{FE}	50	—	300	—
DYNAMIC CHARACTERISTICS							
Collector–Base Capacitance			C_{cb}				pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	MMBR571LT1			—	0.7	1.0	
(V_{CB} = 6.0 Vdc, I_E = 0, f = 1.0 MHz)	MRF5711LT1, MRF571			—	0.75	1.0	
Current Gain–Bandwidth Produc			f_T				GHz
(V_{CE} = 5.0 Vdc, I_C = 50 mAdc, f = 1.0 GHz)	MMBR571LT1			—	8.0	—	
(V_{CE} = 8.0 Vdc, I_C = 50 mAdc, f = 1.0 GHz)	MRF5711LT1, MRF571			—	8.0	—	
FUNCTIONAL TESTS							
Gain @ Noise Figure	MRF571	f = 0.5 GHz	G_{NF}	—	16.5	—	dB
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc)	MRF571	f = 1.0 GHz		10	12	—	
Noise Figure	MRF571	f = 0.5 GHz	NF	—	1.0	—	dB
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc)	MRF571	f = 1.0 GHz		—	1.5	2.0	
		f = 2.0 GHz		—	2.8	—	
Gain @ Noise Figure			G_{NF}				dB
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MMBR571LT1	f = 0.5 GHz		—	16.5	—	
		f = 1.0 GHz		—	10.5	—	
(I_C = 10 mA, V_{CE} = 6.0 Vdc)	MRF5711LT1	f = 1.0 GHz		—	13.5	—	
Noise Figure			NF				dB
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MMBR571LT1	f = 0.5 GHz		—	2.0	—	
		f = 1.0 GHz		—	2.6	—	
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc)	MRF5711LT1	f = 1.0 GHz		—	2.2	—	
Noise Figure			NF_{min}	—	1.6	—	dB
(V_{CE} = 6.0 V, I_C = 10 mA, f = 1.0 GHz)	MRF5711LT1						
Power Gain in 50 Ω System (V_{CE} = 6.0 V, I_C = 10 mA, f = 1.0 GHz)	MRF5711LT1		$\|S_{21}\|^2$	9.0	10	—	dB

TYPICAL CHARACTERISTICS
MMBR571LT1

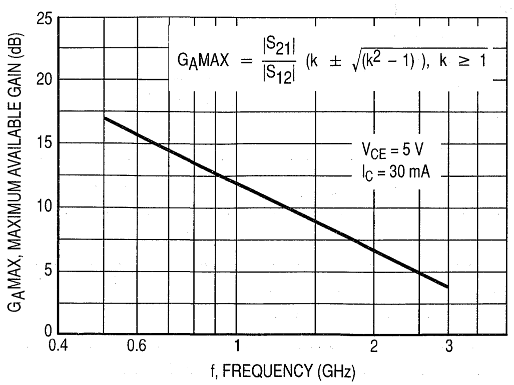


Figure 1. Maximum Available Gain versus Frequency

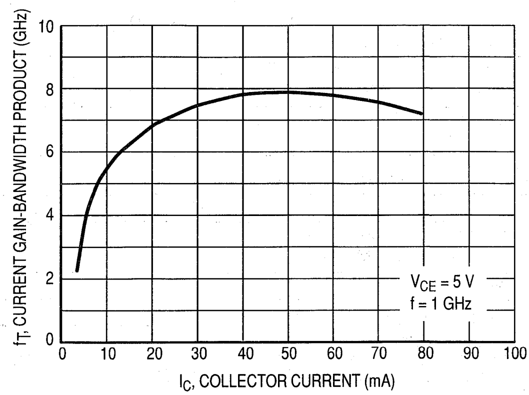


Figure 2. Current Gain–Bandwidth versus Collector Current @ 1.0 GHz

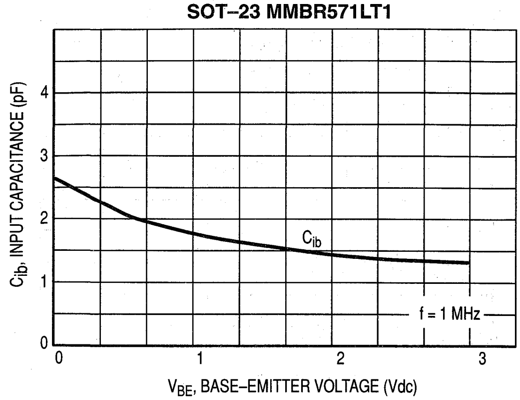


Figure 3. Input Capacitance versus Emitter Base Voltage

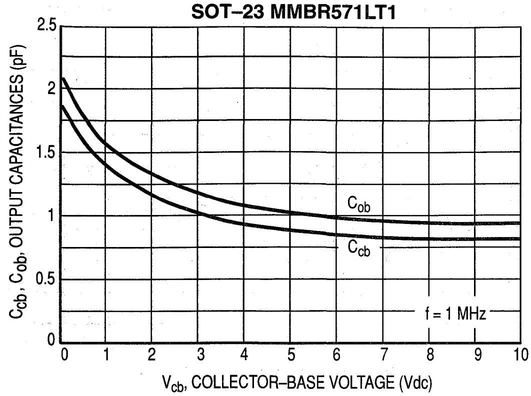


Figure 4. Output Capacitances versus Collector–Base Voltage

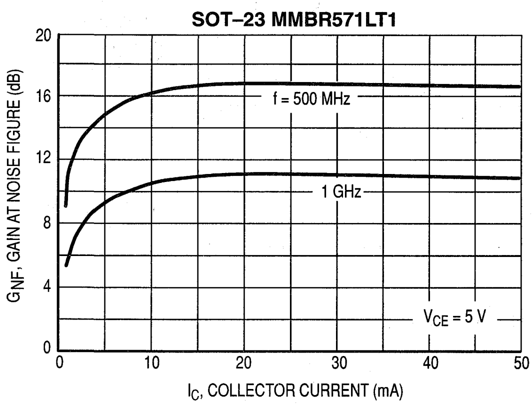


Figure 5. Gain at Noise Figure versus Collector Current

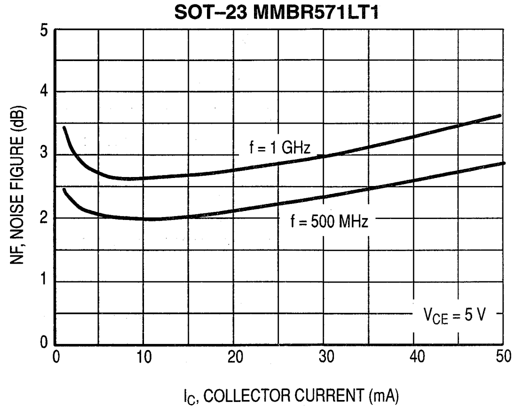


Figure 6. Noise Figure versus Collector Current

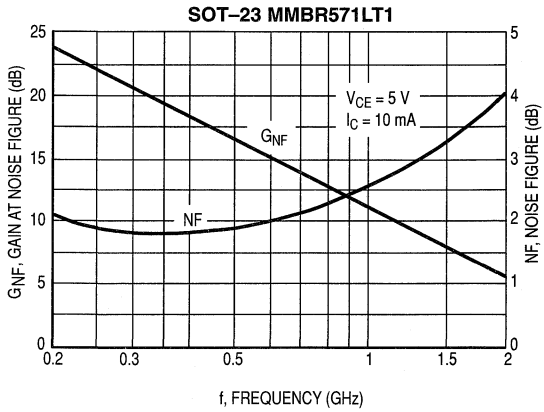


Figure 7. Gain at Noise Figure and Noise Figure versus Frequency

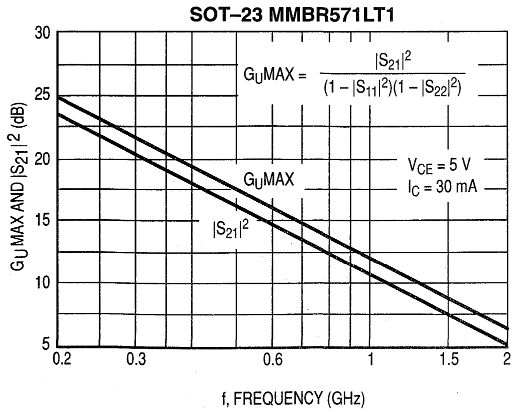


Figure 8. Maximum Unilateral Gain and Insertion Gain versus Frequency

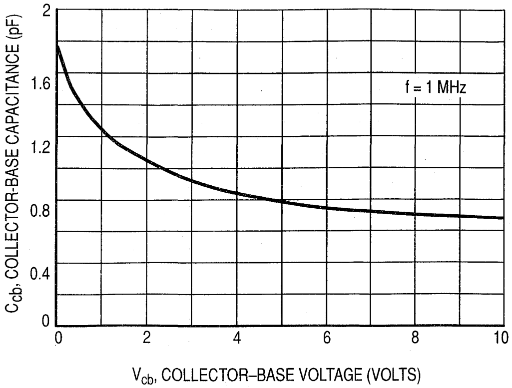


Figure 9. Collector–Base Capacitance versus Collector–Base Voltage

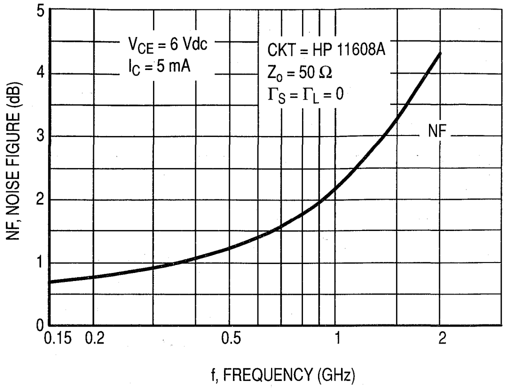


Figure 10. 50 Ω Noise Figure versus Frequency

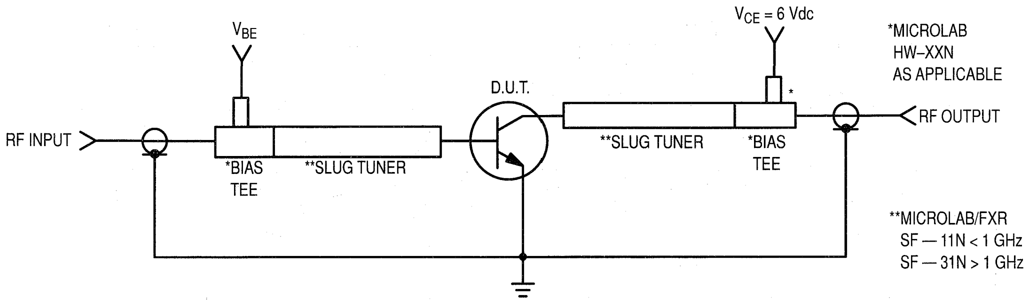


Figure 11. Functional Circuit Schematic

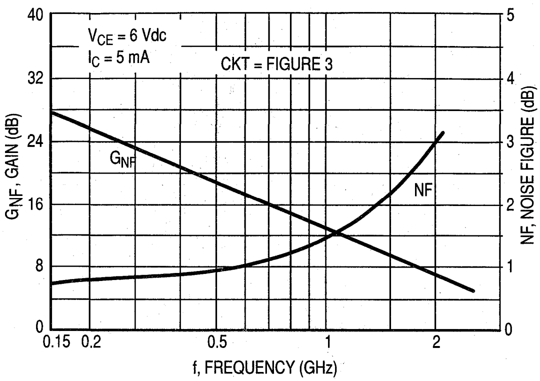


Figure 12. Gain and Noise Figure versus Frequency

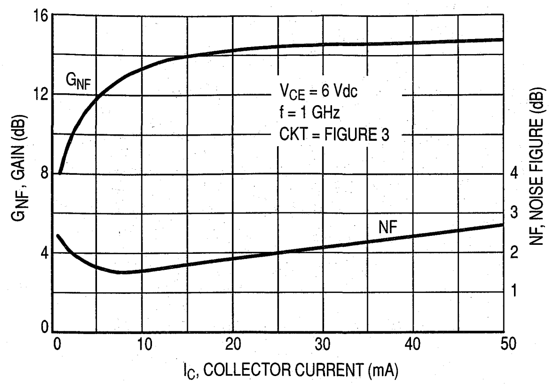


Figure 13. Gain and Noise Figure versus Collector Current

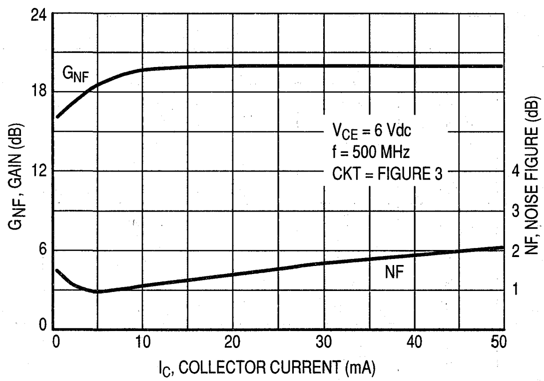


Figure 14. Gain and Noise Figure versus Collector Current

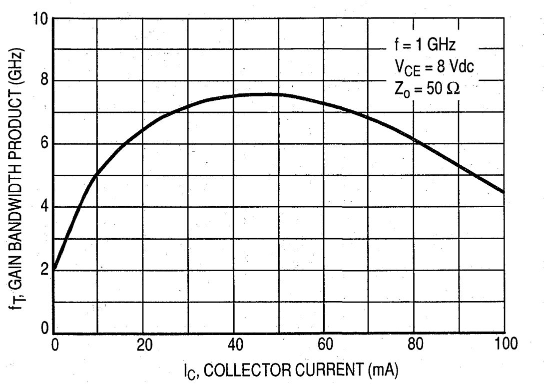


Figure 15. Gain Bandwidth Product versus Collector Current

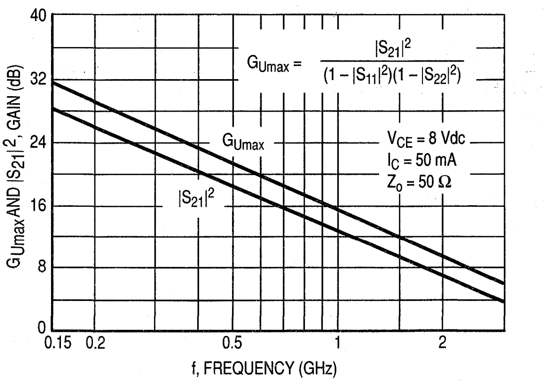


Figure 16. G_{Umax} and $|S_{21}|^2$ versus Frequency

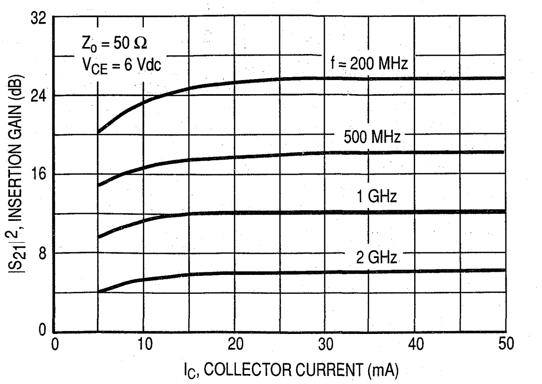


Figure 17. Insertion Gain versus Collector Current

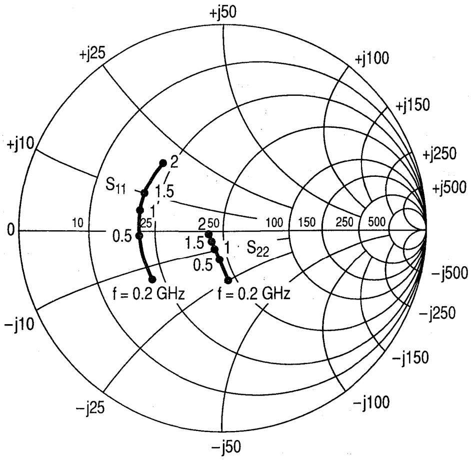


Figure 18. Input/Output Reflection Coefficients versus Frequency
V_{CE} = 5.0 V, I_C = 30 mA

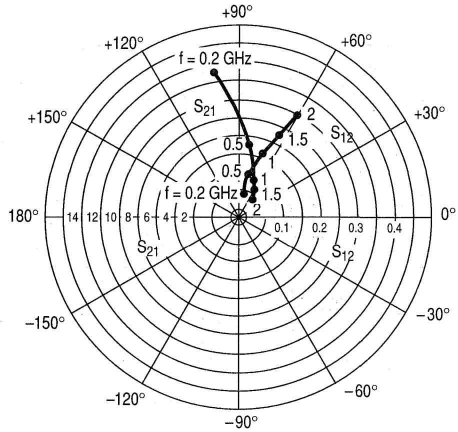
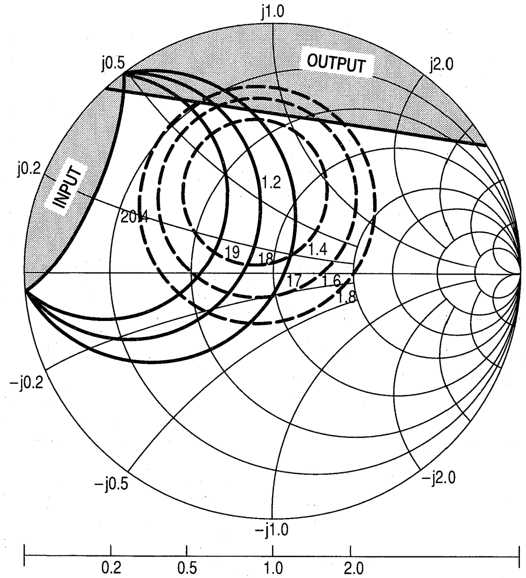


Figure 19. Forward/Reverse Transmission Coefficients versus Frequency
V_{CE} = 5.0 V, I_C = 30 mA

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
5.0	5.0	200	0.68	−82	8.41	126	0.07	53	0.61	−45
		500	0.52	−142	4.62	93	0.10	46	0.35	−60
		1000	0.50	179	2.57	72	0.14	53	0.26	−71
		1500	0.51	161	1.82	57	0.19	58	0.24	−77
		2000	0.52	143	1.48	45	0.24	59	0.22	−86
	15	200	0.46	−125	13.65	108	0.05	60	0.35	−73
		500	0.43	−169	6.03	86	0.09	66	0.17	−94
		1000	0.44	168	3.20	72	0.16	67	0.14	−111
		1500	0.45	152	2.21	58	0.22	64	0.11	−118
		2000	0.46	137	1.80	48	0.29	59	0.10	−131
	30	200	0.42	−148	14.79	102	0.04	68	0.26	−87
		500	0.41	−177	6.31	84	0.09	72	0.14	−115
		1000	0.42	165	3.35	71	0.16	70	0.12	−135
		1500	0.44	151	2.29	59	0.23	65	0.11	−144
		2000	0.44	135	1.84	48	0.30	60	0.10	−157
	50	200	0.41	−159	15.14	98	0.04	73	0.21	−96
		500	0.42	179	6.38	83	0.09	75	0.13	−124
		1000	0.43	163	3.35	70	0.16	71	0.12	−143
		1500	0.44	148	2.32	58	0.23	66	0.10	−151
		2000	0.45	134	1.84	48	0.30	60	0.09	−163

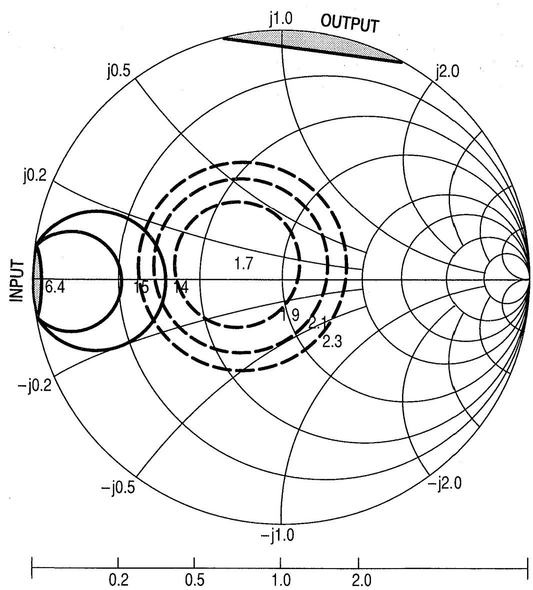
Table 1. MMBR571LT1 Common Emitter S–Parameters



V_{CE} = 5 V
I_C = 10 mA
▒ = Area of Instability

f (GHz)	NF OPT	ΓMS NF OPT	Rn	K
0.5	1.20 dB	0.36 ∠ 104°	7	0.63

Figure 20. MRF5711LT1 Constant Gain and Noise Figure Contours (f = 0.5 GHz)



V_{CE} = 5 V
I_C = 10 mA
▒ = Area of Instability

f (GHz)	NF OPT	ΓMS NF OPT	Rn	K
1.0	1.70 dB	0.20 ∠ 162°	8	0.94

Figure 21. MRF5711LT1 Constant Gain and noise Figure Contours (f = 1.0 GHz)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
6.0	5.0	200	0.79	−90	10.9	128	0.06	46	0.70	−45
		500	0.72	−144	5.7	96	0.08	28	0.42	−66
		1000	0.69	−177	3.0	75	0.09	28	0.31	−77
		1500	0.66	164	2.0	59	0.10	32	0.34	−89
		2000	0.65	147	1.6	47	0.12	38	0.32	−94
	10	200	0.72	−115	15.2	118	0.05	41	0.55	−66
		500	0.69	−160	6.9	92	0.06	34	0.30	−92
		1000	0.67	174	3.6	74	0.08	42	0.21	−108
		1500	0.64	159	2.4	60	0.10	46	0.23	−114
		2000	0.64	143	1.8	49	0.12	50	0.20	−116
	50	200	0.67	−159	20	102	0.02	48	0.33	−111
		500	0.67	179	8.2	85	0.04	58	0.33	−142
		1000	0.66	174	3.8	72	0.07	65	0.21	−158
		1500	0.63	151	2.7	61	0.10	64	0.22	−158
		2000	0.58	138	2.1	51	0.14	62	0.17	−165
8.0	5.0	200	0.80	−87	11.1	130	0.06	47	0.71	−42
		500	0.72	−141	5.9	97	0.08	30	0.44	−60
		1000	0.70	−177	3.1	75	0.09	28	0.33	−68
		1500	0.66	166	2.1	60	0.10	32	0.35	−80
		2000	0.61	149	1.6	47	0.12	39	0.35	−85
	10	200	0.72	−113	15.6	119	0.05	42	0.56	−61
		500	0.68	−159	7.2	92	0.06	34	0.31	−82
		1000	0.66	175	3.7	74	0.08	41	0.21	−92
		1500	0.64	160	2.5	61	0.09	47	0.23	−101
		2000	0.60	144	2.0	49	0.13	50	0.21	−103
	50	200	0.66	−156	20.9	103	0.02	48	0.31	−101
		500	0.65	−179	8.6	85	0.04	58	0.19	−128
		1000	0.64	164	4.3	72	0.07	65	0.16	−144
		1500	0.61	153	2.9	61	0.10	65	0.17	−142
		2000	0.58	137	2.3	51	0.13	64	0.14	−145

Table 2. MRF5711LT1 Common Emitter S–Parameters

TYPICAL CHARACTERISTICS
MRF571

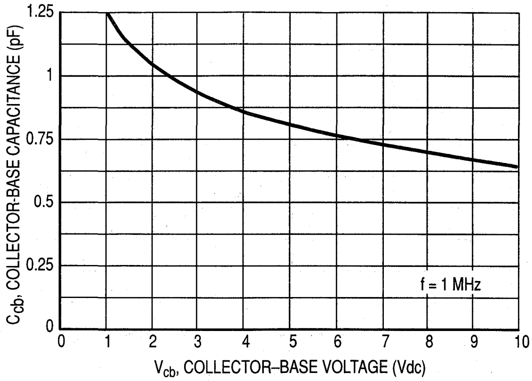


Figure 22. C_{cb}, Collector–Base Capacitance versus Voltage

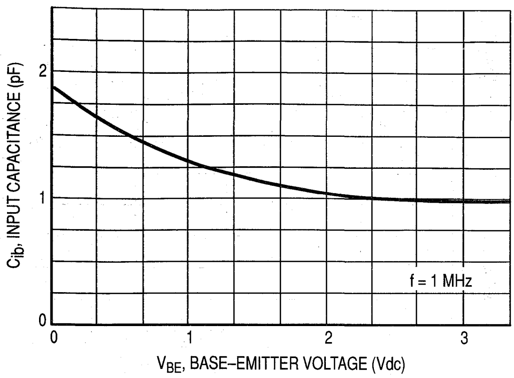


Figure 23. C_{ib}, Input Capacitance versus Emitter Base Voltage

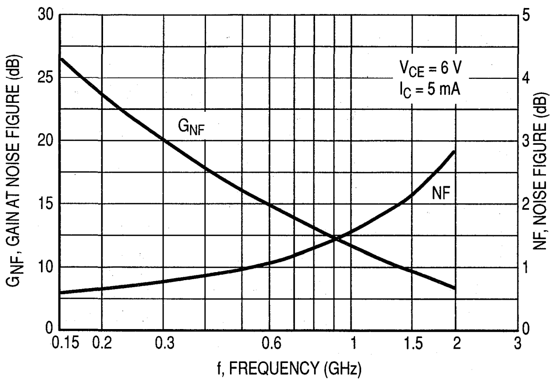


Figure 24. Gain at Noise Figure and Noise Figure versus Frequency

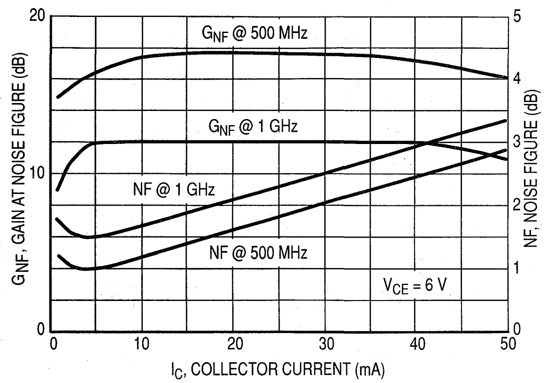


Figure 25. Gain at Noise Figure and Noise Figure versus Collector Current

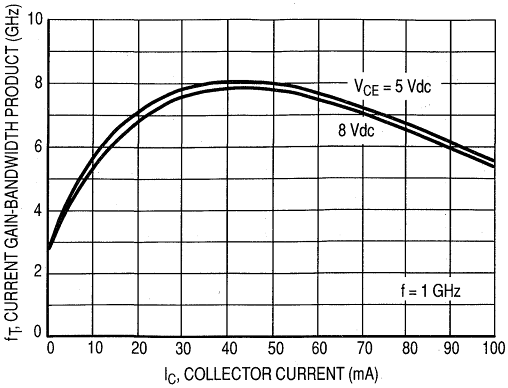


Figure 26. f_T, Current Gain–Bandwidth Product versus Collector Current

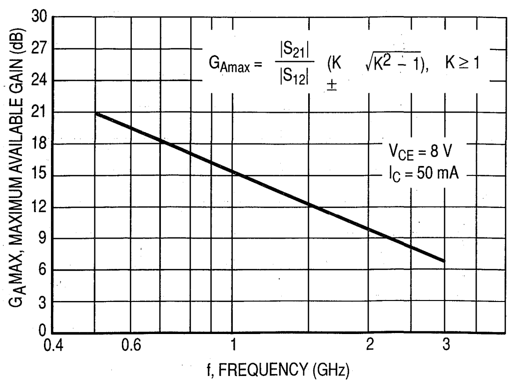


Figure 27. G_{Amax}, Maximum Available Gain versus Frequency

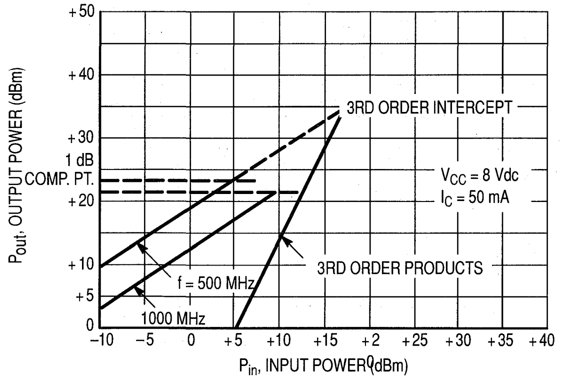


Figure 28. 1.0 dB Compression Point and Third Order Intercept

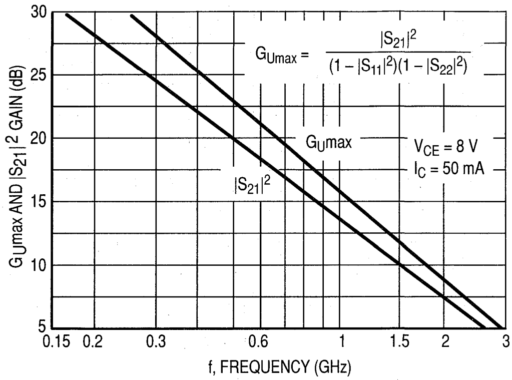


Figure 29. G_Umax and $|S_{21}|^2$ versus Frequency

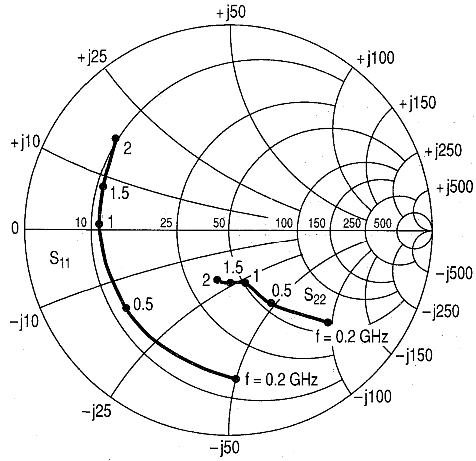


Figure 30. Input/Output Reflection Coefficients versus Frequency (GHz)
V_{CE} = 6.0 V, I_C = 5.0 mA

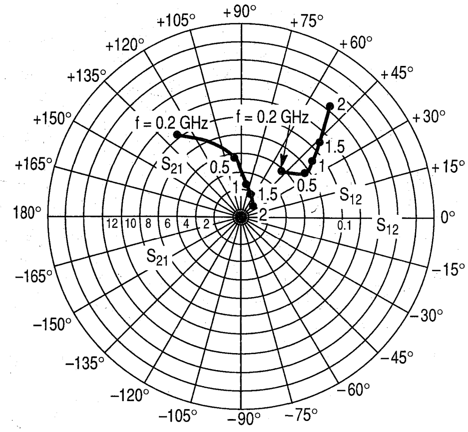
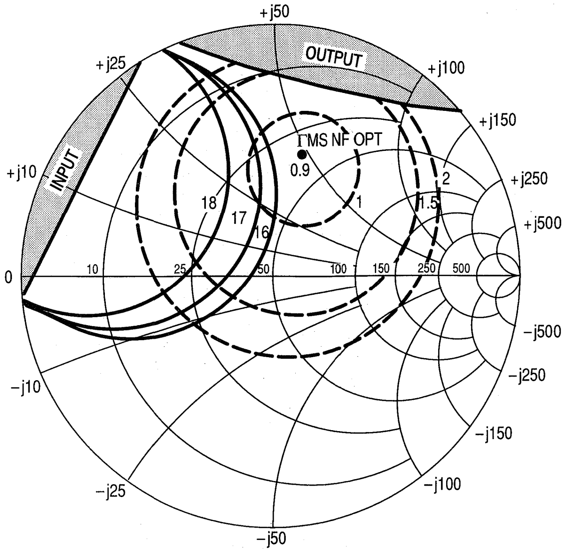


Figure 31. Forward/Reverse Transmission Coefficients versus Frequency (GHz)
V_{CE} = 6.0 V, I_C = 5.0 mA

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11} $\|S_{11}\|$	S_{11} ∠ φ	S_{21} $\|S_{21}\|$	S_{21} ∠ φ	S_{12} $\|S_{12}\|$	S_{12} ∠ φ	S_{22} $\|S_{22}\|$	S_{22} ∠ φ
6.0	5	200	0.74	−86	10.5	129	0.06	48	0.69	−42
		500	0.62	−143	5.5	97	0.08	33	0.41	−59
		1000	0.61	178	3.0	78	0.09	37	0.28	−69
		1500	0.65	158	2.0	62	0.11	44	0.26	−88
		2000	0.70	140	1.6	51	0.14	51	0.27	−99
	10	200	0.64	−111	15	118	0.04	44	0.53	−59
		500	0.58	−160	6.9	93	0.06	42	0.27	−77
		1000	0.59	168	3.7	77	0.09	52	0.16	−91
		1500	0.63	151	2.5	64	0.12	56	0.16	−113
		2000	0.67	134	2.0	53	0.16	57	0.16	−118
	50	200	0.56	−160	20.4	102	0.02	57	0.27	−98
		500	0.57	176	8.4	86	0.05	67	0.14	−130
		1000	0.60	156	4.4	75	0.09	70	0.11	−164
		1500	0.62	152	2.9	64	0.13	68	0.13	−175
		2000	0.66	127	2.4	53	0.18	62	0.11	−178
8.0	5	200	0.75	−83	10.7	129	0.06	49	0.71	−39
		500	0.62	−140	5.1	98	0.08	34	0.43	−54
		1000	0.60	−179	3.7	78	0.09	38	0.31	−62
		1500	0.64	159	2.1	62	0.10	45	0.29	−80
		2000	0.69	141	1.7	52	0.13	52	0.29	−91
	10	200	0.64	−99	15.1	120	0.05	46	0.54	−60
		500	0.52	−152	7.1	94	0.07	45	0.32	−75
		1000	0.52	170	3.7	76	0.10	54	0.15	−82
		1500	0.52	150	2.5	62	0.13	56	0.16	−108
		2000	0.57	133	2.0	51	0.18	55	0.16	−107
	50	200	0.52	−153	19.6	102	0.03	56	0.28	−92
		500	0.52	178	8.1	86	0.05	67	0.16	−98
		1000	0.56	157	4.1	73	0.10	70	0.06	−130
		1500	0.54	139	2.8	62	0.13	68	0.11	−146
		2000	0.59	126	2.2	52	0.19	63	0.10	−137

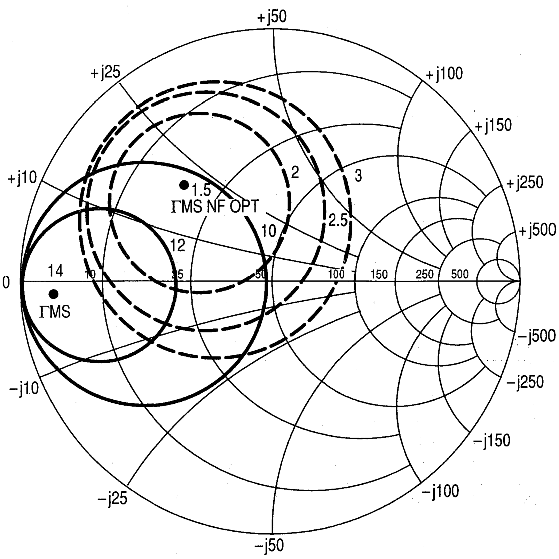
Table 3. MRF571 Common Emitter S–Parameters



V_{CE} = 6.0 V, I_C = 5.0 mA
f = 500 MHz
▨ — REGION OF INSTABILITY

f (GHz)	NF OPT (dB)	Rn (Ω)	NF50 Ω (dB)
0.5	0.9	9.3	1.3

ΓMS NF OPT	K
0.49 ∠ 74°	0.58

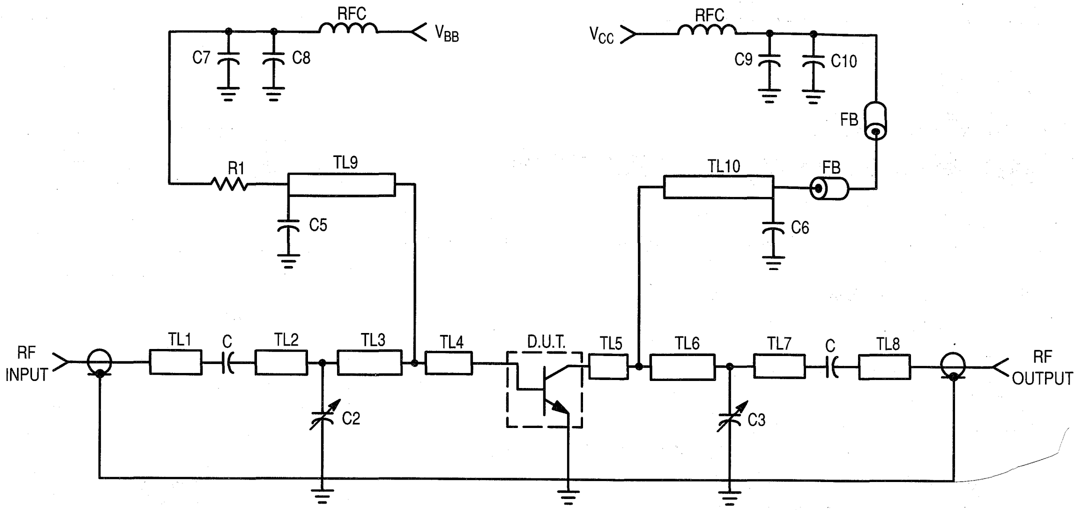


V_{CE} = 6.0 V, I_C = 5.0 mA
f = 1.0 GHz

f (GHz)	NF OPT (dB)	Rn (Ω)	NF50 Ω (dB)	ΓMS NF OPT
1.0	1.5	7.5	2.2	0.48 ∠ 134°

ΓMS	ΓML
0.89 ∠ −179°	0.81 ∠ 66°

Figure 32. MRF571 Constant Gain and Noise Figure Contours



C1, C4, C5, C6, C8, C9 — 100 pF Chip Capacitor
C2, C3 — 0.8–8.0 pF Johanson Capacitor
C7, C10 — 10 μF Tantalum Capacitor
R1 — 1.0 kOhms Res.
RFC — VK–200, Ferroxcube
FB — Ferrite Bead, Ferroxcube 56–590–65/3B
Board Material — 0.0625″ Glass Teflon, $\varepsilon_r = 2.55$

TL1, TL7, TL8 — Microstrip 0.162″ x 0.600″
TL2 — Microstrip 0.162″ x 1.060″
TL3 — Microstrip 0.162″ x 0.700″
TL4, TL5 — Microstrip 0.162″ x 0.440″
TL6 — Microstrip 0.162″ x 1.140″
TL8, TL9 — Microstrip 0.020″ x 2.130″

Figure 33. MRF571 Test Circuit Schematic

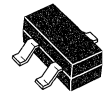
The RF Line
NPN Silicon High-Frequency Transistor

MMBR901LT1, T3
MRF9011LT1

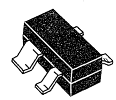
Designed primarily for use in high–gain, low–noise small–signal amplifiers for operation up to 2.5 GHz. Also usable in applications requiring fast switching times.

- High Current–Gain — Bandwidth Product
- Low Noise Figure @ f = 1.0 GHz —
  $NF_{(matched)}$ = 1.8 dB (Typ) (MRF9011LT1)
  = 1.9 dB (Typ) (MMBR901LT1, T3)
- High Power Gain —
  $G_{pe(matched)}$ = 13.5 dB (Typ) @ f = 1.0 GHz (MRF9011LT1)
  = 12.0 dB (Typ) @ f = 1.0 GHz (MMBR901LT1, T3)
- Guaranteed RF Parameters (MRF9011LT1)
- Surface Mounted SOT–23 & SOT–143 Offer Improved RF Performance
  Lower Package Parasitics
  High Gain
- Available in tape and reel packaging options:
  T1 suffix = 3,000 units per reel
  T3 suffix = 10,000 units per reel

I_C = 30 mA
SURFACE MOUNTED
HIGH–FREQUENCY
TRANSISTOR
NPN SILICON



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE, MMBR901LT1, T3



CASE 318A–05, STYLE 1
SOT–143
LOW PROFILE, MRF9011LT1

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage		V_{CEO}	15	Vdc
Collector–Base Voltage		V_{CBO}	25	Vdc
Emitter–Base Voltage		V_{EBO}	2.0	Vdc
Collector Current — Continuous		I_C	30	mAdc
Power Dissipation @ T_C = 75°C (1)	MMBR901LT1, T3; MRF9011LT1	$P_{D(max)}$	0.300	Watt
Derate above 25°C			4.00	mW/°C
Storage Temperature Range	All	T_{stg}	–55 to +150	°C
Maximum Junction Temperature		$T_{J(max)}$	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Storage Temperature	T_{stg}	150	°C
Thermal Resistance, Junction to Case MRF9011LT1, MMBR901LT1, T3	$R_{\theta JC}$	200	°C/W

DEVICE MARKING

MRF9011LT1 = 01	MMBR901LT1, T3 = 7A

NOTE:
1. Case temperature measured on collector lead immediately adjacent to body of package.

REV 8

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	15	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)		$V_{(BR)CBO}$	25	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)		$V_{(BR)EBO}$	2.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)		I_{CBO}	—	—	50	nAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 5.0 Vdc)	MMBR901LT1, T3 MRF9011LT1	h_{FE}	50 30	— 80	200 200	—
DYNAMIC CHARACTERISTICS						
Current–Gain — Bandwidth Product (I_C = 15 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	MRF9011LT1	f_T	—	3.8	—	GHz
Collector–Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	MRF9011LT1	C_{cb}	—	0.55	1.0	pF
FUNCTIONAL TESTS						
Power Gain at Minimum Noise Figure (V_{CE} = 10 Vdc, I_C = 5.0 mA, f = 1.0 GHz)	MRF9011LT1	G_{NFmin}	—	13.5	—	dB
Minimum Noise Figure (Figure 3) (V_{CE} = 10 Vdc, I_C = 5.0 mA, f = 1.0 GHz)	MRF9011LT1	NF_{min}	—	1.8	—	dB
Insertion Gain in 50 Ω System (V_{CE} = 10 Vdc, I_C = 5.0 mA, f = 1.0 GHz)	MRF9011LT1	$\|S_{21}\|^2$	9.0	10.2	—	dB
Minimum Noise Figure (Figure 3) (V_{CE} = 6.0 Vdc, I_C = 5.0 mA, f = 1.0 GHz) (V_{CE} = 10 Vdc, I_C = 5.0 mA, f = 1.0 GHz)	MMBR901LT1, T3	NF_{min}	—	1.9	—	dB
SMALL–SIGNAL CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_C = 5.0 mAdc, f = 1.0 GHz)	MMBR901LT1	C_{obo}	—	—	1.0	pF
Common–Emitter Amplifier Gain (V_{CC} = 6.0 Vdc, I_C = 5.0 mAdc, f = 1.0 GHz)	MMBR901LT1	G_{pe}	—	12	—	dB

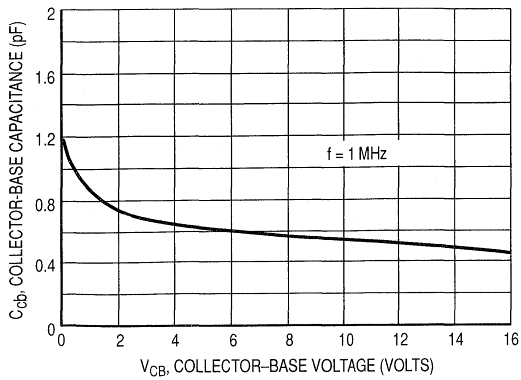


Figure 1. Collector–Base Capacitance versus Collector–Base Voltage

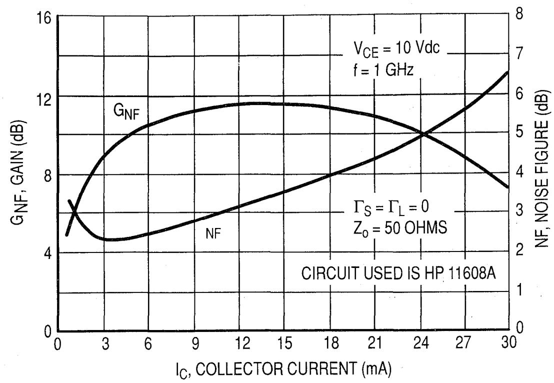
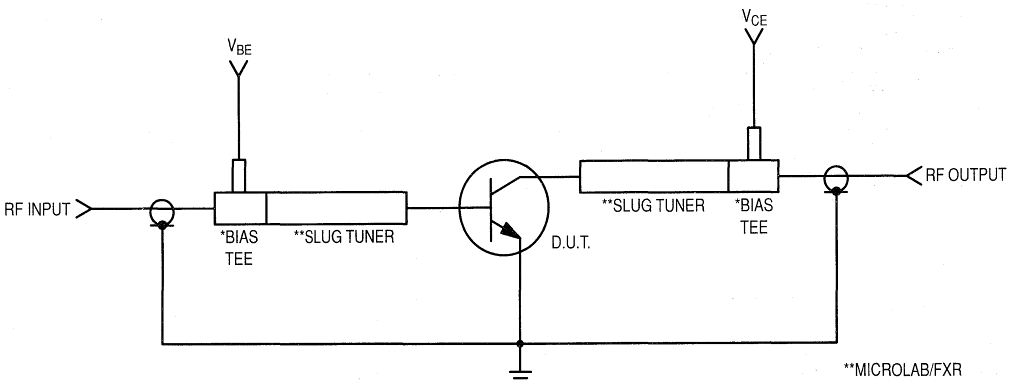


Figure 2. Gain and Noise Figure versus Collector Current



**MICROLAB/FXR
SF–11N FOR f < 1 GHz
SF–31N FOR f > 1 GHz

Figure 3. MRF9011LT1 Functional Circuit Schematic

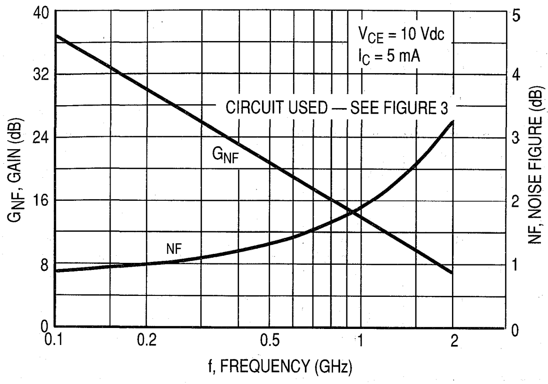


Figure 4. Gain and Noise Figure versus Frequency

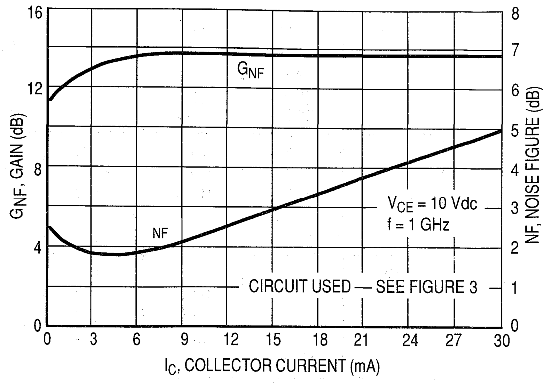


Figure 5. Gain and Noise Figure versus Collector Current

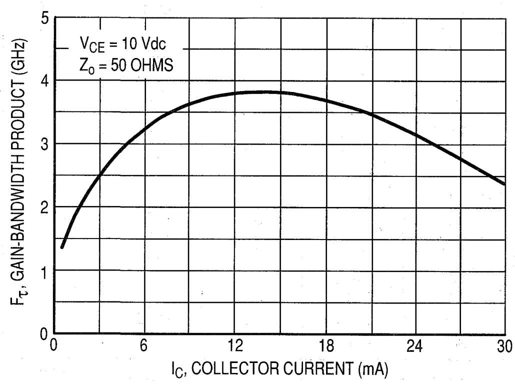


Figure 6. Gain–Bandwidth Product versus Collector Current

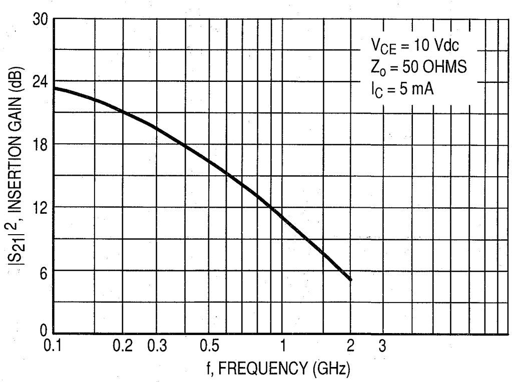


Figure 7. Insertion Gain versus Frequency

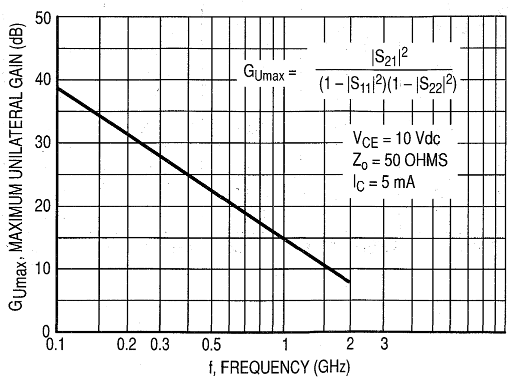


Figure 8. Maximum Unilateral Gain versus Frequency

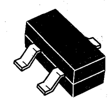
V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
5.0	5.0	100	0.85	−41	13.64	153	0.03	65	0.93	−17
		200	0.78	−76	10.77	134	0.05	54	0.80	−29
		500	0.71	−131	6.10	102	0.08	35	0.55	−42
		1000	0.66	−169	3.22	77	0.08	33	0.45	−48
		2000	0.60	152	1.65	47	0.11	46	0.47	−63
	10	100	0.72	−59	20.01	145	0.03	62	0.87	−23
		200	0.70	−100	14.31	123	0.04	49	0.67	−36
		500	0.66	−150	7.03	94	0.06	38	0.44	−43
		1000	0.63	179	3.57	73	0.07	45	0.37	−46
		2000	0.58	147	1.79	46	0.11	57	0.41	−60
	15	100	0.65	−75	23.44	138	0.02	57	0.81	−27
		200	0.66	−118	15.56	116	0.04	46	0.59	−38
		500	0.65	−159	7.10	90	0.05	42	0.40	−40
		1000	0.63	174	3.57	71	0.06	52	0.35	−43
		2000	0.59	144	1.77	45	0.11	62	0.40	−58
	20	100	0.61	−89	24.32	133	0.02	51	0.77	−28
		200	0.66	−130	15.11	111	0.03	43	0.55	−35
		500	0.66	−166	6.68	88	0.04	46	0.41	−34
		1000	0.65	171	3.32	69	0.06	56	0.39	−39
		2000	0.61	143	1.65	43	0.10	65	0.44	−56
	30	100	0.63	−132	13.18	118	0.02	47	0.72	−15
		200	0.68	−157	7.07	104	0.02	44	0.66	−16
		500	0.69	−177	3.23	90	0.03	55	0.62	−24
		1000	0.70	165	1.78	71	0.05	65	0.59	−38
		2000	0.66	138	0.93	42	0.09	79	0.62	−62
10	5.0	100	0.85	−38	13.67	155	0.03	70	0.93	−14
		200	0.80	−71	10.97	136	0.05	56	0.83	−24
		500	0.70	−126	6.35	104	0.07	37	0.60	−35
		1000	0.65	−166	3.39	78	0.07	36	0.51	−40
		2000	0.58	154	1.74	48	0.10	50	0.54	−55
	10	100	0.75	−55	20.12	147	0.02	66	0.88	−19
		200	0.71	−94	14.60	125	0.04	50	0.72	−30
		500	0.65	−145	7.33	96	0.05	39	0.50	−35
		1000	0.62	−177	3.74	74	0.06	46	0.45	−38
		2000	0.57	149	1.88	47	0.10	60	0.49	−53
	15	100	0.68	−68	23.53	140	0.02	61	0.85	−22
		200	0.67	−110	15.90	119	0.03	49	0.65	−31
		500	0.64	−155	7.45	92	0.04	42	0.47	−32
		1000	0.62	177	3.74	71	0.06	53	0.44	−35
		2000	0.58	146	1.90	45	0.09	65	0.50	−51
	20	100	0.64	−79	24.77	135	0.02	56	0.81	−23
		200	0.64	−122	15.81	114	0.03	46	0.62	−29
		500	0.64	−161	7.10	89	0.04	46	0.48	−28
		1000	0.62	174	3.53	79	0.05	56	0.46	−33
		2000	0.59	145	1.75	44	0.09	68	0.53	−50
	30	100	0.61	−114	16.25	123	0.01	48	0.79	−15
		200	0.63	−147	9.10	107	0.02	49	0.71	−15
		500	0.65	−172	4.22	90	0.03	53	0.66	−22
		1000	0.66	168	2.27	71	0.05	63	0.63	−33
		2000	0.63	140	1.15	41	0.08	79	0.67	−53

Table 1. MRF9011LT1 Common Emitter S–Parameters

The RF Line
NPN Silicon High-Frequency Transistor

MMBR911LT1

I_C = 60 mA
LOW NOISE
HIGH–FREQUENCY
TRANSISTOR
NPN SILICON



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE

Designed for low noise, wide dynamic range front–end amplifiers and low–noise VCO's. Available in a surface–mountable plastic package. This Motorola small–signal plastic transistor offers superior quality and performance at low cost.

- High Gain–Bandwidth Product
  f_T = 7.0 GHz (Typ) @ 30 mA
- Low Noise Figure
  NF = 1.7 dB (Typ) @ 500 MHz
- High Gain
  G_{NF} = 17 dB (Typ) @ 10 mA/500 MHz
- State–of–the–Art Technology
  Fine Line Geometry
  Ion–Implanted Arsenic Emitters
  Gold Top Metallization and Wires
  Silicon Nitride Passivation
- Available in tape and reel packaging options:
  T1 suffix = 3,000 units per reel

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	12	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Emitter–Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Continuous	I_C	60	mA
Power Dissipation @ T_{case} = 75°C (1) Derate linearly above T_{case} = 75°C	$P_{D(max)}$	333 4.44	mW mW/°C
Storage Temperature	T_{stg}	–55 to +150	°C
Maximum Junction Temperature	T_{Jmax}	150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	225	°C/W

DEVICE MARKING

MMBR911LT1 = 7P

NOTE:
1. Case temperature measured on collector lead immediately adjacent to body of package.

REV 8

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0)	$V_{(BR)CEO}$	12	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	20	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)	$V_{(BR)EBO}$	2.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 30 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	—	200	—
DYNAMIC CHARACTERISTICS					
Collector–Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	—	1.0	pF
Current Gain–Bandwidth Product (V_{CE} = 10 Vdc, I_C = 30 mAdc, f = 1.0 GHz)	f_T	—	6.0	—	GHz
FUNCTIONAL TESTS					
Gain @ Noise Figure (I_C = 10 mAdc, V_{CE} = 10 Vdc) f = 0.5 GHz	G_{NF}	—	17	—	dB
f = 1.0 GHz		—	11	—	
Noise Figure (I_C = 10 mAdc, V_{CE} = 10 Vdc) f = 0.5 GHz	NF	—	2.0	—	dB
f = 1.0 GHz		—	2.9	—	

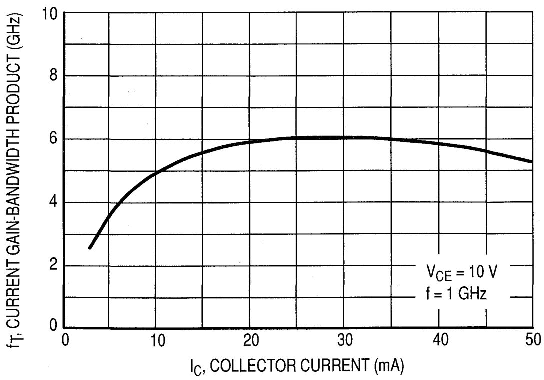


Figure 1. Current Gain–Bandwidth versus Collector Current @ 1.0 GHz

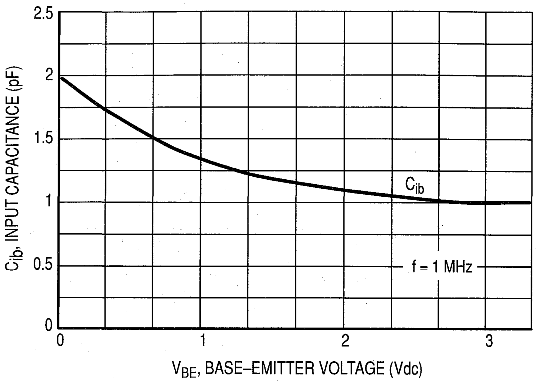


Figure 2. Input Capacitance versus Base–Emitter Voltage

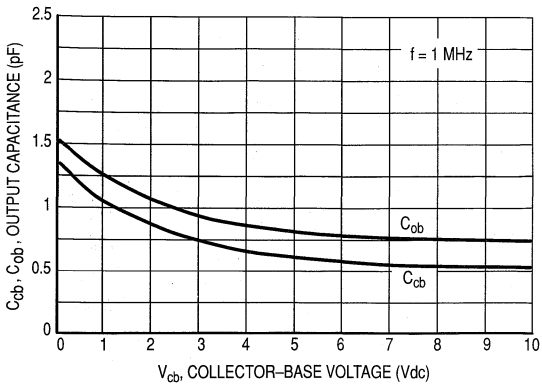


Figure 3. Output Capacitances versus Collector–Base Voltage

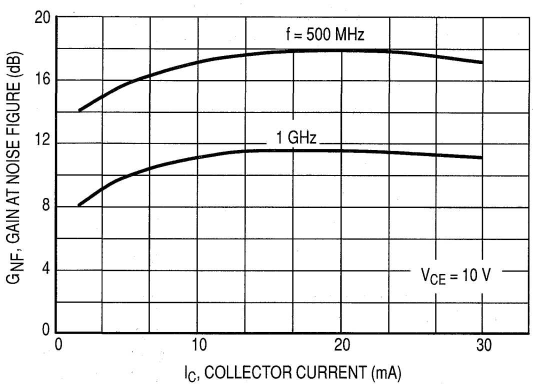


Figure 4. Gain at Noise Figure versus Collector Current

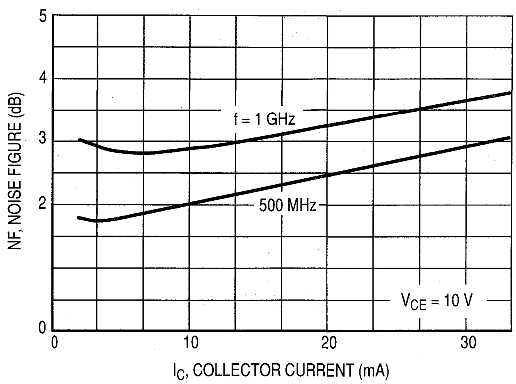


Figure 5. Noise Figure versus Collector Current

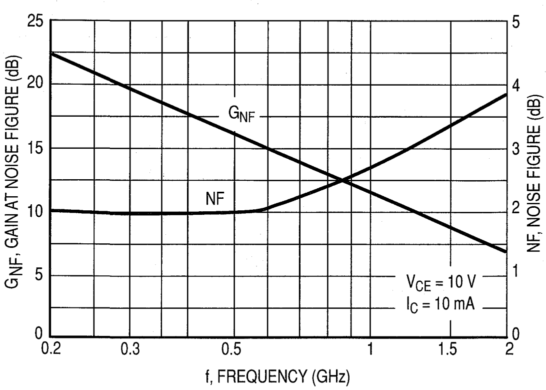


Figure 6. Gain at Noise Figure and Noise Figure versus Frequency

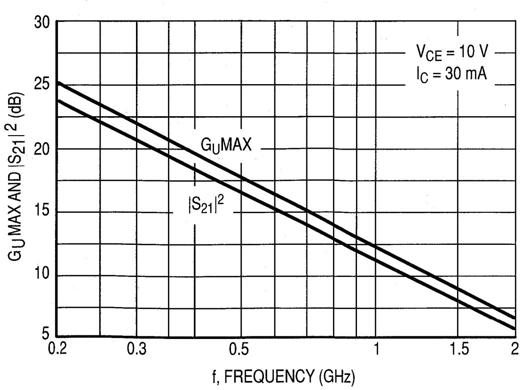


Figure 7. Maximum Unilateral Gain and Insertion Gain versus Frequency

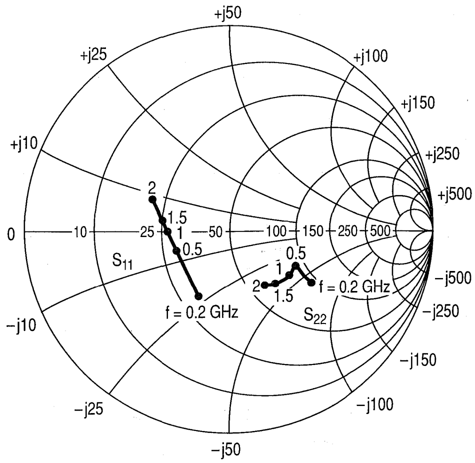


Figure 8. Input and Output Reflection Coefficients versus Frequency
V_{CE} = 10 V, I_C = 30 mA

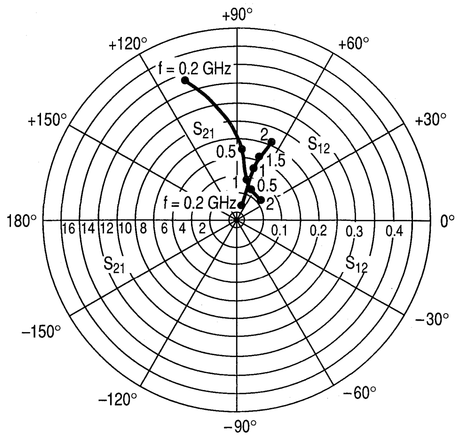


Figure 9. Forward and Reverse Transmission Coefficients versus Frequency
V_{CE} = 10 V, I_C = 30 mA

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
10	2.0	200	0.82	−45	4.14	145	0.06	66	0.88	−16
		500	0.60	−96	3.23	112	0.09	49	0.71	−27
		1000	0.47	−149	2.16	85	0.11	49	0.62	−34
		1500	0.46	−179	1.59	71	0.13	55	0.58	−43
		2000	0.47	162	1.35	57	0.16	62	0.56	−51
	5.0	200	0.66	−63	8.63	134	0.05	64	0.75	−25
		500	0.43	−117	5.29	100	0.07	58	0.55	−31
		1000	0.37	−163	3.05	82	0.11	63	0.48	−36
		1500	0.38	176	2.17	70	0.15	65	0.45	−44
		2000	0.40	160	1.81	57	0.19	65	0.43	−51
	10	200	0.49	−83	12.70	124	0.04	65	0.62	−30
		500	0.33	−134	6.42	94	0.07	66	0.44	−32
		1000	0.32	−171	3.53	80	0.12	70	0.41	−36
		1500	0.35	173	2.46	69	0.16	69	0.38	−45
		2000	0.37	159	2.04	58	0.20	66	0.35	−52
	20	200	0.36	−103	15.25	114	0.03	69	0.52	−32
		500	0.28	−149	6.95	90	0.06	72	0.39	−30
		1000	0.29	−176	3.73	78	0.12	73	0.37	−35
		1500	0.33	172	2.60	68	0.17	71	0.34	−43
		2000	0.36	158	2.14	58	0.21	67	0.32	−52
	30	200	0.32	−114	15.64	109	0.03	71	0.48	−29
		500	0.27	−156	6.92	88	0.06	73	0.38	−27
		1000	0.29	−178	3.71	78	0.12	74	0.37	−33
		1500	0.34	170	2.58	68	0.16	72	0.34	−44
		2000	0.37	156	2.13	57	0.21	68	0.32	−51

Table 1. Common Emitter S–Parameters

The RF Line

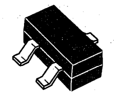
NPN Silicon Low Noise, High-Frequency Transistors

Designed for use in high gain, low noise small–signal amplifiers. This series features excellent broadband linearity and is offered in a variety of packages.

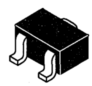
- Fully Implanted Base and Emitter Structure
- 9 Finger, 1.25 Micron Geometry with Gold Top Metal
- Gold Sintered Back Metal
- Available in tape and reel packaging options:
  T1 suffix = 3,000 units per reel
  T3 suffix = 10,000 units per reel

MMBR941
MRF947
MRF9411
SERIES

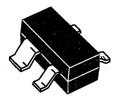
I_C = 50 mA
LOW NOISE
HIGH–FREQUENCY
TRANSISTORS



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE
MMBR941LT1, T3, MMBR941BLT1



CASE 419–02, STYLE 3
MRF947AT1, MRF947BT1,
MRF947T1, T3



CASE 318A–05, STYLE 1
SOT–143
LOW PROFILE
MRF9411LT1

MAXIMUM RATINGS

Rating	Symbol	MMBR941LT1, T3	MRF9411LT1	MRF947 Series	Unit
Collector–Emitter Voltage	V_{CEO}	10	10	10	Vdc
Collector–Base Voltage	V_{CBO}	20	20	20	Vdc
Emitter–Base Voltage	V_{EBO}	1.5	1.5	1.5	Vdc
Power Dissipation (1) $T_C = 75°C$ Derate linearly above $T_{case} = 75°C$ @	P_{Dmax}	0.25 3.33	0.25 3.33	0.188 2.5	Watts mW/°C
Collector Current — Continuous (2)	I_C	50	50	50	mA
Maximum Junction Temperature	T_{Jmax}	150	150	150	°C
Storage Temperature	T_{stg}	–55 to +150	–55 to +150	–55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	300	300	400	°C/W

DEVICE MARKING

MMBR941LT1 = 7Y	MMBR941BLT1 = 7N	MRF947T1, T3 = A	MRF947BT1 = H
MRF9411LT1 = 10	MRF947AT1 = G		

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (3)						
Collector–Emitter Breakdown Voltage ($I_C = 0.1$ mA, $I_B = 0$)	All	$V_{(BR)CEO}$	10	12	—	Vdc
Collector–Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	All	$V_{(BR)CBO}$	20	23	—	Vdc
Emitter Cutoff Current ($V_{EB} = 1.0$ V, $I_C = 0$)	All	I_{EBO}	—	—	0.1	μAdc
Collector Cutoff Current ($V_{CB} = 10$ V, $I_E = 0$)	All	I_{CBO}	—	—	0.1	μAdc
ON CHARACTERISTICS (3)						
DC Current Gain ($V_{CE} = 6.0$ V, $I_C = 5.0$ mA)	(MMBR941LT1, MRF9411LT1) (MMBR941BLT1)	h_{FE}	50 100	— —	200 200	—
DC Current Gain ($V_{CE} = 1.0$ V, $I_C = 500$ μA)	MRF947T1, MRF947BT1	h_{FE1}	50	—	—	—
DC Current Gain ($V_{CE} = 6.0$ V, $I_C = 5.0$ mA)	MRF947T1, T3 MRF947AT1 MRF947BT1	h_{FE2} h_{FE3} h_{FE4}	50 75 100	— — —	— 150 200	—
DYNAMIC CHARACTERISTICS						
Collector–Base Capacitance ($V_{CB} = 10$ V, $I_E = 0$, f = 1.0 MHz)	All	C_{cb}	—	0.35	—	pF
Current Gain — Bandwidth Product ($V_{CE} = 6.0$ V, $I_C = 15$ mA, f = 1.0 GHz)	All	f_T	—	8.0	—	GHz

NOTE:
1. To calculate the junction temperature use $T_J = P_D \times R_{\theta JC} + T_{CASE}$. Case temperature measured on collector lead immediately adjacent to body of package.
2. I_C — Continuous (MTBF ≈ 10 years).
3. Pulse width ≤ 300 μs, duty cycle ≤ 2% pulsed.

PERFORMANCE CHARACTERISTICS

Conditions	Symbol	MRF9411LT1			MMBR941LT1, T3			MRF947 Series			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Insertion Gain	$\lvert S_{21}\rvert^2$										dB
(V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)		—	16	—	—	14	—	—	14	—	
(V_{CE} = 6.0 V, I_C = 15 mA, f = 2.0 GHz)		—	10	—	—	8.0	—	—	10.8	—	
Maximum Unilateral Gain (1)	$G_{U\,max}$										dB
(V_{CE} = 6.0 V, I_C = 15 mA, f = 1.0 GHz)		—	18	—	—	16	—	—	14.8	—	
(V_{CE} = 6.0 V, I_C = 15 mA, f = 2.0 GHz)		—	12	—	—	10	—	—	11.6	—	
Noise Figure — Minimum (Figure 9)	NF_{MIN}										dB
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		—	1.5	—	—	1.5	—	—	1.5	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 2.0 GHz)		—	2.1	—	—	2.1	—	—	2.1	—	
Associated Gain at Minimum NF (Figure 9)	G_{NF}										dB
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		—	15	—	—	14	—	—	14	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 2.0 GHz)		—	9.5	—	—	8.5	—	—	10	—	
Noise Figure — 50 ohm Source (V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)	$NF_{50\,\Omega}$	—	1.9	2.8	—	1.9	2.8	—	1.9	2.8	dB

NOTE:
1. Maximum Unilateral Gain is $GU_{max} = \dfrac{\lvert S_{21}\rvert^2}{(1-\lvert S_{11}\rvert^2)(1-\lvert S_{22}\rvert^2)}$

TYPICAL CHARACTERISTICS
MMBR941LT1, T3; MMBR941BLT1; MRF9411LT1; MRF9411BLT1

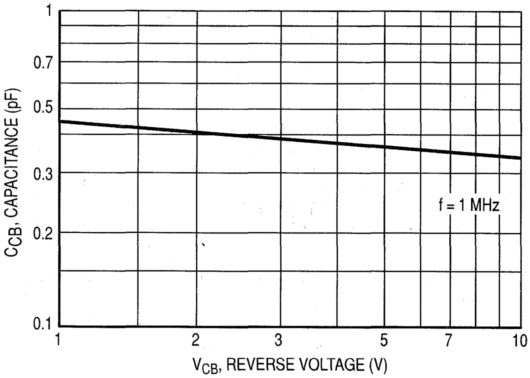


Figure 1. Collector–Base Capacitance versus Voltage

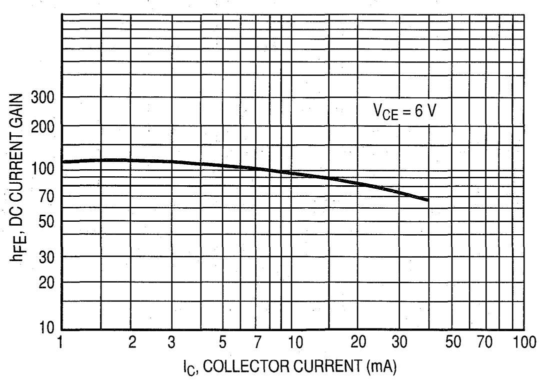


Figure 2. DC Current Gain versus Collector Current

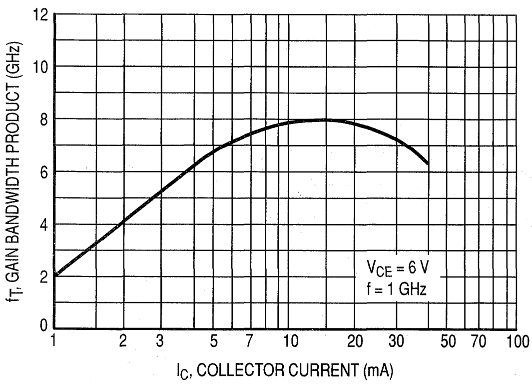


Figure 3. Gain Bandwidth Product versus Collector Current

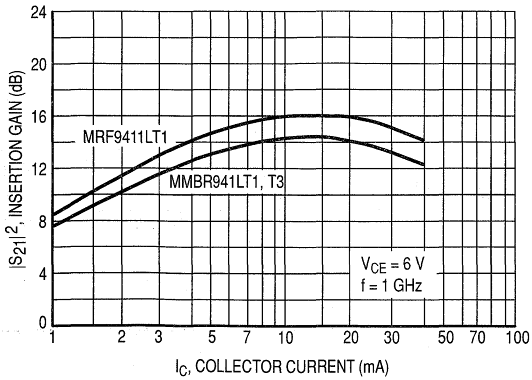


Figure 4. Insertion Gain versus Collector Current

FORWARD INSERTION GAIN AND MAXIMUM UNILATERAL GAIN versus FREQUENCY

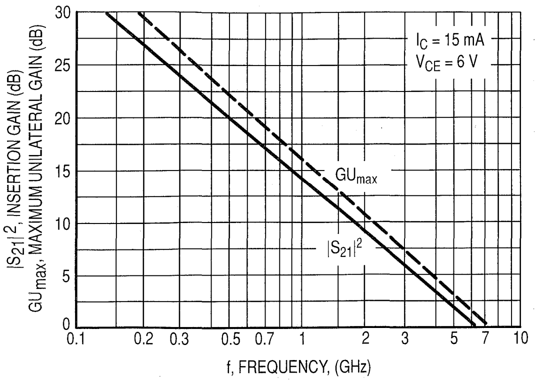


Figure 5. MMBR941LT1, T3

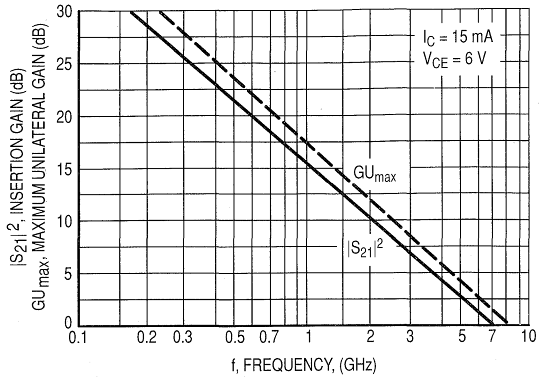


Figure 6. MRF9411LT1

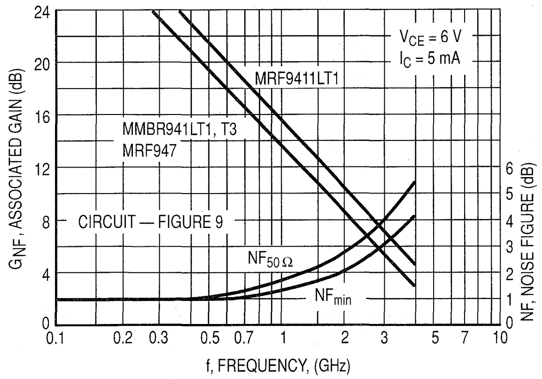


Figure 7. Noise Figure and Associated Gain versus Frequency

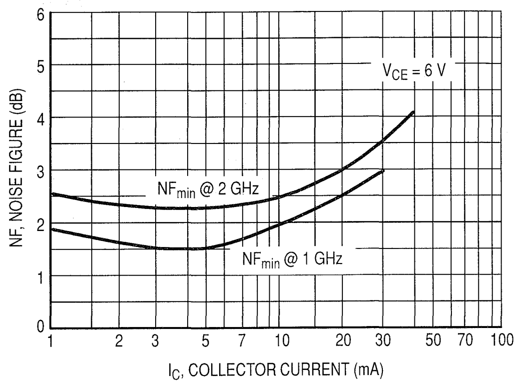


Figure 8. Minimum Noise Figure versus Collector Current

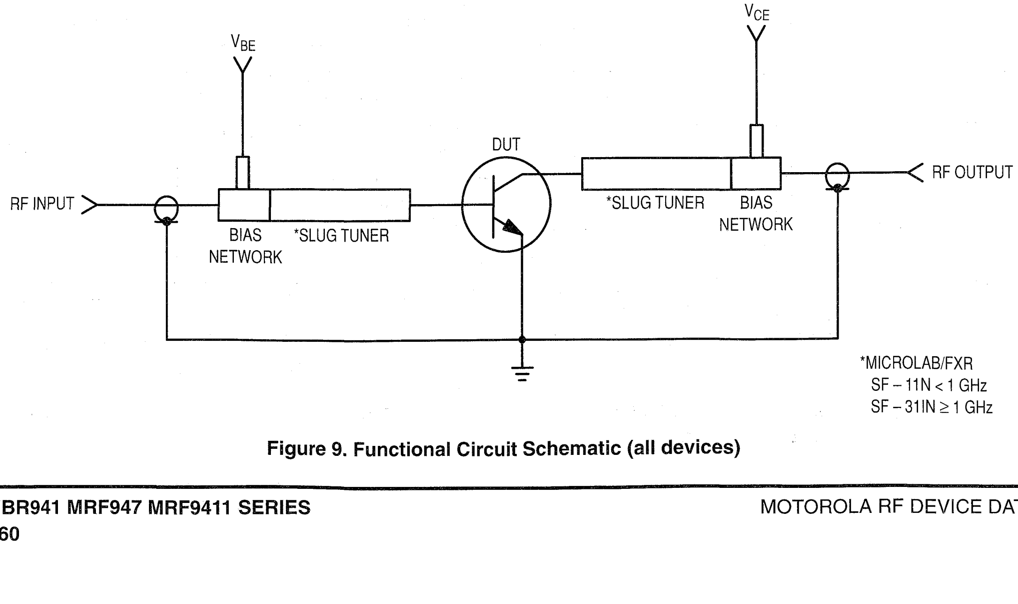


Figure 9. Functional Circuit Schematic (all devices)

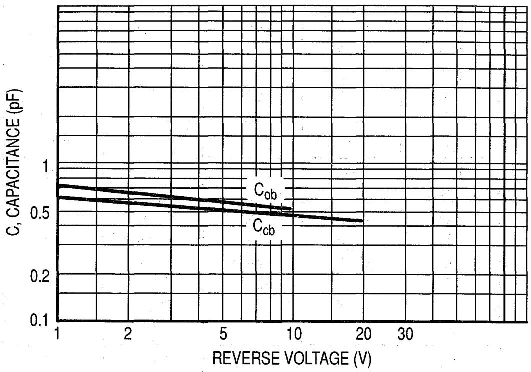


Figure 10. Capacitance versus Voltage

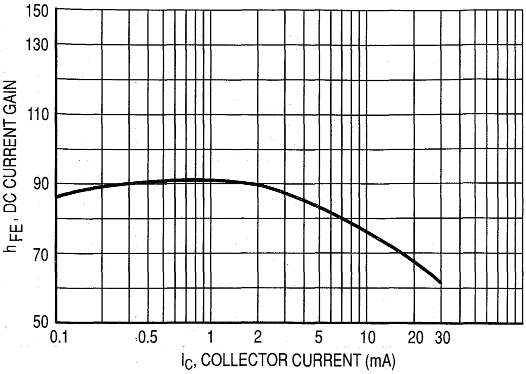


Figure 11. DC Current Gain versus Collector Current

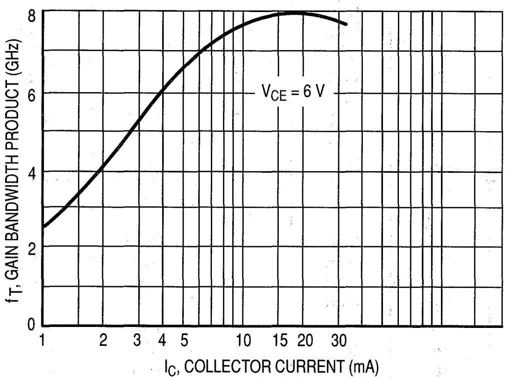


Figure 12. Gain–Bandwidth Product versus Collector Current

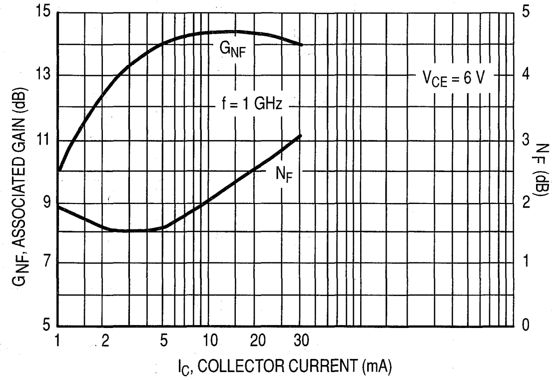


Figure 13. Associated Gain and Minimum Noise Figure versus Collector Current

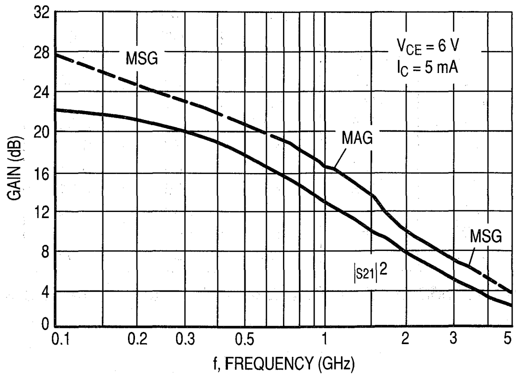


Figure 14. Forward Insertion Gain and Maximum Stable/Available Power Gain versus Frequency

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	∠ φ	Mag	∠ φ	Mag	∠ φ	Mag	∠ φ
1.0	0.5	100	0.97	−11	1.78	170	0.03	83	0.99	−4.7
		200	0.96	−22	1.74	161	0.06	76	0.99	−9.1
		500	0.90	−53	1.60	133	0.13	56	0.93	−21
		900	0.75	−89	1.37	105	0.18	37	0.83	−33
		1000	0.72	−98	1.32	100	0.18	33	0.82	−36
		1500	0.63	−132	1.07	74	0.19	20	0.75	−47
		2000	0.57	−163	0.89	55	0.16	15	0.72	−57
		3000	0.55	144	0.67	30	0.15	40	0.71	−76
	1.0	100	0.95	−13	3.37	169	0.03	81	0.99	−6.2
		200	0.93	−27	3.27	158	0.06	73	0.98	−12
		500	0.81	−62	2.85	128	0.12	52	0.86	−26
		900	0.63	−101	2.21	101	0.15	37	0.73	−38
		1000	0.60	−110	2.08	96	0.15	34	0.71	−40
		1500	0.51	−144	1.59	73	0.16	27	0.64	−49
		2000	0.46	−173	1.28	56	0.16	29	0.61	−58
		3000	0.46	138	0.95	30	0.19	44	0.60	−75
6.0	5.0	100	0.82	−25	14.6	159	0.02	77	0.94	−13
		200	0.75	−47	12.6	142	0.04	68	0.85	−22
		400	0.55	−79	9.2	120	0.05	61	0.69	−31
		600	0.42	−98	6.9	106	0.07	60	0.60	−32
		800	0.33	−114	5.3	97	0.08	61	0.56	−33
		1000	0.28	−129	4.5	90	0.09	62	0.52	−33
		1500	0.25	−155	3.1	77	0.13	67	0.51	−37
		2000	0.16	176	2.4	66	0.16	68	0.51	−36
		2500	0.21	151	2.0	57	0.20	69	0.48	−40
		3000	0.18	122	1.7	50	0.23	68	0.48	−44
		3500	0.30	108	1.5	42	0.27	66	0.45	−46
		4000	0.29	91	1.4	37	0.32	64	0.42	−53
	10	100	0.67	−37	23.5	149	0.02	74	0.88	−18
		200	0.54	−64	18.1	129	0.03	68	0.73	−28
		400	0.37	−96	11.3	108	0.05	67	0.56	−31
		600	0.26	−114	8.0	98	0.06	67	0.50	−30
		800	0.21	−130	6.0	91	0.08	70	0.47	−30
		1000	0.18	−147	5.1	85	0.09	70	0.45	−30
		1500	0.18	−167	3.4	74	0.13	72	0.46	−34
		2000	0.11	159	2.6	64	0.17	71	0.46	−34
		2500	0.17	140	2.2	56	0.21	69	0.44	−38
		3000	0.15	107	1.8	59	0.25	67	0.45	−41
		3500	0.27	100	1.7	42	0.28	65	0.42	−42
		4000	0.26	85	1.5	37	0.33	61	0.39	−49
	15	100	0.56	−46	28.6	143	0.02	73	0.83	−22
		200	0.43	−75	20.2	122	0.03	67	0.65	−30
		400	0.29	−107	11.8	104	0.04	70	0.50	−30
		600	0.22	−125	8.2	95	0.06	74	0.46	−28
		800	0.18	−141	6.2	88	0.08	74	0.45	−27
		1000	0.16	−158	5.1	83	0.09	74	0.43	−28
		1500	0.17	−174	3.4	72	0.13	73	0.44	−32
		2000	0.11	150	2.6	63	0.17	72	0.45	−33
		2500	0.17	138	2.2	55	0.21	70	0.43	−37
		3000	0.15	102	1.9	49	0.25	67	0.44	−39
		3500	0.28	98	1.7	42	0.29	65	0.40	−41
		4000	0.25	82	1.5	37	0.32	61	0.38	−47

Table 1. MMBR941LT1, T3 Common Emitter S–Parameters

VCE (Volts)	IC (mA)	f (MHz)	S11		S21		S12		S22	
			Mag	∠ φ	Mag	∠ φ	Mag	∠ φ	Mag	∠ φ
6.0	20	100	0.49	−52	31.5	139	0.01	70	0.79	−23
		200	0.36	−84	21.1	118	0.02	69	0.60	−29
		400	0.25	−115	12.1	101	0.04	73	0.48	−29
		600	0.20	−134	8.3	93	0.06	74	0.45	−26
		800	0.16	−150	6.2	87	0.07	75	0.44	−26
		1000	0.15	−166	5.1	82	0.09	75	0.42	−26
		1500	0.16	−176	3.5	75	0.14	74	0.44	−31
		2000	0.12	144	2.6	63	0.17	73	0.45	−32
		2500	0.17	133	2.2	55	0.22	70	0.43	−36
		3000	0.16	101	1.9	49	0.25	68	0.44	−39
		3500	0.28	98	1.6	41	0.29	65	0.41	−40
		4000	0.26	82	1.5	36	0.33	61	0.39	−47
	30	100	0.41	−65	34.3	134	0.01	70	0.74	−25
		200	0.30	−99	21.6	113	0.02	70	0.56	−28
		400	0.23	−131	11.9	98	0.04	76	0.47	−25
		600	0.20	−147	8.1	91	0.06	76	0.45	−24
		800	0.18	−163	6.1	84	0.07	78	0.44	−23
		1000	0.17	−177	5.0	80	0.09	78	0.43	−24
		1500	0.18	174	3.4	70	0.13	76	0.45	−30
		2000	0.14	141	2.5	61	0.17	74	0.47	−31
		2500	0.20	131	2.1	54	0.21	71	0.45	−36
		3000	0.18	104	1.8	47	0.25	69	0.46	−39
		3500	0.31	100	1.6	40	0.29	65	0.42	−42
		4000	0.29	84	1.5	35	0.33	62	0.40	−48

Table 1. MMBR941LT1, T3 Common Emitter S–Parameters (continued)

VCE (Volts)	IC (mA)	f (MHz)	S11		S21		S12		S22	
			Mag	∠ φ	Mag	∠ φ	Mag	∠ φ	Mag	∠ φ
1.0	0.5	100	0.97	−10	1.78	171	0.03	83	100	−4.7
		200	0.97	−20	1.75	163	0.05	77	100	−9.2
		500	0.93	−49	1.62	137	0.12	57	0.94	−21
		900	0.81	−84	1.43	110	0.18	36	0.86	−35
		1000	0.79	−92	1.38	104	0.19	32	0.84	−38
		1500	0.72	−125	1.12	78	0.20	14	0.77	−50
		2000	0.68	−152	0.92	57	0.20	1	0.74	−61
		3000	0.66	169	0.68	27	0.16	−11	0.73	−82
	1.0	100	0.95	−13	3.37	170	0.03	82	0.99	−6.2
		200	0.94	−25	3.30	161	0.05	74	0.98	−12
		500	0.88	−59	2.96	133	0.16	53	0.89	−27
		1000	0.70	−107	2.26	101	0.16	29	0.74	−44
		1500	0.64	−139	1.72	78	0.17	15	0.66	−55
		2000	0.61	−165	1.36	59	0.17	6.7	0.62	−65
		3000	0.61	160	0.97	32	0.14	3.0	0.61	−84

Table 2. MRF9411LT1 Common Emitter S–Parameters

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	∠ φ	Mag	∠ φ	Mag	∠ φ	Mag	∠ φ
6.0	5.0	100	0.73	−24	14	164	0.02	92	0.96	−11
		200	0.74	−47	12.9	150	0.03	65	0.90	−20
		400	0.66	−83	10.4	129	0.05	56	0.75	−32
		600	0.62	−108	8.4	115	0.06	45	0.65	−40
		800	0.56	−127	6.7	105	0.07	46	0.60	−43
		1000	0.54	−141	5.6	96	0.07	51	0.57	−46
		1500	0.46	−166	3.9	82	0.08	55	0.52	−50
		2000	0.43	172	2.9	70	0.09	56	0.50	−54
		2500	0.41	151	2.3	62	0.11	61	0.48	−60
		3000	0.44	128	1.9	55	0.14	62	0.49	−65
		3500	0.49	117	1.6	47	0.15	61	0.46	−74
		4000	0.57	101	1.4	42	0.16	62	0.47	−81
		5000	0.60	92	1.2	32	0.21	60	0.46	−105
		6000	0.58	88	1.0	20	0.25	61	0.51	−137
	10	100	0.64	−39	23.6	157	0.01	59	0.91	−16
		200	0.60	−71	20	139	0.02	70	0.80	−27
		400	0.54	−112	13.9	117	0.03	57	0.61	−39
		600	0.52	−135	10.3	104	0.04	50	0.51	−43
		800	0.49	−151	8.0	96	0.05	54	0.46	−44
		1000	0.47	−161	6.5	89	0.06	60	0.46	−46
		1500	0.41	177	4.4	77	0.08	62	0.44	−47
		2000	0.40	158	3.2	67	0.09	65	0.43	−52
		2500	0.39	139	2.6	60	0.11	68	0.41	−56
		3000	0.44	118	2.1	53	0.13	69	0.43	−62
		3500	0.49	110	1.8	47	0.15	67	0.39	−72
		4000	0.54	96	1.6	42	0.18	65	0.41	−78
		5000	0.63	88	1.3	32	0.23	61	0.40	−101
		6000	0.58	86	1.1	20	0.26	62	0.44	−136
	15	100	0.56	−51	29.5	152	0.01	78	0.87	−20
		200	0.53	−88	23.5	131	0.02	63	0.73	−31
		400	0.51	−128	15.1	111	0.03	63	0.54	−40
		600	0.49	−148	11.8	99	0.04	56	0.46	−42
		800	0.48	−161	8.3	92	0.04	59	0.42	−41
		1000	0.46	−170	6.7	86	0.05	59	0.41	−44
		1500	0.41	−171	4.4	75	0.07	70	0.42	−45
		2000	0.40	152	3.3	66	0.09	71	0.41	−50
		2500	0.39	135	2.6	59	0.11	71	0.41	−55
		3000	0.45	116	2.2	53	0.14	73	0.42	−61
		3500	0.50	108	1.9	46	0.17	70	0.39	−70
		4000	0.55	94	1.6	41	0.19	67	0.41	−76
		5000	0.61	87	1.3	32	0.22	62	0.34	−114
		6000	0.58	85	1.1	21	0.27	63	0.43	−135
	30	100	0.45	−82	36.3	142	0.01	62	0.79	−23
		200	0.48	−121	25.5	121	0.01	48	0.62	−31
		400	0.49	−152	14.6	103	0.02	58	0.47	−33
		600	0.50	−166	10.2	93	0.03	60	0.44	−34
		800	0.49	−175	7.7	87	0.04	65	0.42	−34
		1000	0.48	177	6.1	81	0.05	76	0.43	−37
		1500	0.45	162	4.1	71	0.07	75	0.45	−39
		2000	0.45	145	3.0	62	0.09	78	0.44	−46
		2500	0.44	130	2.4	56	0.11	79	0.44	−53
		3000	0.50	113	1.9	50	0.13	79	0.45	−58
		3500	0.55	105	1.6	43	0.15	75	0.44	−70
		4000	0.61	92	1.5	39	0.19	73	0.45	−76
		5000	0.65	84	1.2	30	0.24	68	0.43	−100
		6000	0.61	82	1.0	19	0.28	64	0.48	−135

Table 2. MRF9411LT1 Common Emitter S–Parameters (continued)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	NF_{min} (dB)	Γ_o (MAG, ANGLE)	r_N
6	5	1000	1.5	0.33 ∠ 77	0.28
		1500	1.75	0.26 ∠ 141	0.3

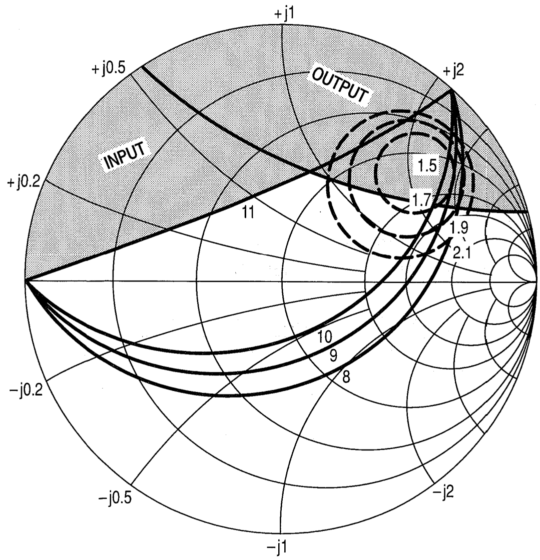
Table 3. MRF947 Series Typical Noise Parameters

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	∠φ	Mag	∠φ	Mag	∠φ	Mag	∠φ
1.0	0.5	100	0.966	−11	1.776	170	0.031	83	0.998	−5
		200	0.956	−23	1.735	161	0.061	75	0.991	−9
		500	0.892	−55	1.587	132	0.135	55	0.923	−21
		900	0.749	−91	1.355	104	0.185	35	0.827	−34
		1000	0.720	−100	1.300	98	0.190	32	0.808	−36
		1500	0.637	−134	1.057	73	0.196	18	0.743	−47
		2000	0.587	−164	0.883	53	0.176	12	0.708	−58
		3000	0.572	149	0.672	27	0.149	33	0.680	−82
	1.0	100	0.941	−14	3.391	168	0.031	81	0.991	−6
		200	0.921	−28	3.285	158	0.060	73	0.974	−12
		500	0.806	−65	2.844	128	0.123	51	0.852	−27
		900	0.638	−104	2.196	101	0.158	35	0.717	−39
		1500	0.533	−146	1.580	72	0.168	25	0.619	−50
		2000	0.495	−174	1.281	55	0.164	25	0.581	−60
		3000	0.494	144	0.956	29	0.187	39	0.554	−81
2.0	0.5	100	0.979	−9	1.827	173	0.030	85	0.996	−4
		200	0.960	−18	1.909	165	0.060	80	0.991	−9
		500	0.920	−43	1.652	144	0.132	65	0.940	−19
		1000	0.749	−77	1.451	116	0.196	47	0.842	−32
		1500	0.674	−105	1.190	94	0.214	36	0.774	−39
		2000	0.548	−128	1.077	79	0.189	33	0.692	−43
		3000	0.480	−178	0.808	60	0.153	55	0.625	−52
	2.0	100	0.907	−16	6.640	167	0.029	81	0.977	−9
		200	0.846	−32	6.419	156	0.054	73	0.944	−17
		500	0.711	−68	4.874	128	0.104	57	0.770	−32
		1000	0.495	−106	3.178	103	0.138	50	0.603	−41
		1500	0.405	−131	2.358	86	0.157	52	0.542	−45
		2000	0.314	−155	1.910	75	0.173	58	0.490	−44
		3000	0.296	158	1.394	59	0.228	68	0.454	−47
	5.0	100	0.780	−28	14.100	159	0.027	78	0.932	−15
		200	0.676	−51	12.219	142	0.046	67	0.831	−27
		500	0.470	−95	7.373	113	0.078	59	0.568	−40
		1000	0.327	−132	4.148	92	0.114	62	0.436	−43
		1500	0.271	−153	2.921	81	0.151	66	0.413	−44
		2000	0.218	−177	2.295	72	0.188	69	0.394	−41
		3000	0.237	138	1.661	58	0.265	70	0.372	−43

Table 4. MRF947 Series Common Emitter S–Parameters

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	∠φ	Mag	∠φ	Mag	∠φ	Mag	∠φ
2.0	10	100	0.608	−43	21.812	149	0.022	72	0.859	−23
		200	0.488	−73	16.618	129	0.038	65	0.689	−35
		500	0.330	−119	8.427	103	0.065	66	0.438	−41
		1000	0.262	−152	4.484	87	0.109	71	0.354	−40
		1500	0.227	−169	3.114	77	0.155	73	0.358	−42
		2000	0.197	166	2.423	69	0.198	73	0.355	−38
		3000	0.233	128	1.755	57	0.281	71	0.338	−40
	30	100	0.353	−100	25.543	131	0.018	70	0.653	−29
		200	0.353	−135	15.823	112	0.026	68	0.484	−34
		500	0.346	−163	6.979	93	0.054	76	0.367	−29
		1000	0.337	177	3.637	80	0.103	79	0.351	−30
		1500	0.324	166	2.518	71	0.150	79	0.372	−36
		2000	0.319	148	1.975	63	0.197	78	0.378	−35
		3000	0.374	122	1.441	51	0.290	75	0.363	−42
6.0	0.5	100	0.978	−9	1.791	173	0.024	86	0.995	−4
		200	0.964	−17	1.889	166	0.049	80	0.994	−7
		500	0.932	−40	1.643	146	0.110	67	0.953	−16
		1000	0.765	−73	1.473	121	0.165	50	0.869	−28
		1500	0.688	−100	1.206	98	0.184	39	0.812	−35
		2000	0.554	−123	1.099	84	0.162	38	0.735	−38
		3000	0.463	−174	0.823	64	0.136	63	0.671	−46
	2.0	100	0.918	−15	6.614	168	0.023	84	0.983	−7
		200	0.862	−29	6.456	157	0.045	75	0.956	−14
		500	0.729	−62	5.010	131	0.089	60	0.809	−27
		1000	0.504	−99	3.344	106	0.121	53	0.654	−35
		1500	0.397	−123	2.485	90	0.137	55	0.599	−38
		2000	0.295	−146	2.013	78	0.152	62	0.553	−37
		3000	0.257	162	1.452	62	0.202	73	0.523	−40
	5.0	100	0.806	−24	14.025	161	0.022	78	0.947	−13
		200	0.704	−45	12.425	144	0.040	70	0.861	−23
		500	0.487	−85	7.751	116	0.068	62	0.627	−33
		1000	0.316	−120	4.399	95	0.101	65	0.505	−35
		1500	0.245	−141	3.112	83	0.134	69	0.488	−36
		2000	0.177	−166	2.447	74	0.167	72	0.473	−33
		3000	0.185	140	1.743	61	0.237	74	0.457	−36
	10	100	0.657	−37	22.098	151	0.019	75	0.888	−18
		200	0.526	−64	17.304	132	0.033	68	0.741	−29
		500	0.328	−105	9.028	106	0.056	67	0.509	−33
		1000	0.228	−138	4.844	89	0.096	73	0.438	−31
		1500	0.184	−156	3.359	80	0.138	75	0.440	−34
		2000	0.140	175	2.591	72	0.175	76	0.441	−31
		3000	0.172	126	1.852	60	0.249	75	0.430	−33
	20	100	0.492	−53	28.934	142	0.017	72	0.808	−23
		200	0.372	−85	19.971	121	0.028	70	0.630	−31
		500	0.249	−127	9.335	100	0.053	74	0.454	−28
		1000	0.201	−156	4.878	86	0.094	78	0.418	−27
		1500	0.174	−171	3.358	77	0.138	79	0.432	−30
		2000	0.149	161	2.580	70	0.177	78	0.444	−28
		3000	0.193	121	1.852	58	0.253	76	0.435	−32

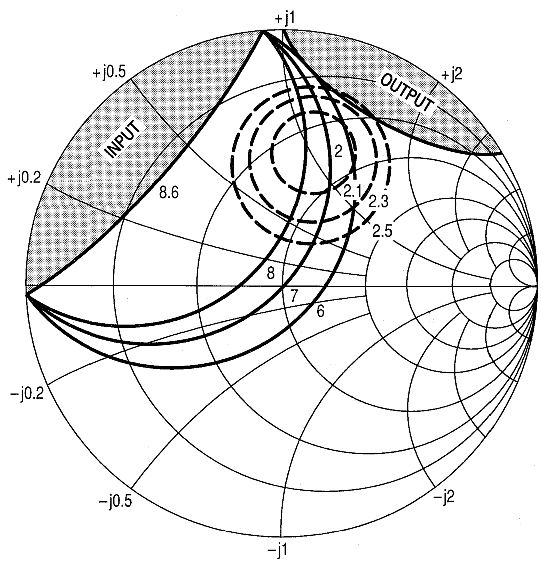
Table 4. MRF947 Series Common Emitter S–Parameters (continued)



V_{CE} = 1.0 V
I_C = 0.5 mA
▨ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
0.5	1.54	0.71 ∠ 39°	38	0.28

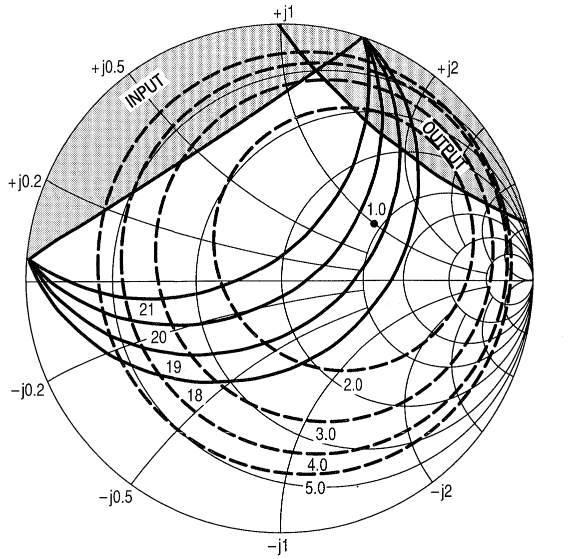
Figure 15. MMBR941LT1, T3 Constant Gain and Noise Figure Contours (f = 1.0 GHz)



V_{CE} = 1.0 V
I_C = 0.5 mA
▨ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
1.0	1.95	0.55 ∠ 76°	28	0.51

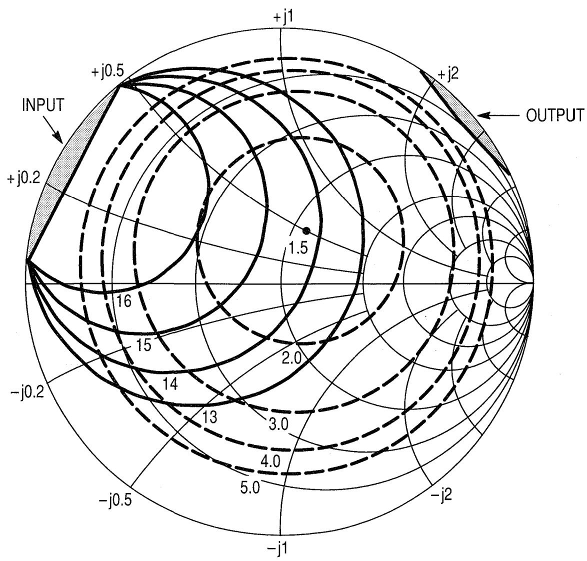
Figure 16. MMBR941LT1, T3 Constant Gain and Noise Figure Contours (f = 0.5 GHz)



V_{CE} = 6.0 V
I_C = 5.0 mA
▨ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
0.5	1.0	0.43 ∠ 30°	18	0.58

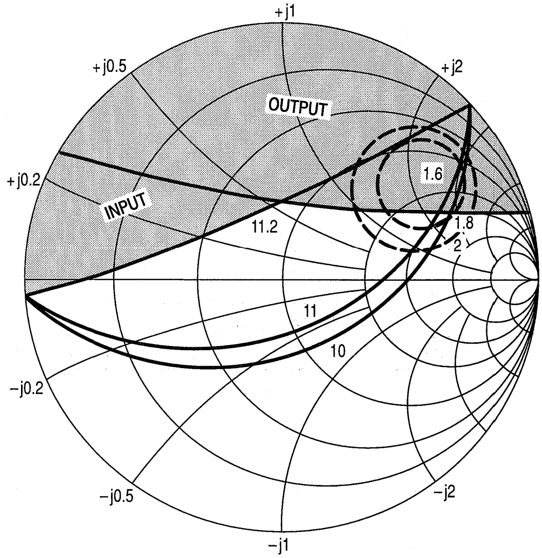
Figure 17. MMBR941LT1, T3 Constant Gain and Noise Figure Contours (f = 0.5 GHz)



V_{CE} = 6.0 V
I_C = 5.0 mA
▨ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
1.0	1.5	0.22 ∠ 64°	13	0.93

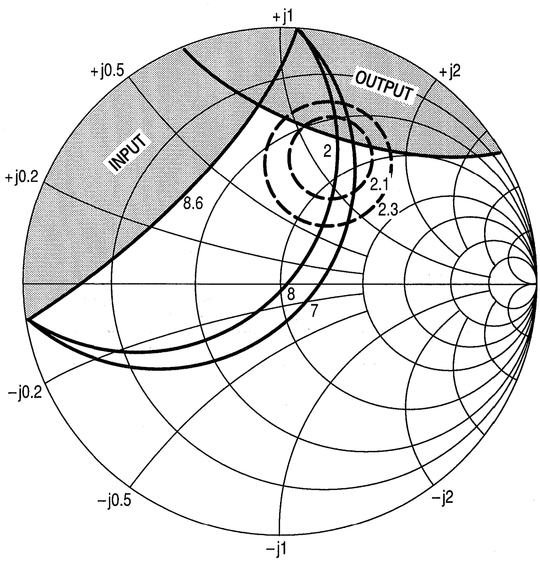
Figure 18. MMBR941LT1, T3 Constant Gain and Noise Figure Contours (f = 1.0 GHz)



V_{CE} = 1.0 V
I_C = 0.5 mA
▨ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
0.5	1.60	0.70 ∠ 35°	40	0.22

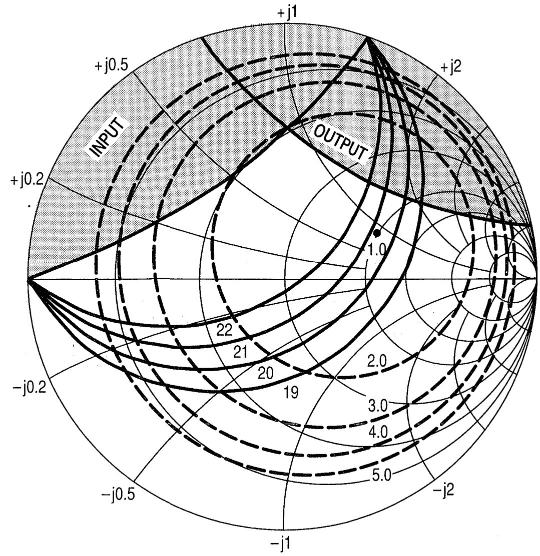
Figure 19. MRF9411LT1 Constant Gain and Noise Figure Contours (f = 0.5 GHz)



V_{CE} = 1.0 V
I_C = 0.5 mA
▨ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
1.0	1.95	0.55 ∠ 69°	30	0.39

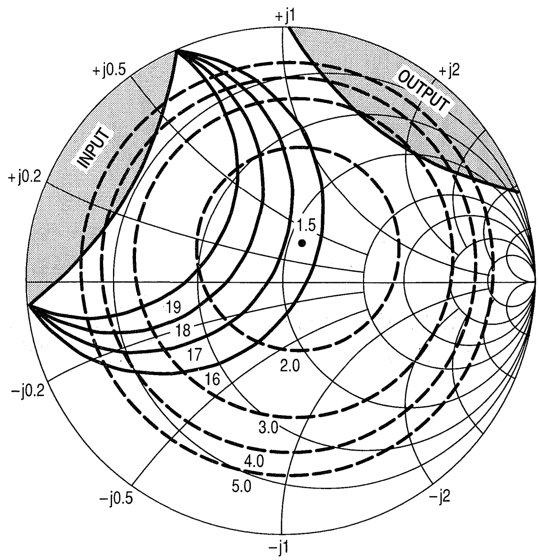
Figure 20. MRF9411LT1 Constant Gain and Noise Figure Contours (f = 1.0 GHz)



V_{CE} = 6.0 V
I_C = 5.0 mA
▒ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
0.5	1.0	0.40 ∠ 28°	17	0.29

Figure 21. MRF9411LT1 Constant Gain and Noise Figure Contours (f = 0.5 GHz)



V_{CE} = 6.0 V
I_C = 5.0 mA
▒ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
1.0	1.5	0.17 ∠ 60°	13	0.53

Figure 22. MRF9411LT1 Constant Gain and Noise Figure Contours (f = 1.0 GHz)

V_{CE} = 6 V
I_C = 5 mA

f (GHz)	NF OPT	Γ_o	R_N	K
1.0	1.5 dB	0.33 ∠ 77°	14	0.87

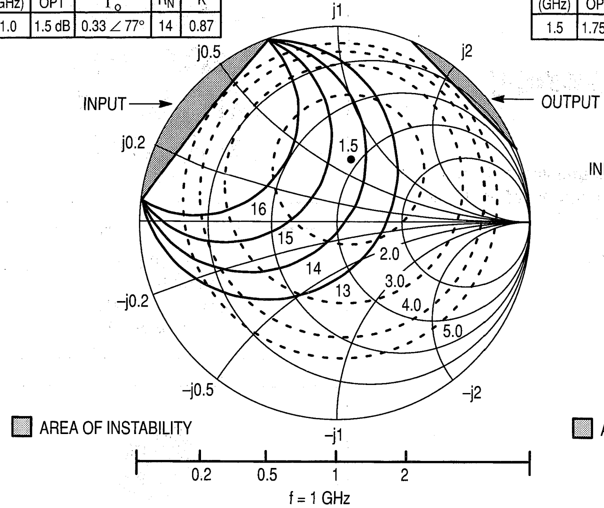


Figure 23. MRF947 Series Constant Gain and Noise Figure Contours

V_{CE} = 6 V
I_C = 5 mA

f (GHz)	NF OPT	Γ_o	R_N	K
1.5	1.75 dB	0.26 ∠ 141°	15	0.96

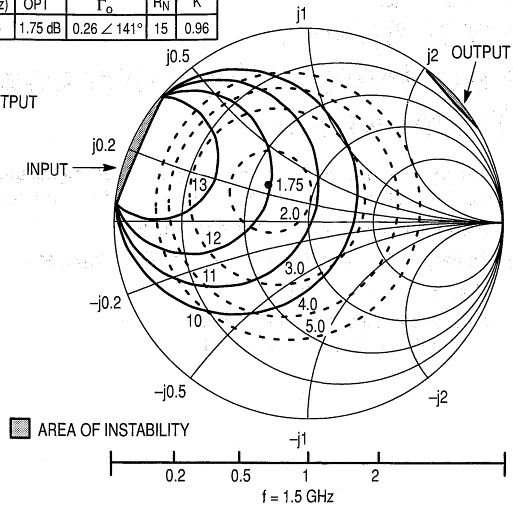


Figure 24. MRF947 Series Constant Gain and Noise Figure Contours

V_{CE} = 1 V
I_C = 0.5 mA

f (GHz)	NF OPT	ΓMS NF OPT	R_N	K
1.0	1.95 dB	0.59 ∠ 72°	30	0.50

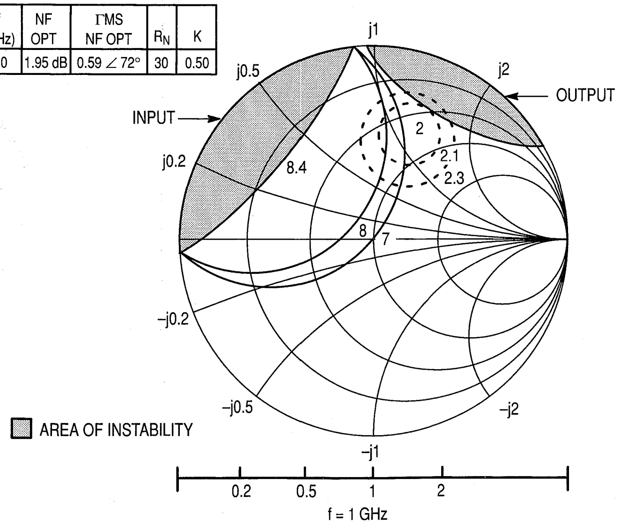


Figure 25. MRF947 Series Constant Gain and Noise Figure Contours

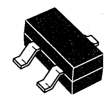
The RF Line
NPN Silicon Low Noise, High-Frequency Transistors

Designed for use in high gain, low noise small–signal amplifiers. This series features excellent broadband linearity and is offered in a variety of packages.

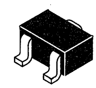
- Fully Implanted Base and Emitter Structure
- 18 Finger, 1.25 Micron Geometry with Gold Top Metal
- Gold Sintered Back Metal
- Available in tape and reel packaging options:
  T1 suffix = 3,000 units per reel

MMBR951
MRF957
MRF9511
SERIES

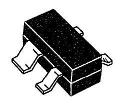
I_C = 100 mA
LOW NOISE
HIGH–FREQUENCY
TRANSISTORS



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE
MMBR951LT1, MMBR951ALT1



CASE 419–02, STYLE 3
MRF957T1



CASE 318A–05, STYLE 1
SOT–143
LOW PROFILE
MRF9511LT1

REV 8

MAXIMUM RATINGS

Rating	Symbol	MMBR951LT1 MMBR951ALT1	MRF9511LT1	MRF957T1	Unit
Collector–Emitter Voltage	V_{CEO}	10	10	10	Vdc
Collector–Base Voltage	V_{CBO}	20	20	20	Vdc
Emitter–Base Voltage	V_{EBO}	1.5	1.5	15	Vdc
Power Dissipation (1) $T_C = 75°C$ Derate linearly above $T_{case} = 75°C$ @	$P_{D(max)}$	0.322 4.29	0.322 4.29	0.227 3.03	Watts mW/°C
Collector Current — Continuous (2)	I_C	100	100	100	mA
Maximum Junction Temperature	T_{Jmax}	150	150	150	°C
Storage Temperature	T_{stg}	−55 to +150	−55 to +150	−55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	233	233	330	°C/W

DEVICE MARKING

MRF9511LT1 = 11	MMBR951ALT1 = AAG	MMBR951LT1 = 7Z	MRF957T1 = B

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (3)					
Collector–Emitter Breakdown Voltage ($I_C = 0.1$ mA, $I_B = 0$)	$V_{(BR)CEO}$	10	13	—	Vdc
Collector–Base Breakdown Voltage ($I_C = 0.1$ mA, $I_E = 0$)	$V_{(BR)CBO}$	20	25	—	Vdc
Emitter Cutoff Current ($V_{EB} = 1.0$ V, $I_C = 0$)	I_{EBO}	—	—	0.1	μAdc
Collector Cutoff Current ($V_{CB} = 10$ V, $I_E = 0$)	I_{CBO}	—	—	0.1	μAdc
ON CHARACTERISTICS (3)					
DC Current Gain ($V_{CE} = 6.0$ V, $I_C = 5.0$ mA) All ($V_{CE} = 6.0$ V, $I_C = 5.0$ mA) MMBR951ALT1	h_{FE}	 50 75	 — —	 200 150	—
DYNAMIC CHARACTERISTICS					
Collector–Base Capacitance ($V_{CB} = 10$ V, $I_E = 0$, f = 1.0 MHz)	C_{cb}	—	0.45	1.0	pF
Current Gain — Bandwidth Product ($V_{CE} = 6.0$ V, $I_C = 30$ mA, f = 1.0 GHz)	f_T	—	8.0	—	GHz

NOTES:
1. To calculate the junction temperature use $T_J = (P_D \times R_{\theta JA}) + T_{CASE}$. Case temperature measured on collector lead immediately adjacent to body of package.
2. I_C — Continuous (MTBF ≈ 10 years).
3. Pulse width ≤ 300 μs, duty cycle ≤ 2% pulsed.

PERFORMANCE CHARACTERISTICS

Conditions	Symbol	MRF9511LT1			MMBR951LT1 MMBR951ALT1			MRF957T1			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Insertion Gain	$\lvert S_{21}\rvert^2$										dB
(V_{CE} = 6.0 V, I_C = 30 mA, f = 1.0 GHz)		—	14.5	—	—	12.5	—	—	13.3	—	
(V_{CE} = 6.0 V, I_C = 30 mA, f = 2.0 GHz)		—	9.0	—	—	7.0	—	—	—	—	
(V_{CE} = 5.0 V, I_C = 30 mA, f = 1.5 GHz)		—	—	—	—	—	—	—	10.1	—	
Maximum Unilateral Gain (1)	$G_{U\,max}$										dB
(V_{CE} = 8.0 V, I_C = 30 mA, f = 1.0 GHz)		—	17	—	—	14	—	—	14	—	
(V_{CE} = 8.0 V, I_C = 30 mA, f = 2.0 GHz)		—	10.5	—	—	8.0	—	—	—	—	
(V_{CE} = 5.0 V, I_C = 30 mA, f = 1.5 GHz)		—	—	—	—	—	—	—	10.8	—	
Noise Figure — Minimum (Figure 9)	NF_{MIN}										dB
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		—	1.3	—	—	1.3	—	—	1.5	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 2.0 GHz)		—	2.1	—	—	2.1	—	—	—	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.5 GHz)		—	—	—	—	—	—	—	2.0	—	
Associated Gain at Minimum NF (Figure 9)	G_{NF}										dB
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)		—	14	—	—	13	—	—	11.8	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 2.0 GHz)		—	9.0	—	—	7.5	—	—	—	—	
(V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.5 GHz)		—	—	—	—	—	—	—	9.0	—	
Noise Figure — 50 ohm Source (V_{CE} = 6.0 V, I_C = 5.0 mA, f = 1.0 GHz)	$NF_{50\,\Omega}$	—	1.9	2.8	—	1.9	2.8	—	1.9	2.8	dB

NOTE:
1. Maximum Unilateral Gain is $GU_{max} = \dfrac{\lvert S_{21}\rvert^2}{(1-\lvert S_{11}\rvert^2)(1-\lvert S_{22}\rvert^2)}$

TYPICAL CHARACTERISTICS
MMBR951LT1, MMBR951ALT1, MRF9511LT1

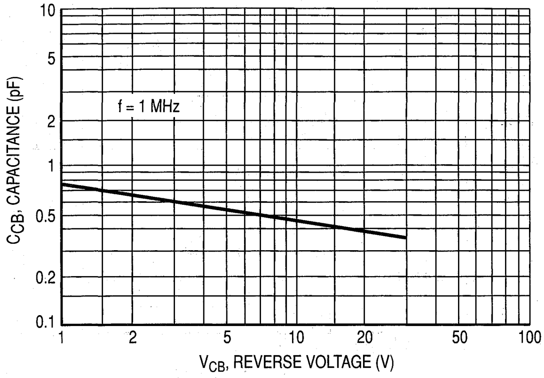


Figure 1. Collector–Base Capacitance versus Voltage

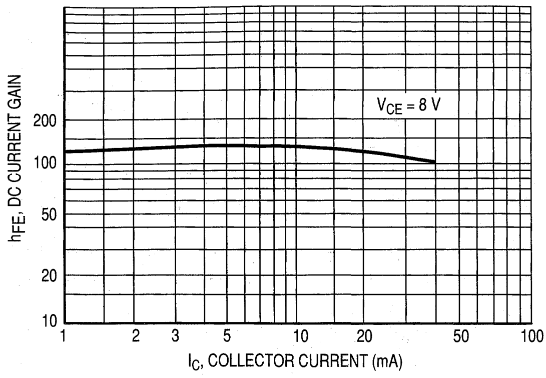


Figure 2. DC Current Gain versus Collector Current

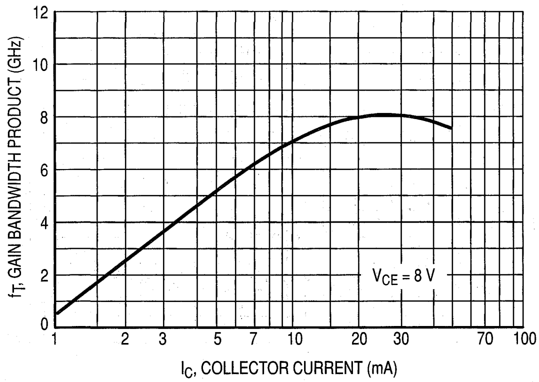


Figure 3. Gain Bandwidth Product versus Collector Current

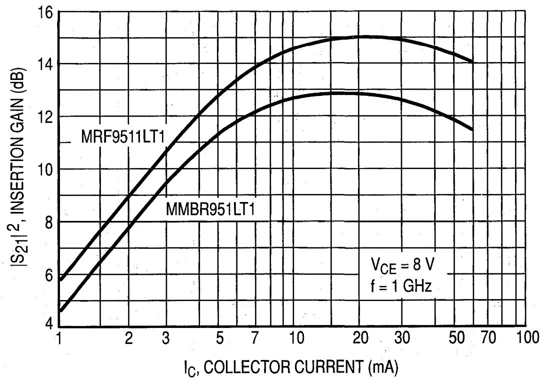


Figure 4. Insertion Gain versus Collector Current

TYPICAL FORWARD INSERTION GAIN AND MAXIMUM UNILATERAL GAIN versus FREQUENCY

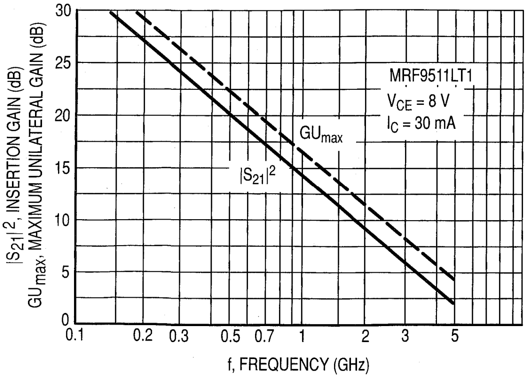


Figure 5. MRF9511LT1

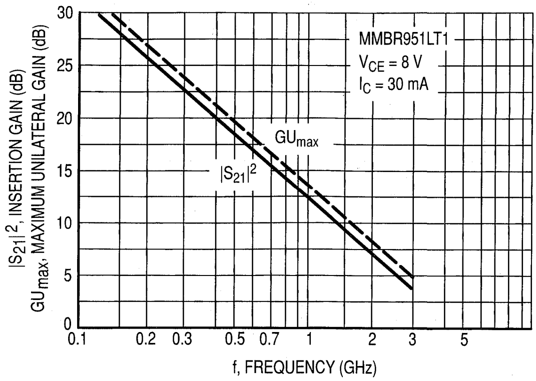


Figure 6. MMBR951LT1

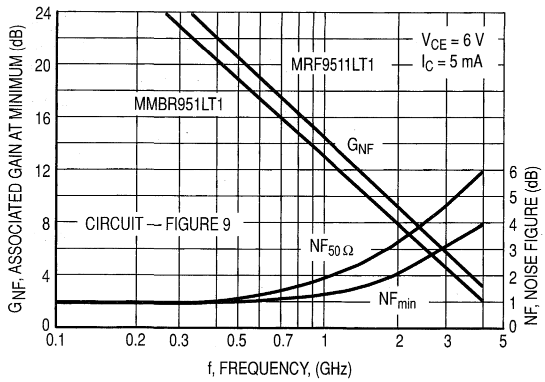


Figure 7. Typical Noise Figure and Associated Gain versus Frequency

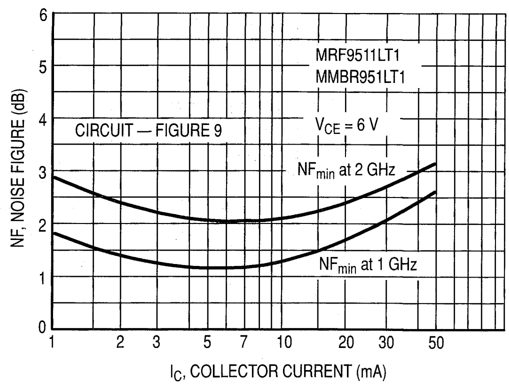


Figure 8. Typical Noise Figure versus Collector Current

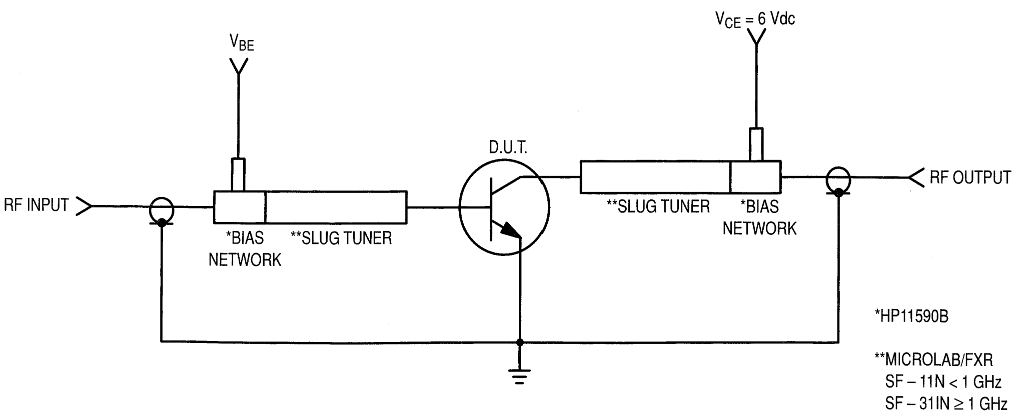


Figure 9. Functional Circuit Schematic (All Devices)

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
6.0	5.0	100	0.82	−36.6	14.0	153	0.04	44.7	0.88	−18.2
		500	0.50	−119	6.6	104	0.07	48.2	0.52	−40
		1000	0.39	−162	3.5	81	0.11	55	0.43	−43
		2000	0.32	150	1.9	57	0.21	66	0.42	−50
		3000	0.36	110	1.4	40	0.31	66	0.40	−67
	10	100	0.66	−54	22.6	142	0.03	60	0.78	−29
		500	0.38	−138	7.8	96	0.07	55	0.40	−42
		1000	0.32	−176	4.0	78	0.13	71	0.34	−47
		2000	0.26	142	2.2	57	0.22	70	0.36	−46
		3000	0.31	105	1.6	41	0.32	64	0.33	−62
	20	100	0.49	−76	30	131	0.01	85	0.67	−37
		500	0.32	−153	8.3	92	0.08	76	0.34	−39
		1000	0.29	175	4.3	77	0.11	67	0.29	−44
		2000	0.24	137	2.3	57	0.24	71	0.32	−48
		3000	0.28	102	1.6	42	0.34	63	0.29	−60
	30	100	0.40	−94	33	125	0.03	87	0.58	−42
		500	0.30	−162	8.4	90	0.07	84	0.31	−35
		1000	0.29	170	4.3	76	0.12	80	0.27	−39
		2000	0.24	134	2.3	56	0.23	71	0.33	−48
		3000	0.30	101	1.6	41	0.35	66	0.30	−60
	60	100	0.38	−126	31	116	0.03	74	0.49	−37
		500	0.37	−176	7.3	77.6	0.05	84	0.34	−26
		1000	0.36	163	3.7	73.4	0.12	84	0.34	−37
		2000	0.33	130	2.0	52	0.22	78	0.37	−48
		3000	0.38	98	1.4	37	0.34	69	0.34	−62
8.0	5.0	100	0.83	−35	13.9	154	0.04	92	0.90	−19
		500	0.51	−117	6.7	104	0.08	51	0.55	−38
		1000	0.38	−160	3.6	82	0.10	72	0.44	−42
		2000	0.31	151	1.9	58	0.20	73	0.46	−47
		3000	0.35	110	1.4	41	0.32	71	0.43	−63
	10	100	0.67	−52	23	143	0.02	96	0.81	−28
		500	0.37	−135	7.9	97	0.07	64	0.43	−38
		1000	0.30	−173	4.1	80	0.11	78	0.37	−41
		2000	0.25	143	2.2	57	0.21	74	0.38	−47
		3000	0.30	105	1.6	42	0.31	67	0.34	−60
	20	100	0.51	−72	30	131	0.02	68	0.68	−35
		500	0.31	−150	8.5	92	0.07	75	0.36	−36
		1000	0.28	177	4.3	77	0.13	76	0.32	−39
		2000	0.23	138	2.3	57	0.22	72	0.35	−45
		3000	0.27	103	1.6	42	0.31	64	0.31	−58
	30	100	0.42	−87	33	125	0.02	71	0.61	−38
		500	0.31	−159	8.6	90	0.07	71	0.33	−33
		1000	0.27	172	4.4	76	0.11	74	0.32	−39
		2000	0.23	135	2.3	57	0.22	73	0.34	−42
		3000	0.28	102	1.6	41	0.31	65	0.33	−55
	60	100	0.39	−119	32	117	0.02	31	0.52	−31
		500	0.36	−174	7.4	87	0.06	84	0.37	−25
		1000	0.35	164	3.8	74	0.11	78	0.35	−33
		2000	0.32	131	2.0	53	0.22	81	0.42	−41
		3000	0.37	100	1.4	38	0.33	70	0.40	−62

Table 1. MMBR951LT1 Common Emitter S–Parameters

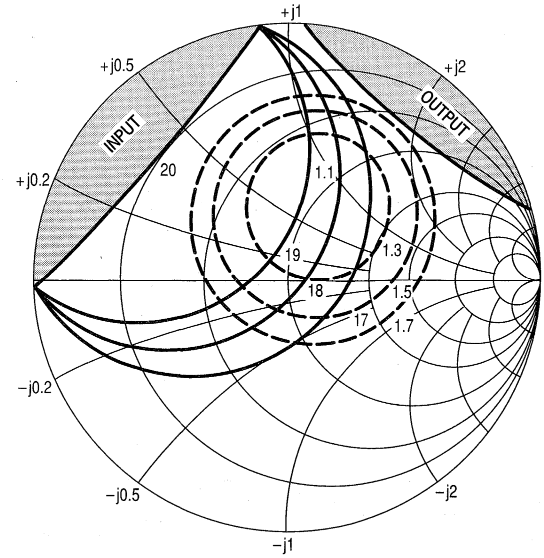
V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\lvert S_{11} \rvert$	∠ φ	$\lvert S_{21} \rvert$	∠ φ	$\lvert S_{12} \rvert$	∠ φ	$\lvert S_{22} \rvert$	∠ φ
6.0	5.0	100	0.81	−48	13.69	152	0.04	66	0.88	−22
		500	0.67	−122	7.58	92	0.07	41	0.57	−50
		1000	0.61	−157	4.65	76	0.09	40	0.45	−62
		1500	0.57	86	2.87	70	0.10	44	0.42	−71
		2000	0.54	156	2.14	60	0.12	52	0.42	−75
		2500	0.55	121	1.72	51	0.14	57	0.40	−86
		3000	0.57	121	1.48	44	0.17	59	0.39	−97
		3500	0.65	110	1.28	38	0.21	60	0.37	−112
		4000	0.67	100	1.14	33	0.24	54	0.38	−130
	10	100	0.71	−56	24.07	149	0.03	66	0.86	−28
		500	0.60	−143	9.47	101	0.05	46	0.41	−62
		1000	0.56	−176	4.97	81	0.07	51	0.30	−73
		1500	0.53	167	3.35	69	0.10	57	0.31	−78
		2000	0.50	148	2.54	60	0.13	63	0.30	−78
		2500	0.52	132	2.02	52	0.16	63	0.29	−89
		3000	0.54	116	1.75	45	0.19	61	0.29	−78
		3500	0.60	106	1.53	39	0.22	60	0.26	−115
		4000	0.64	97	1.35	34	0.26	57	0.28	−133
	20	100	0.59	−80	33.51	138	0.02	61	0.75	−38
		500	0.56	−159	10.39	95	0.04	54	0.31	−69
		1000	0.54	175	5.36	79	0.07	62	0.23	−79
		1500	0.51	161	3.58	68	0.10	66	0.25	−82
		2000	0.49	142	2.75	60	0.13	68	0.25	−80
		2500	0.52	128	2.18	52	0.16	66	0.23	−91
		3000	0.53	112	1.88	45	0.20	63	0.23	−99
		3500	0.60	103	1.65	39	0.24	62	0.21	−117
		4000	0.63	95	1.46	34	0.27	57	0.22	−137
	30	100	0.54	−97	37.48	133	0.02	57	0.67	−43
		500	0.56	−166	10.60	93	0.04	59	0.27	−70
		1000	0.54	171	5.45	78	0.07	68	0.21	−80
		1500	0.51	158	3.62	67	0.10	69	0.24	−81
		2000	0.50	140	2.73	60	0.13	70	0.23	−79
		2500	0.52	126	2.19	51	0.17	68	0.23	−90
		3000	0.53	111	1.89	45	0.20	64	0.23	−97
		3500	0.60	102	1.65	38	0.24	62	0.20	−115
		4000	0.63	94	1.47	33	0.27	58	0.22	−136
	60	100	0.54	−128	36.66	123	0.01	57	0.56	−43
		500	0.60	−177	8.97	89	0.03	67	0.27	−50
		1000	0.59	166	4.62	75	0.06	73	0.25	−59
		1500	0.56	153	3.05	64	0.09	75	0.29	−68
		2000	0.55	136	2.29	56	0.13	76	0.30	−71
		2500	0.57	125	1.85	48	0.16	74	0.29	−83
		3000	0.59	110	1.59	42	0.20	69	0.30	−92
		3500	0.65	102	1.41	36	0.23	67	0.27	−108
		4000	0.69	93	1.22	31	0.27	62	0.29	−130

(continued)

Table 1. MRF9511LT1 Common Emitter S–Parameters

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle \phi$	$\|S_{21}\|$	$\angle \phi$	$\|S_{12}\|$	$\angle \phi$	$\|S_{22}\|$	$\angle \phi$
8.0	5.0	100	0.84	−36	14.65	158	0.03	72	0.94	−18
		500	0.68	−120	7.79	110	0.07	42	0.58	−48
		1000	0.60	−161	4.32	86	0.08	41	0.44	−60
		1500	0.56	88	2.95	71	0.10	45	0.44	−68
		2000	0.53	157	2.19	60	0.11	53	0.44	−71
		2500	0.55	140	1.76	51	0.14	58	0.42	−82
		3000	0.56	122	1.50	44	0.17	60	0.42	−92
		3500	0.63	112	1.33	39	0.18	62	0.38	−107
		4000	0.68	105	1.18	33	0.21	63	0.36	−125
	10	100	0.73	−53	24.04	150	0.02	68	0.87	−26
		500	0.60	−140	9.68	101	0.05	46	0.43	−58
		1000	0.55	−174	5.10	82	0.07	52	0.32	−66
		1500	0.52	169	3.42	69	0.09	58	0.33	−72
		2000	0.49	149	2.59	61	0.12	63	0.33	−73
		2500	0.51	133	2.06	52	0.15	63	0.32	−83
		3000	0.53	116	1.78	45	0.19	63	0.32	−91
		3500	0.64	109	1.60	38	0.20	62	0.28	−108
		4000	0.67	101	1.39	34	0.23	60	0.29	−131
	20	100	0.61	−76	33.76	139	0.02	60	0.76	−36
		500	0.56	−157	10.72	96	0.04	54	0.32	−63
		1000	0.53	176	5.53	79	0.07	62	0.29	−70
		1500	0.50	162	3.69	68	0.10	66	0.27	−75
		2000	0.48	143	2.79	60	0.13	68	0.27	−74
		2500	0.51	129	2.22	52	0.16	68	0.26	−84
		3000	0.52	112	1.92	46	0.19	65	0.26	−91
		3500	0.59	104	1.75	40	0.21	64	0.24	−109
		4000	0.63	98	1.54	35	0.24	59	0.25	−131
	30	100	0.57	−89	37.35	134	0.02	58	0.71	−40
		500	0.55	−163	10.82	94	0.04	57	0.29	−63
		1000	0.53	128	5.54	78	0.07	65	0.24	−69
		1500	0.50	159	3.69	67	0.10	69	0.26	−73
		2000	0.49	141	2.77	59	0.13	70	0.27	−71
		2500	0.51	127	2.23	51	0.16	69	0.26	−82
		3000	0.52	112	1.93	45	0.19	66	0.26	−89
		3500	0.61	106	1.68	40	0.21	64	0.21	−110
		4000	0.66	97	1.51	34	0.24	60	0.23	−130
	60	100	0.55	−122	34.92	126	0.01	52	0.59	−37
		500	0.59	−175	8.71	91	0.03	65	0.33	−42
		1000	0.58	167	4.52	76	0.06	73	0.30	−53
		1500	0.55	154	3.04	65	0.09	75	0.34	−62
		2000	0.54	138	2.28	56	0.12	77	0.35	−66
		2500	0.57	125	1.82	48	0.16	76	0.34	−78
		3000	0.59	110	1.56	42	0.19	72	0.35	−88
		3500	0.66	104	1.28	36	0.22	70	0.32	−105
		4000	0.70	95	1.14	32	0.26	66	0.32	−132

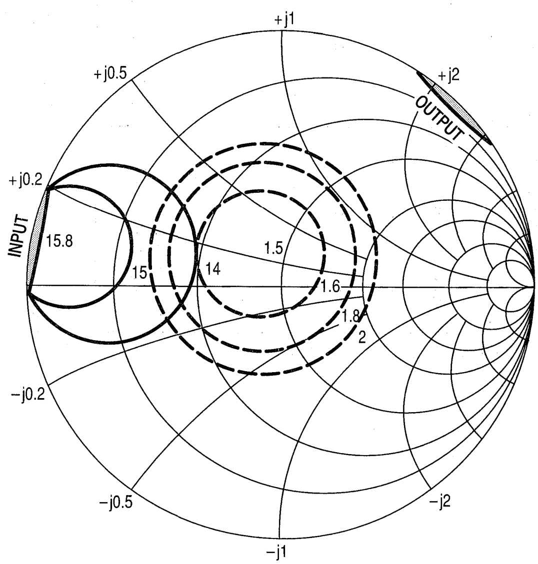
Table 1. MRF9511LT1 Common Emitter S–Parameters (continued)



V_{CE} = 6.0 V
I_C = 5.0 mA
▨ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	Rn	K
0.5	1.13	0.35 ∠ 68°	9	0.68

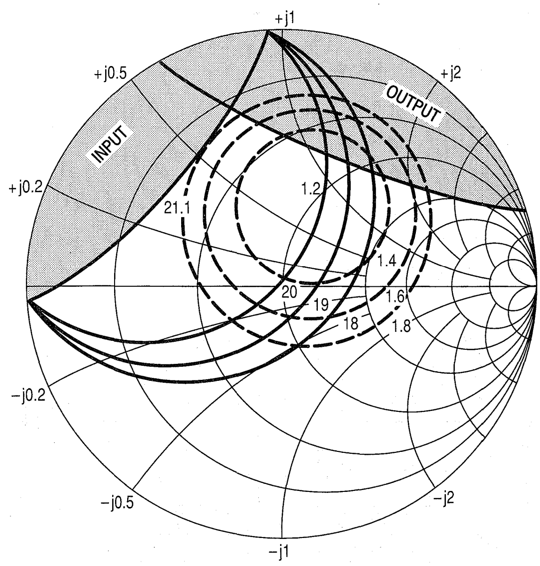
Figure 10. MMBR951LT1 Constant Gain and Noise Figure Contours (f = 0.5 GHz)



V_{CE} = 6.0 V
I_C = 5.0 mA
▨ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	Rn	K
1.0	1.45	0.16 ∠ 124°	8	0.97

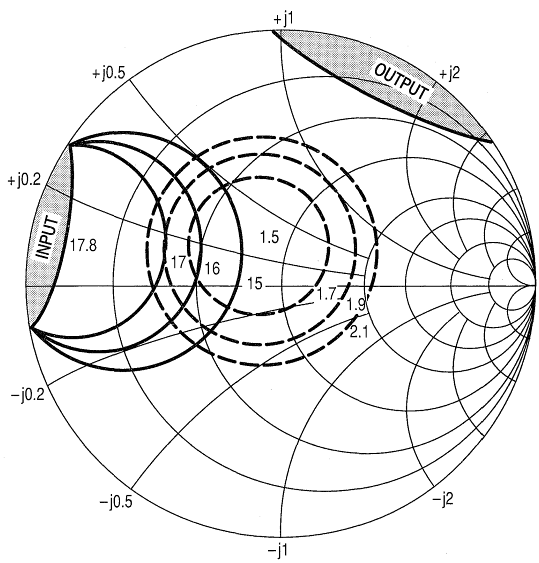
Figure 11. MMBR951LT1 Constant Gain and Noise Figure Contours (f = 1.0 GHz)



V_{CE} = 6.0 V
I_C = 5.0 mA
▒ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	Rn	K
0.5	1.20	0.37 ∠ 69°	10	0.42

Figure 12. MRF9511LT1 Constant Gain and Noise Figure Contours (f = 0.5 GHz)



V_{CE} = 6.0 V
I_C = 5.0 mA
▒ — AREA OF INSTABILITY

f (GHz)	NF OPT (dB)	ΓMS NF OPT	Rn	K
1.0	1.50	0.19 ∠ 120°	9	0.74

Figure 13. MRF9511LT1 Constant Gain and Noise Figure Contours (f = 1.0 GHz)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	NF_{min} (dB)	Γ_o (MAG, ANG)	r_N (ohms)
6.0	5.0	1000 1500	1.7 2.0	0.27 ∠ 97 0.21 ∠ 54	0.2 0.28

Table 2. MRF957T1 Typical Noise Parameters

TYPICAL CHARACTERISTICS
MRF957T1

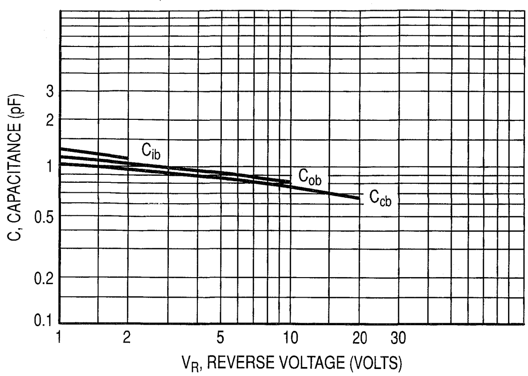


Figure 14. Capacitance versus Voltage

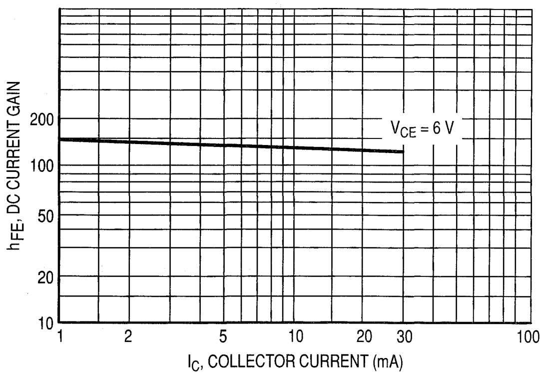


Figure 15. DC Current Gain versus Collector Current

TYPICAL CHARACTERISTICS
MRF957T1

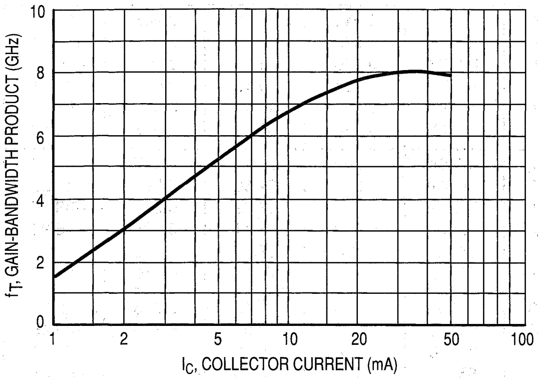


Figure 16. Gain–Bandwidth Product versus Collector Current

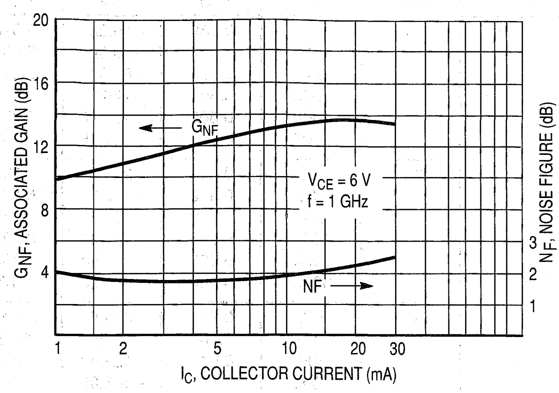


Figure 17. Associated Gain versus Collector Current

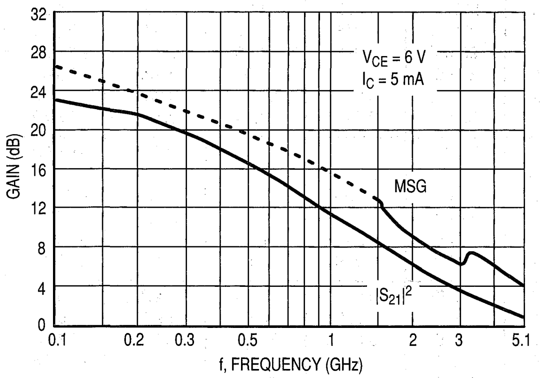


Figure 18. Insertion Gain and Maximum Stable Power Gain versus Frequency

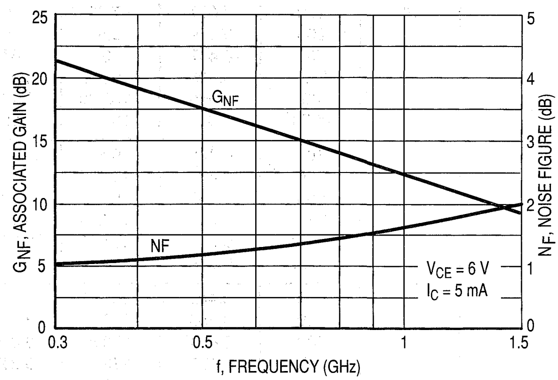


Figure 19. Noise Figure and Associated Gain versus Frequency

V_{CE} = 6.0 V I_C = 5.0 mA

f (GHz)	NF OPT	Γ_o	R_N	K
1.0	1.5 dB	0.27 ∠ 97°	10	0.91

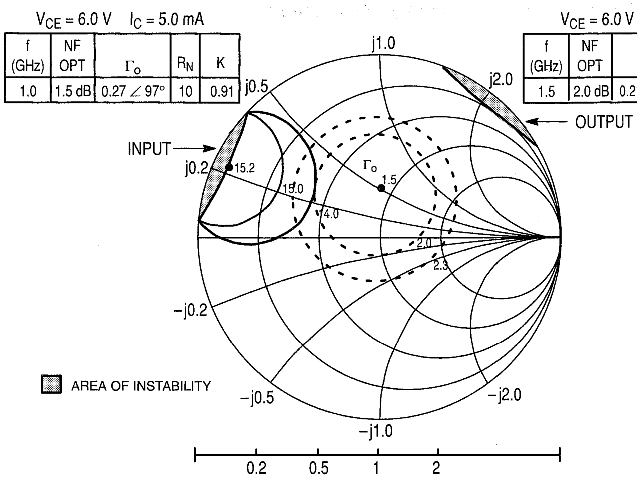


Figure 20. Constant Gain and Noise Figure Contours f = 1.0 GHz

V_{CE} = 6.0 V I_C = 5.0 mA

f (GHz)	NF OPT	Γ_o	R_N	K
1.5	2.0 dB	0.21 ∠ 54°	14	1.02

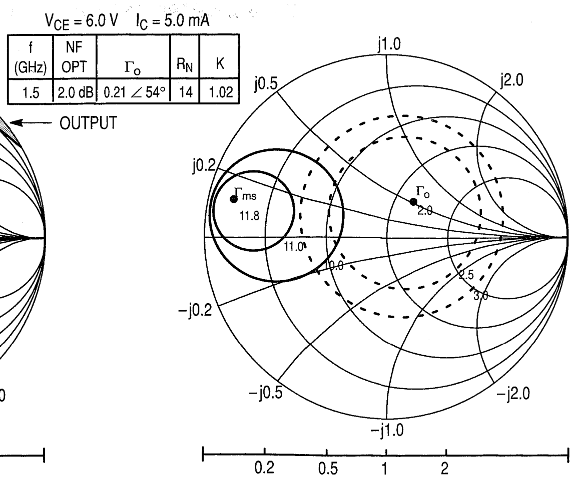


Figure 21. Constant Gain and Noise Figure Contours f = 1.5 GHz

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
2.0	1.0	100	0.959	−19.22	3.518	166.25	0.044	78.43	0.986	−8.12
		200	0.922	−38.32	3.482	153.75	0.079	69.06	0.948	−15.98
		500	0.825	−81.94	2.614	122.98	0.146	44.99	0.803	−30.02
		1000	0.690	−125.83	1.737	93.40	0.167	30.15	0.662	−41.41
		2000	0.600	−174.02	1.079	63.65	0.131	44.93	0.576	−51.42
		3000	0.640	147.15	0.791	50.62	0.196	80.39	0.517	−64.42
	2.0	100	0.922	−24.97	6.598	162.54	0.042	75.55	0.967	−12.35
		200	0.862	−48.55	6.177	147.47	0.075	64.60	0.893	−23.28
		500	0.713	−96.45	4.140	116.09	0.123	43.92	0.671	−38.55
		1000	0.586	−137.24	2.483	90.37	0.140	38.71	0.524	−46.93
		2000	0.506	179.54	1.462	64.47	0.158	57.00	0.456	−51.97
		3000	0.546	144.80	1.079	49.98	0.232	74.13	0.416	−61.22
	5.0	100	0.815	−39.45	14.163	153.09	0.038	70.19	0.895	−22.63
		200	0.708	−71.89	11.635	133.50	0.061	58.57	0.739	−38.46
		500	0.541	−121.43	6.284	104.78	0.090	49.12	0.454	−52.31
		1000	0.461	−155.05	3.428	85.44	0.123	54.90	0.337	−56.38
		2000	0.406	169.75	1.921	65.04	0.198	65.80	0.304	−54.16
		3000	0.438	139.42	1.424	51.41	0.282	69.61	0.276	−57.77
	10	100	0.667	−57.75	22.121	142.36	0.032	64.38	0.788	−34.26
		200	0.559	−95.89	15.709	121.54	0.048	57.27	0.574	−52.06
		500	0.447	−140.52	7.417	98.06	0.075	58.00	0.317	−63.32
		1000	0.405	−166.70	3.921	82.59	0.123	66.07	0.235	−65.49
		2000	0.360	162.90	2.155	65.25	0.222	69.45	0.220	−57.93
		3000	0.390	134.95	1.597	52.60	0.311	68.14	0.196	−57.79
	30	100	0.435	−99.80	31.662	125.82	0.023	62.49	0.570	−51.69
		200	0.421	−135.04	18.696	108.07	0.034	64.74	0.360	−68.74
		500	0.398	−162.97	8.025	91.81	0.069	71.43	0.192	−75.85
		1000	0.382	−179.33	4.163	79.67	0.127	74.17	0.151	−77.73
		2000	0.347	155.68	2.269	64.55	0.240	72.04	0.155	−63.30
		3000	0.379	130.21	1.686	52.60	0.336	67.80	0.132	−60.40
	60	100	0.442	−131.87	26.755	118.52	0.021	62.60	0.422	−56.23
		200	0.483	−155.78	15.086	103.17	0.032	66.87	0.261	−70.51
		500	0.484	−173.89	6.390	88.79	0.067	74.30	0.154	−73.64
		1000	0.472	172.69	3.317	76.81	0.127	76.73	0.140	−74.96
		2000	0.452	149.80	1.834	60.68	0.243	72.97	0.155	−66.57
		3000	0.496	126.23	1.393	48.59	0.345	68.81	0.131	−71.10

(continued)

Table 3. MRF957T1 Typical Common Emitter S–Parameters

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
5.0	1.0	100	0.965	−17.73	3.508	167.36	0.035	78.18	0.990	−6.80
		200	0.931	−35.39	3.495	155.78	0.065	71.66	0.958	−13.35
		500	0.835	−77.08	2.680	126.50	0.122	48.12	0.839	−25.23
		1000	0.694	−120.78	1.820	97.22	0.143	33.67	0.713	−35.51
		2000	0.583	−170.80	1.133	67.35	0.115	50.88	0.629	−44.48
		3000	0.615	148.45	0.813	53.19	0.182	85.71	0.565	−55.47
	2.0	100	0.932	−22.38	6.532	164.05	0.034	77.81	0.975	−9.92
		200	0.875	−44.00	6.217	150.00	0.061	67.15	0.914	−18.98
		500	0.726	−89.77	4.314	119.58	0.106	47.42	0.724	−31.79
		1000	0.582	−131.10	2.638	93.76	0.122	41.23	0.586	−39.20
		2000	0.483	−176.30	1.544	67.35	0.140	60.85	0.521	−43.55
		3000	0.515	146.92	1.117	52.27	0.208	78.88	0.479	−51.26
	5.0	100	0.836	−34.35	14.112	155.49	0.031	71.72	0.920	−18.06
		200	0.731	−63.59	11.971	137.05	0.052	61.40	0.785	−31.06
		500	0.539	−112.00	6.737	107.93	0.080	51.32	0.522	−41.63
		1000	0.438	−147.18	3.710	88.06	0.110	57.59	0.408	−43.94
		2000	0.364	175.10	2.050	67.58	0.175	68.31	0.383	−42.49
		3000	0.392	142.26	1.501	53.59	0.251	73.36	0.357	−45.46
	10	100	0.704	−49.02	22.526	145.79	0.027	67.46	0.831	−27.03
		200	0.577	−83.93	16.647	125.23	0.042	59.78	0.634	−41.45
		500	0.421	−129.59	8.120	100.71	0.069	60.52	0.385	−47.31
		1000	0.361	−158.62	4.290	84.82	0.109	67.54	0.305	−46.57
		2000	0.307	168.57	2.330	67.52	0.196	71.46	0.305	−42.00
		3000	0.332	137.50	1.706	54.85	0.277	71.05	0.288	−42.21
	20	100	0.559	−66.34	30.018	136.00	0.023	64.88	0.720	−35.45
		200	0.453	−103.91	19.598	116.12	0.036	61.80	0.501	−48.64
		500	0.358	−143.87	8.835	96.19	0.064	68.23	0.298	−49.15
		1000	0.324	−167.05	4.595	83.08	0.112	72.95	0.247	−47.12
		2000	0.278	163.88	2.462	67.27	0.208	72.96	0.263	−41.09
		3000	0.306	133.94	1.809	55.45	0.291	70.31	0.249	−39.38
	30	100	0.492	−73.65	32.055	131.68	0.022	64.17	0.669	−37.70
		200	0.412	−110.53	20.121	113.25	0.033	64.60	0.459	−49.28
		500	0.345	−147.89	8.900	94.88	0.062	69.52	0.278	−48.58
		1000	0.319	−169.39	4.646	82.13	0.113	74.20	0.234	−46.64
		2000	0.277	162.38	2.492	67.55	0.210	73.10	0.255	−40.63
		3000	0.305	133.57	1.821	55.24	0.295	70.42	0.239	−38.73

Table 3. MRF957T1 Typical Common Emitter S–Parameters (continued)

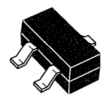
The RF Line
NPN Silicon High-Frequency Transistor

MMBR5031LT1

Designed for thick and thin–film circuits using surface mount components and requiring low–noise, high–gain signal amplification at frequencies to 1.0 GHz.

- High Gain — G_{pe} = 17 dB Typ @ f = 450 MHz
- Low Noise — NF = 2.5 dB Typ @ f = 450 MHz
- Available in tape and reel packaging options:
  T1 suffix = 3,000 units per reel

RF AMPLIFIER TRANSISTOR NPN SILICON



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE
(TO–236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	10	Vdc
Collector–Base Voltage	V_{CBO}	15	Vdc
Emitter–Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	20	mAdc
Maximum Junction Temperature	T_{Jmax}	150	°C
Power Dissipation, T_{case} = 75°C (1) Derate linearly above T_{case} = 75°C @	$P_{D(max)}$	0.300 4.00	W mW/°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Storage Temperature	T_{stg}	–55 to +150	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	250	°C/W

DEVICE MARKING

MMBR5031LT1 = 7G

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	10	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.01 mAdc, I_E = 0)	$V_{(BR)CBO}$	15	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.01 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 6.0 Vdc, I_E = 0)	I_{CBO}	—	—	10	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc)	h_{FE}	25	—	300	—
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	—	1,000	—	MHz
Collector–Base Capacitance (V_{CE} = 6.0 Vdc, I_E = 0, f = 0.1 MHz)	C_{cb}	—	—	1.5	pF
Minimum Noise Figure (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz)	NF_{min}	—	2.5	—	dB
Common–Emitter Amplifier Power Gain (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz)	G_{pe}	—	17	25	dB

NOTE:
1. Case temperature measured on collector lead immediately adjacent to body of package.

REV 7

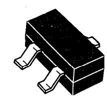
The RF Line
NPN Silicon High-Frequency Transistor

MMBR5179LT1

Designed for small–signal amplification at frequencies to 500 MHz. Specifically packaged for use in thick and thin–film circuits using surface mount components.

- High Gain — G_{pe} = 15 dB Typ @ f = 200 MHz
- Low Noise — NF = 4.5 dB Typ @ f = 200 MHz
- Available in tape and reel packaging options:
  T1 suffix = 3,000 units per reel

RF AMPLIFIER
TRANSISTOR
NPN SILICON



CASE 318–08, STYLE 6
SOT–23
LOW PROFILE
(TO–236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	12	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Emitter–Base Voltage	V_{EBO}	2.5	Vdc
Collector Current — Continuous	I_C	50	mAdc
Maximum Junction Temperature	T_{Jmax}	150	°C
Power Dissipation, T_{case} = 75°C (1) Derate linearly above T_{case} = 75°C @	$P_{D(max)}$	0.375 5.00	W mW/°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Storage Temperature	T_{stg}	–55 to +150	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	200	°C/W

DEVICE MARKING

MMBR5179LT1 = 7H

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 3.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	12	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.01 mAdc, I_E = 0)	$V_{(BR)CBO}$	20	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.01 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	0.02	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3.0 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	25	—	—	—
Collector–Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	—	—	0.4	Vdc
Base–Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	—	—	1.0	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	—	1,400	—	MHz
Collector–Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{cb}	—	—	1.0	pF
50 ohm Noise Figure (I_C = 1.5 mAdc, V_{CE} = 6.0 Vdc, R_S = 50 Ω, f = 200 MHz)	NF	—	4.5	—	dB
Common–Emitter Amplifier Power Gain (V_{CE} = 6.0 Vdc, I_C = 5.0 mAdc, f = 200 MHz)	G_{pe}	—	15	—	dB

NOTE:
1. Case temperature measured on collector lead immediately adjacent to body of package.

REV 7

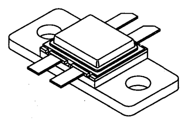
The RF Line
UHF Power Transistor

MRA0510-50H

Designed primarily for wideband, large–signal output and driver amplifier stages in the 500 to 1000 MHz frequency range.

- Designed for Class AB Linear Power Amplifiers
- Specified 28 Volt, 1000 MHz Characteristics:
  Output Power — 50 Watts
  Power Gain — 7 dB (Min), Class AB
- Built–In Matching Network for Broadband Operation
- Gold Metallization for Improved Reliability
- Diffused Ballast Resistors
- Hermetic Package for Military/Space Applications

7.0 dB, 500 – 1000 MHz
50 W
BROADBAND
UHF POWER TRANSISTOR



CASE 391–03, STYLE 1
(HLP–42)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.715	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, RF, Junction to Case (T_C = 70°C)	$R_{\theta JC}$	1.4	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Breakdown Voltage (I_C = 25 mA, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mA, I_E = 0)	$V_{(BR)CBO}$	60	–	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 5 mA, I_C = 0)	$V_{(BR)EBO}$	4	–	–	Vdc
Collector–Emitter Breakdown Voltage (I_C = 25 mA, R_{BE} = 1 Ω)	$V_{(BR)CER}$	50	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 V, I_E = 0)	I_{CBO}	–	–	25	mAdc

(1) Each transistor chip measured separately.

(continued)

REV 1

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1 A, V_{CE} = 5 V)	h_{FE}	20	–	80	–
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{CB} = 28 V, I_E = 0, f = 1 MHz)	C_{ob}	–	–	24	pF
FUNCTIONAL TESTS (2)					
Common–Emitter Amplifier Power Gain (V_{CE} = 28 V, P_{out} = 50 W, f = 1 GHz, I_{CQ} = 2 x 120 mA)	G_{PE1}	7	–	–	dB
Load Mismatch (V_{CE} = 28 V, I_{CQ} = 2 x 120 mA, P_{out} = 50 W, f = 1 GHz, Load VSWR = 5:1, All Phase Angles)	ψ	No Degradation in Output Power			
Broadband Power Gain (V_{CE} = 28 V, P_{out} = 45 W, f = 500 mHz and 1 GHz, I_{CQ} = 2 x 120 mA)	G_{PE2}	6.5	–	–	dB

(1) Each transistor chip measured separately.
(2) Both transistor chips operating in push–pull amplifier.

TYPICAL CHARACTERISTICS

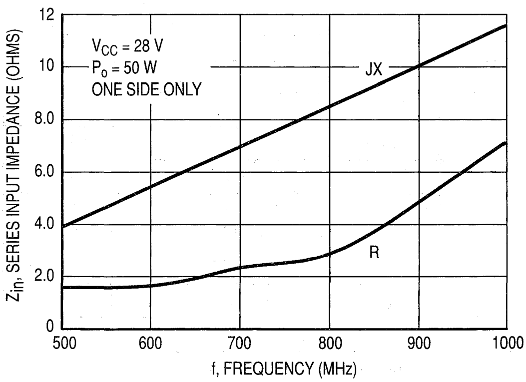


Figure 1. Input Impedance versus Frequency

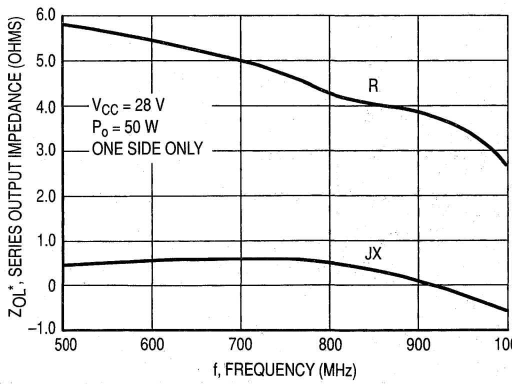


Figure 2. Output Impedance versus Frequency

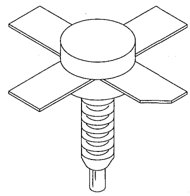
The RF Line
UHF Power Transistor

MRA1000-3.5L

Designed primarily for wideband, large–signal output and driver amplifier stages to 1000 MHz.

- Designed for Class A Linear Power Amplifiers
- Specified 19 Volt, 1000 MHz Characteristics:
  Output Power — 3.5 Watts
  Power Gain — 10 dB, Small–Signal
- Built–In Matching Network for Broadband Operation
- Gold Metallization for Improved Reliability
- Diffused Ballast Resistors

10 dB, 1000 MHz
3.5 W
BROADBAND
UHF POWER TRANSISTOR



CASE 145D–02, STYLE 1
(.380 SOE)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	28	Vdc
Collector–Base Voltage	V_{CBO}	50	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	22 0.125	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (T_C = 70°C)	$R_{\theta JC}$	8	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mA, I_B = 0)	$V_{(BR)CEO}$	28	–	–	Vdc
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{BE} = 0)	$V_{(BR)CES}$	50	–	–	Vdc
Collector–Base Breakdown Voltage (I_C = 10 mA, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 5 mA, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 V, I_E = 0)	I_{CBO}	–	–	10	mAdc

(continued)

REV 1

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mA, V_{CE} = 5 V)	h_{FE}	20	–	90	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 V, I_E = 0, f = 1 MHz)	C_{ob}	–	–	15	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Small–Signal Gain (V_{CE} = 19 V, P_{in} = 1 mW, f = 1 GHz, I_C = 600 mA)	G_{SS}	10	–	–	dB
Load Mismatch (V_{CE} = 19 V, I_C = 600 mA, P_{out} = 3.5 W, f = 1 GHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No Degradation in Output Power			
Overdrive (V_{CE} = 19 V, I_C = 600 mA, f = 1 GHz) (No degradation)	P_{inover}	–	–	1.75	W

TYPICAL CHARACTERISTICS

Table 1. Common Emitter S–Parameters

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	∠ φ	Mag	∠ φ	Mag	∠ φ	Mag	∠ φ
19	600	0.5	0.91	174	1.78	53	0.03	23	0.55	–164
		0.6	0.9	173	1.64	47	0.03	21	0.58	–170
		0.7	0.87	171	1.53	36	0.03	19	0.63	–159
		0.8	0.85	168	1.51	24	0.03	15	0.68	–157
		0.9	0.82	168	1.49	10	0.03	5	0.74	–158
		1	0.78	168	1.5	–7	0.03	–4	0.83	–160

Table 2. Z_{in} and Z_{OL}* versus Frequency

V_{CC} = 19 V, P_c = 3.5 W

Freq. (MHz)	Z_{OL}*		Z_{in} (Ohms)	
	Re	Im	Re	Im
500	14.6	–6.31	2.36	2.53
600	13.2	–4.07	2.74	3.18
700	11.7	–8.95	3.36	4.14
800	9.95	–9.65	4.12	5.13
900	7.72	–9.72	4.99	5.33
1000	4.67	–8.74	6.36	5.04

Z_{OL}* = Conjugate of the optimum lead impedance into which the device output operates at a given frequency, output power and voltage.

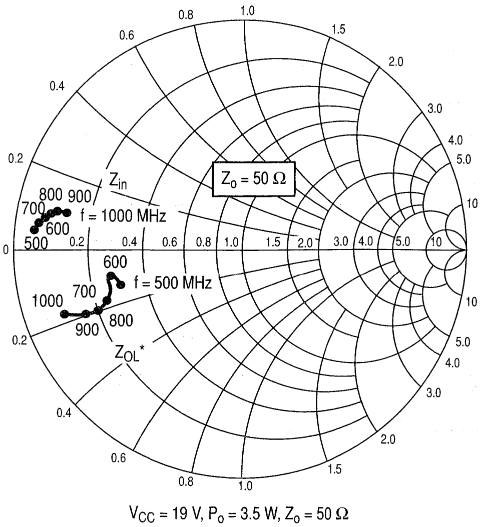


Figure 1. Series Equivalent Input/Output Impedance

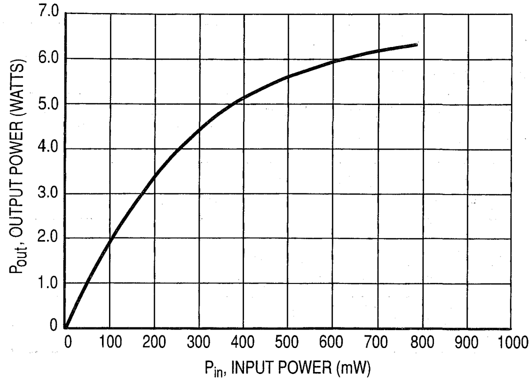
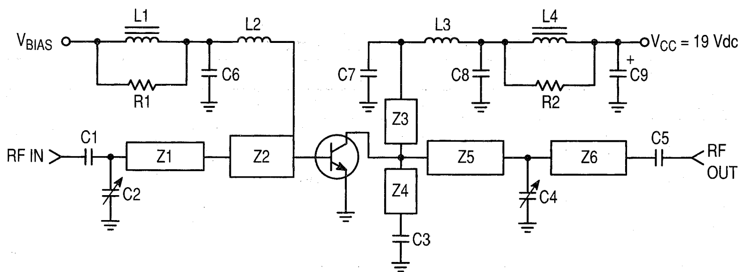


Figure 2. Power Input versus Power Output



C1, C3, C5, C6, C7	500 pF, ATC	L4	8T, 20 Gauge on 275 Mil Ferrite Toroid
C2, C4	0.8 – 10 pF, JFD	R1, R2	15 Ω, 1/4 Watt
C9	0.1 μF, 50 V, Ceramic	Z1	50 Ω, Microstripline, ℓ = 0.110 λ
L1	7T, 20 Gauge on 200 Mil Ferrite Toroid	Z2	10 Ω, Microstripline, ℓ = 0.162 λ
L2	8T, 20 Gauge, 100 Mil Dia.	Z3, Z4	50 Ω, Microstripline, ℓ = 0.052 λ
L3	11T, 20 Gauge, 100 Mil Dia.	Z5	24 Ω, Microstripline, ℓ = 0.080 λ
		Z6	50 Ω, Microstripline, ℓ = 0.125 λ

Figure 3. 1 GHz Test Circuit

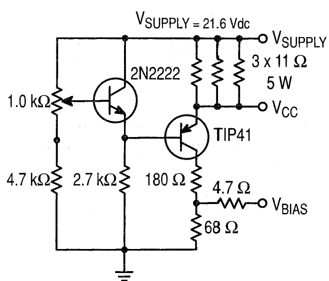


Figure 4. Bias Circuit

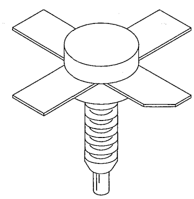
The RF Line
UHF Power Transistor

MRA1000-7L

. . . designed primarily for wideband, large–signal output and driver amplifier stages to 1000 MHz.

- Designed for Class A Linear Power Amplifiers
- Specified 19 Volt, 1000 MHz Characteristics:
  Output Power — 7.0 Watts
  Power Gain — 9.0 dB Min, Small–Signal
- Built–In Matching Network for Broadband Operation
- Gold Metallization for Improved Reliability
- Diffused Ballast Resistors
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

9.0 dB, TO 1000 MHz
7.0 WATTS BROADBAND
UHF POWER TRANSISTOR



CASE 145D–02, STYLE 1
(.380 SOE)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	28	Vdc
Collector–Base Voltage	V_{CBO}	50	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	42 0.25	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (T_C = 70°C)	$R_{\theta JC}$	4.0	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mA, I_B = 0)	$V_{(BR)CEO}$	28	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mA, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 20 mA, I_E = 0)	$V_{(BR)CBO}$	50	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mA, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 19 V, I_E = 0)	I_{CBO}	—	—	15	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	20	—	90	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 V, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	22	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Small–Signal Gain (V_{CE} = 19 V, f = 1.0 GHz, I_C = 1.2 A)	G_{SS}	9.0	10	—	dB
Load Mismatch (V_{CE} = 19 V, I_C = 1.2 A, P_{out} = 7.0 W, f = 1.0 GHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No Degradation in Output Power			
Overdrive (V_{CE} = 19 V, I_C = 1.2 A, f = 1.0 GHz) (No degradation)	$P_{in_{over}}$	—	—	3.5	W
Output Power, 1.0 dB Compression Point (V_{CE} = 19 V, f = 1.0 GHz, I_C = 1.2 A)	$P_{o1\ dB}$	7.0	—	—	W

REV 6

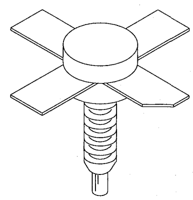
The RF Line
UHF Power Transistor

MRA1000-14L

. . . designed primarily for wideband, large–signal output and driver amplifier stages to 1000 MHz.

- Designed for Class A Linear Power Amplifiers
- Specified 19 Volt, 1000 MHz Characteristics:
  Output Power — 14 Watts
  Power Gain — 8.0 dB, Small–Signal
- Built–In Matching Network for Broadband Operation
- Gold Metallization for Improved Reliability
- Diffused Ballast Resistors
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

8.0 dB, TO 1000 MHz
14 WATTS BROADBAND
UHF POWER TRANSISTOR



CASE 145D–02, STYLE 1
(.380 SOE)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	28	Vdc
Collector–Base Voltage	V_{CBO}	50	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	83 0.48	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (T_C = 70°C)	$R_{\theta JC}$	2.1	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mA, I_B = 0)	$V_{(BR)CEO}$	28	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 25 mA, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mA, I_E = 0)	$V_{(BR)CBO}$	50	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mA, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 19 V, I_E = 0)	I_{CBO}	—	—	20	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	20	—	90	—

(continued)

REV 6

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 V, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	40	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Small–Signal Gain (V_{CE} = 19 V, P_{in} = 1.0 mW, f = 1.0 GHz, I_C = 2.4 A)	G_{SS}	8.0	—	—	dB
Load Mismatch (V_{CE} = 19 V, I_C = 2.4 A, P_{out} = 14 W, f = 1.0 GHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No Degradation in Output Power			
Overdrive (V_{CE} = 19 V, I_C = 2.4 A, f = 1.0 GHz) (No degradation)	$P_{in_{over}}$	—	—	7.0	W
Output Power, 1.0 dB Compression Point (V_{CE} = 19 V, f = 1.0 GHz, I_C = 2.4 A)	$P_{o1\,dB}$	14	—	—	W

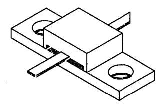
The RF Line
Microwave Power Transistor

MRA1600-2

Designed primarily for large–signal output and driver amplifier stages for mobile satellite up links.

- Designed for Class C, Common Base Power Amplifiers
- Specified 28 Volt, 1640 MHz Characteristics:
  Output Power = 2.0 to 30 Watts
  Power Gain = 7.0 to 8.4 dB (Min)
  Collector Efficiency = 39% to 45% (Min)
- Internally Compensated
- Gold Metallization for Improved Reliability
- Diffused Ballast Resistors

7.0 – 8.4 dB
1600 – 1660 MHz
2.0 – 30 W
NARROWBAND MICROWAVE POWER TRANSISTOR



CASE 394–03, STYLE 1
(MRA .25)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CES}	50	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current – Continuous	I_C	0.5	Adc
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, RF, Junction to Case (Rated P_{out})	$R_{\theta JC}$	15	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mA, V_{BE} = 0)	$V_{(BR)CES}$	50	–	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.25 mA, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CB} = 28 V, I_E = 0)	I_{CBO}	0.5	–	–	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.1 A, V_{CE} = 5.0 V)	h_{FE}	10	–	100	–

(continued)

REV 1

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 V, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	4.5	pF
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CE} = 28 V, P_{out} = 2.2 W, f = 1.60 and 1.64 GHz)	G_{PB}	8.4	–	–	dB
Collector Efficiency (V_{CE} = 28 V, P_{out} = 2.2 W, f = 1.60 and 1.64 GHz)	η_c	39	–	–	%

TYPICAL CHARACTERISTICS

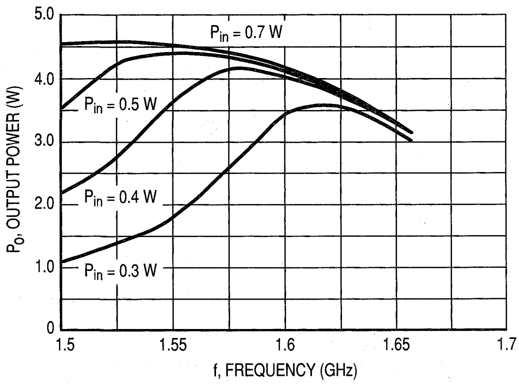


Figure 1. Output Power versus Frequency

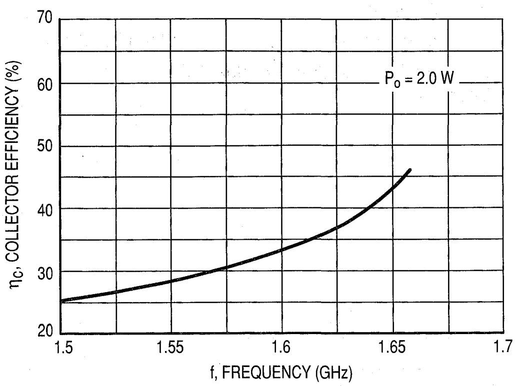


Figure 2. Efficiency versus Frequency

Table 1. Input/Output Impedances (P_o = 2.2 W, V_{CE} = 28 V)

f (GHz)	R_{IN}	JX_{IN}	R_O(1)	JX_O(1)
1.500	17.662	10.579	8.813	–17.216
1.525	17.146	10.661	8.001	–17.786
1.550	16.608	10.328	7.240	–18.350
1.575	16.087	9.986	6.728	–19.386
1.600	15.596	9.635	6.408	–20.420
1.625	15.149	9.273	6.164	–20.950
1.650	14.643	8.913	5.793	–21.495
1.675	14.214	8.541	5.416	–22.565
1.700	13.823	8.581	5.027	–23.122

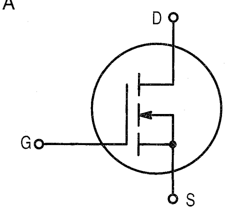
(1) Z_{OL}^* = R_O + JX_O is the conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode

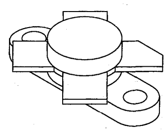
MRF134

. . . designed for wideband large–signal amplifier and oscillator applications up to 400 MHz range.

- Guaranteed 28 Volt, 150 MHz Performance
  Output Power = 5.0 Watts
  Minimum Gain = 11 dB
  Efficiency — 55% (Typical)
- Small–Signal and Large–Signal Characterization
- Typical Performance at 400 MHz, 28 Vdc, 5.0 W
  Output = 10.6 dB Gain
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 2.0 dB (Typ) at 200 mA, 150 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation



5.0 W, to 400 MHz
N–CHANNEL MOS
BROADBAND RF POWER
FET



CASE 211–07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	0.9	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	17.5 0.1	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

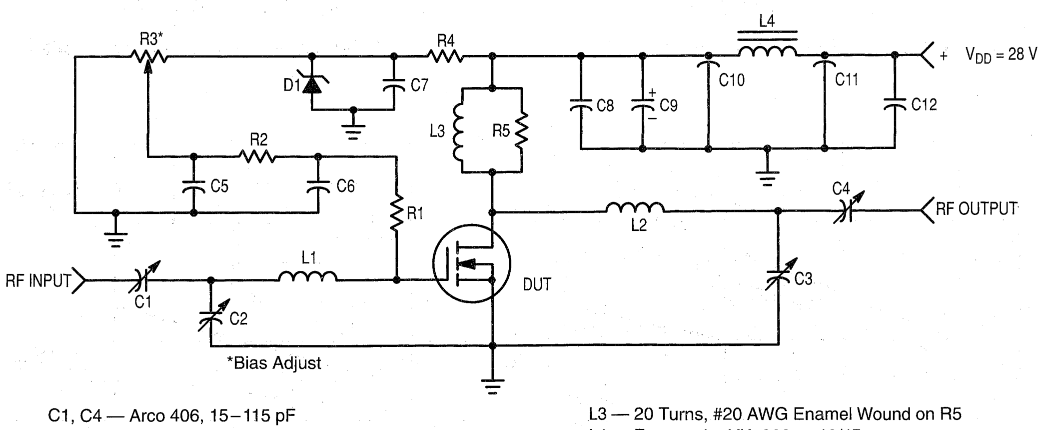
Rating	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 10 mA, V_{DS} = 10 V)	$V_{GS(th)}$	1.0	3.5	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	80	110	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	7.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	9.7	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.3	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 200 mA, f = 150 MHz)	NF	—	2.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 5.0 W, I_{DQ} = 50 mA)	G_{ps}				dB
f = 150 MHz (Fig. 1)		11	14	—	
f = 400 MHz (Fig. 14)		—	10.6	—	
Drain Efficiency (Fig. 1) (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 150 MHz, I_{DQ} = 50 mA)	η	50	55	—	%
Electrical Ruggedness (Fig. 1) (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 150 MHz, I_{DQ} = 50 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			



C1, C4 — Arco 406, 15–115 pF
C2 — Arco 403, 3.0–35 pF
C3 — Arco 402, 1.5–20 pF
C5, C6, C7, C8, C12 — 0.1 μF Erie Redcap
C9 — 10 μF, 50 V
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 3 Turns, 0.310″ ID, #18 AWG Enamel, 0.2″ Long
L2 — 3–1/2 Turns, 0.310″ ID, #18 AWG Enamel, 0.25″ Long
L3 — 20 Turns, #20 AWG Enamel Wound on R5
L4 — Ferroxcube VK–200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
R5 — 1.0 MΩ, 2.0 W Carbon
Board — G10, 62 mils

Figure 1. 150 MHz Test Circuit

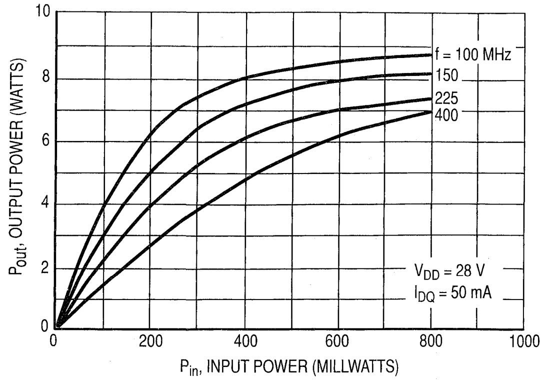


Figure 2. Output Power versus Input Power

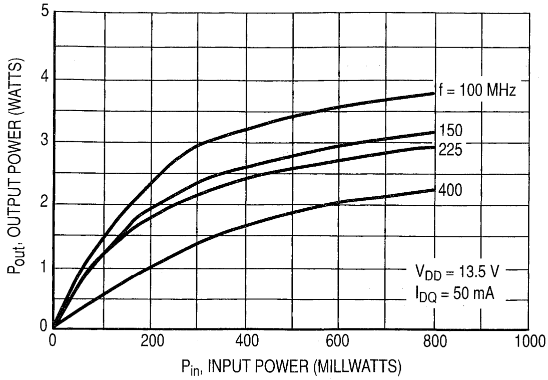


Figure 3. Output Power versus Input Power

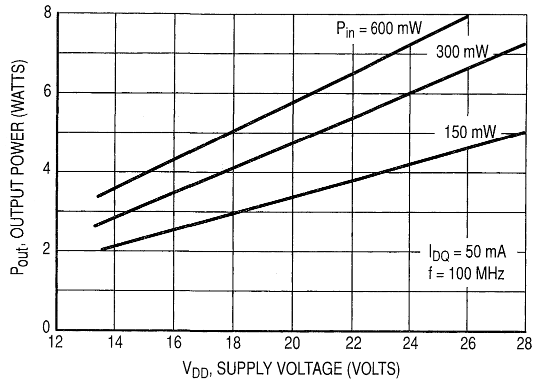


Figure 4. Output Power versus Supply Voltage

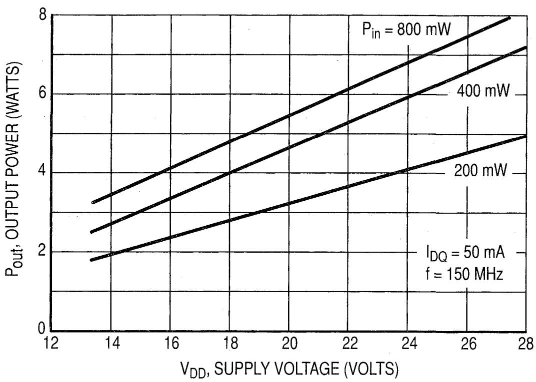


Figure 5. Output Power versus Supply Voltage

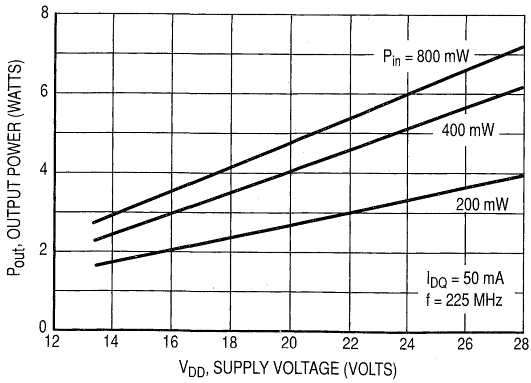


Figure 6. Output Power versus Supply Voltage

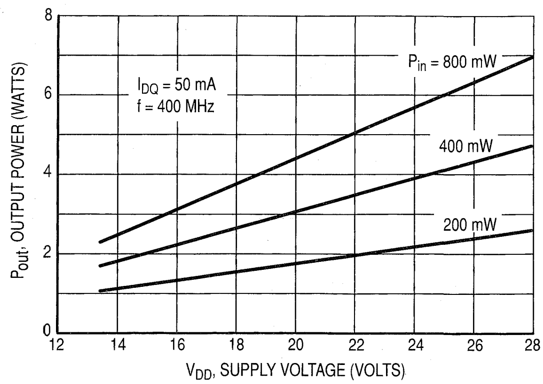


Figure 7. Output Power versus Supply Voltage

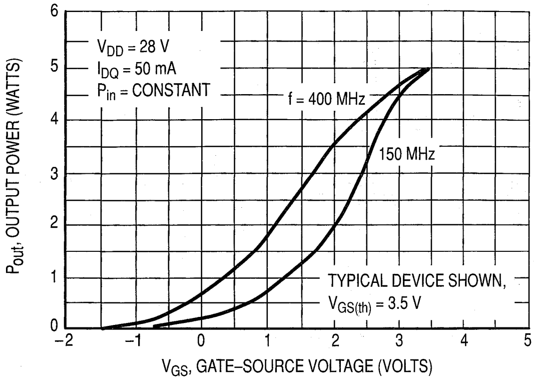


Figure 8. Output Power versus Gate Voltage

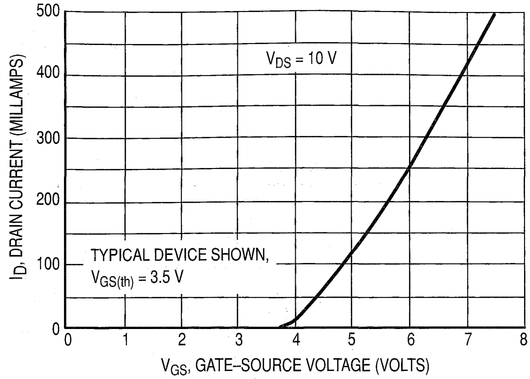


Figure 9. Drain Current versus Gate Voltage (Transfer Characteristics)

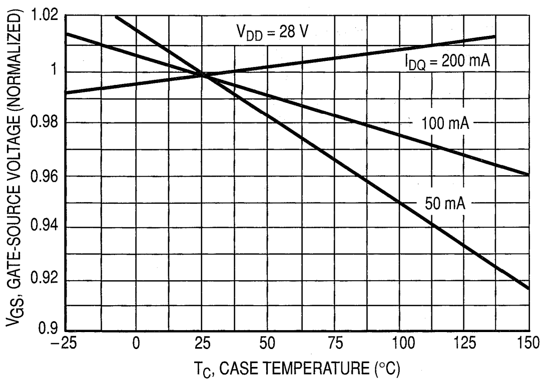


Figure 10. Gate–Source Voltage versus Case Temperature

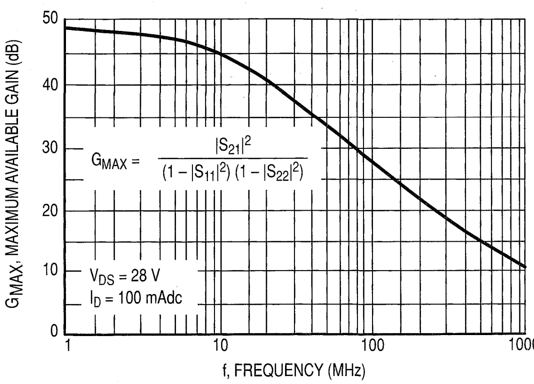


Figure 11. Maximum Available Gain versus Frequency

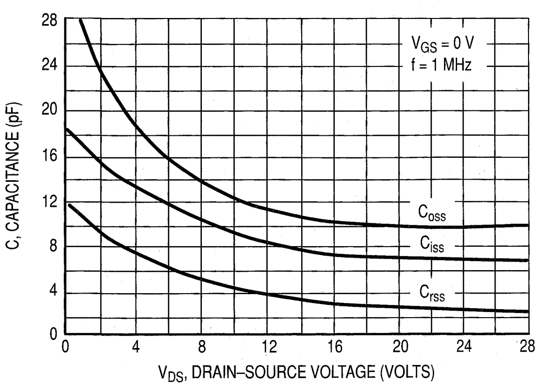


Figure 12. Capacitance versus Voltage

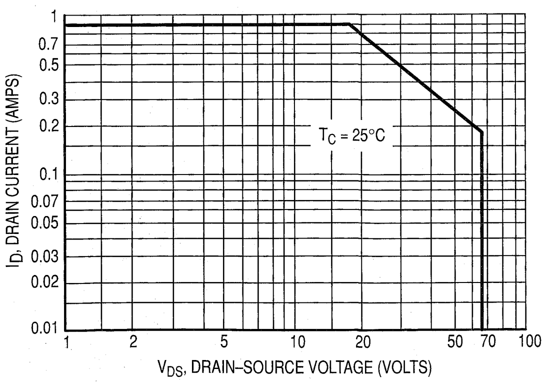
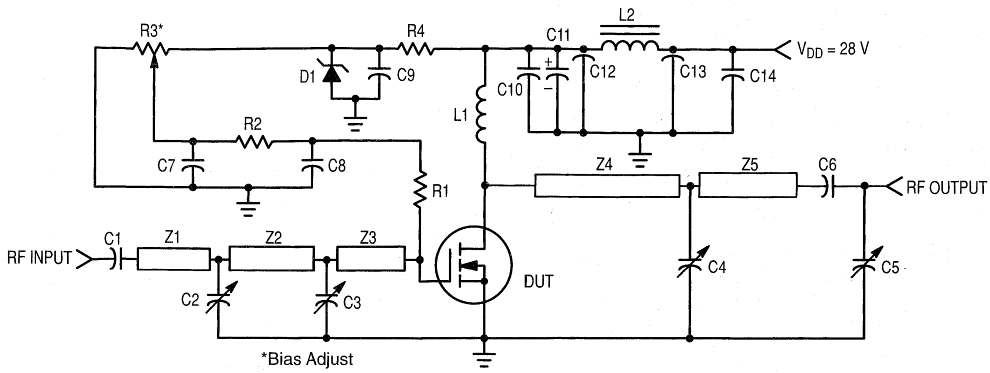
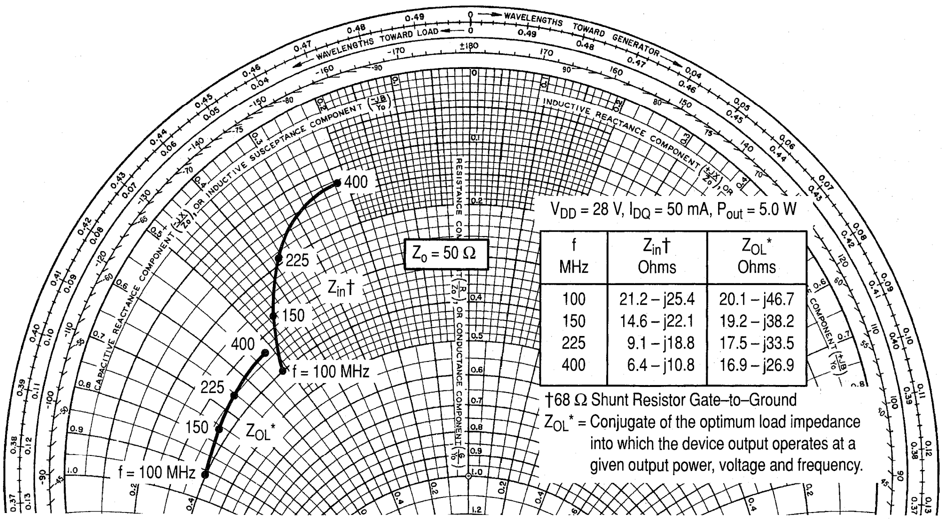


Figure 13. Maximum Rated Forward Biased Safe Operating Area



C1, C6 — 270 pF, ATC 100 mils
C2, C3, C4, C5 — 0–20 pF Johanson
C7, C9, C10, C14 — 0.1 μF Erie Redcap, 50 V
C8 — 0.001 μF
C11 — 10 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 6 Turns, 1/4″ ID, #20 AWG Enamel
L2 — Ferroxcube VK–200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
Z1 — 1.4″ x 0.166″ Microstrip
Z2 — 1.1″ x 0.166″ Microstrip
Z3 — 0.95″ x 0.166″ Microstrip
Z4 — 2.2″ x 0.166″ Microstrip
Z5 — 0.85″ x 0.166″ Microstrip
Board — Glass Teflon, 62 mils

Figure 14. 400 MHz Test Circuit



f MHz	Z_{in}† Ohms	Z_{OL}* Ohms
100	21.2 – j25.4	20.1 – j46.7
150	14.6 – j22.1	19.2 – j38.2
225	9.1 – j18.8	17.5 – j33.5
400	6.4 – j10.8	16.9 – j26.9

Figure 15. Large–Signal Series Equivalent Input/Output Impedances, Z_{in}†, Z_{OL}*

f (MHz)	S11		S21		S12		S22	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1.0	0.989	−1.0	11.27	179	0.0014	89	0.954	−1.0
2.0	0.989	−2.0	11.27	179	0.0028	89	0.954	−2.0
5.0	0.988	−5.0	11.26	176	0.0069	86	0.954	−4.0
10	0.985	−10	11.20	173	0.014	83	0.951	−9.0
20	0.977	−20	10.99	166	0.027	76	0.938	−18
30	0.965	−30	10.66	159	0.039	69	0.918	−26
40	0.950	−39	10.25	153	0.051	63	0.895	−34
50	0.931	−47	9.777	147	0.060	57	0.867	−42
60	0.912	−53	9.359	142	0.069	53	0.846	−49
70	0.892	−58	8.960	138	0.077	49	0.828	−56
80	0.874	−62	8.583	135	0.085	46	0.815	−62
90	0.855	−66	8.190	131	0.091	43	0.801	−68
100	0.833	−70	7.808	128	0.096	40	0.785	−74
110	0.827	−73	7.661	125	0.101	38	0.784	−77
120	0.821	−76	7.515	122	0.107	36	0.784	−82
130	0.814	−79	7.368	119	0.113	34	0.784	−85
140	0.808	−82	7.222	116	0.119	32	0.783	−88
150	0.802	−86	7.075	114	0.125	31	0.783	−90
160	0.788	−89	6.810	112	0.127	30	0.780	−92
170	0.774	−92	6.540	110	0.128	28	0.774	−94
180	0.763	−94	6.220	108	0.130	26	0.762	−98
190	0.751	−97	5.903	106	0.132	24	0.760	−100
200	0.740	−100	5.784	104	0.134	23	0.758	−103
225	0.719	−104	5.334	100	0.136	20	0.757	−107
250	0.704	−108	4.904	97	0.139	19	0.758	−110
275	0.687	−113	4.551	92	0.141	16	0.757	−114
300	0.673	−117	4.219	89	0.141	14	0.750	−117
325	0.668	−120	3.978	86	0.142	12	0.757	−120
350	0.669	−123	3.737	83	0.142	10	0.766	−121
375	0.662	−125	3.519	80	0.143	9.0	0.768	−123
400	0.654	−127	3.325	77	0.142	8.0	0.772	−124
425	0.650	−129	3.170	75	0.140	7.0	0.772	−125
450	0.638	−131	3.048	72	0.141	6.0	0.783	−125
475	0.614	−132	2.898	71	0.136	6.0	0.786	−126
500	0.641	−133	2.833	68	0.136	5.0	0.795	−127
525	0.638	−135	2.709	66	0.135	5.0	0.801	−127
550	0.633	−137	2.574	64	0.133	4.0	0.802	−128
575	0.628	−138	2.481	62	0.131	5.0	0.805	−128
600	0.625	−140	2.408	60	0.129	5.0	0.814	−128

The Power RF characterization data were measured with a 68 ohm resistor shunting the MRF134 input port. The scattering parameters were measured on the MRF134 device alone with no external components.

(continued)

Table 1. Common Source Scattering Parameters
V_{DS} = 28 V, I_D = 100 mA

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
625	0.619	−142	2.334	58	0.128	5.0	0.818	−129
650	0.617	−144	2.259	56	0.125	6.0	0.824	−130
675	0.618	−146	2.192	55	0.123	7.0	0.834	−130
700	0.619	−147	2.124	53	0.122	8.0	0.851	−131
725	0.618	−150	2.061	51	0.120	9.0	0.859	−132
750	0.614	−152	1.983	49	0.118	11	0.857	−133
775	0.609	−154	1.908	48	0.119	13	0.865	−133
800	0.562	−155	1.877	49	0.118	15	0.872	−133
825	0.587	−156	1.869	46	0.119	16	0.869	−134
850	0.593	−158	1.794	44	0.118	18	0.875	−135
875	0.597	−160	1.749	43	0.119	18	0.881	−135
900	0.598	−162	1.700	41	0.118	18	0.889	−136
925	0.592	−164	1.641	40	0.115	18	0.888	−138
950	0.588	−166	1.590	39	0.112	20	0.877	−138
975	0.586	−168	1.572	39	0.108	23	0.864	−137
1000	0.590	−171	1.551	37	0.107	28	0.863	−137

The Power RF characterization data were measured with a 68 ohm resistor shunting the MRF134 input port. The scattering parameters were measurd on the MRF134 device alone with no external components.

Table 1. Common Source Scattering Parameters (continued)
V_{DS} = 28 V, I_D = 100 mA

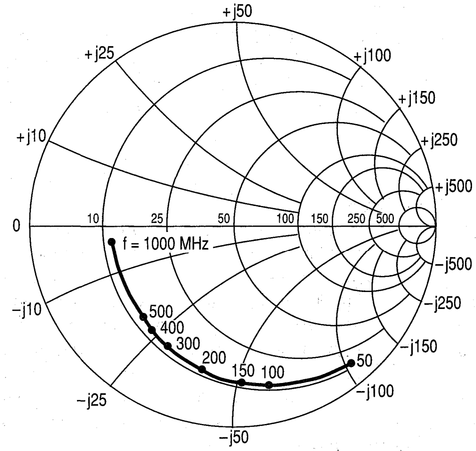


Figure 16. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 100 mA

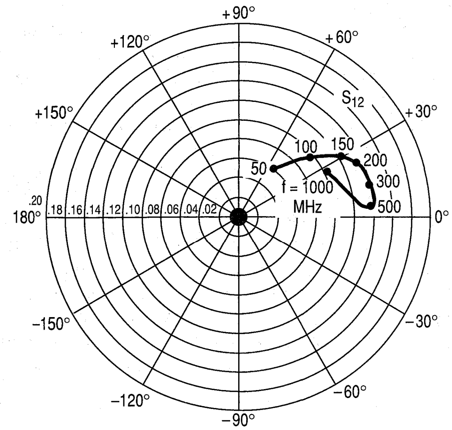


Figure 17. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 100 mA

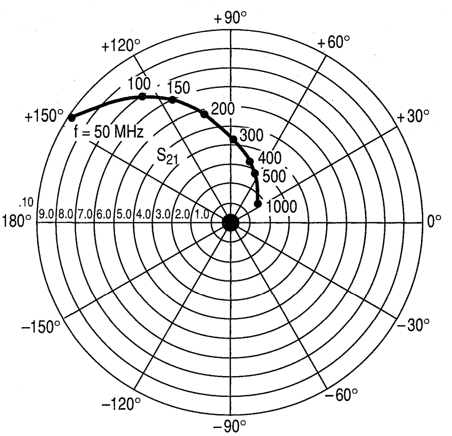


Figure 18. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 100 mA

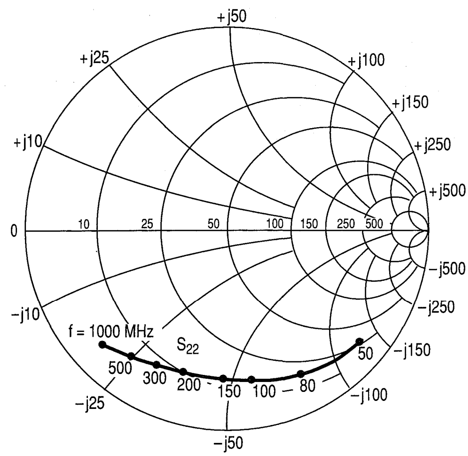


Figure 19. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 100 mA

DESIGN CONSIDERATIONS

The MRF134 is a RF power N–Channel enhancement mode field–effect transistor (FET) designed especially for VHF power amplifier and oscillator applications. Motorola RF MOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove vertical power FETs.

Motorola Application Note AN–211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF134 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF134 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF134 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF134. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF134, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The MRF134 was characterized with a 68–ohm input shunt loading resistor. Two port parameter stability analysis with the MRF134 s–parameters provides a useful–tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A for a discussion of two port network theory and stability.

Input resistive loading is not feasible in low noise applications. The MRF134 noise figure data was generated in a circuit with drain loading and a low loss input network.

The RF MOSFET Line
RF Power Field-Effect Transistors
N-Channel Enhancement-Mode MOSFETs

MRF136
MRF136Y

**15 W, 30 W, to 400 MHz
N–CHANNEL
MOS BROADBAND
RF POWER FETs**

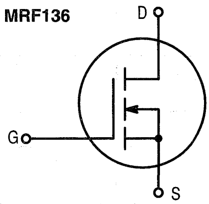
. . . designed for wideband large–signal amplifier and oscillator applications up to 400 MHz range, in either single ended or push–pull configuration.

- Guaranteed 28 Volt, 150 MHz Performance

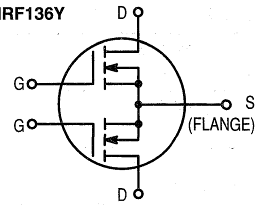
MRF136	**MRF136Y**
Output Power = 15 Watts	Output Power = 30 Watts
Narrowband Gain = 16 dB (Typ)	Broadband Gain = 14 dB (Typ)
Efficiency = 60% (Typical)	Efficiency = 54% (Typical)

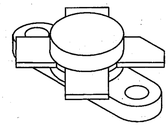
- Small–Signal and Large–Signal Characterization
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Space Saving Package For Push–Pull Circuit Applications — MRF136Y
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

MRF136

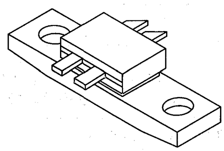


MRF136Y





**CASE 211–07, STYLE 2
MRF136**



**CASE 319B–02, STYLE 1
MRF136Y**

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		MRF136	MRF136Y	
Drain–Source Voltage	V_{DSS}	65	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	65	Vdc
Gate–Source Voltage	V_{GS}	±40		Vdc
Drain Current — Continuous	I_D	2.5	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	55 0.314	100 0.571	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150		°C
Operating Junction Temperature	T_J	200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
		MRF136	MRF136Y	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.2	1.75	°C/W

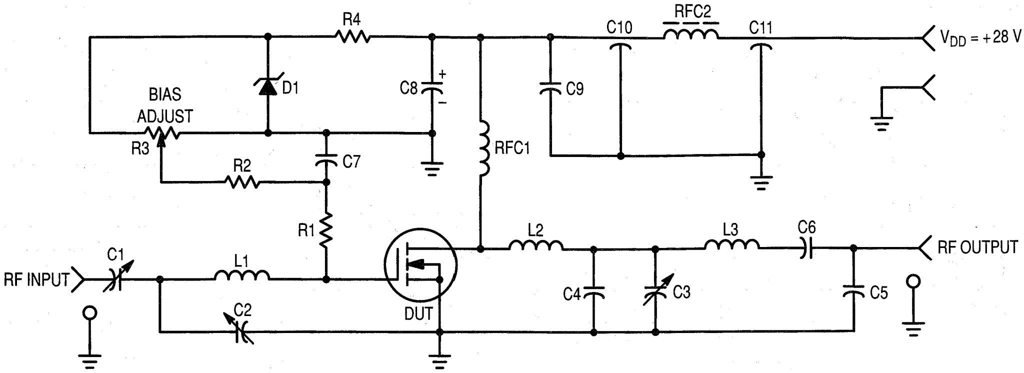
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero–Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.0	mAdc
Gate–Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 250 mA)	g_{fs}	250	400	—	mmhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	24	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	27	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	5.5	—	pF
FUNCTIONAL CHARACTERISTICS (2)					
Noise Figure MRF136 (V_{DS} = 28 Vdc, I_D = 500 mA, f = 150 MHz)	NF	—	1.0	—	dB
Common Source Power Gain (Figure 1) MRF136 (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA)	G_{ps}	13	16	—	dB
Common Source Power Gain (Figure 2) MRF136Y (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 100 mA)	G_{ps}	12	14	—	dB
Drain Efficiency (Figure 1) MRF136 (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA)	η	50	60	—	%
Drain Efficiency (Figure 2) MRF136Y (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 100 mA)	η	50	54	—	%
Electrical Ruggedness (Figure 1) MRF136 (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
Electrical Ruggedness (Figure 2) MRF136Y (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

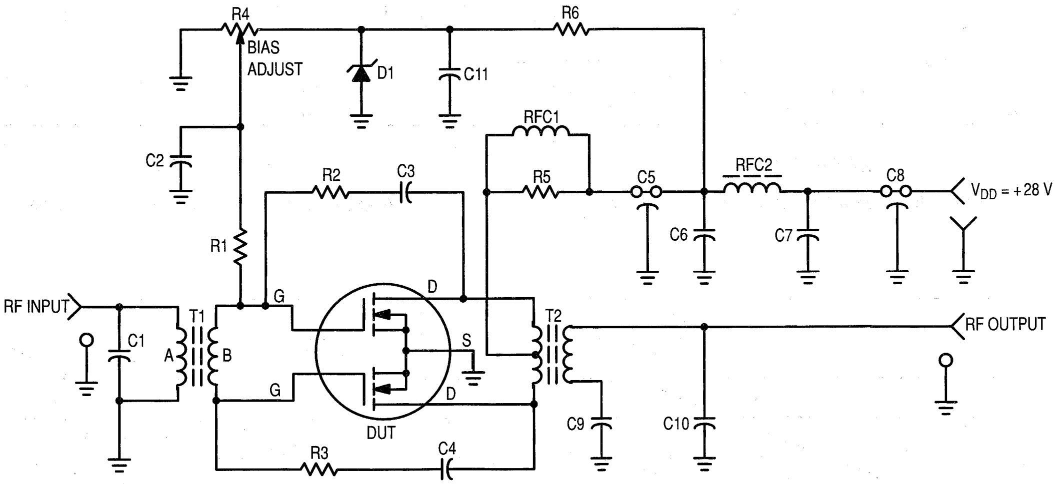
NOTES:
1. For MRF136Y, each side measured separately.
2. For MRF136Y measured in push–pull configuration.



C1, C2 — Arco 406, 15–115 pF or Equivalent
C3 — Arco 404, 8–60 pF or Equivalent
C4 — 43 pF Mini–Unelco or Equivalent
C5 — 24 pF Mini–Unelco or Equivalent
C6 — 680 pF, 100 Mils Chip
C7 — 0.01 μF Ceramic
C8 — 100 μF, 40 V
C9 — 0.1 μF Ceramic
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — 2 Turns, 0.29″ ID, #18 AWG, 0.10″ Long
L2 — 2 Turns, 0.23″ ID, #18 AWG, 0.10″ Long
L3 — 2–1/4 Turns, 0.29″ ID, #18 AWG, 0.125″ Long
RFC1 — 20 Turns, 0.30″ ID, #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK–200 — 19/4B
R1 — 27 Ω, 1 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ
R4 — 1.8 kΩ, 1/2 W
Board Material — 0.062″ G10, 1 oz. Cu Clad, Double Sided

Figure 1. 150 MHz Test Circuit (MRF136)



C1 — 5.0 pF
C2, C3, C4, C6, C7, C9, C11 — 0.1 μF Ceramic
C5, C8 — 680 pF Feedthru
C10 — 15 pF
D1 — 1N4740 Motorola Zener
RFC1 — 17 Turns, #24 AWG Wound on R5
RFC2 — Ferroxcube VK–200–19/4B or Equivalent
R1 — 10 kΩ, 1/4 W
R2, R3 — 560 Ω, 1/2 W
R4 — 10 Turns, 10 kΩ

R5 — 56 kΩ, 1 W
R6 — 1.6 kΩ, 1/4 W
T1 — Primary Winding — 3 Turns #28 Enameled Wire.
— Secondary Winding — 2 Turns #28 Enameled Wire. Both windings wound through a Fair/Rite Balun 65 core. Part #2865002402.
T2 — 1:1 Transformer Wound Bifilar — 2 Turns Twisted Pair #24 Enameled Wire through a Indiana General Balun Q1 core. Part #18006–1–Q1. Primary winding center tapped.
Board Material — 0.062″ G10, 1 oz. Cu Clad, Double Sided

Figure 2. 30–150 MHz Test Circuit (MRF136Y)

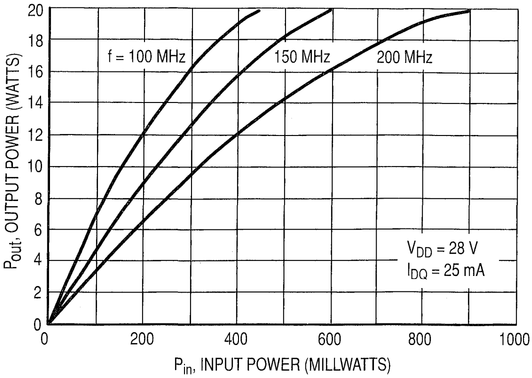


Figure 3. Output Power versus Input Power

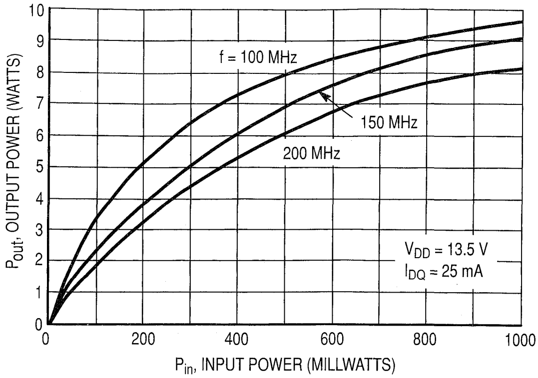


Figure 4. Output Power versus Input Power

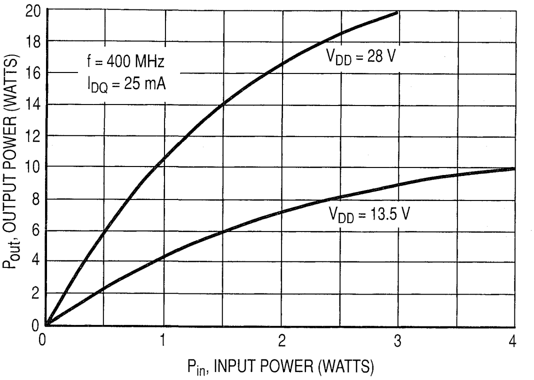


Figure 5. Output Power versus Input Power

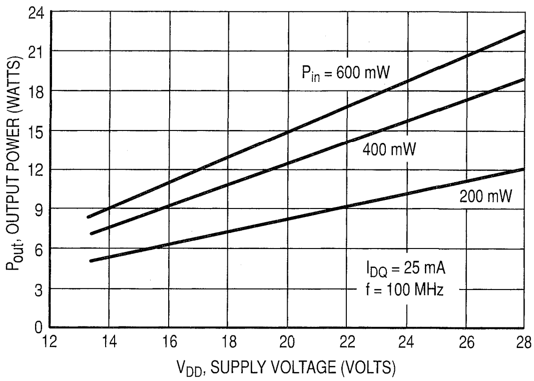


Figure 6. Output Power versus Supply Voltage

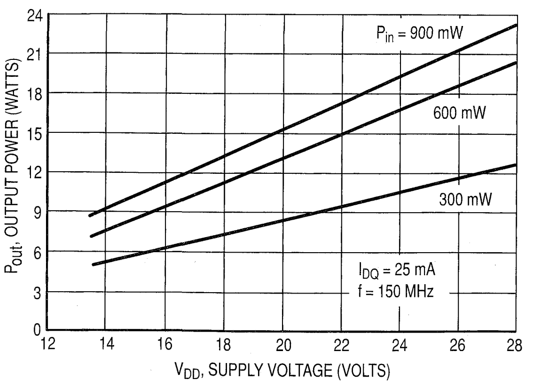


Figure 7. Output Power versus Supply Voltage

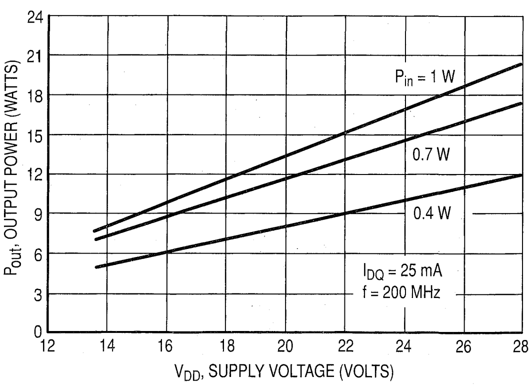


Figure 8. Output Power versus Supply Voltage

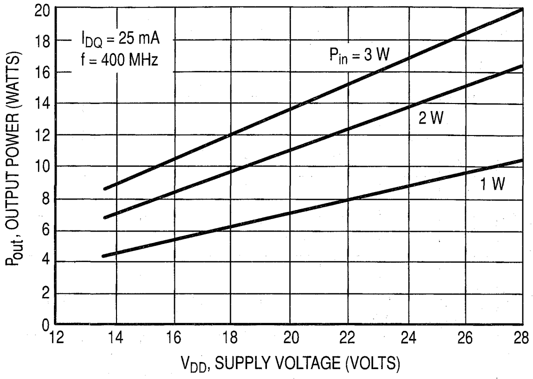


Figure 9. Output Power versus Supply Voltage MRF136

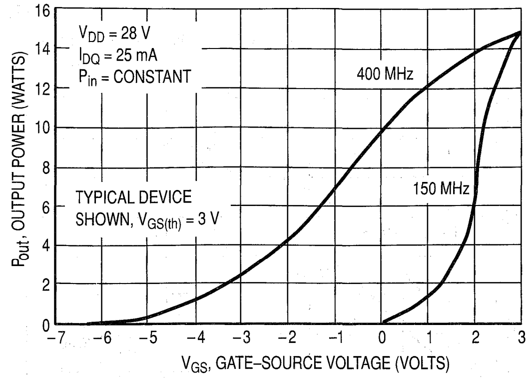


Figure 10. Output Power versus Gate Voltage MRF136

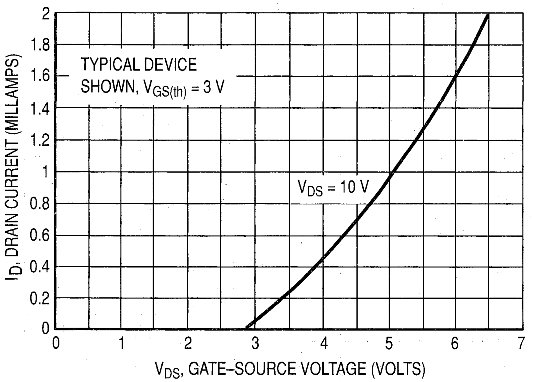


Figure 11. Drain Current versus Gate Voltage (Transfer Characteristics)* MRF136/MRF136Y

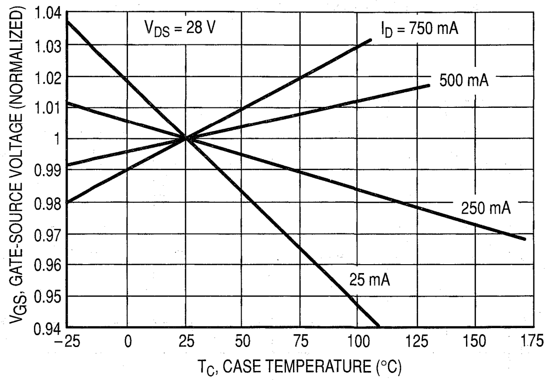


Figure 12. Gate–Source Voltage versus Case Temperature* MRF136/MRF136Y

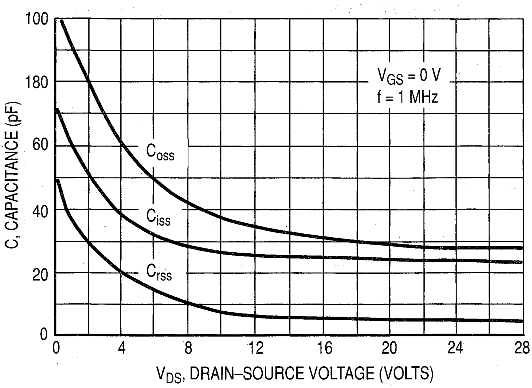


Figure 13. Capacitance versus Drain–Source Voltage* MRF136/MRF136Y

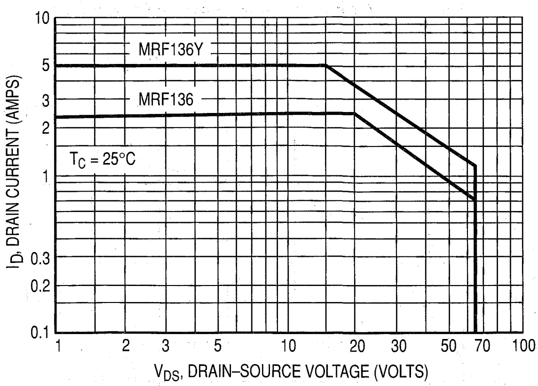


Figure 14. DC Safe Operating Area MRF136/MRF136Y

*Data shown applies to MRF136 and each half of MRF136Y.

MRF136Y
TYPICAL PERFORMANCE IN BROADBAND TEST CIRCUIT
(Refer to Figure 2)

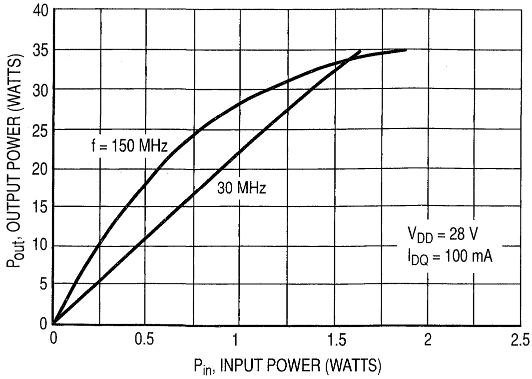


Figure 15. Output Power versus Input Power

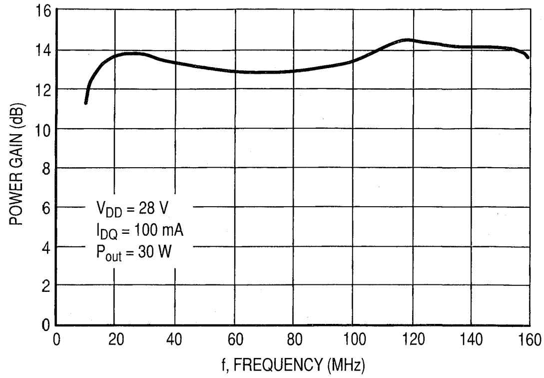


Figure 16. Power Gain versus Frequency

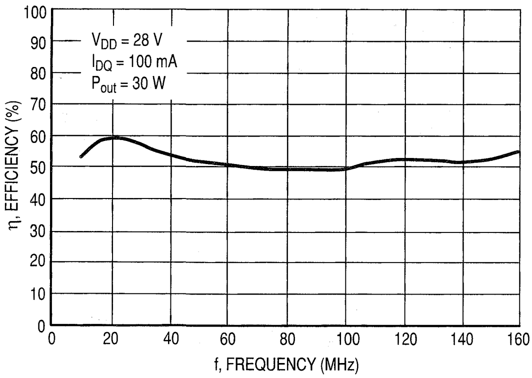


Figure 17. Drain Efficiency versus Frequency

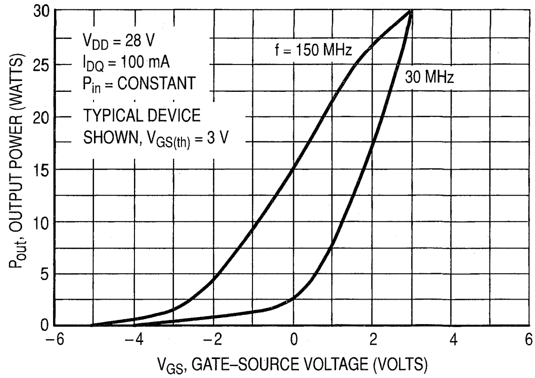


Figure 18. Output Power versus Gate Voltage

TYPICAL 400 MHz PERFORMANCE

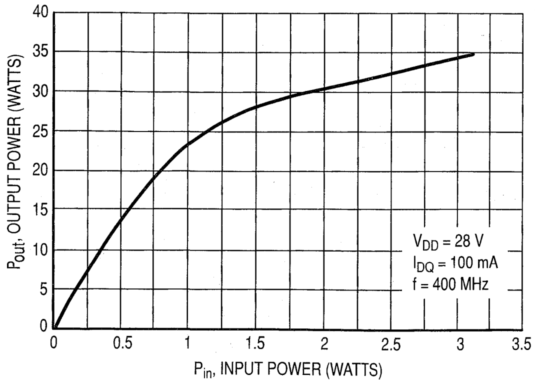


Figure 19. Output Power versus Input Power

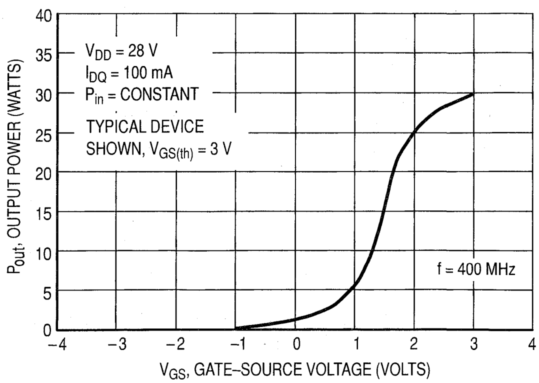


Figure 20. Output Power versus Gate Voltage

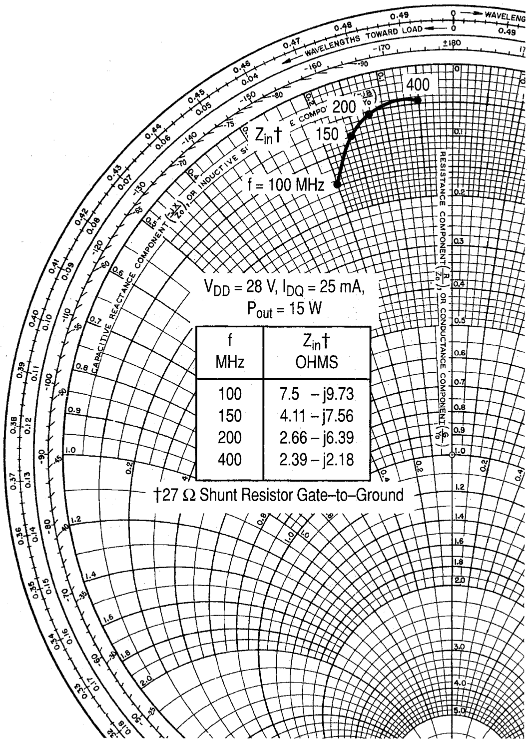


Figure 21. Large–Signal Series Equivalent Input Impedance, Z_{in}† MRF136

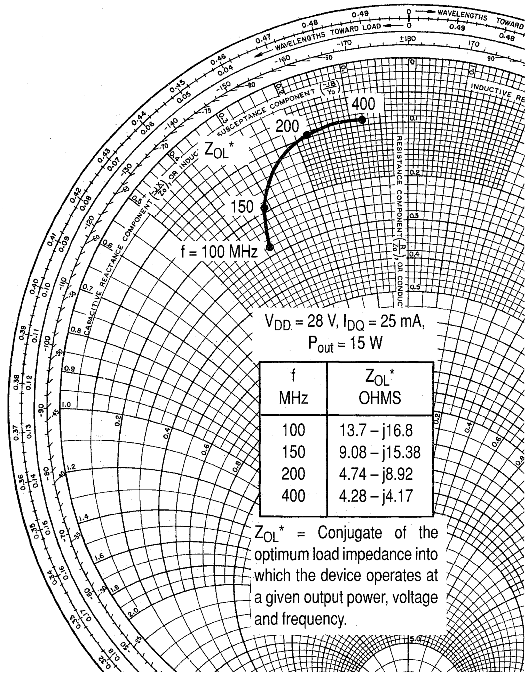


Figure 22. Large–Signal Series Equivalent Output Impedance, Z_{OL}* MRF136

Z_{in} & Z_{OL}* are given from drain–to–drain and gate–to–gate respectively.

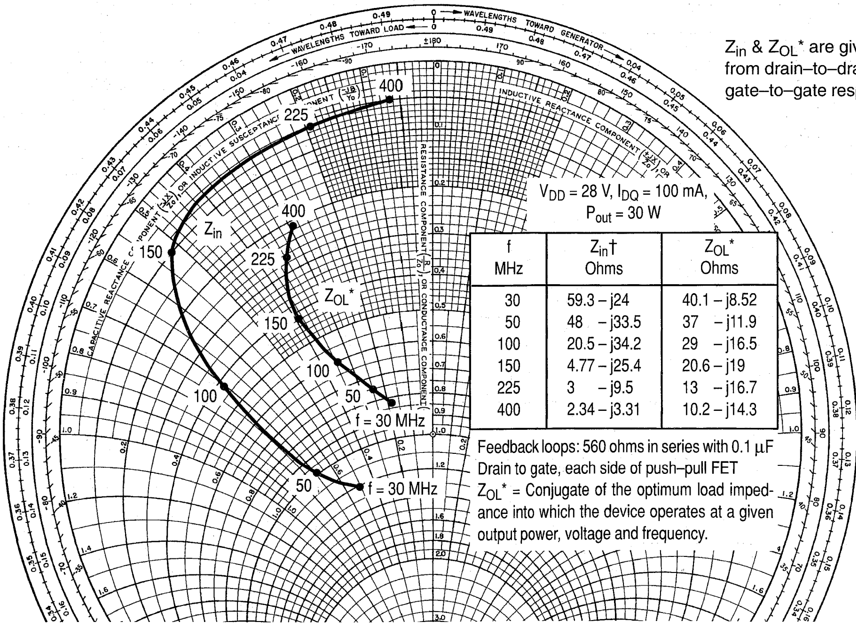


Figure 23. Input and Outut Impedance MRF136Y

f (MHz)	S11 |S11|	S11 ∠ φ	S21 |S21|	S21 ∠ φ	S12 |S12|	S12 ∠ φ	S22 |S22|	S22 ∠ φ
2.0	0.988	−11	41.19	173	0.006	67	0.729	−12
5.0	0.970	−27	40.07	164	0.014	62	0.720	−31
10	0.923	−52	35.94	149	0.026	54	0.714	−58
20	0.837	−88	27.23	129	0.040	36	0.690	−96
30	0.784	−111	20.75	117	0.046	27	0.684	−118
40	0.751	−125	16.49	108	0.048	22	0.680	−131
50	0.733	−135	13.41	103	0.050	19	0.679	−139
60	0.720	−142	11.43	99	0.050	16	0.678	−145
70	0.709	−147	9.871	96	0.050	14	0.679	−149
80	0.707	−152	8.663	93	0.051	13	0.683	−153
90	0.706	−155	7.784	91	0.051	13	0.682	−155
100	0.708	−157	7.008	88	0.051	13	0.680	−157
110	0.711	−159	6.435	86	0.051	14	0.681	−158
120	0.714	−161	5.899	85	0.051	15	0.682	−159
130	0.717	−163	5.439	82	0.052	16	0.684	−160
140	0.720	−164	5.068	80	0.052	17	0.684	−161
150	0.723	−165	4.709	80	0.052	18	0.686	−161
160	0.727	−166	4.455	78	0.052	18	0.690	−161
170	0.732	−167	4.200	77	0.052	18	0.694	−162
180	0.735	−168	3.967	75	0.052	19	0.699	−162
190	0.738	−169	3.756	74	0.052	19	0.703	−163
200	0.740	−170	3.545	73	0.052	20	0.706	−163
225	0.746	−171	3.140	69	0.053	22	0.717	−163
250	0.742	−172	2.783	67	0.053	25	0.724	−163
275	0.744	−173	2.540	64	0.054	27	0.724	−163
300	0.751	−174	2.323	60	0.055	29	0.736	−163
325	0.757	−175	2.140	58	0.058	32	0.749	−163
350	0.760	−176	1.963	54	0.059	35	0.758	−163
375	0.762	−177	1.838	52	0.062	38	0.768	−163
400	0.774	−179	1.696	50	0.065	41	0.783	−163
425	0.775	−179	1.590	48	0.068	43	0.793	−163
450	0.781	+179	1.493	46	0.071	46	0.805	−163
475	0.787	+177	1.415	43	0.074	47	0.813	−164
500	0.792	+176	1.332	40	0.079	48	0.825	−164
525	0.797	+175	1.259	38	0.083	50	0.831	−164
550	0.801	+175	1.185	37	0.088	51	0.843	−164
575	0.810	+174	1.145	36	0.094	52	0.855	−164
600	0.816	+173	1.091	34	0.101	52	0.869	−165
625	0.818	+171	1.041	32	0.106	53	0.871	−165
650	0.825	+170	0.994	30	0.112	53	0.884	−165
675	0.834	+169	0.962	29	0.119	53	0.890	−165
700	0.837	+168	0.922	27	0.127	53	0.906	−166
725	0.836	+167	0.879	25	0.133	52	0.909	−167
750	0.841	+166	0.838	25	0.140	53	0.917	−167
775	0.844	+165	0.824	24	0.148	52	0.933	−167
800	0.846	+163	0.785	21	0.154	50	0.941	−168

Table 1. Common Source Scattering Parameters
V_{DS} = 28 V, I_D = 0.5 A

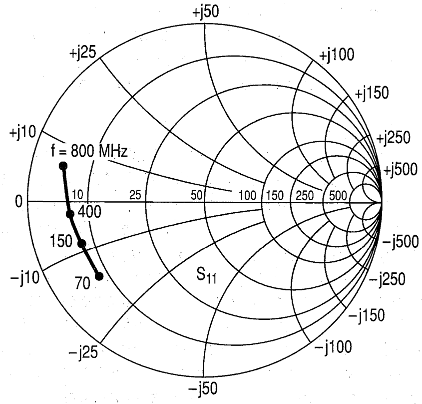


Figure 24. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

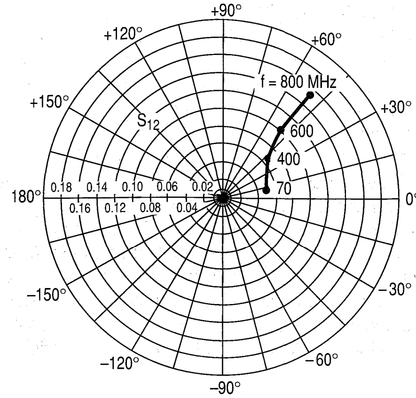


Figure 25. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

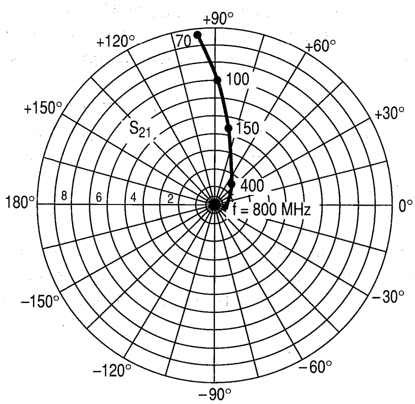


Figure 26. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

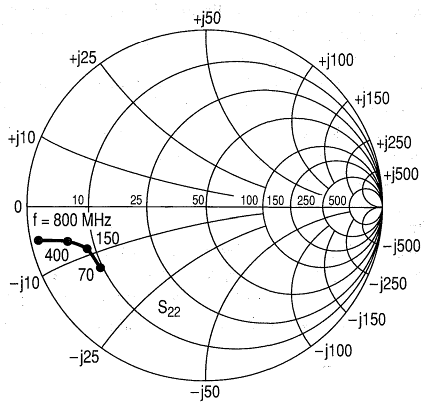


Figure 27. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

DESIGN CONSIDERATIONS

The MRF136 and MRF136Y are RF power N–Channel enhancement mode field–effect transistors (FETs) designed especially for HF and VHF power amplifier applications. Motorola RF MOS FETs feature planar design for optimum manufacturability.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF136 and MRF136Y are enhancement mode FETs and, therefore, do not conduct when drain voltage is applied without gate bias. A positive gate voltage causes drain current to flow (see Figure 11). RF power FETs require forward bias for optimum gain and power output. A Class AB condition with quiescent drain current (I_{DQ}) in the 25–100 mA range is sufficient for many applications. For special requirements such as linear amplification, I_{DQ} may have to be adjusted to optimize the critical parameters.

The MOS gate is a dc open circuit. Since the gate bias circuit does not have to deliver any current to the FET, a simple resistive divider arrangement may sometimes suffice for this function. Special applications may require more elaborate gate bias systems.

GAIN CONTROL

Power output of the MRF136 and MRF136Y may be controlled from rated values down to the milliwatt region (>20 dB reduction in power output with constant input power) by varying the dc gate voltage. This feature, not available in bipolar RF power devices, facilitates the incorporation of manual gain control, AGC/ALC and modulation schemes into system designs. A full range of power output control may require dc gate voltage excursions into the negative region.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for MRF136 and MRF136Y. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. Both small signal scattering parameters (MRF136 only) and large signal impedance parameters are provided. Large signal impedances should be used for network designs wherever possible. While the s parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is particularly useful at frequencies outside those presented in the large signal impedance plots.

RF power FETs are triode devices and are therefore not unilateral. This, coupled with the very high gain, yields a device capable of self oscillation. Stability may be achieved using techniques such as drain loading, input shunt resistive loading, or feedback. S parameter stability analysis can provide useful information in the selection of loading and/or feedback to insure stable operation. The MRF136 was characterized with a 27 ohm input shunt loading resistor, while the MRF136Y was characterized with a resistive feedback loop around each of its two active devices.

For further discussion of RF amplifier stability and the use of two port parameters in RF amplifier design, see Motorola Application Note AN215A on page 6–204 in the RF Device Data (DL110 Rev 1).

LOW NOISE OPERATION

Input resistive loading will degrade noise performance, and noise figure may vary significantly with gate driving impedance. A low loss input matching network with its gate impedance optimized for lowest noise is recommended.

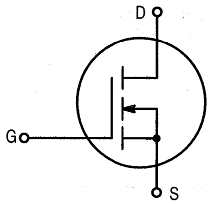
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode

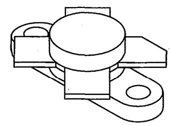
MRF137

. . . designed for wideband large–signal output and driver stages up to 400 MHz range.

- Guaranteed 28 Volt, 150 MHz Performance
  Output Power = 30 Watts
  Minimum Gain = 13 dB
  Efficiency — 60% (Typical)
- Small–Signal and Large–Signal Characterization
- Typical Performance at 400 MHz, 28 Vdc, 30 W
  Output = 7.7 dB Gain
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 1.5 dB (Typ) at 1.0 A, 150 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

30 W, to 400 MHz
N–CHANNEL MOS
BROADBAND RF POWER
FET





CASE 211–07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.571	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

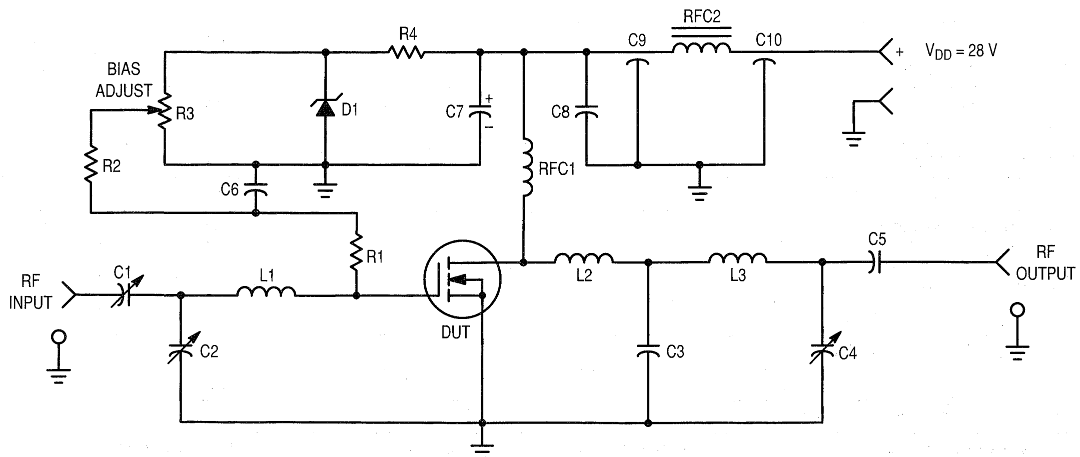
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	4.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 500 mA)	g_{fs}	500	750	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	48	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	54	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	11	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 1.0 A, f = 150 MHz)	NF	—	1.5	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 25 mA) f = 150 MHz (Figure 1) f = 400 MHz (Figure 14)	G_{ps}	13 —	16 7.7	— —	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 25 mA)	η	50	60	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			



C1 — Arco 403, 3.0–35 pF, or equivalent
C2 — Arco 406, 15–115 pF, or equivalent
C3 — 56 pF Mini–Unelco, or equivalent
C4 — Arco 404, 8.0–60 pF, or equivalent
C5 — 680 pF, 100 Mils Chip
C6 — 0.01 μF, 100 V, Disc Ceramic
C7 — 100 μF, 40 V
C8 — 0.1 μF, 50 V, Disc Ceramic
C9, C10 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — 2 Turns, 0.29″ ID, #18 AWG Enamel, Closewound
L2 — 1–1/4 Turns, 0.2″ ID, #18 AWG Enamel, Closewound
L3 — 2 Turns, 0.2″ ID, #18 AWG Enamel, Closewound
RFC1 — 20 Turns, 0.30″ ID, #20 AWG Enamel, Closewound
RFC2 — Ferroxcube VK–200 — 19/4B
R1 — 10 kΩ, 1/2 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ
R4 — 1.8 kΩ, 1/2 W
Board — G10, 62 Mils

Figure 1. 150 MHz Test Circuit

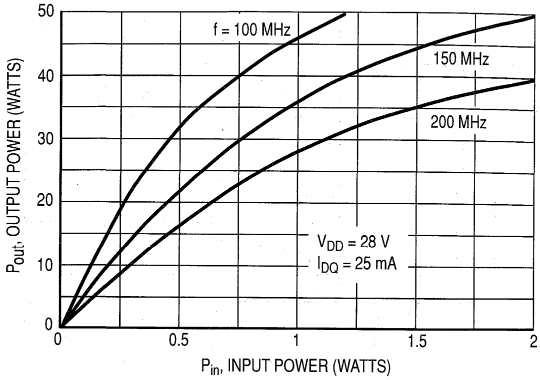


Figure 2. Output Power versus Input Power

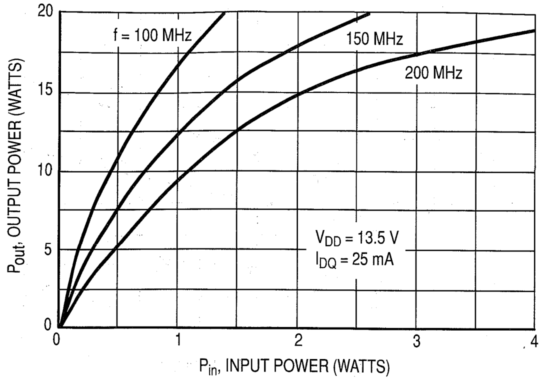


Figure 3. Output Power versus Input Power

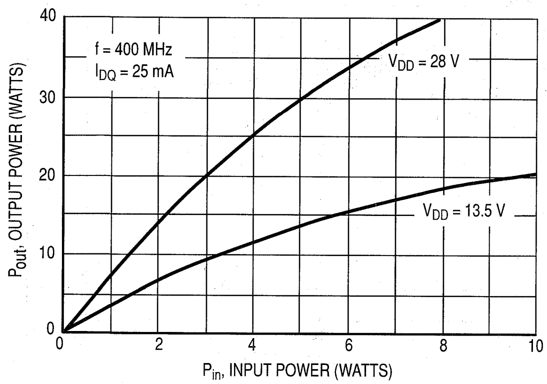


Figure 4. Output Power versus Input Power

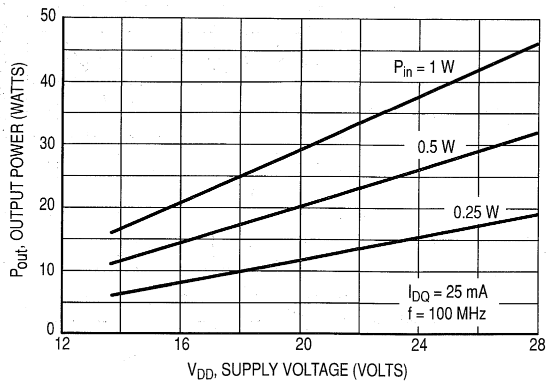


Figure 5. Output Power versus Supply Voltage

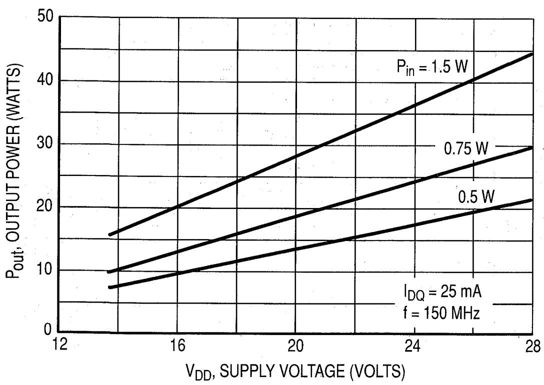


Figure 6. Output Power versus Supply Voltage

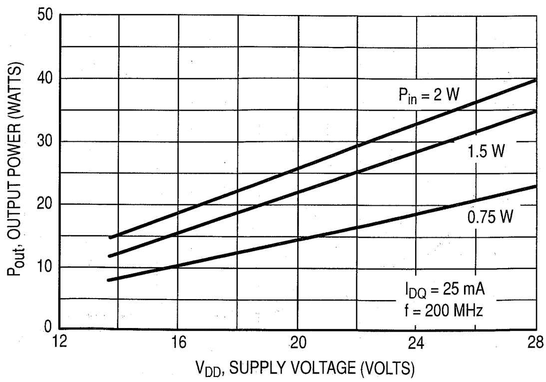


Figure 7. Output Power versus Supply Voltage

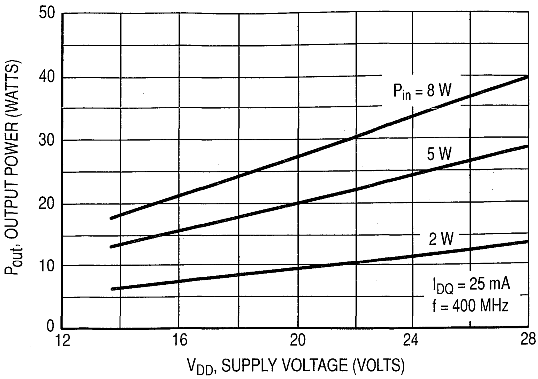


Figure 8. Output Power versus Supply Voltage

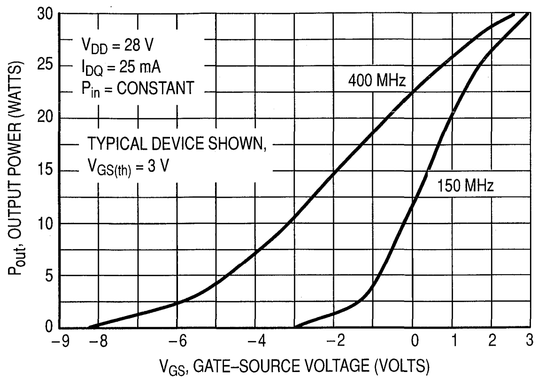


Figure 9. Output Power versus Gate Voltage

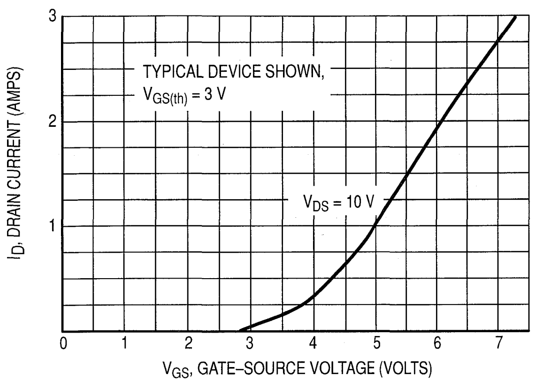


Figure 10. Drain Current versus Gate Voltage (Transfer Characteristics)

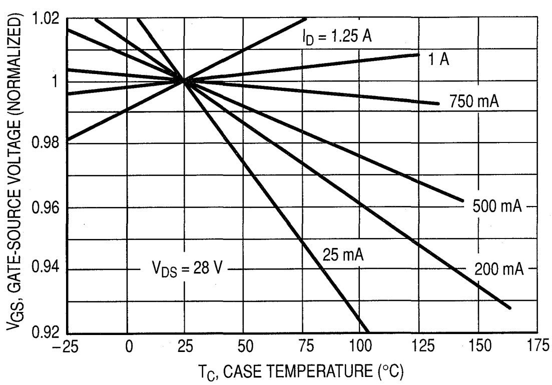


Figure 11. Gate Source Voltage versus Case Temperature

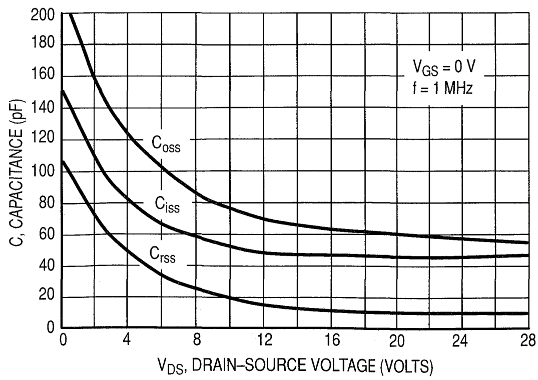


Figure 12. Capacitance versus Drain–Source Voltage

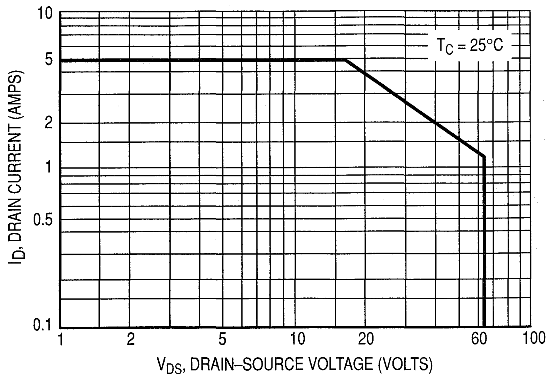
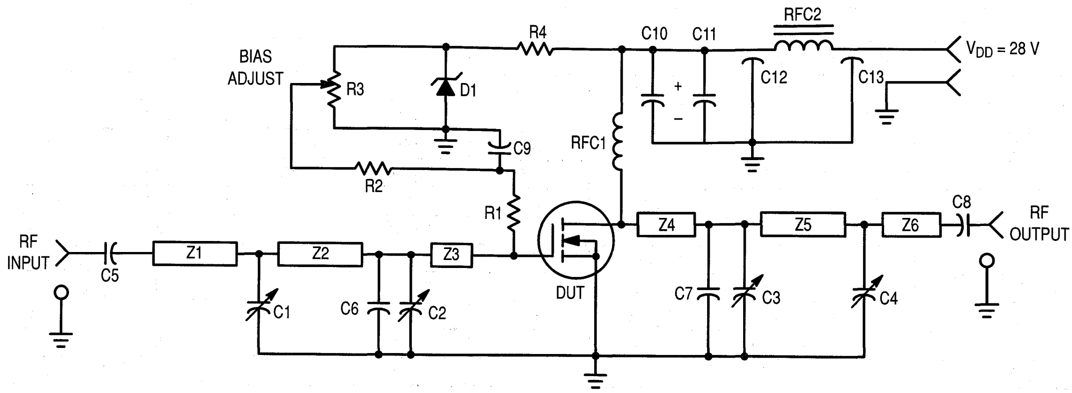
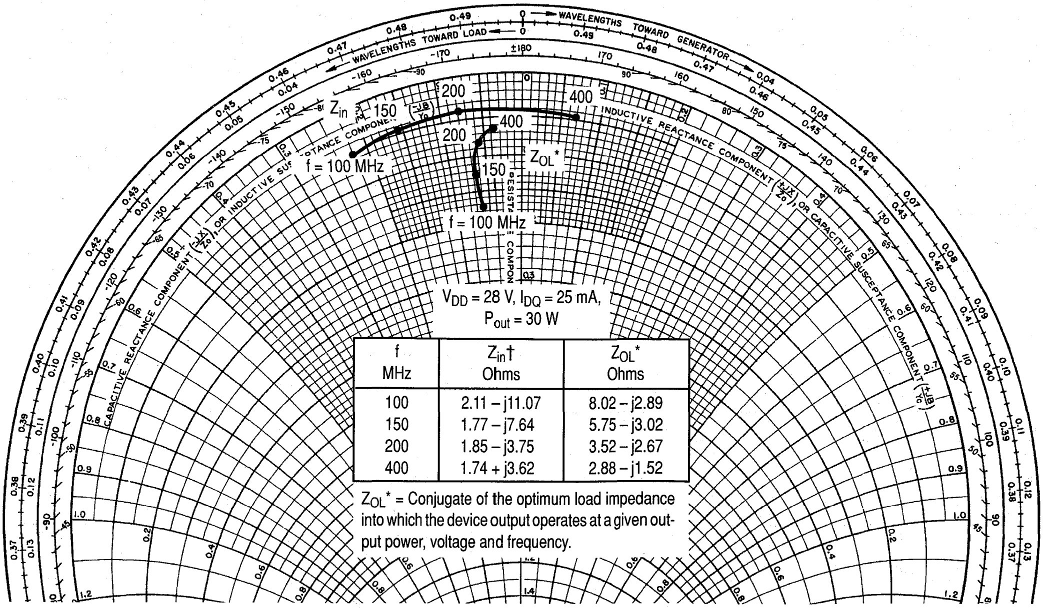


Figure 13. DC Safe Operating Area



C1, C2, C3, C4 — 0–20 pF Johanson, or equivalent
C5, C8 — 270 pF, 100 Mil Chip
C6, C7 — 24 pF Mini–Unelco, or equivalent
C9 — 0.01 μF, 100 V, Disc Ceramic
C10 — 100 μF, 40 V
C11 — 0.1 μF, 50 V, Disc Ceramic
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
R1, R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ
R4 — 1.8 kΩ, 1/2 W
Z1 — 2.9″ x 0.166″ Microstrip
Z2, Z4 — 0.35″ x 0.166″ Microstrip
Z3 — 0.40″ x 0.166″ Microstrip
Z5 — 1.05″ x 0.166″ Microstrip
Z6 — 1.9″ x 0.166″ Microstrip
RFC1 — 6 Turns, 0.300″ ID, #20 AWG Enamel, Closewound
RFC2 — Ferroxcube VK–200 — 19/4B
Board — Glass Teflon, 62 Mils

Figure 14. 400 MHz Test Circuit



f MHz	Z_{in}† Ohms	Z_{OL}* Ohms
100	2.11 – j11.07	8.02 – j2.89
150	1.77 – j7.64	5.75 – j3.02
200	1.85 – j3.75	3.52 – j2.67
400	1.74 + j3.62	2.88 – j1.52

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 15. Large–Signal Series Equivalent Input and Output Impedance, Z_{in}, Z_{OL}*

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
2.0	0.977	−32	59.48	163	0.011	67	0.661	−36
5.0	0.919	−70	48.67	142	0.024	44	0.692	−78
10	0.852	−109	33.50	122	0.032	29	0.747	−117
20	0.817	−140	19.05	106	0.037	16	0.768	−146
30	0.814	−153	13.11	99	0.038	14	0.774	−157
40	0.811	−159	9.88	95	0.038	13	0.782	−162
50	0.812	−164	7.98	92	0.038	12	0.787	−165
60	0.813	−166	6.66	89	0.038	12	0.787	−168
70	0.815	−168	5.708	86	0.038	11	0.787	−169
80	0.816	−170	5.003	84	0.038	11	0.787	−170
90	0.817	−171	4.560	83	0.038	12	0.787	−171
100	0.817	−172	4.170	81	0.039	13	0.787	−172
110	0.818	−173	3.670	80	0.039	13	0.788	−172
120	0.820	−173	3.420	79	0.039	13	0.788	−173
130	0.821	−173	3.170	79	0.039	13	0.788	−173
140	0.822	−174	2.980	78	0.039	13	0.788	−173
150	0.823	−175	2.826	77	0.039	14	0.788	−173
160	0.824	−175	2.650	76	0.039	14	0.790	−174
170	0.825	−176	2.438	75	0.039	14	0.792	−174
180	0.827	−176	2.325	73	0.039	15	0.793	−174
190	0.829	−177	2.175	72	0.039	16	0.796	−174
200	0.831	−177	2.084	71	0.039	16	0.799	−174
225	0.836	−178	1.824	69	0.039	18	0.805	−174
250	0.846	−178	1.621	66	0.039	21	0.816	−174
275	0.853	−179	1.462	64	0.039	23	0.822	−174
300	0.853	−179	1.319	61	0.040	25	0.833	−174
325	0.856	−179	1.194	59	0.040	27	0.828	−174
350	0.857	+179	1.089	56	0.040	30	0.842	−174
375	0.861	+179	1.014	54	0.042	32	0.849	−174
400	0.865	+178	0.927	51	0.043	35	0.856	−174
425	0.875	+178	0.876	49	0.045	37	0.866	−174
450	0.881	+178	0.810	46	0.046	40	0.870	−174
475	0.886	+177	0.755	44	0.046	43	0.875	−174
500	0.887	+177	0.694	41	0.051	43	0.888	−174
525	0.888	+176	0.677	39	0.052	43	0.890	−174
550	0.896	+176	0.625	36	0.055	45	0.898	−174
575	0.907	+175	0.603	34	0.058	45	0.913	−174
600	0.910	+175	0.585	32	0.061	45	0.918	−174
625	0.910	+174	0.563	30	0.065	45	0.945	−174
650	0.920	+174	0.543	28	0.069	46	0.952	−174
675	0.938	+173	0.533	26	0.074	47	0.974	−174
700	0.943	+171	0.515	24	0.078	47	0.958	−176
725	0.934	+170	0.491	22	0.079	46	0.953	−177
750	0.940	+170	0.475	22	0.084	48	0.943	−177
775	0.953	+169	0.477	21	0.090	48	0.957	−177
800	0.959	+168	0.467	17	0.093	48	0.957	−179

Table 1. Common Source Scattering Parameters
50 Ω System
V_{DS} = 28 V, I_D = 0.75 A

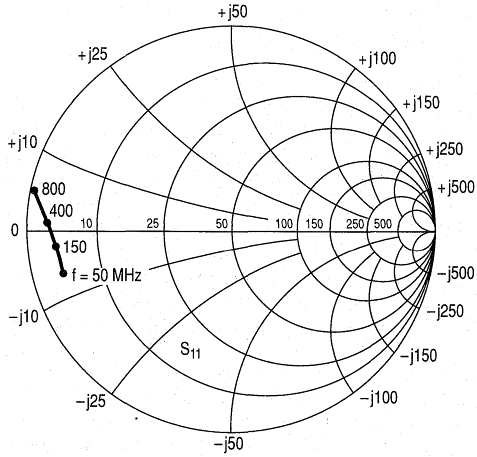


Figure 16. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.75 A

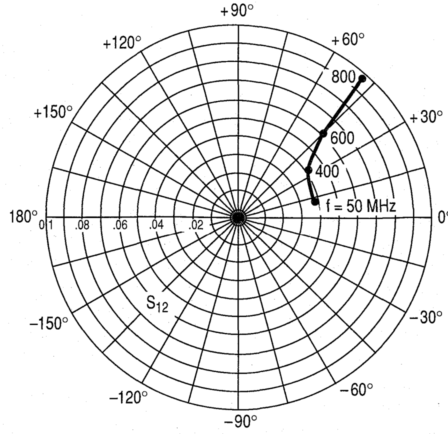


Figure 17. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.75 A

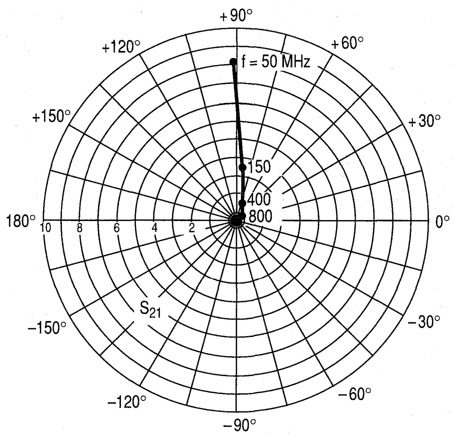


Figure 18. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.75 A

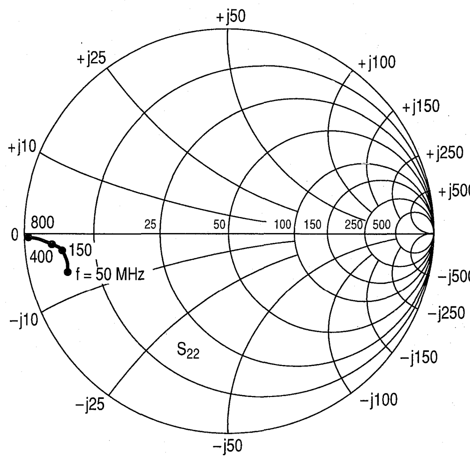


Figure 19. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.75 A

DESIGN CONSIDERATIONS

The MRF137 is a RF power N–Channel enhancement mode field–effect transistor (FET) designed especially for VHF power amplifier applications. Motorola RF MOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove vertical power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF137 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 10 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF137 was characterized at I_{DQ} = 25 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF137 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 9.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF137. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF137, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF137 s–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A for a discussion of two port network theory and stability.

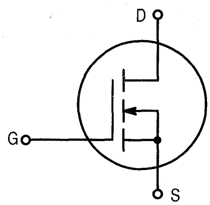
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode

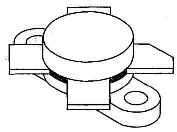
MRF140

Designed primarily for linear large–signal output stages up to 150 MHz frequency range.

- Specified 28 Volts, 30 MHz Characteristics
  Output Power = 150 Watts
  Power Gain = 15 dB (Typ)
  Efficiency = 40% (Typ)
- Superior High Order IMD
- $IMD_{(d3)}$ (150 W PEP) — –30 dB (Typ)
- $IMD_{(d11)}$ (150 W PEP) — –60 dB (Typ)
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR

**150 W, to 150 MHz
N–CHANNEL MOS
LINEAR RF POWER
FET**





CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage	V_{DGO}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.7	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

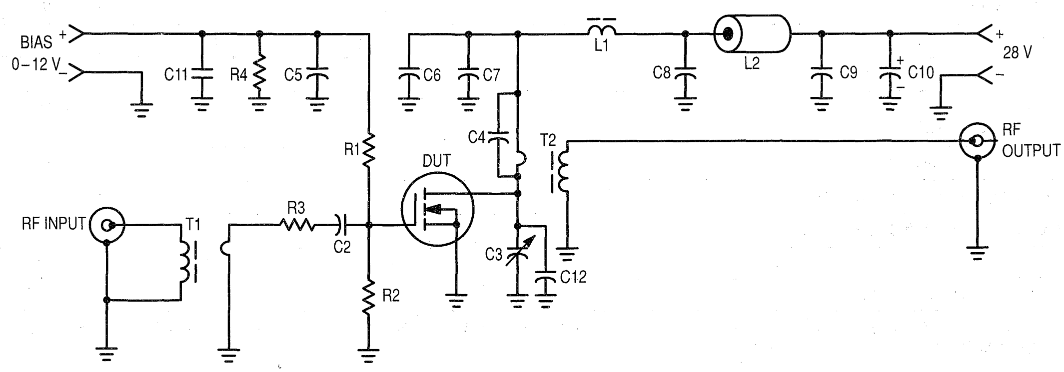
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 8

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1.0	µAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 Adc)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	4.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	450	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	400	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	75	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (30 MHz) (V_{DD} = 28 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA) (150 MHz)	G_{ps}	— —	15 6.0	— —	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_D (Max) = 6.5 A)	η	—	40	—	%
Intermodulation Distortion (1) (V_{DD} = 28 V, P_{out} = 150 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	−30 −60	— —	dB
Load Mismatch (V_{DD} = 28 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C2, C5, C6, C7, C8, C9 — 0.1 µF Ceramic Chip or Monolythic with Short Leads
C3 — Arco 469
C4 — 820 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 µF/100 V Electrolytic
C11 — 1 µF, 50 V, Tantalum
C12 — 330 pF, Dipped Mica (Short leads)

L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 µH
L2 — Ferrite Bead(s), 2.0 µH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 1.0 Ω/1.0 W Carbon or Parallel Two 2 Ω, 1/2 W Resistors
R4 — 1 kΩ/1/2 W Carbon
T1 — 16:1 Broadband Transformer
T2 — 1:25 Broadband Transformer

Figure 1. 30 MHz Test Circuit (Class AB)

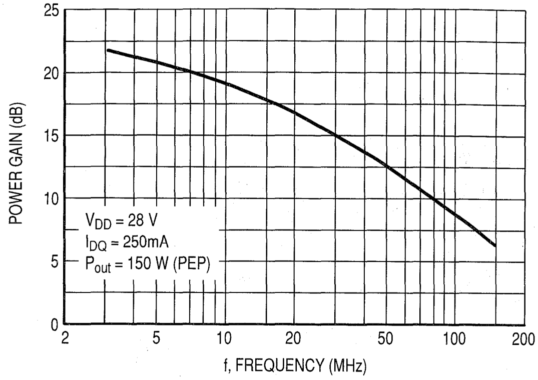


Figure 2. Power Gain versus Frequency

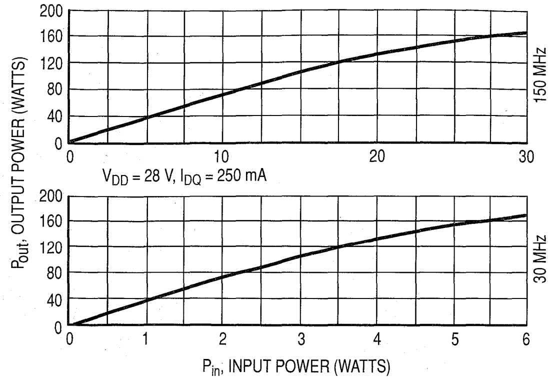


Figure 3. Output Power versus Input Power

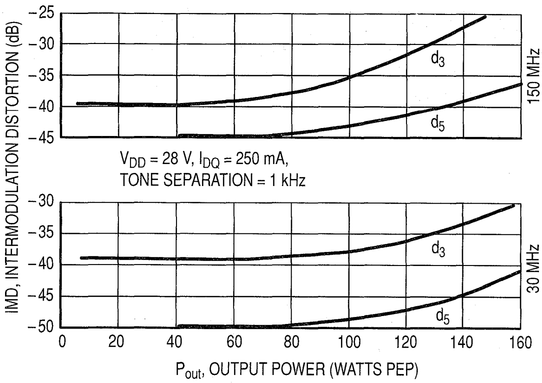


Figure 4. IMD versus P_{out}

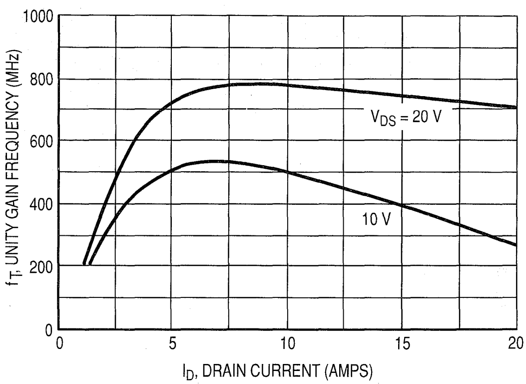


Figure 5. Common Source Unity Gain Frequency versus Drain Current

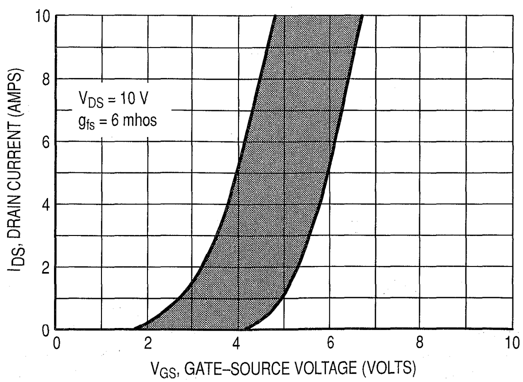
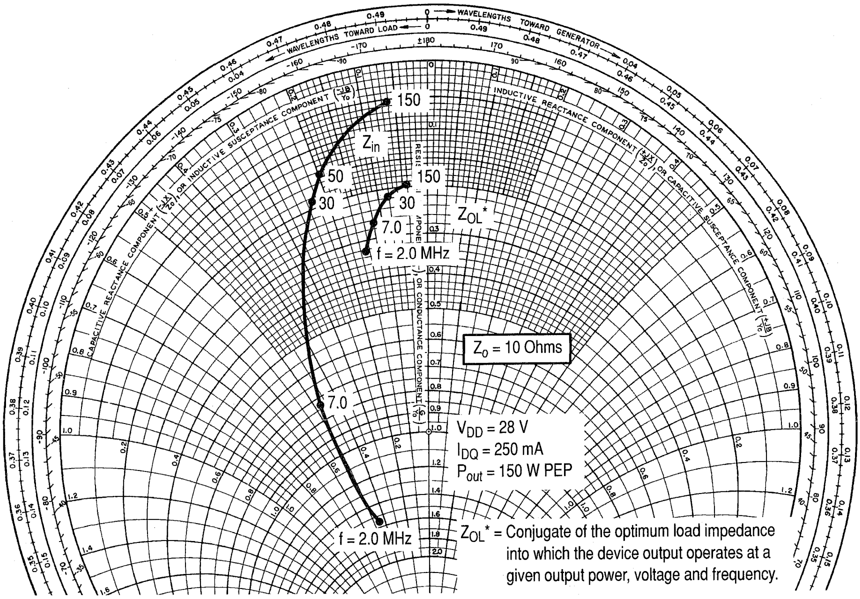
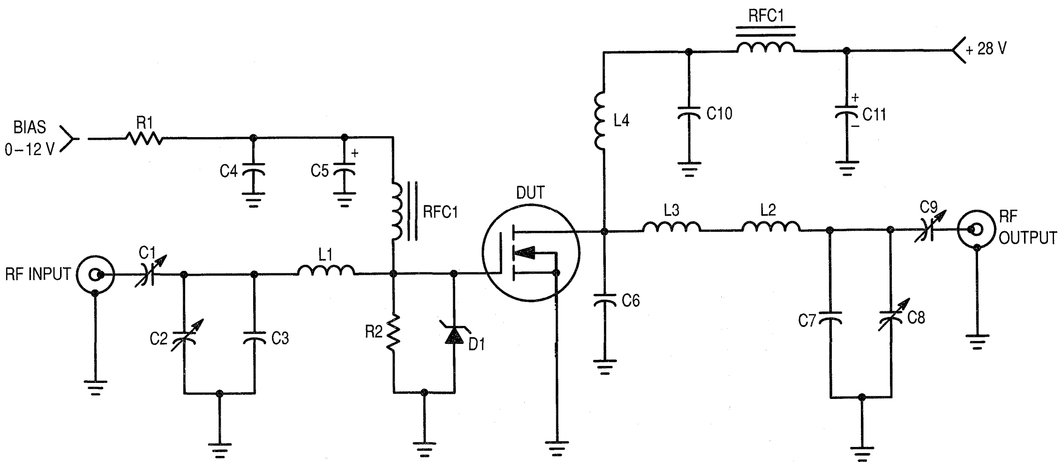


Figure 6. Gate Voltage versus Drain Current



NOTE: Gate Shunted by 25 Ohms.

Figure 7. Series Equivalent Impedance



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF, Unelco
C4 — 0.1 µF, Ceramic
C5 — 1.0 µF, 15 WV Tantalum
C6 — 15 pF, Unelco J101
C7 — 25 pF, Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 µF, Ceramic
C11 — 15 µF, 35 WV Electrolytic

L1 — 3/4″, #18 AWG into Hairpin
L2 — Printed Line, 0.200″ x 0.500″
L3 — 7/8″, #16 AWG into Hairpin
L4 — 2 Turns, #16 AWG, 5/16 ID
RFC1 — 5.6 µH, Molded Choke
RFC2 — VK200–4B
R1, R2 — 150 Ω, 1.0 W Carbon

Figure 8. 150 MHz Test Circuit (Class AB)

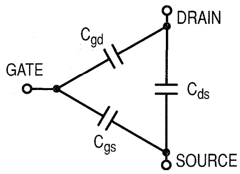
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

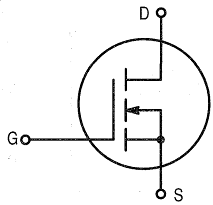
MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode MOSFET

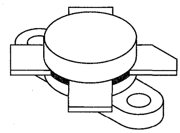
MRF141

Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 30 MHz, 28 V:
  Output Power — 150 W
  Gain — 18 dB (22 dB Typ)
  Efficiency — 40%
- Typical Performance at 175 MHz, 50 V:
  Output Power — 150 W
  Gain — 13 dB
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability



150 W, 28 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET



CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage	V_{DGO}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

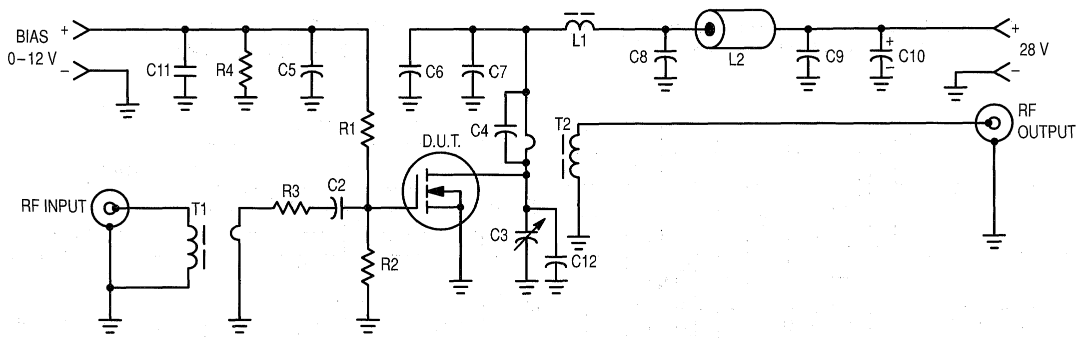
NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 8

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	420	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	35	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain, f = 30; 30.001 MHz (V_{DD} = 28 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA) f = 175 MHz	G_{ps}	16 —	20 10	— —	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 250 mA, I_D (Max) = 5.95 A)	η	40	45	—	%
Intermodulation Distortion (1) (V_{DD} = 28 V, P_{out} = 150 W (PEP), f = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	−30 −60	−28 —	dB
Load Mismatch (V_{DD} = 28 V, P_{out} = 150 W (PEP), f1 = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 28 V, P_{out} = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 4.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	23 −50 −75	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C2, C5, C6, C7, C8, C9 — 0.1 μF Ceramic Chip or Monolythic with Short Leads
C3 — Arco 469
C4 — 820 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 μF/100 V Electrolytic
C11 — 1 μF, 50 V, Tantalum
C12 — 330 pF, Dipped Mica (Short leads)

L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 μH
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 1.0 Ω/1.0 W Carbon or Parallel Two 2 Ω, 1/2 W Resistors
R4 — 1 kΩ/1/2 W Carbon
T1 — 16:1 Broadband Transformer
T2 — 1:25 Broadband Transformer
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε_r = 5

Figure 1. 30 MHz Test Circuit (Class AB)

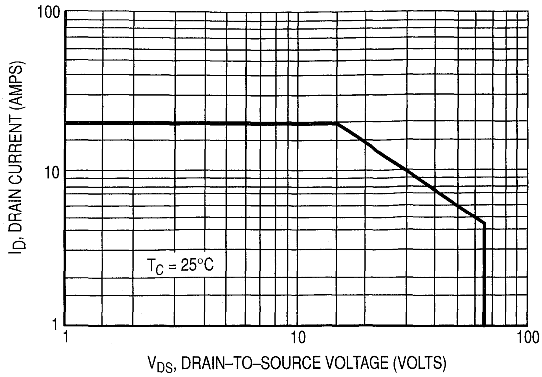


Figure 2. DC Safe Operating Area

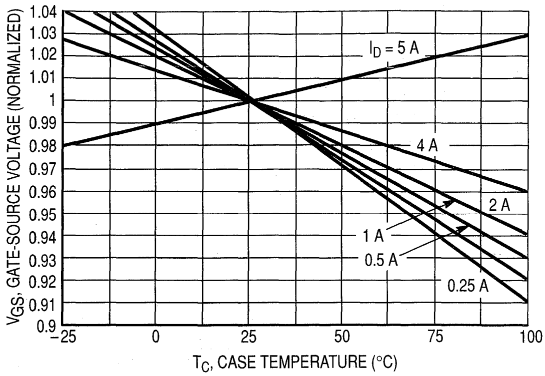


Figure 3. Gate–Source Voltage versus Case Temperature

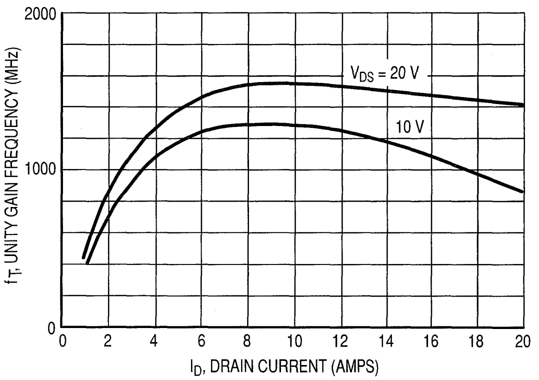


Figure 4. Common Source Unity Gain Frequency versus Drain Current

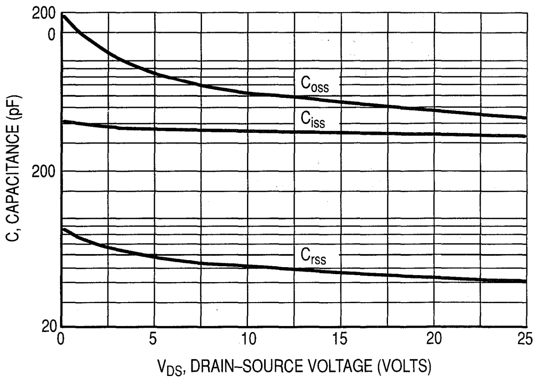


Figure 5. Capacitance versus Drain–Source Voltage

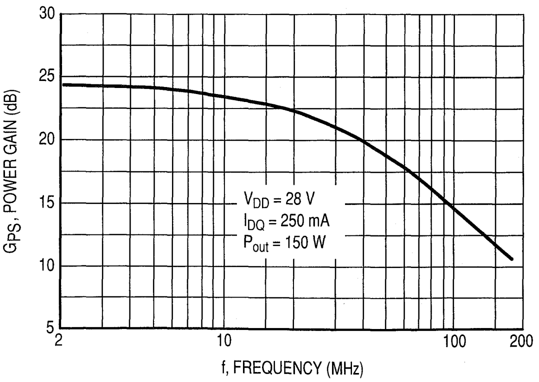


Figure 6. Power Gain versus Frequency

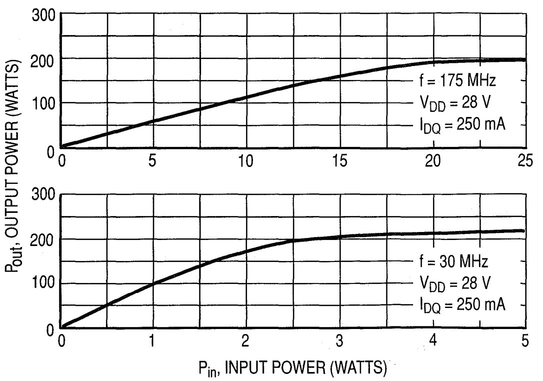


Figure 7. Output Power versus Input Power

TYPICAL CHARACTERISTICS

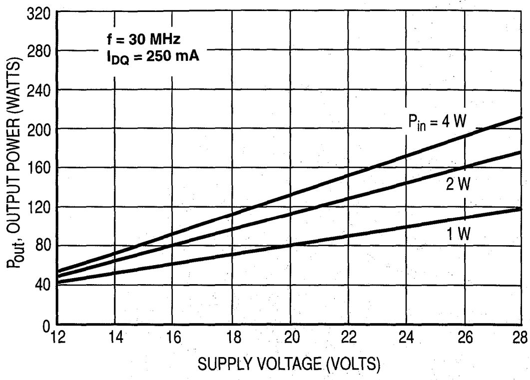


Figure 8. Output Power versus Supply Voltage

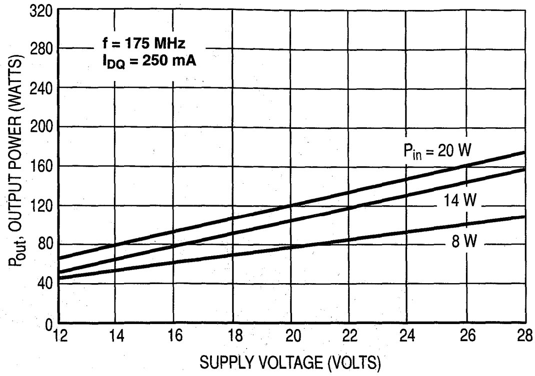


Figure 9. Output Power versus Supply Voltage

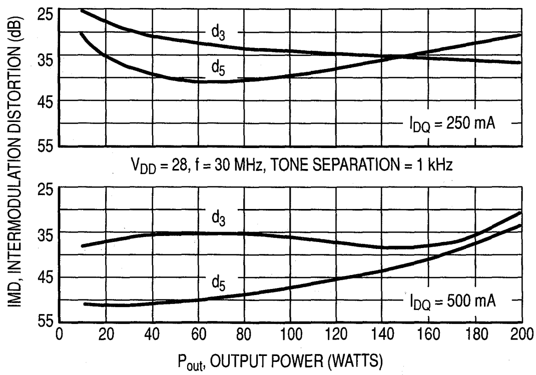


Figure 10. IMD versus P_{out} (PEP)

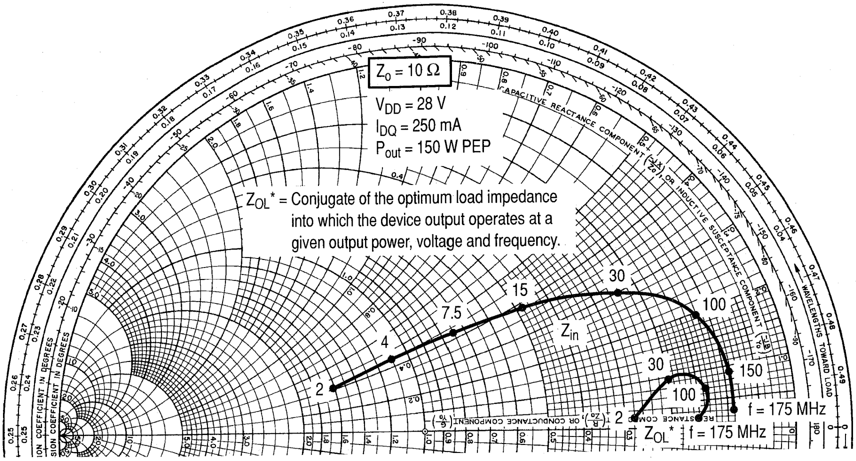
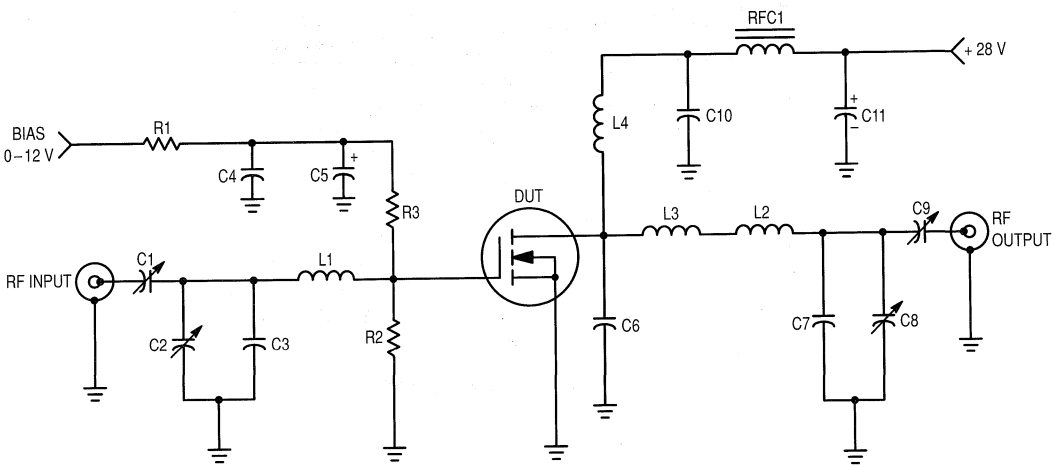


Figure 11. Input and Output Impedances



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF, Unelco
C4 — 0.1 µF, Ceramic
C5 — 1.0 µF, 15 WV Tantalum
C6 — 25 pF, Unelco J101
C7 — 25 pF, Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 µF, Ceramic
C11 — 15 µF, 35 WV Electrolytic

L1 — 3/4″, #18 AWG into Hairpin
L2 — Printed Line, 0.200″ x 0.500″
L3 — 7/8″, #16 AWG into Hairpin
L4 — 2 Turns, #16 AWG, 5/16 ID
RFC1 — 5.6 µH, Molded Choke
RFC2 — VK200–4B
R1 — 150 Ω, 1.0 W Carbon
R2 — 10 kΩ, 1/2 W Carbon
R3 — 120 Ω, 1/2 W Carbon

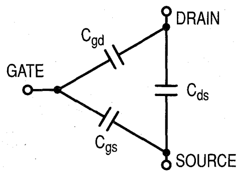
Figure 12. 175 MHz Test Circuit (Class AB)

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} = C_{gs}$
$C_{oss} = C_{gd} = C_{ds}$
$C_{rss} = C_{gd}$

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 4 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of this device is essentially capacitor. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the device due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — This device does not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF141 is an RF Power, MOS, N–channel enhancement mode field–effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF141 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF141 was characterized at I_{DQ} = 250 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

GAIN CONTROL

Power output of the MRF141 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

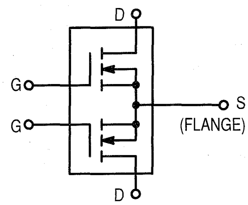
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode MOSFET

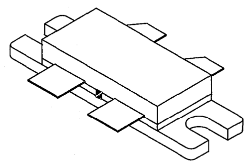
MRF141G

Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 175 MHz, 28 V:
  Output Power — 300 W
  Gain — 12 dB (14 dB Typ)
  Efficiency — 50%
- Low Thermal Resistance — 0.35°C/W
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability

300 W, 28 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET





CASE 375–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage	V_{DGO}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	32	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	500 2.85	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{θJC}$	0.35	°C/W

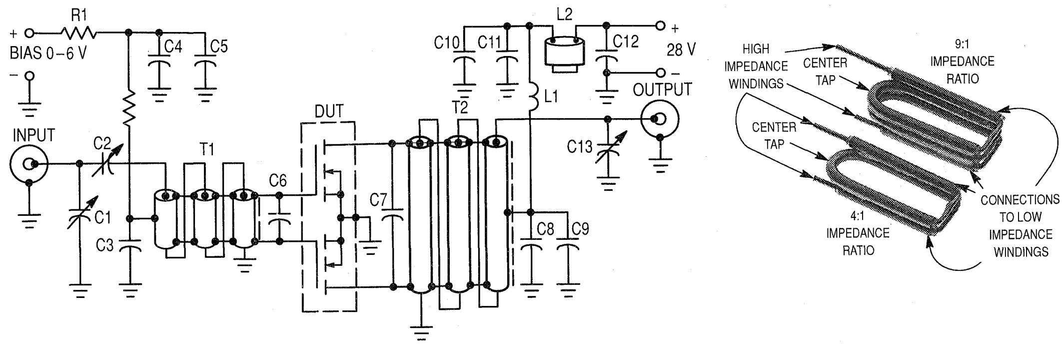
NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	420	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	35	—	pF
FUNCTIONAL TESTS (2)					
Common Source Amplifier Power Gain (V_{DD} = 28 V, P_{out} = 300 W, I_{DQ} = 500 mA, f = 175 MHz)	G_{ps}	12	14	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 300 W, f = 175 MHz, I_D (Max) = 21.4 A)	η	45	55	—	%
Load Mismatch (V_{DD} = 28 V, P_{out} = 300 W, I_{DQ} = 500 mA, f = 175 MHz, VSWR 5:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each side measured separately.
2. Measured in push–pull configuration.



C1 — Arco 402, 1.5–20 pF
C2 — Arco 406, 15–115 pF
C3, C4, C8, C9, C10 — 1000 pF Chip
C5, C11 — 0.1 μF Chip
C6 — 330 pF Chip
C7 — 200 pF and 180 pF Chips in Parallel
C12 — 0.47 μF Ceramic Chip, Kemet 1215 or Equivalent
C13 — Arco 403, 3.0–35 pF
L1 — 10 Turns AWG #16 Enameled Wire, Close Wound, 1/4″ I.D.
L2 — Ferrite Beads of Suitable Material for 1.5–2.0 μH Total Inductance
R1 — 100 Ohms, 1/2 W
R2 — 1.0 kOhm, 1/2 W

Unless Otherwise Noted, All Chip Capacitors are ATC Type 100 or Equivalent.

T1 — 9:1 RF Transformer. Can be made of 15–18 Ohms Semirigid Co–Ax, 62–90 Mils O.D.
T2 — 1:9 RF Transformer. Can be made of 15–18 Ohms Semirigid Co–Ax, 70–90 Mils O.D.

Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, $\varepsilon_r = 5$

NOTE: For stability, the input transformer T1 must be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

See pictures for construction details.

Figure 1. 175 MHz Test Circuit

TYPICAL CHARACTERISTICS

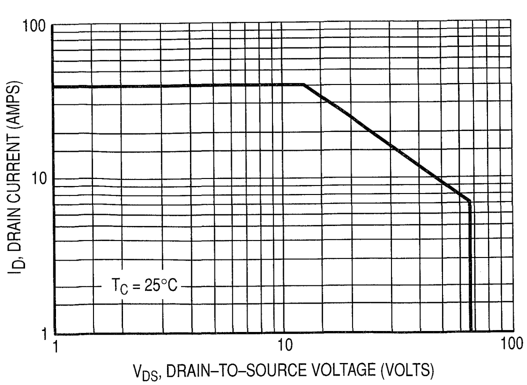


Figure 2. DC Safe Operating Area

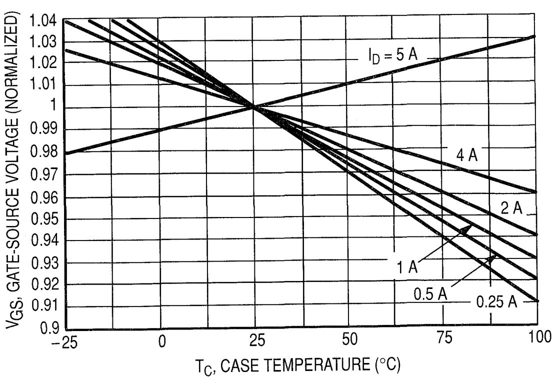
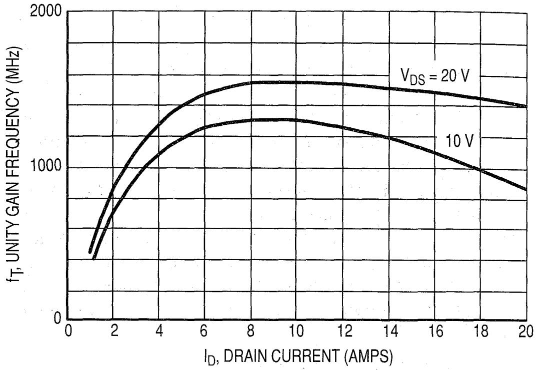


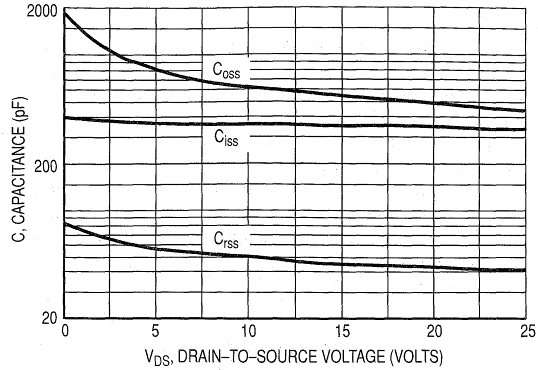
Figure 3. Gate–Source Voltage versus Case Temperature

TYPICAL CHARACTERISTICS



NOTE: Data shown applies to each half of MRF141G.

Figure 4. Common Source Unity Gain Frequency versus Drain Current



NOTE: Data shown applies to each half of MRF141G.

Figure 5. Capacitance versus Drain–Source Voltage

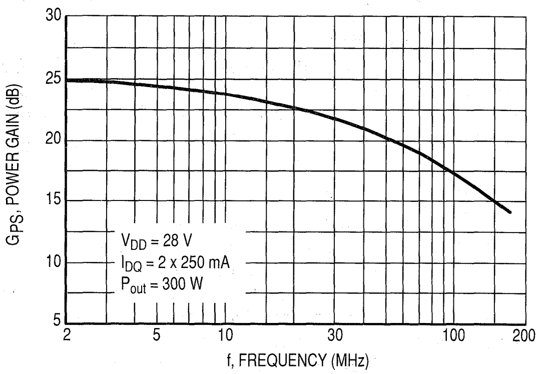


Figure 6. Power Gain versus Frequency

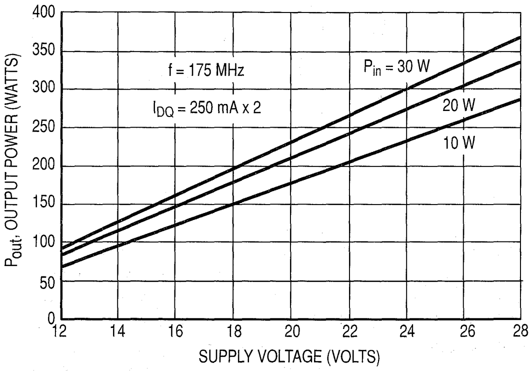
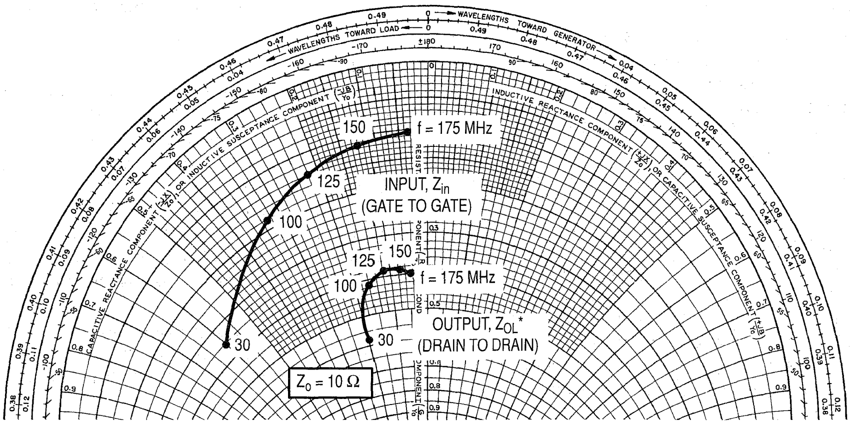


Figure 7. Output Power versus Supply Voltage



Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 8. Input and Output Impedances

RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

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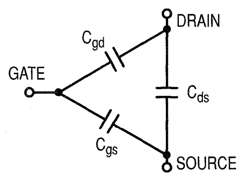

$C_{iss} = C_{gd} = C_{gs}$
$C_{oss} = C_{gd} = C_{ds}$
$C_{rss} = C_{gd}$

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 4 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

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HANDLING CONSIDERATIONS

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GAIN CONTROL

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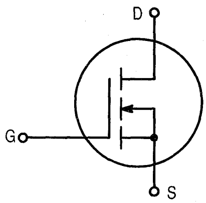
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode

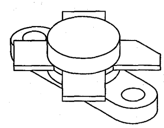
MRF148

Designed for power amplifier applications in industrial, commercial and amateur radio equipment to 175 MHz.

- Superior High Order IMD
- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 30 Watts
  Power Gain = 18 dB (Typ)
  Efficiency = 40% (Typ)
- $IMD_{(d3)}$ (30 W PEP) — –35 dB (Typ)
- $IMD_{(d11)}$ (30 W PEP) — –60 dB (Typ)
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR

30 W, to 175 MHz
N–CHANNEL MOS
LINEAR RF POWER
FET





CASE 211–07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	120	Vdc
Drain–Gate Voltage	V_{DGO}	120	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	6.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

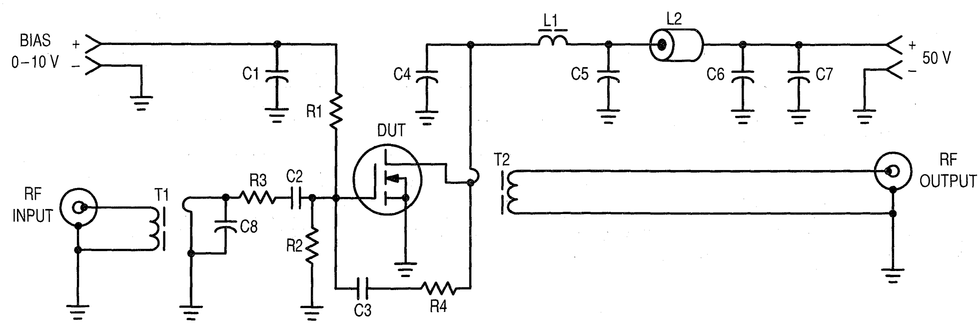
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 2.5 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	0.8	1.2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	50	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	35	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	8.0	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (30 MHz) (V_{DD} = 50 V, P_{out} = 30 W (PEP), I_{DQ} = 100 mA) (175 MHz)	G_{ps}	— —	18 15	— —	dB
Drain Efficiency (30 W PEP) (V_{DD} = 50 V, f = 30 MHz, I_{DQ} = 100 mA) (30 W CW)	η	— —	40 50	— —	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	−35 −60	— —	dB
Load Mismatch (V_{DD} = 50 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 50 V, P_{out} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 1.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	20 −50 −70	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1, C2, C3, C4, C5, C6 — 0.1 µF Ceramic Chip or Equivalent
C7 — 10 µF, 100 V Electrolytic
C8 — 100 pF Dipped Mica
L1 — VK200 20/4B Ferrite Choke or Equivalent (3.0 µH)
L2 — Ferrite Bead(s), 2.0 µH

R1, R2 — 200 Ω, 1/2 W Carbon
R3 — 4.7 Ω, 1/2 W Carbon
R4 — 470 Ω, 1.0 W Carbon
T1 — 4:1 Impedance Transformer
T2 — 1:2 Impedance Transformer

Figure 1. 2.0 to 50 MHz Broadband Test Circuit

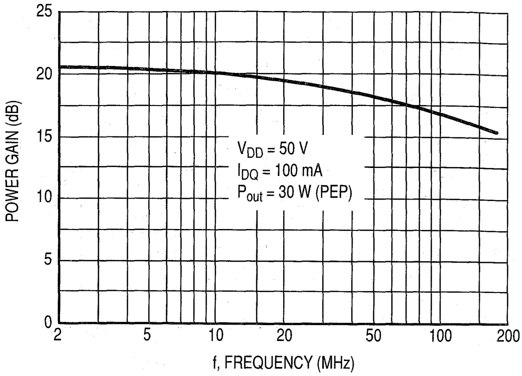


Figure 2. Power Gain versus Frequency

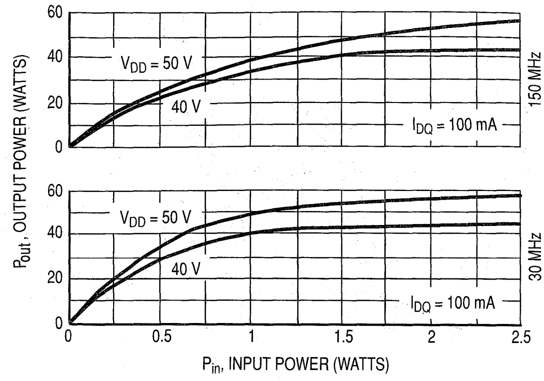


Figure 3. Output Power versus Input Power

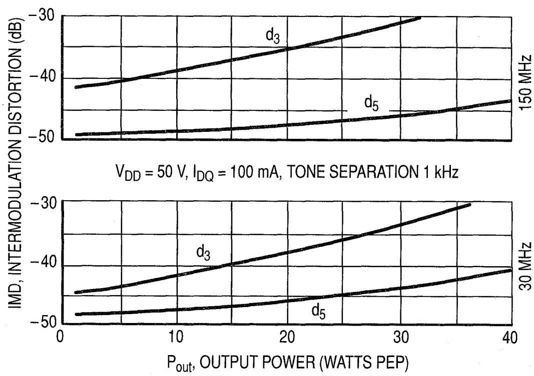


Figure 4. IMD versus P_{out}

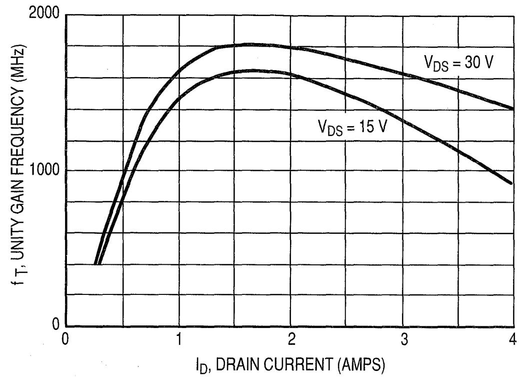
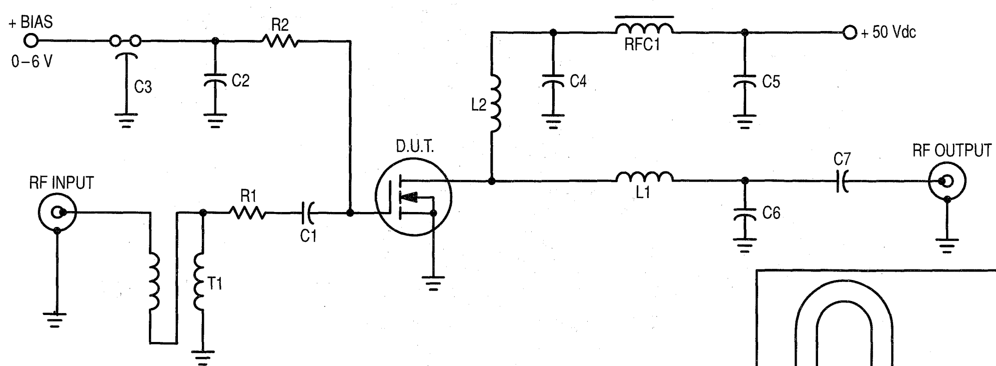
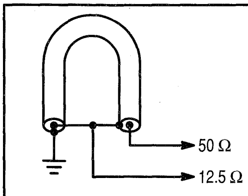


Figure 5. Common Source Unity Gain Frequency versus Drain Current



C1 — 91 pF Unelco Type MCM 01/010
C2, C4 — 0.1 μF Erie Red Cap
C3 — Allen Bradley 680 pF Feed Thru
C5 — 1.0 μF, 50 Vdc Electrolytic
C6 — 15 pF Unelco Type J101
C7 — 24 pF Unelco Type MCM 01/010
L1 — 2 Turns #18 AWG, 5/16″ ID
L2 — 4 Turns #18 AWG, 5/16″ ID
R1 — 1.0 Ohm, 1/4 W Carbon
R2 — 2000 Ohm, 1/4 W Carbon
RFC1 — VK200 21/4B
T1 — 4:1 Transformer, 1.75″ Subminiature Coaxial Cable



T1 — 4:1 Impedance Ratio Transformer, Line Impedance = 25 Ω

Figure 6. 150 MHz Test Circuit

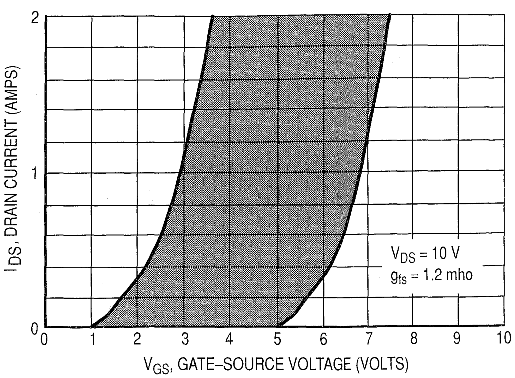


Figure 7. Gate Voltage versus Drain Current

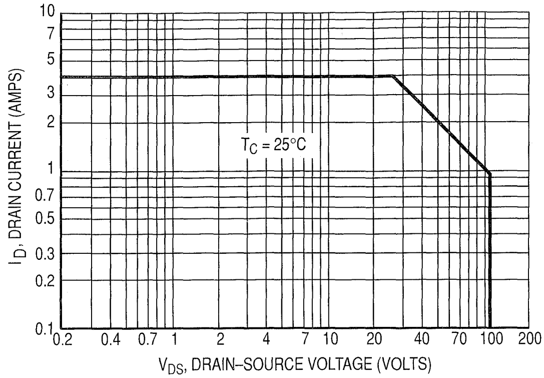
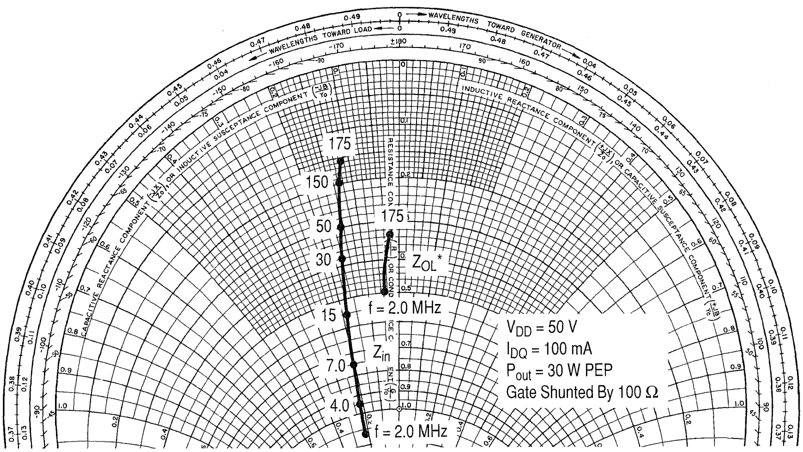


Figure 8. DC Safe Operating Area (SOA)



Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a *given output power, voltage and frequency.*

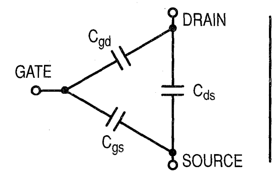
Figure 9. Impedance Coordinates — 50 Ohm Characteristic Impedance

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$$C_{iss} = C_{gd} + C_{gs}$$
$$C_{oss} = C_{gd} + C_{ds}$$
$$C_{rss} = C_{gd}$$

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

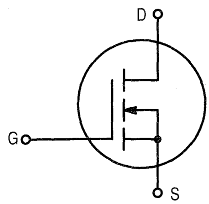
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode

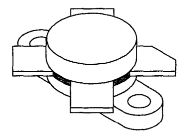
MRF150

150 W, to 150 MHz
N–CHANNEL MOS
LINEAR RF POWER
FET

Designed primarily for linear large–signal output stages up to 150 MHz frequency range.

- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 150 Watts
  Power Gain = 17 dB (Typ)
  Efficiency = 45% (Typ)
- Superior High Order IMD
- $IMD_{(d3)}$ (150 W PEP) — –32 dB (Typ)
- $IMD_{(d11)}$ (150 W PEP) — –60 dB (Typ)
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR





CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

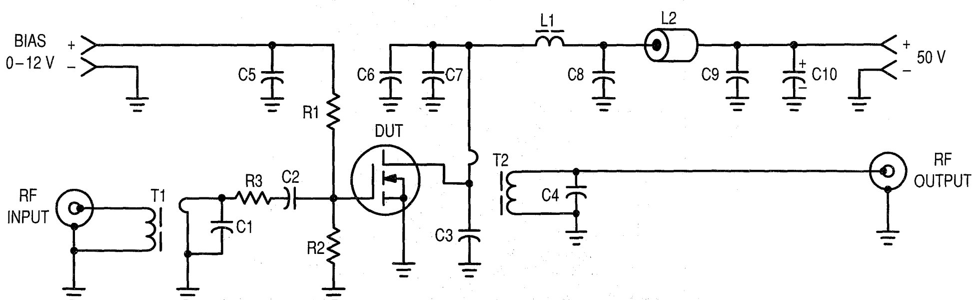
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 8

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	4.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	400	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	240	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	40	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA) f = 30 MHz f = 150 MHz	G_{ps}	— —	17 8.0	— —	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_D (Max) = 3.75 A)	η	—	45	—	%
Intermodulation Distortion (1) (V_{DD} = 50 V, P_{out} = 150 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	−32 −60	— —	dB
Load Mismatch (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 50 V, P_{out} = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 3.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	20 −50 −75	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1 — 470 pF Dipped Mica
C2, C5, C6, C7, C8, C9 — 0.1 μF Ceramic Chip or Monolythic with Short Leads
C3 — 200 pF Unencapsulated Mica or Dipped Mica with Short Leads
C4 — 15 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 μF/100 V Electrolytic
L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 μH
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 3.3 Ω/1.0 W Carbon (or 2.0 x 6.8 Ω/1/2 W in Parallel
T1 — 9:1 Broadband Transformer
T2 — 1:9 Broadband Transformer

Figure 1. 30 MHz Test Circuit (Class AB)

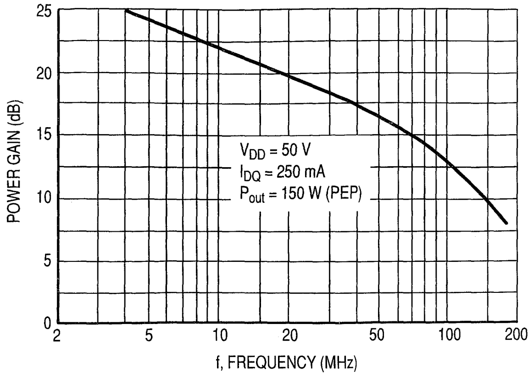


Figure 2. Power Gain versus Frequency

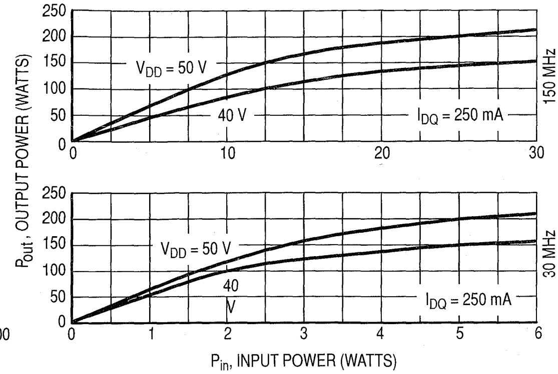


Figure 3. Output Power versus Input Power

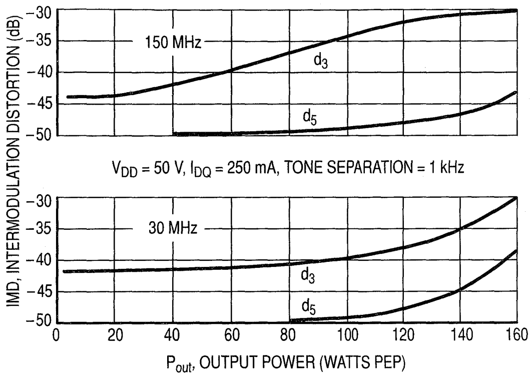


Figure 4. IMD versus P_{out}

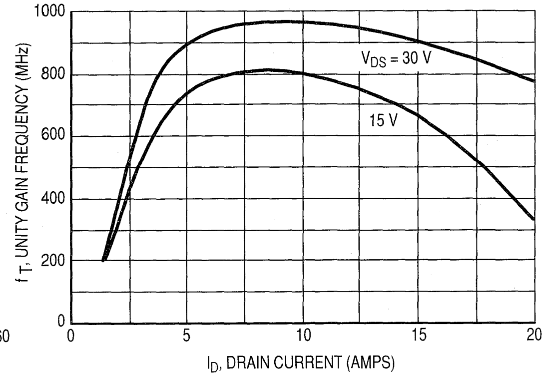


Figure 5. Common Source Unity Gain Frequency versus Drain Current

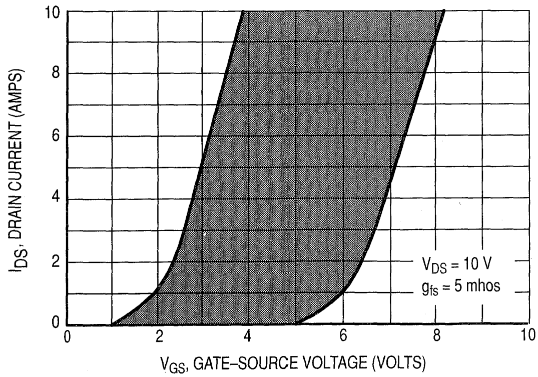
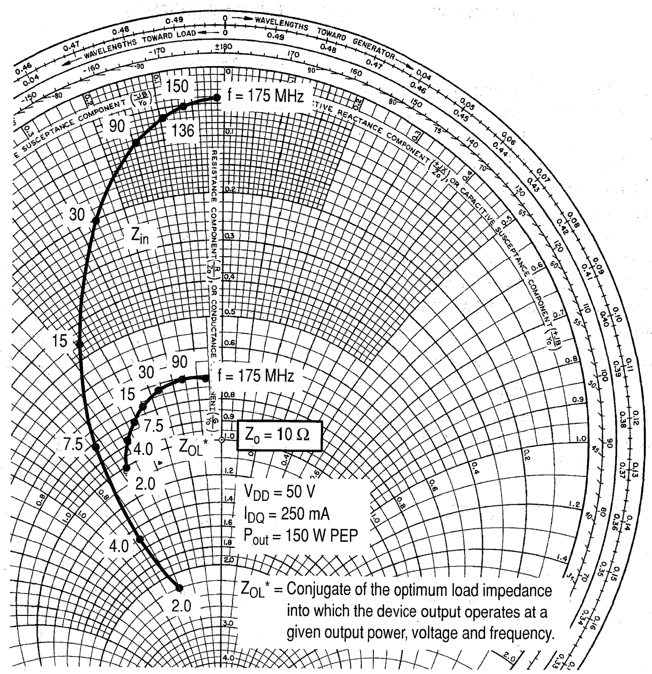
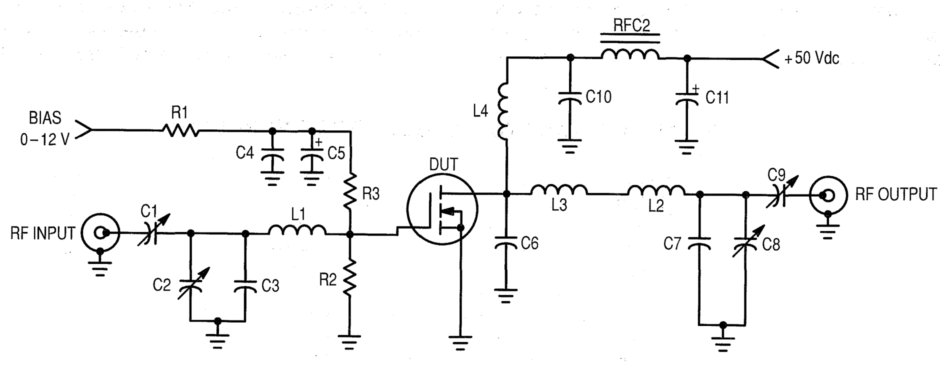


Figure 6. Gate Voltage versus Drain Current



NOTE: Gate Shunted by 25 Ohms.

Figure 7. Series Equivalent Impedance



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF, Unelco
C4 — 0.1 μF, Ceramic
C5 — 1.0 μF, 15 WV Tantalum
C6 — 25 pF, Unelco J101
C7 — 25 pF, Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 μF, Ceramic
C11 — 15 μF, 60 WV Electrolytic

L1 — 3/4″, 18 AWG into Hairpin
L2 — Printed Line, 0.200″ x 0.500″
L3 — 1″, #16 AWG into Hairpin
L4 — 2 Turns #16 AWG, 5/16 ID
RFC1 — 5.6 μH, Choke
RFC2 — VK200–4B
R1 — 150 Ω, 1.0 W Carbon
R2 — 10 kΩ, 1/2 W Carbon
R3 — 120 Ω, 1/2 W Carbon

Figure 8. 150 MHz Test Circuit (Class AB)

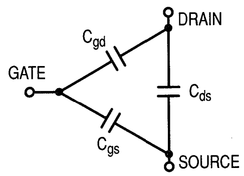
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

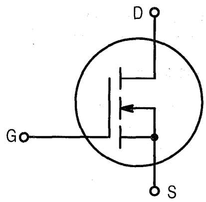
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode MOSFET

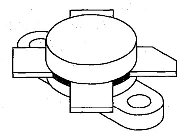
MRF151

Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 30 MHz, 50 V:
  Output Power — 150 W
  Gain — 18 dB (22 dB Typ)
  Efficiency — 40%
- Typical Performance at 175 MHz, 50 V:
  Output Power — 150 W
  Gain — 13 dB
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability

150 W, 50 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET





CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

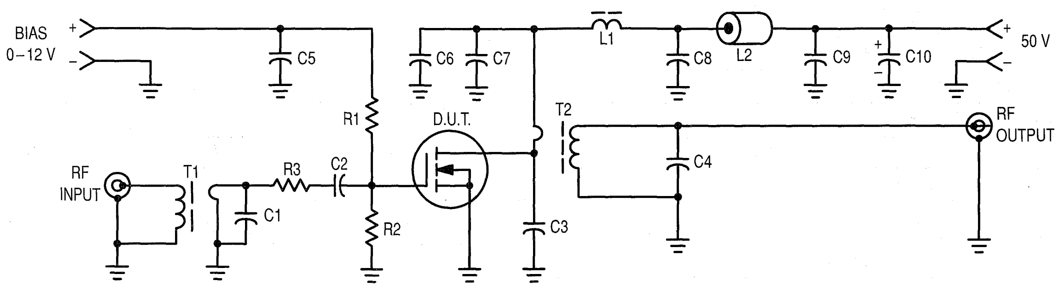
NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 8

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

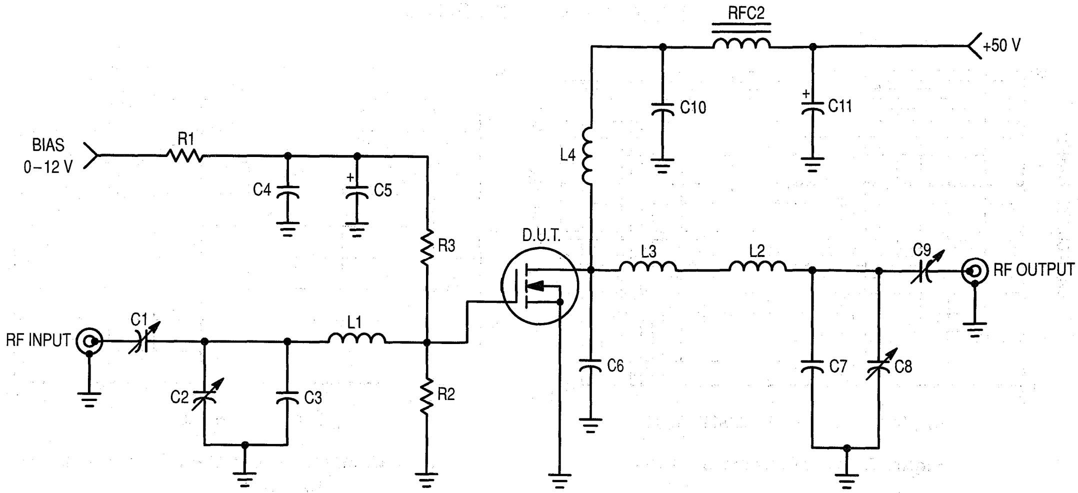
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	220	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	15	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain, f = 30; 30.001 MHz (V_{DD} = 50 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA) f = 175 MHz	G_{ps}	18 —	22 13	— —	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_D (Max) = 3.75 A)	η	40	45	—	%
Intermodulation Distortion (1) (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	−32 −60	−30 —	dB
Load Mismatch (V_{DD} = 50 V, P_{out} = 150 W (PEP), f1 = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 50 V, P_{out} = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 3.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	23 −50 −75	— — —	dB

NOTE:
1. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1 — 470 pF Dipped Mica
C2, C5, C6, C7, C8, C9 — 0.1 μF Ceramic Chip or Monolythic with Short Leads
C3 — 200 pF Unencapsulated Mica or Dipped Mica with Short Leads
C4 — 15 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 μF/100 V Electrolytic
L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 μH
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 51 Ω/1.0 W Carbon
R3 — 3.3 Ω/1.0 W Carbon (or 2.0 x 6.8 Ω/1/2 W in Parallel)
T1 — 9:1 Broadband Transformer
T2 — 1:9 Broadband Transformer
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε_r = 5

Figure 1. 30 MHz Test Circuit



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF, Unelco
C4 — 0.1 μF, Ceramic
C5 — 1.0 μF, 15 WV Tantalum
C6 — 15 pF, Unelco J101
C7 — 25 pF, Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 μF, Ceramic
C11 — 15 μF, 60 WV Electrolytic
D1 — 1N5347 Zener Diode

L1 — 3/4″, #18 AWG into Hairpin
L2 — Printed Line, 0.200″ x 0.500″
L3 — 1″, #16 AWG into Hairpin
L4 — 2 Turns, #16 AWG, 5/16 ID
RFC1 — 5.6 μH, Choke
RFC2 — VK200–4B
R1 — 150 Ω, 1.0 W Carbon
R2 — 10 kΩ, 1/2 W Carbon
R3 — 120 Ω, 1/2 W Carbon
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, $\varepsilon_r = 5.0$

Figure 2. 175 MHz Test Circuit

TYPICAL CHARACTERISTICS

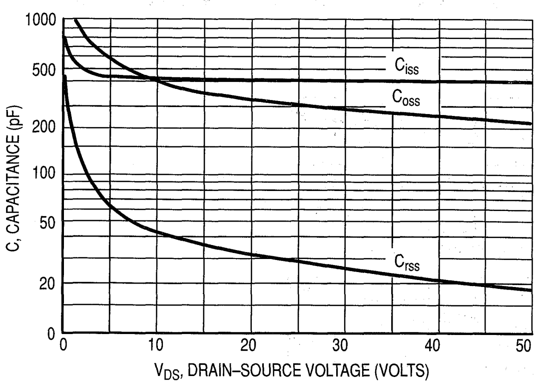


Figure 3. Capacitance versus Drain–Source Voltage

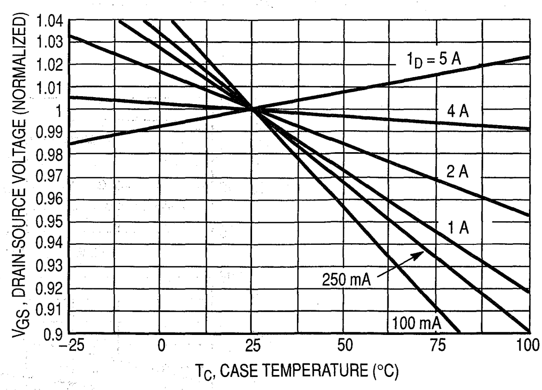


Figure 4. Gate–Source Voltage versus Case Temperature

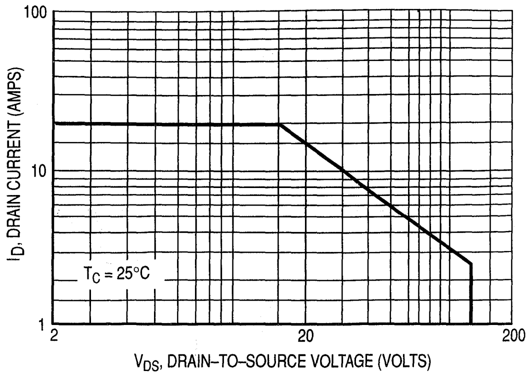


Figure 5. DC Safe Operating Area

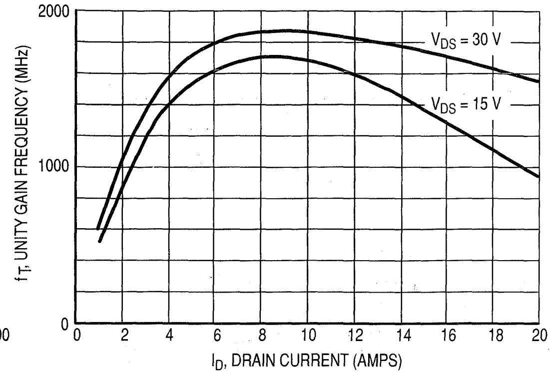


Figure 6. Common Source Unity Gain Frequency versus Drain Current

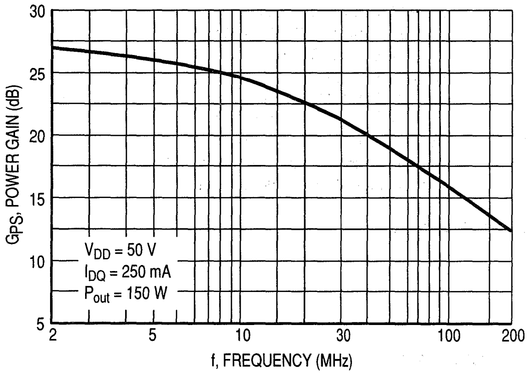


Figure 7. Power Gain versus Frequency

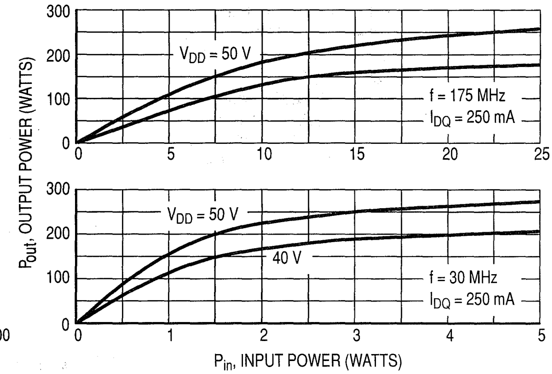


Figure 8. Output Power versus Input Power

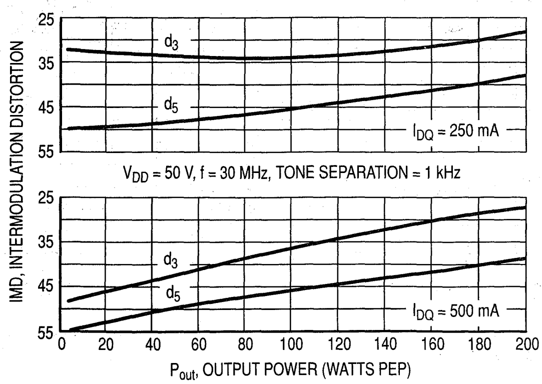


Figure 9. IMD versus P_{out}

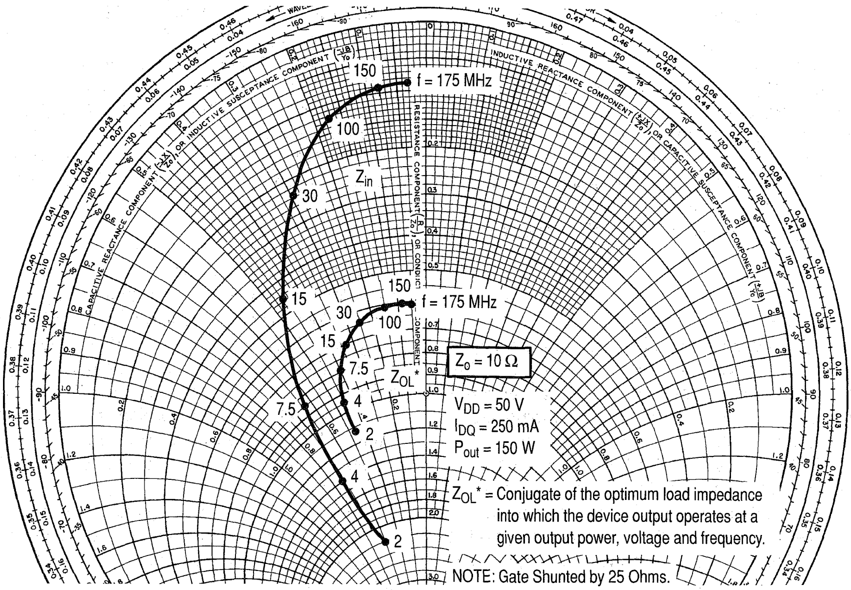


Figure 10. Series Equivalent Impedance

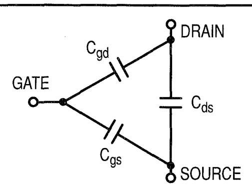
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} = C_{gs}$
$C_{oss} = C_{gd} = C_{ds}$
$C_{rss} = C_{gd}$

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 6 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of this device is essentially capacitor. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the device due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — This device does not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

DESIGN CONSIDERATIONS

The MRF151 is an RF Power, MOS, N–channel enhancement mode field–effect transistor (FET) designed for HF and VHF power amplifier applications.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power MOSFETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF151 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF151 was characterized at I_{DQ} = 250 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

GAIN CONTROL

Power output of the MRF151 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

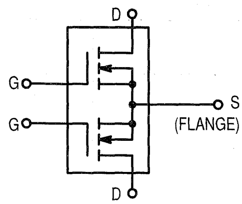
The RF MOSFET Line
RF Power Field-Effect Transistor
N–Channel Enhancement–Mode MOSFET

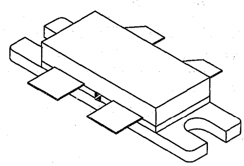
MRF151G

Designed for broadband commercial and military applications at frequencies to 175 MHz. The high power, high gain and broadband performance of this device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 175 MHz, 50 V:
  Output Power — 300 W
  Gain — 14 dB (16 dB Typ)
  Efficiency — 50%
- Low Thermal Resistance — 0.35°C/W
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability

300 W, 50 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET





CASE 375–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	40	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	500 2.85	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

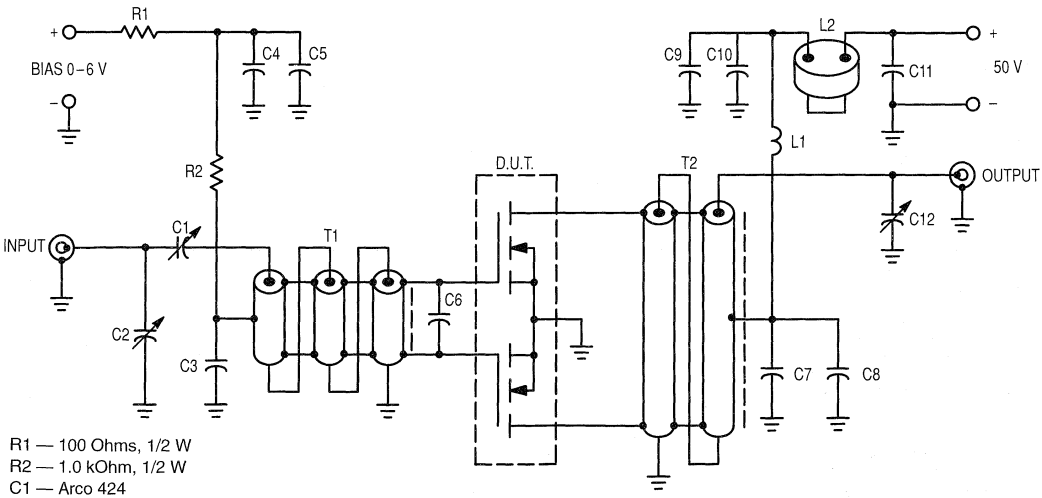
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.35	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 8

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Each Side)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (Each Side)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	5.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS (Each Side)					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	220	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	15	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 300 W, I_{DQ} = 500 mA, f = 175 MHz)	G_{ps}	14	16	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 300 W, f = 175 MHz, I_D (Max) = 11 A)	η	50	55	—	%
Load Mismatch (V_{DD} = 50 V, P_{out} = 300 W, I_{DQ} = 500 mA, VSWR 5:1 at all Phase Angles)	ψ	No Degradation in Output Power			



R1 — 100 Ohms, 1/2 W
R2 — 1.0 kOhm, 1/2 W
C1 — Arco 424
C2 — Arco 404
C3, C4, C7, C8, C9 — 1000 pF Chip
C5, C10 — 0.1 μF Chip
C6 — 330 pF Chip
C11 — 0.47 μF Ceramic Chip, Kemet 1215 or Equivalent (100 V)
C12 — Arco 422
L1 — 10 Turns AWG #18 Enameled Wire, Close Wound, 1/4″ I.D.
L2 — Ferrite Beads of Suitable Material for 1.5–2.0 μH Total Inductance

Unless Otherwise Noted, All Chip Capacitors are ATC Type 100 or Equivalent.

T1 — 9:1 RF Transformer. Can be made of 15–18 Ohms Semirigid Co–Ax, 62–90 Mils O.D.
T2 — 1:4 RF Transformer. Can be made of 16–18 Ohms Semirigid Co–Ax, 70–90 Mils O.D.
Board Material — 0.062″ Fiberglass (G10), 1 oz. Copper Clad, 2 Sides, ε_r = 5.0

NOTE: For stability, the input transformer T1 must be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

See Figure 6 for construction details of T1 and T2.

Figure 1. 175 MHz Test Circuit

TYPICAL CHARACTERISTICS

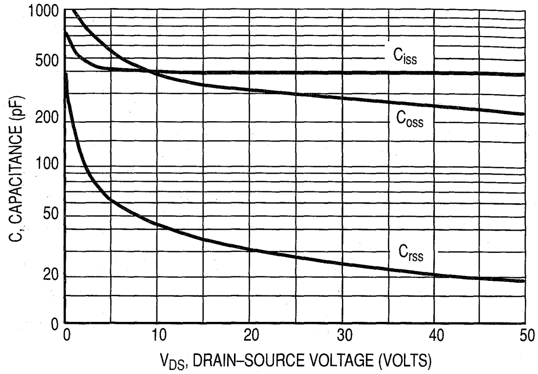


Figure 2. Capacitance versus Drain–Source Voltage*

*Data shown applies to each half of MRF151G.

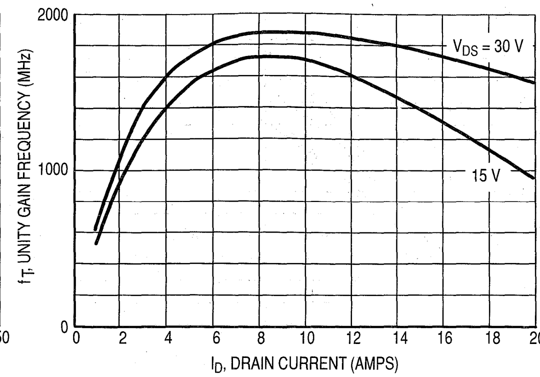


Figure 3. Common Source Unity Gain Frequency versus Drain Current*

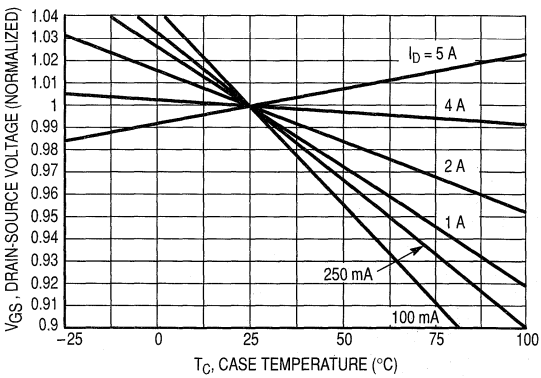


Figure 4. Gate–Source Voltage versus Case Temperature*

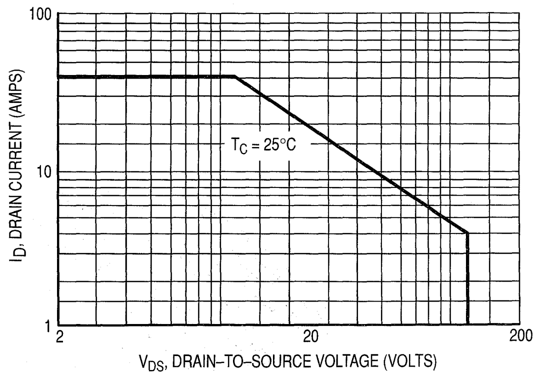


Figure 5. DC Safe Operating Area

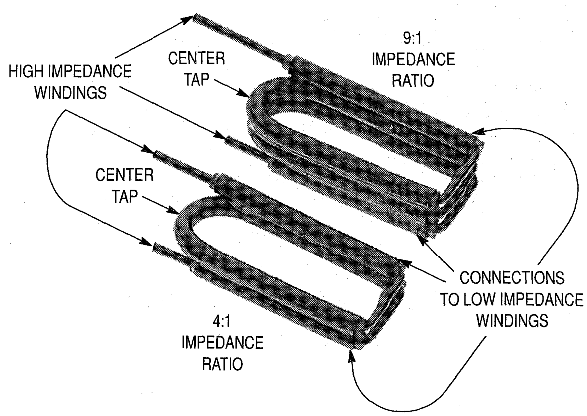


Figure 6. RF Transformer

TYPICAL CHARACTERISTICS

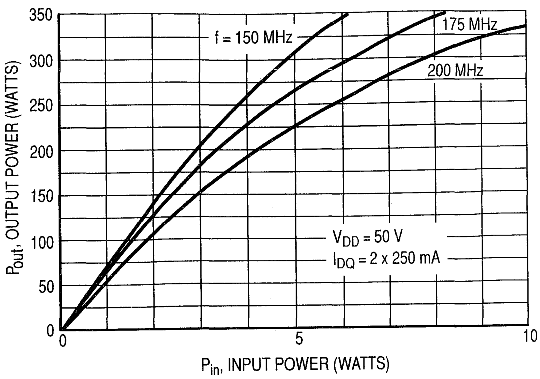


Figure 7. Output Power versus Input Power

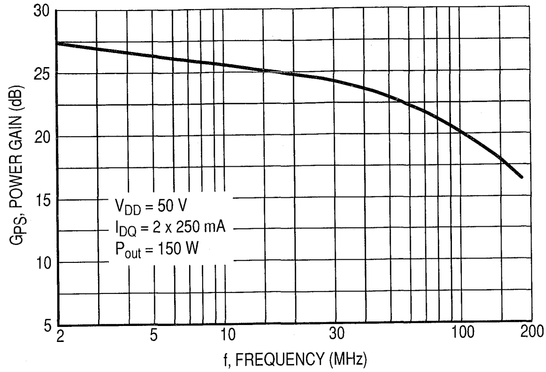
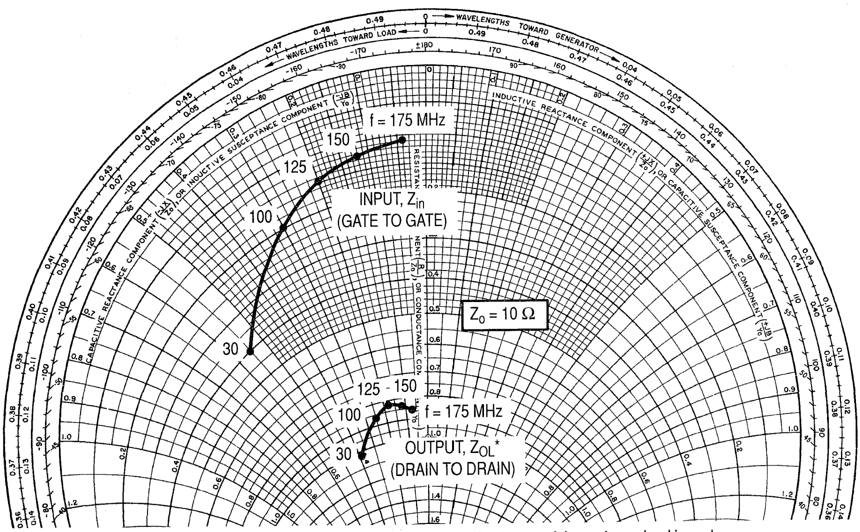


Figure 8. Power Gain versus Frequency



Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 9. Input and Output Impedance

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal anode gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

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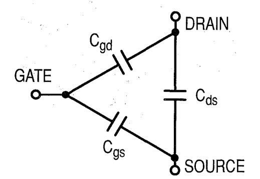

$C_{iss} = C_{gd} = C_{gs}$
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HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

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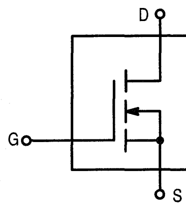
The RF MOSFET Line
RF Power Field Effect Transistor
N–Channel Enhancement–Mode MOSFET

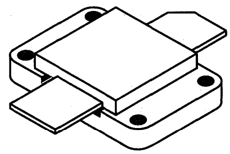
MRF154

Designed primarily for linear large–signal output stages in the 2.0–100 MHz frequency range.

- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 600 Watts
  Power Gain = 17 dB (Typ)
  Efficiency = 45% (Typ)

600 W, 50 V, 80 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET





CASE 368–03, STYLE 2
(HOG PAC)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	60	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1350 7.7	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

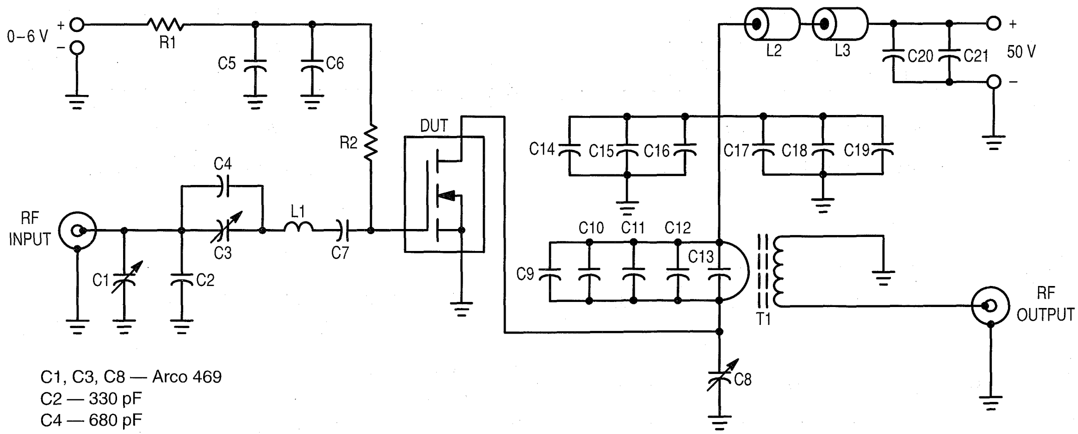
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.13	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	20	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 40 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 20 A)	g_{fs}	16	20	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1600	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	950	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	175	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 600 W, I_{DQ} = 800 mA, f = 30 MHz)	G_{ps}	—	17	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 600 W, I_{DQ} = 800 mA, f = 30 MHz)	η	—	45	—	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 600 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 800 mA)	$IMD_{(d3)}$	—	−25	—	dB



C1, C3, C8 — Arco 469
C2 — 330 pF
C4 — 680 pF
C5, C19, C20 — 0.47 μF, RMC Type 2225C
C6, C7, C14, C15, C16 — 0.1 μF
C9, C10, C11 — 470 pF
C12 — 1000 pF
C13 — Two Unencapsulated 1000 pF Mica, in Series
C17, C18 — 0.039 μF
C21 — 10 μF/100 V Electrolytic
L1 — 2 Turns #16 AWG, 1/2″ ID, 3/8″ Long
L2, L3 — Ferrite Beads, Fair–Rite Products Corp. #2673000801

R1, R2 — 10 Ohms/2.0 W Carbon
T1 — RF Transformer, 1:25 Impedance Ratio. See Motorola Application Note AN749, Figure 4 for details. Ferrite Material: 2 Each, Fair–Rite Products Corp. #2667540001

All capacitors ATC type 100/200 chips or equivalent unless otherwise noted.

Figure 1. 30 MHz Test Circuit

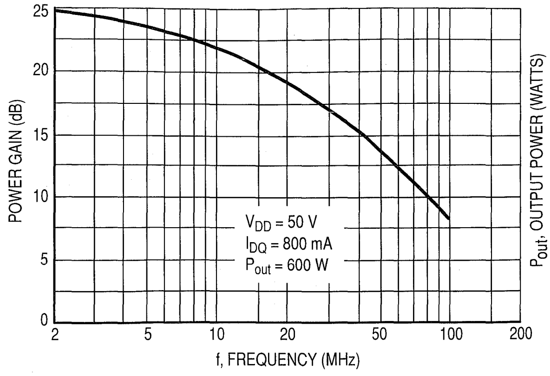


Figure 2. Power Gain versus Frequency

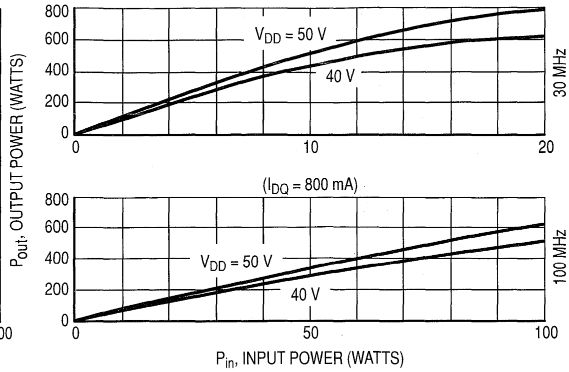


Figure 3. Output Power versus Input Power

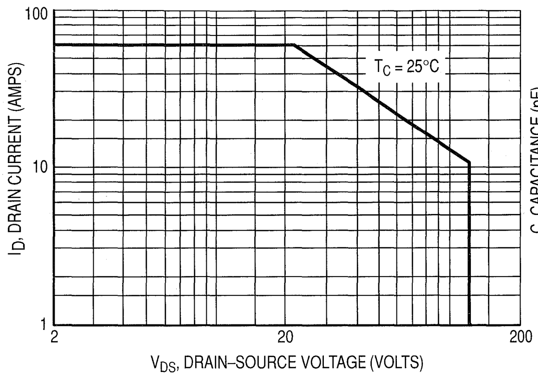


Figure 4. DC Safe Operating Area

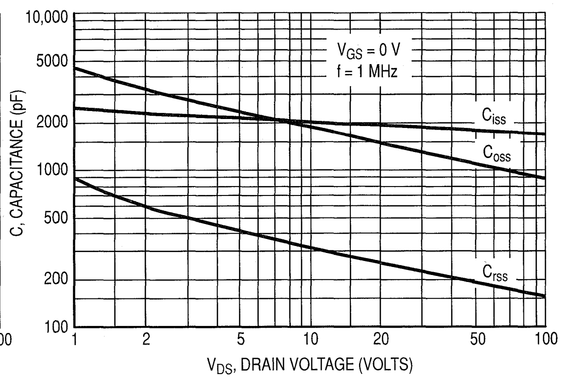


Figure 5. Capacitance versus Drain Voltage

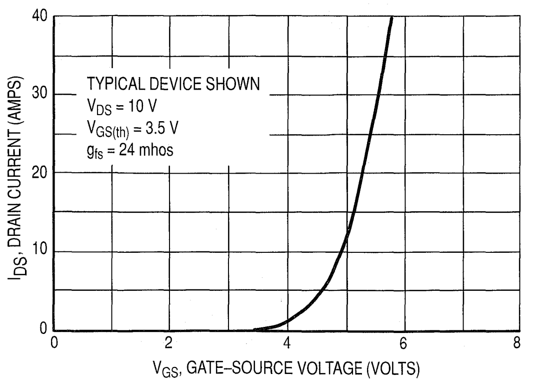


Figure 6. Gate Voltage versus Drain Current

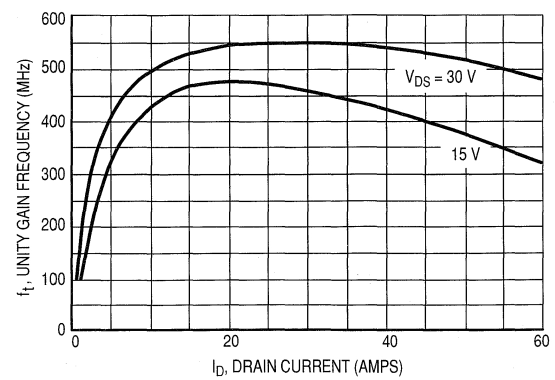


Figure 7. Common Source Unity Gain Frequency versus Drain Current

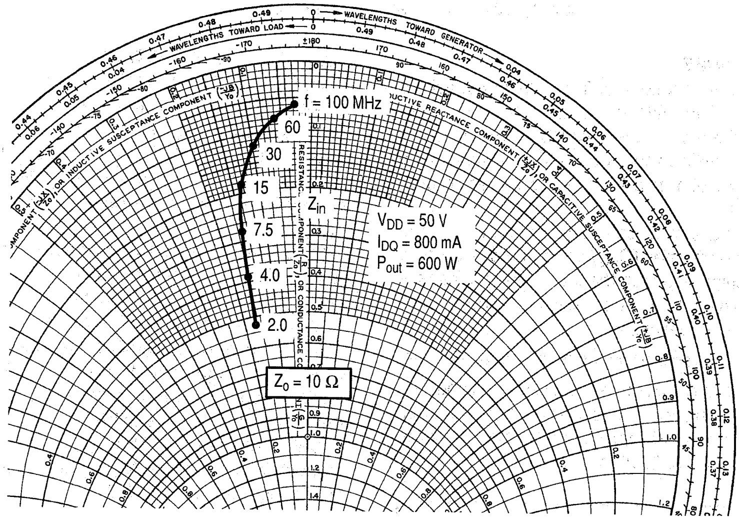
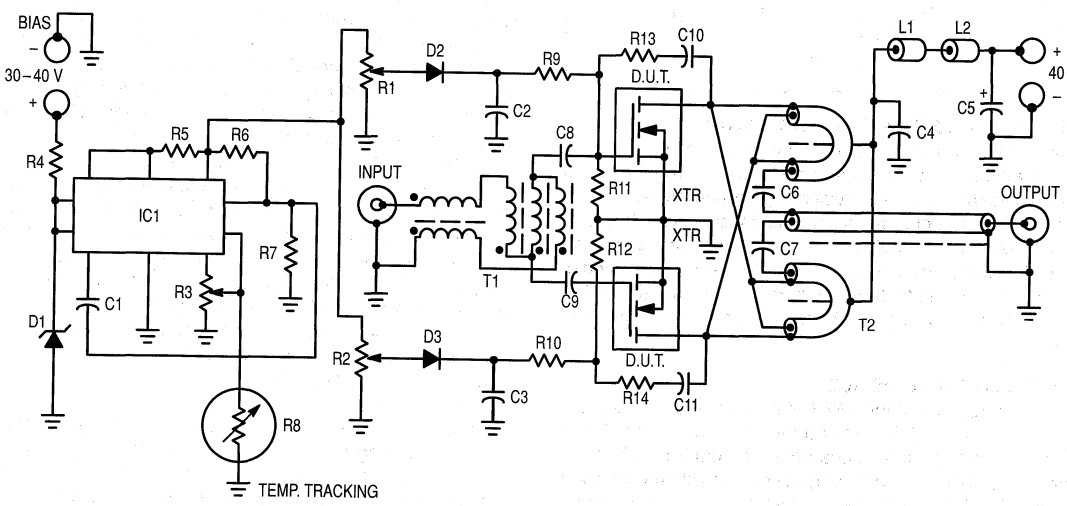


Figure 8. Series Equivalent Impedance



C1 — 1000 pF Ceramic
C2, C3, C4, C8, C9, C10, C11 — 0.1 μF Ceramic
C5 — 10 μF/100 V Electrolytic
C6, C7 — 0.1 μF Ceramic, (ATC 200/823 or Equivalent)
D1 — 28 V Zener, 1N5362 or Equivalent
D3 — 1N4148
IC1 — MC1723
L1, L2 — Fair–Rite Products Corp. Ferrite Beads #2673000801
R1, R2, R3 — 10 k Trimpot
R4 — 1.0 k/1.0 W
R5 — 10 Ohms
R6 — 2.0 k
R7 — 10 k
R8 — Thermistor, 10 k (25°C), 2.5 k (75°C)
R9, R10 — 100 Ohms
R11, R12 — 1.0 k
R13, R14 — 50–100 Ohms, 4.0 x 2.0 W Carbon in Parallel
T1 — 9:1 Transformer, Trifilar and Balun Wound on Separate Fair–Rite Products Corp. Balun Cores #286100012, 5 Turns Each.
T2 — 1:9 Transformer, Balun 50 Ohm CO–AX Cable RG–188, Low Impedance Lines W.L. Gore 16 Ohms CO–AX Type CXN 1837. Each Winding Threaded Through Two Fair–Rite Products Corp. #2661540001 Ferrite Sleeves (6 Each).
XTR — MRF154

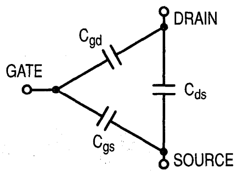
Figure 9. 20–80 MHz 1.0 kW Broadband Amplifier

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

MOUNTING OF HIGH POWER RF POWER TRANSISTORS

The package of this device is designed for conduction cooling. It is extremely important to minimize the thermal resistance between the device flange and the heat dissipator.

Since the device mounting flange is made of soft copper, it may be deformed during various stages of handling or during transportation. It is recommended that the user makes a final inspection on this before the device installation. ±0.0005″ is considered sufficient for the flange bottom.

The same applies to the heat dissipator in the device mounting area. If copper heatsink is not used, a copper head spreader is strongly recommended between the device mounting surfaces and the main heatsink. It should be at least 1/4″ thick and extend at least one inch from the flange edges. A thin layer of thermal compound in all interfaces is, of course, essential. The recommended torque on the 4–40 mounting screws should be in the area of 4–5 lbs.–inch, and spring type lock washers along with flat washers are recommended.

For die temperature calculations, the Δ temperature from a corner mounting screw area to the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions (dissipation 150 W and 300 W respectively).

The main heat dissipator must be sufficiently large and have low R_θ for moderate air velocity, unless liquid cooling is employed.

CIRCUIT CONSIDERATIONS

At high power levels (500 W and up), the circuit layout becomes critical due to the low impedance levels and high RF currents associated with the output matching. Some of the components, such as capacitors and inductors must also withstand these currents. The component losses are directly proportional to the operating frequency. The manufacturers specifications on capacitor ratings should be consulted on these aspects prior to design.

Push–pull circuits are less critical in general, since the ground referenced RF loops are practically eliminated, and the impedance levels are higher for a given power output. High power broadband transformers are also easier to design than comparable LC matching networks.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

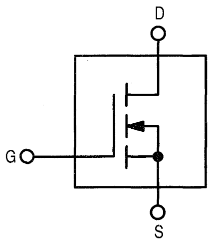
The RF Power MOS Line
Power Field Effect Transistor
N–Channel Enhancement Mode

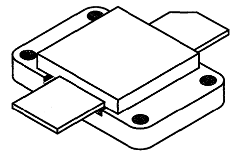
MRF157

Designed primarily for linear large–signal output stages to 80 MHz.

- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 600 Watts
  Power Gain = 21 dB (Typ)
  Efficiency = 45% (Typ)

600 W, to 80 MHz
MOS LINEAR
RF POWER FET





CASE 368–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Drain–Gate Voltage	V_{DGO}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	60	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1350 7.7	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

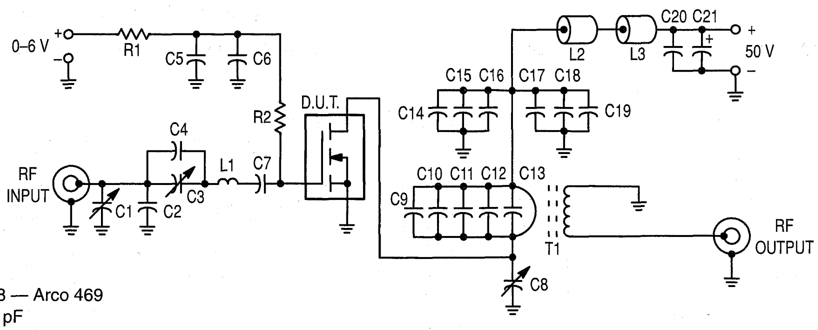
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{θJC}$	0.13	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	20	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 40 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 20 A)	g_{fs}	16	24	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	1800	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	750	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	75	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 600 W, I_{DQ} = 800 mA, f = 30 MHz)	G_{ps}	15	21	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 600 W, f = 30 MHz, I_{DQ} = 800 mA)	h	40	45	—	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 600 W(PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 800 mA)	$IMD_{(d3)}$	—	−25	—	dB



C1, C3, C8 — Arco 469
C2 — 330 pF
C4 — 680 pF
C5, C19, C20 — 0.47 μF, RMC Type 2225C
C6, C7, C14, C15, C16 — 0.1 μF
C9, C10, C11 — 470 pF
C12 — 1000 pF
C13 — Two Unencapsulated 1000 pF Mica, in Series
C17, C18 — 0.039 μF
C21 — 10 μF/100 V Electrolytic
L1 — 2 Turns #16 AWG, 1/2″ ID, 3/8″ Long
L2, L3 — Ferrite Beads, Fair–Rite Products Corp. #2673000801

R1, R2 — 10 Ohms/2W Carbon
T1 — RF Transformer, 1:25 Impedance Ratio. See Motorola Application Note AN749, Figure 4 for details. Ferrite Material: 2 Each, Fair–Rite Products Corp. #2667540001

All capacitors ATC type 100/200 chips or equivalent unless otherwise noted.

Figure 1. 30 MHz Test Circuit

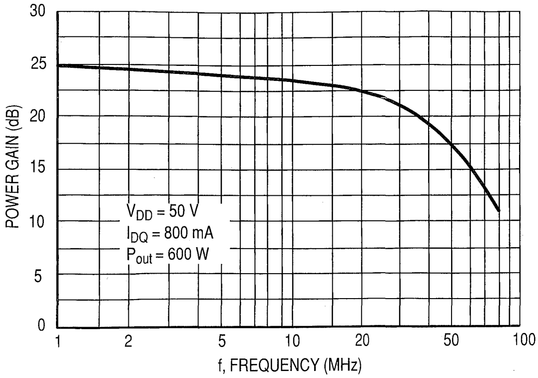


Figure 2. Power Gain versus Frequency

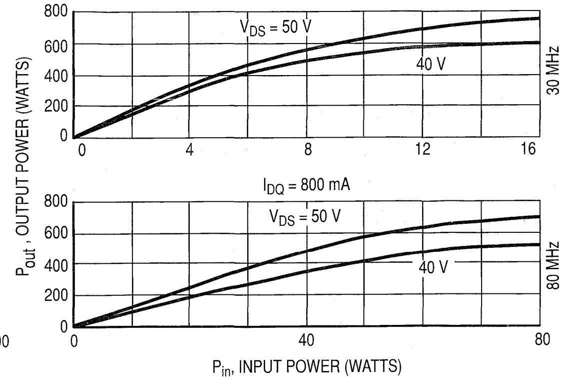


Figure 3. Output Power versus Input Power

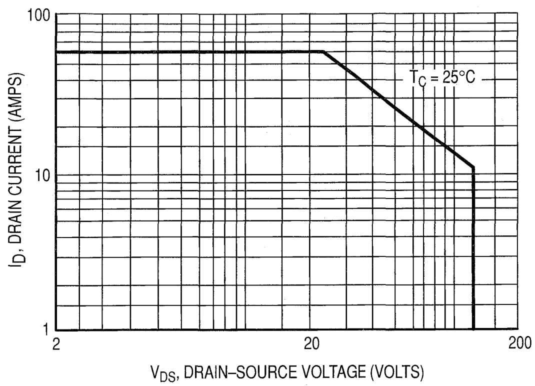


Figure 4. DC Safe Operating Area

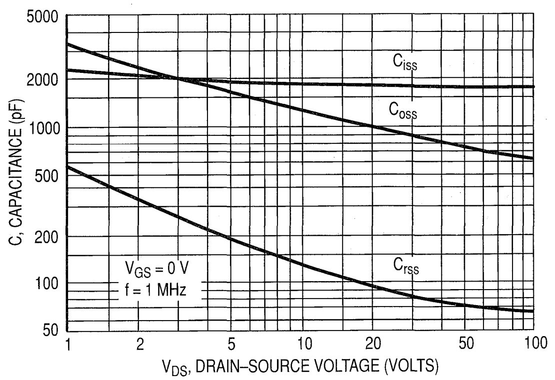


Figure 5. Capacitance versus Drain Voltage

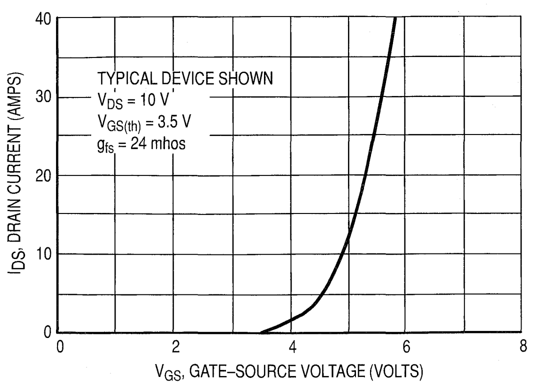


Figure 6. Gate Voltage versus Drain Current

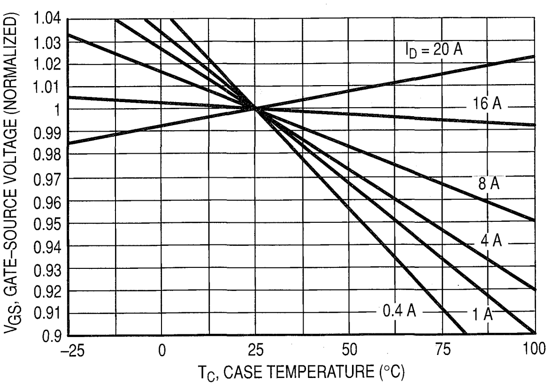


Figure 7. Gate–Source Voltage versus Case Temperature

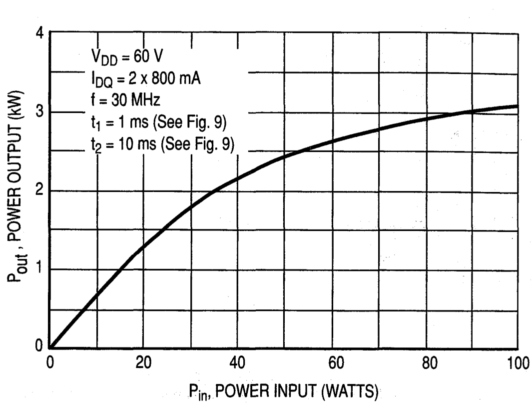


Figure 8. Output Power versus Input Power Under Pulse Conditions (2 x MRF157)

Note: Pulse data for this graph was taken in a push–pull circuit similar to the one shown. However, the output matching network was modified for the higher level of peak power.

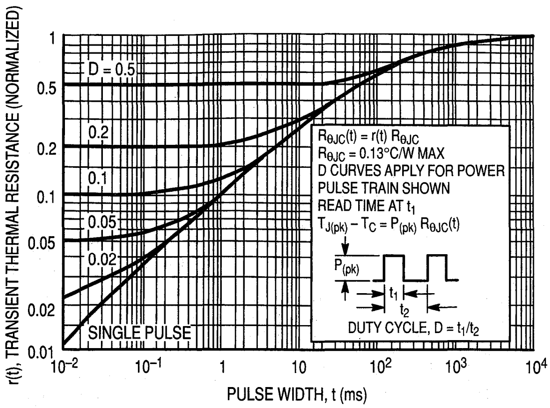
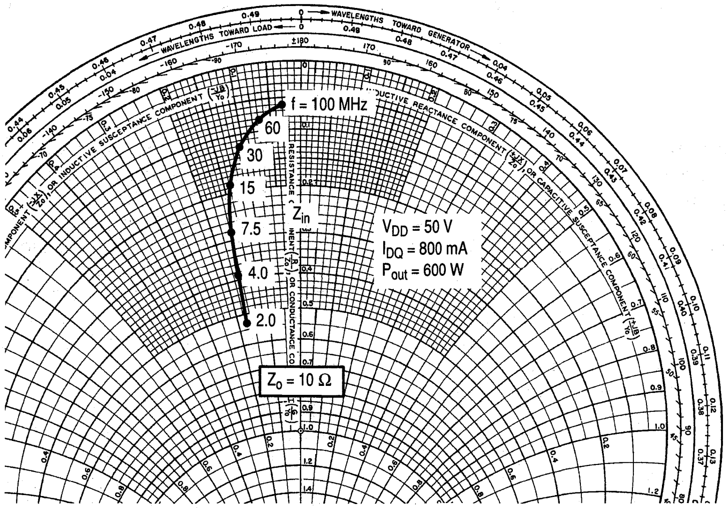
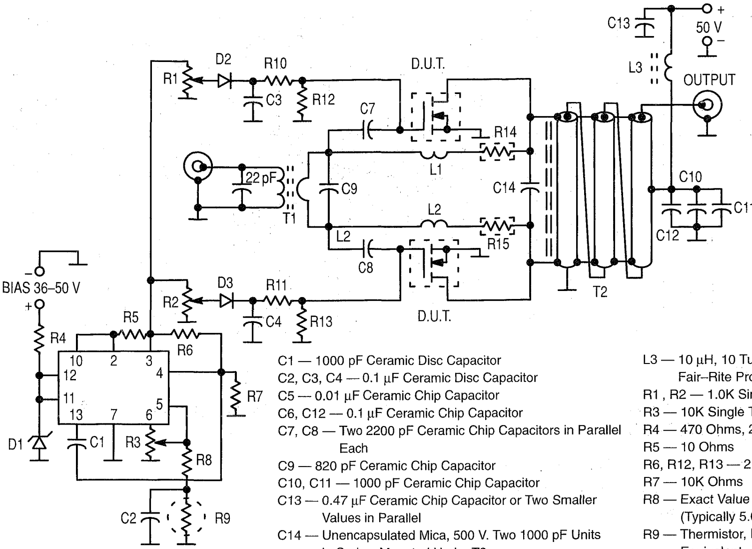


Figure 9. Thermal Response versus Pulse Width



Note: To determine Z_{OL}*, use formula $\frac{(V_{CC} - V_{sat})^2}{2\ P_o} = Z_{OL}^*$

Figure 10. Series Equivalent Impedance



C1 — 1000 pF Ceramic Disc Capacitor
C2, C3, C4 — 0.1 μF Ceramic Disc Capacitor
C5 — 0.01 μF Ceramic Chip Capacitor
C6, C12 — 0.1 μF Ceramic Chip Capacitor
C7, C8 — Two 2200 pF Ceramic Chip Capacitors in Parallel Each
C9 — 820 pF Ceramic Chip Capacitor
C10, C11 — 1000 pF Ceramic Chip Capacitor
C13 — 0.47 μF Ceramic Chip Capacitor or Two Smaller Values in Parallel
C14 — Unencapsulated Mica, 500 V. Two 1000 pF Units in Series, Mounted Under T2
D1 — 1N5357A or Equivalent
D2, D3 — 1N4148 or Equivalent.
IC1 — MC1723 (723) Voltage Regulator
L1, L2 — 15 ηH, Connecting Wires to R14 and R15, 2.5 cm Each #20 AWG
L3 — 10 μH, 10 Turns #12 AWG Enameled Wire on Fair–Rite Products Corp. Ferrite Toroid #5961000401 or Equivalent
R1 , R2 — 1.0K Single Turn Trimpots
R3 — 10K Single Turn Trimpot
R4 — 470 Ohms, 2.0 Watts
R5 — 10 Ohms
R6, R12, R13 — 2.0K Ohms
R7 — 10K Ohms
R8 — Exact Value Depends on Thermistor R9 used (Typically 5.0–10K)
R9 — Thermistor, Keystone RL1009–5820–97–D1 or Equivalent
R10, R11 — 100 Ohms, 1.0W Carbon
R14, R15 — EMC Technology Model 5308 or KDI Pyrofilm PPR 870–150–3 Power Resistors, 25 Ohms
T1, T2 — 9:1 and 1:9 Impedance Ratio RF Transformers

Unless otherwise noted, all resistors are 1/2 watt metal film type. All chip capacitors except C13 are ATC type 100/200B or Dielectric Laboratories type C17.

Figure 11. 2.0 to 50 MHz, 1.0 kW Wideband Amplifier

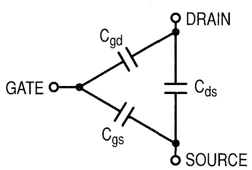
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the TMOS® FET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

IMPEDANCE CHARACTERISTICS

Device input and output impedances are normally obtained by measuring their conjugates in an optimized narrow band test circuit. These test circuits are designed and constructed for a number of frequency points depending on the frequency coverage of characterization. For low frequencies the circuits consist of standard LC matching networks including variable capacitors for peak tuning. At increasing power levels the output impedance decreases, resulting in higher RF currents in the matching network. This makes the practicality of output impedance measurements in the manner described questionable at power levels higher than 200–300 W for devices operated at 50 V and 150–200 W for devices operated at 28 V. The physical sizes and values required for the components to withstand the RF currents increase to a point where physical construction of the output matching network gets difficult if not impossible. For this reason the output impedances are not given for high power devices such as the MRF154 and MRF157. However, formulas like $\frac{(V_{DS} - V_{sat})^2}{2P_{out}}$ for a single ended design or $\frac{2((V_{DS} - V_{sat})^2)}{P_{out}}$ for a push–pull design can be used to obtain reasonably close approximations to actual values.

MOUNTING OF HIGH POWER RF POWER TRANSISTORS

The package of this device is designed for conduction cooling. It is extremely important to minimize the thermal resistance between the device flange and the heat dissipator.

If a copper heatsink is not used, a copper head spreader is strongly recommended between the device mounting surfaces and the main heatsink. It should be at least 1/4″ thick and extend at least one inch from the flange edges. A thin layer of thermal compound in all interfaces is, of course, essential. The recommended torque on the 4–40 mounting screws should be in the area of 4–5 lbs.–inch, and spring type lock washers along with flat washers are recommended.

For die temperature calculations, the Δ temperature from a corner mounting screw area to the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions (dissipation 150 W and 300 W respectively).

The main heat dissipator must be sufficiently large and have low R_{θ} for moderate air velocity, unless liquid cooling is employed.

CIRCUIT CONSIDERATIONS

At high power levels (500 W and up), the circuit layout becomes critical due to the low impedance levels and high RF currents associated with the output matching. Some of the components, such as capacitors and inductors must also withstand these currents. The component losses are directly proportional to the operating frequency. The manufacturers specifications on capacitor ratings should be consulted on these aspects prior to design.

Push–pull circuits are less critical in general, since the ground referenced RF loops are practically eliminated, and the impedance levels are higher for a given power output. High power broadband transformers are also easier to design than comparable LC matching networks.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$R_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

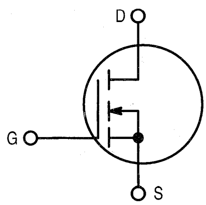
The RF TMOS® Line
Power Field Effect Transistor
N–Channel Enhancement Mode

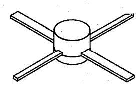
MRF158

**2.0 W, to 500 MHz
TMOS
BROADBAND
RF POWER FET**

Designed for wideband large–signal amplifier and oscillator applications to 500 MHz.

- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 2.0 Watts
  Minimum Gain = 16 dB
  Efficiency = 55% (Typical)
- Grounded Source Package for High Gain and Excellent Heat Dissipation (MRF158R)
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.





CASE 305A–01, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	8.0 45	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

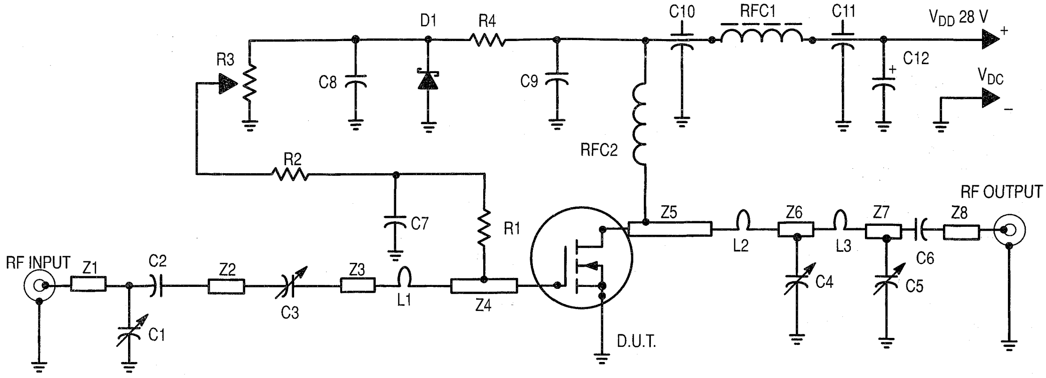
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	13.2	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 6

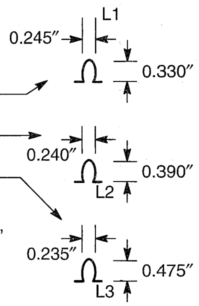
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	0.5	mAdc
Gate–Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 10 mA, V_{DS} = 10 V)	$V_{GS(th)}$	1.0	4.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	50	85	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	4.2	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	0.45	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	G_{ps}	16	20	—	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	η	45	55	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 V, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	Z_{in}	—	8.8 – j27.37	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, P_{out} = 2.0 W, f = 400 MHz, I_{DQ} = 100 mA)	Z_{out}	—	16.96 – j62	—	Ohms



C1, C4, C5 — Johanson Trimmer Capacitor, 2–20 pF
C2, C6 — 270 pF Chip Capacitor
C3 — Arco 404
C7, C8, C9 — 0.1 µF
C10, C11 — 680 pF Feed Through
C12 — 50 µF, 50 V
D1 — 1N5925A Motorola Zener
L1 — #18 AWG, Hairpin 0.825″ long, bend into hairpin
L2 — #18 AWG, Hairpin 0.875″ long, bend into hairpin
L3 — #18 AWG, Hairpin 0.965″ long, bend into hairpin

Board Material — 0.062″, Teflon Fiberglass, 2 oz., Copper clad both sides, $\epsilon_r = 2.55$



R1 — 91 Ω 1/2 Watt
R2 — 10 kΩ 1/2 Watt
R3 — 10 kΩ, 10 Turns Bourns
R4 — 1.8 k 1.4 Watt
RFC1 — Ferroxcube VK200–19/4B
RFC2 — 10 Turns #20 AWG Enameled, 0.250″ ID
Z1 — Microstrip Line 0.150″ wide, 0.420″ long
Z2 — Microstrip Line 0.150″ wide, 0.420″ long
Z3 — Microstrip Line 0.150″ wide, 0.475″ long
Z4 — Microstrip Line 0.150″ wide, 0.825″ long
Z5 — Microstrip Line 0.150″ wide, 0.750″ long
Z6 — Microstrip Line 0.150″ wide, 0.500″ long
Z7 — Microstrip Line 0.150″ wide, 0.500″ long
Z8 — Microstrip Line 0.150″ wide, 0.450″ long

Figure 1. 400 MHz Test Circuit

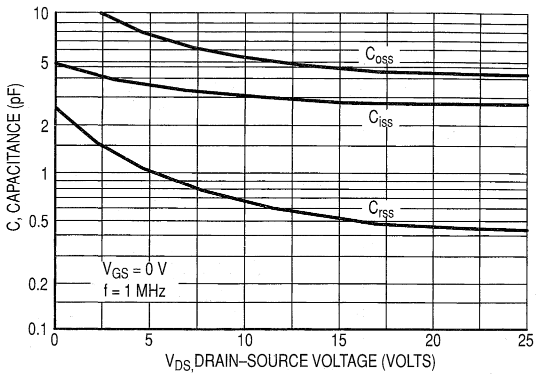


Figure 2. Capacitance versus Drain–Source Voltage

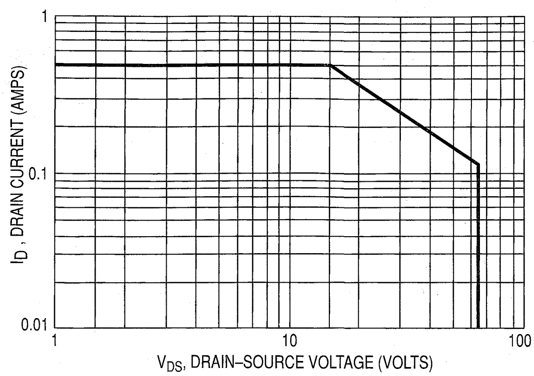


Figure 3. DC Safe Operating Area

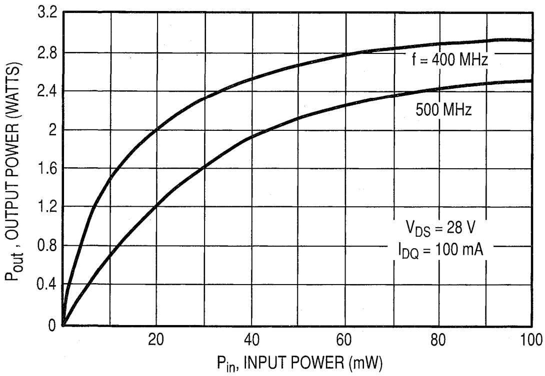


Figure 4. Output Power versus Input Power

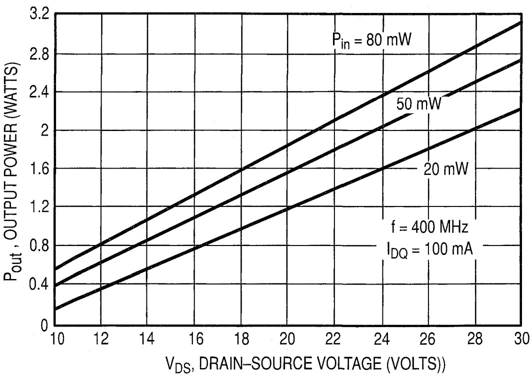


Figure 5. Output Power versus Voltage

Table 1. Typical Common Emitter S–Parameters

V_{DS} (Volts)	I_D (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
28	100	5	1.00	−2.0	3.84	−179	0.003	73	0.97	−2.0
		10	1.00	−2.0	3.81	179	0.004	83	0.97	−2.0
		30	1.00	−7.0	3.74	174	0.011	81	0.97	−6.0
		50	1.00	−11	3.72	170	0.018	78	0.96	−9.0
		100	0.98	−21	3.62	159	0.034	70	0.95	−19
		200	0.93	−41	3.28	137	0.061	52	0.90	−35
		300	0.88	−58	2.88	120	0.077	39	0.86	−50
		400	0.83	−75	2.57	104	0.088	27	0.81	−63
		500	0.79	−87	2.24	91	0.090	17	0.78	−74
		600	0.75	−99	1.94	78	0.084	8.0	0.75	−84
		700	0.73	−110	1.72	68	0.077	2.0	0.75	−93
		800	0.72	−120	1.52	58	0.067	−3.0	0.75	−99
		900	0.71	−130	1.35	48	0.055	−6.0	0.74	−108
		1000	0.71	−139	1.18	40	0.043	−4.0	0.73	−114

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

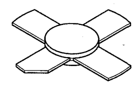
The RF MOSFET Line
Power Field Effect Transistor
N–Channel Enhancement–Mode MOSFET

MRF160

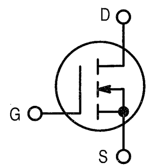
Designed primarily for wideband large–signal output and driver from 30–500 MHz.

- Typical Performance at 400 MHz, 28 Vdc
  Output Power = 4.0 Watts
  Gain = 17 dB
  Efficiency = 50%
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Low C_{rss} – 0.8 pF Typical at V_{DS} = 28 Volts

4.0 W, to 400 MHz
MOSFET BROADBAND
RF POWER FET



CASE 249–06, STYLE 3



MAXIMUM RATINGS *(T_J = 25°C unless otherwise noted)*

Rating	Symbol	Value	Unit
Drain–Gate Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	± 40	Vdc
Drain Current–Continuous	I_D	1.0	ADC
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	24 0.14	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

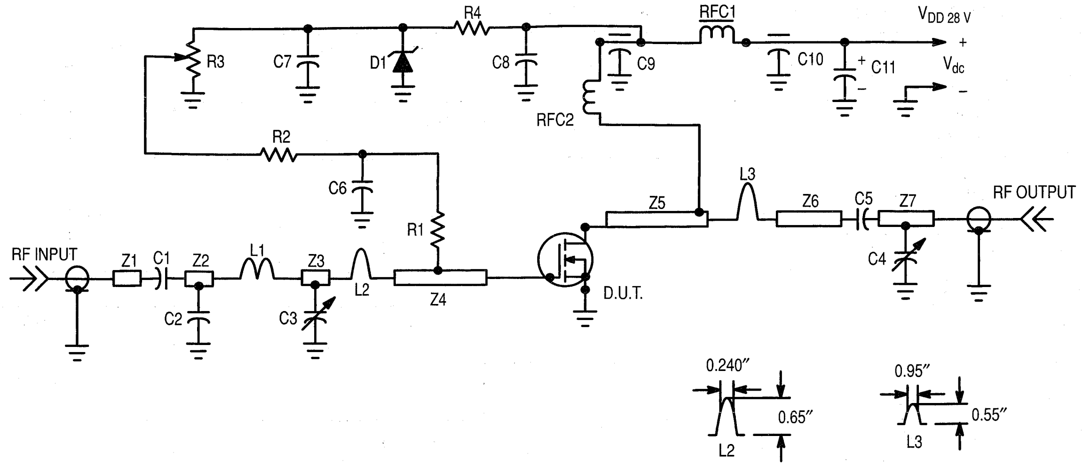
Thermal Resistance — Junction to Case	$R_{\theta JC}$	7.2	°C/W

NOTE: Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{DS} = 0 Vdc, V_{GS} = 0 Vdc, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 V)	I_{DSS}	—	—	0.8	mA
Gate–Source Leakage Current (V_{GS} = 40 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1.0	µA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 10 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain Source On–Voltage ($V_{DS\ (on)}$, V_{GS} = 10 Vdc, I_D = 500 mA)	$V_{DS(on)}$	—	3.8	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 250 mA)	g_{fs}	110	160	—	mS
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	6.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{oss}	—	8.0	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{rss}	—	0.8	—	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 4.0 W, f = 400 MHz, I_{DQ} = 50 mA)	G_{ps}	15	17	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 4.0 W, f = 400 MHz, I_{DQ} = 50 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 4.0 W, f = 400 MHz, I_{DQ} = 50 mA) Load VSWR = 30:1 at All Phase Angles at Frequency of Test	ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 Vdc, P_{out} = 4.0 W, f = 400 MHz, I_{DQ} = 50 mA)	Z_{in}	—	5.23–j 27.2	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 Vdc, P_{out} = 4.0 W, f = 400 MHz, I_{DQ} = 50 mA)	Z_{out}	—	14.7–j 31.2	—	Ohms



C1, C5	220 pF, Chip Capacitor
C2	18 pF, ATC Chip Capacitor
C3	2.0–20 pF, Johanson Trimmer Capacitor
C4	2.0–10 pF, Johanson Trimmer Capacitor
C6, C7, C8	0.1 μF
C9, C10	680 pF, Feed Through
C11	50 μF, 50 V
L1	#20 AWG, 1 Turn 0.255″ ID
L2	#20 AWG, Hairpin 1.3″ long, bend into hairpin
L3	#20 AWG, Hairpin 1.1″ long, bend into hairpin
R1	160 Ω, 1/2 Watt
R2	10 kΩ, 1/2 Watt

R3	10 kΩ, 10 Turns Bourns
R4	1.8 kΩ, 1/4 Watt
RFC1	Ferroxcube VK200–19/4B
RFC2	10 Turns, #20 AWG, Enameled Close Wound, 0.250″ ID
Z1	Microstrip Line 0.167″ wide, 0.820″ long
Z2	Microstrip Line 0.240″ wide, 0.240″ long
Z3	Microstrip Line 0.240″ wide, 0.240″ long
Z4	Microstrip Line 0.230″ wide, 0.590″ long
Z5	Microstrip Line 0.230″ wide, 0.580″ long
Z6	Microstrip Line 0.167″ wide, 0.620″ long
Z7	Microstrip Line 0.167″ wide, 0.800″ long

Board Material 0.060″ Glass Teflon® 2 oz. Copper clad both sides $\varepsilon_r = 2.55$

Figure 1. 400 MHz Test Circuit

Typical Characteristics

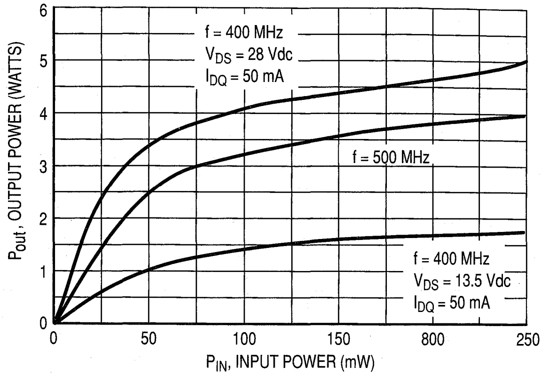


Figure 2. Output Power versus Input Power

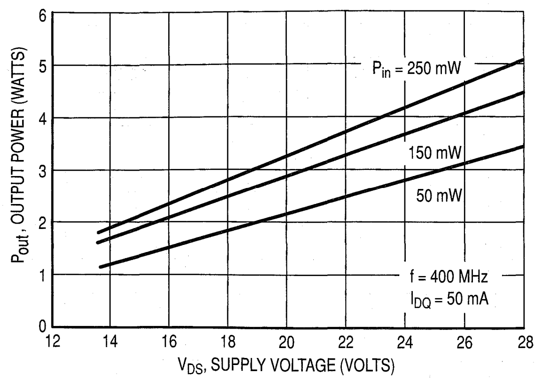


Figure 3. Output Power versus Voltage

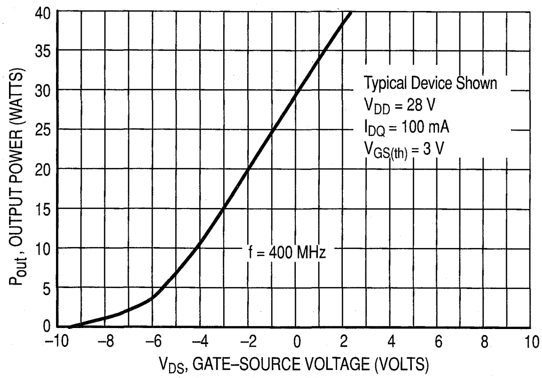


Figure 4. Output Power versus Gate Voltage

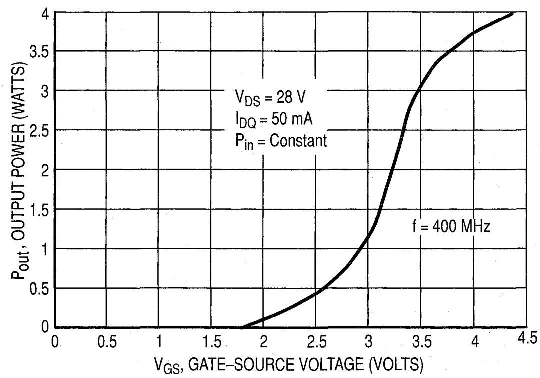


Figure 5. Output Power versus Gate Voltage

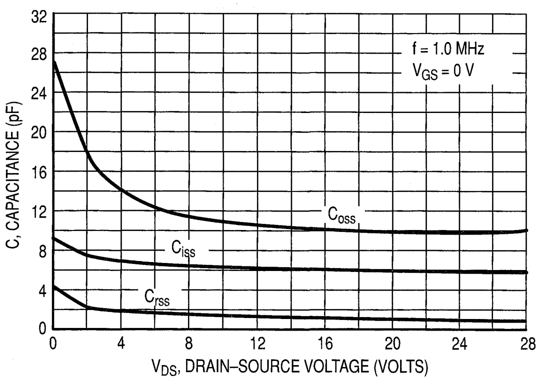


Figure 6. Capacitance versus Drain–Source Voltage

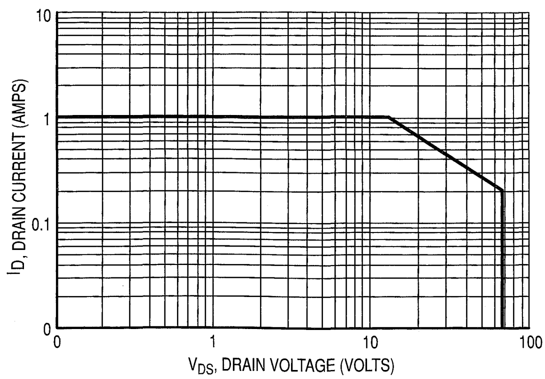


Figure 7. DC Safe Operating Area

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
10	0.96	−2.0	14.47	177	0.01	96	1.11	−5.0
30	0.99	−16	13.34	169	0.02	79	0.92	−11
50	0.97	−28	12.96	159	0.03	70	0.90	−22
75	0.94	−40	12.24	148	0.04	60	0.87	−35
100	0.90	−52	11.40	139	0.05	51	0.84	−45
120	0.87	−61	10.70	132	0.05	45	0.81	−53
150	0.83	−72	9.66	123	0.06	37	0.77	−63
170	0.81	−79	9.05	118	0.06	33	0.75	−69
200	0.78	−88	8.21	110	0.06	26	0.72	−77
220	0.77	−93	7.67	106	0.07	23	0.71	−81
250	0.75	−100	7.00	100	0.07	18	0.69	−87
300	0.72	−110	6.00	92	0.07	12	0.67	−96
350	0.71	−118	5.24	84	0.07	6.0	0.66	−103
390	0.71	−124	4.73	79	0.07	1.0	0.66	−108
400	0.70	−125	4.63	77	0.07	0	0.67	−109
410	0.70	−127	4.52	76	0.07	−1.0	0.66	−110
450	0.70	−131	4.10	71	0.07	−5.0	0.66	−114
470	0.70	−133	3.93	69	0.06	−6.0	0.67	−116
500	0.70	−137	3.68	65	0.06	−8.0	0.67	−118
600	0.71	−145	3.01	55	0.06	−14	0.69	−126
700	0.72	−153	2.51	46	0.05	−18	0.71	−132
800	0.73	−160	2.13	37	0.04	−21	0.73	−137
900	0.75	−166	1.83	30	0.03	−19	0.75	−142
1000	0.76	−171	1.60	23	0.03	−10	0.77	−146
1100	0.77	−177	1.40	16	0.02	3.0	0.79	−151
1200	0.78	177	1.25	10	0.02	18	0.80	−155
1300	0.79	172	1.11	4.0	0.03	29	0.82	−159
1400	0.81	166	1.00	−1.0	0.03	35	0.83	−163
1500	0.81	161	0.90	−6.0	0.03	48	0.85	−166

Table 1. Common Source Scattering Parameters (V_{DS} = 28 Vdc, I_D = 200 mA, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$|S_{11}|$	∠φ	$|S_{21}|$	∠φ	$|S_{12}|$	∠φ	$|S_{22}|$	∠φ
10	0.96	– 4.0	16.09	176	0.01	85	1.08	– 8.0
20	1.00	–15	14.82	171	0.02	82	0.88	–10
30	0.98	– 23	14.64	164	0.03	73	0.89	– 20
50	0.94	– 39	13.76	152	0.04	63	0.86	– 38
85	0.86	– 61	11.81	134	0.06	47	0.79	– 61
150	0.73	– 91	8.63	112	0.08	27	0.70	– 91
170	0.71	– 97	7.90	107	0.09	23	0.68	– 98
200	0.68	–106	6.97	101	0.09	17	0.67	–106
210	0.68	–109	6.68	99	0.09	15	0.66	–108
250	0.66	–117	5.75	92	0.09	10	0.65	–116
300	0.64	–126	4.85	84	0.09	4.0	0.64	–124
350	0.64	–133	4.18	78	0.09	–1.0	0.64	–129
390	0.64	–137	3.75	73	0.09	– 5.0	0.65	–133
400	0.64	–138	3.66	71	0.09	– 6.0	0.65	–134
410	0.64	–140	3.57	70	0.09	–7.0	0.65	–135
450	0.64	–143	3.23	66	0.08	–10	0.66	–138
470	0.65	–145	3.08	64	0.08	–11	0.66	–139
500	0.65	–147	2.88	61	0.08	–13	0.67	–141
550	0.66	–151	2.59	56	0.08	–16	0.67	–144
600	0.67	–154	2.35	52	0.07	–18	0.68	–146
700	0.69	–160	1.96	43	0.07	– 22	0.71	–150
800	0.70	–166	1.67	35	0.06	– 25	0.73	–154
900	0.72	–171	1.43	28	0.05	– 24	0.75	–158
1000	0.74	–177	1.26	22	0.04	– 21	0.77	–161
1100	0.74	178	1.11	16	0.04	–14	0.78	–164
1200	0.76	173	0.99	10	0.04	– 6.0	0.80	–168
1300	0.78	168	0.88	5.0	0.04	2.0	0.81	–171
1400	0.79	163	0.80	0	0.03	8.0	0.83	–174
1500	0.80	158	0.72	– 5.0	0.03	19	0.84	–177

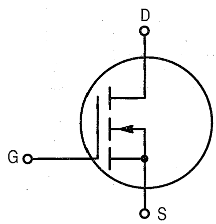
Table 2. Common Source Scattering Parameters (V_{DS} = 12.5 Vdc, I_D = 200 mA, 50 Ω System)

MRF166C

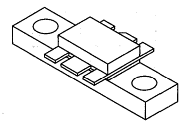
The RF MOSFET Line
RF Power
Field Effect Transistors
N–Channel Enhancement Mode MOSFETs

Designed primarily for wideband large–signal output and driver from 30–500 MHz.

- Low C_{rss} — 4.5 pF @ V_{DS} = 28 V
- MRF166C — Typical Performance at 400 MHz, 28 Vdc
  Output Power = 20 W
  Gain = 17 dB
  Efficiency = 55%
- Replacement for Industry Standards such as MRF136, DV2820, BLF244, SD1902, and ST1001
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



**20 W, 500 MHz
MOSFET
BROADBAND
RF POWER FETs**



CASE 319–07, STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Gate Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Adc
Drain Current — Continuous	I_D	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	70 0.4	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

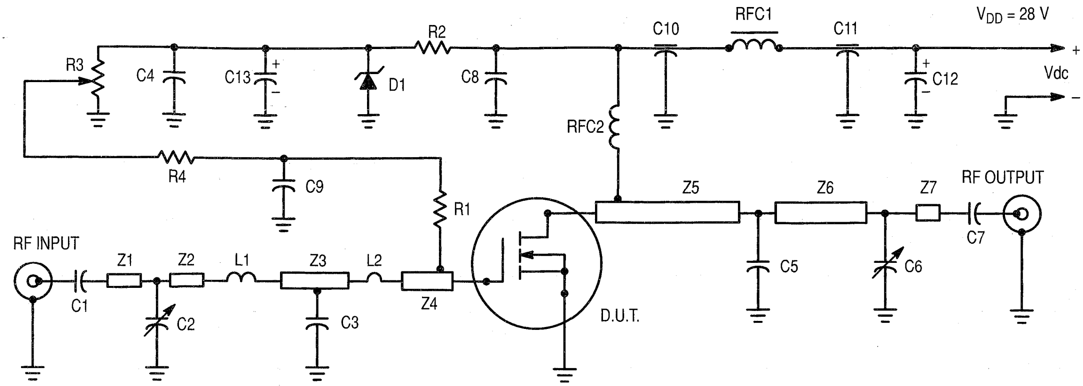
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 V, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	V
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	1.0	mA
Gate–Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0 V)	I_{GSS}	—	—	1.0	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	V
Forward Transconductance (V_{DS} = 10 V, I_D = 1.5 A)	g_{fs}	600	800	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	30	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{oss}	—	35	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{rss}	—	4.5	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DD} = 28 V, f = 30 MHz, I_{DQ} = 50 mA)	NF	—	2.5	—	dB
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 100 mA)	G_{ps}	14	17	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 20 W, f = 400 MHz, I_{DQ} = 100 mA, Load VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			



C1, C7 — 270 pF Chip Capacitor
C2, C6 — Johanson Trimmer Capacitor, 2–20 pF
C3 — 21 pF Mini Unelco
C4, C8, C9 — 0.01 μF
C5 — 18 pF Mini Unelco
C10, C11 — 680 pF Feed Through
C12, C13 — 50 μF, 50 V
D1 — 1N5925A Motorola Zener

Board Material — Teflon fiberglass
2 oz. Copper clad both sides, ε_r = 2.55
0.060″ Dielectric Thickness

L1 — #18 AWG, 2 Turns, 0.25″ ID, 0.15″ Wide
L2 — #18 AWG Hairpin 0.7″ long, bend into hairpin
RFC1 — Ferroxcube VK200–19/4B
RFC2 — 18 Turns #18 AWG Enameled, 0.3″ ID
R1 — 220 Ω 1/2 Watt
R2 — 1.8 kΩ 1/4 Watt
R3 — 10 kΩ, 10 Turns Bourns
R4 — 10 k 1/4 Watt
Z1 — Microstrip Line 0.150″ wide, 0.420″ long
Z2 — Microstrip Line 0.150″ wide, 0.350″ long
Z3 — Microstrip Line 0.150″ wide, 0.350″ long
Z4 — Microstrip Line 0.150″ wide, 0.450″ long
Z5 — Microstrip Line 0.150″ wide, 1.1″ long
Z6 — Microstrip Line 0.150″ wide, 0.650″ long
Z7 — Microstrip Line 0.150″ wide, 0.200″ long

Figure 1. MRF166C 400 MHz Test Circuit

TYPICAL CHARACTERISTICS

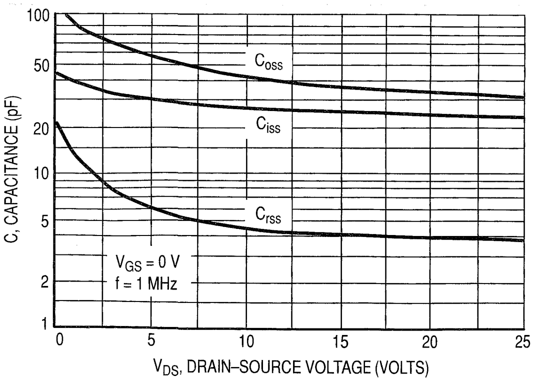


Figure 2. Capacitance versus Drain–Source Voltage

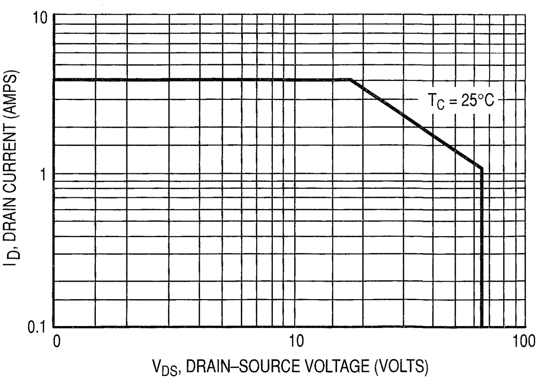


Figure 3. DC Safe Operating Area

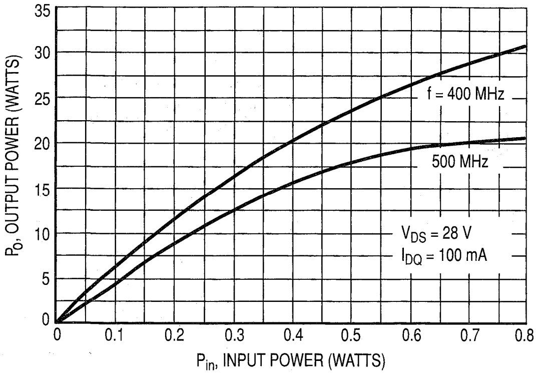


Figure 4. Output Power versus Input Power

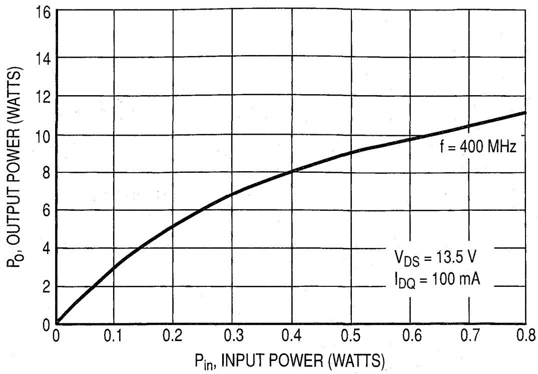


Figure 5. Output Power versus Input Power

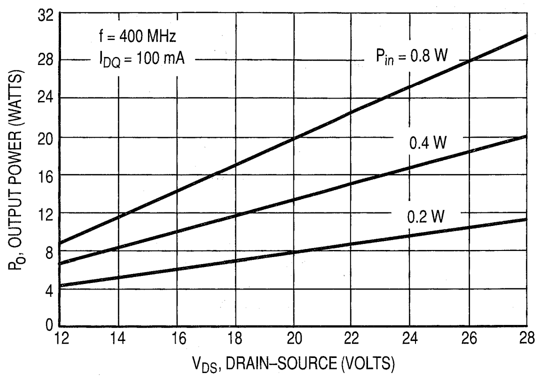
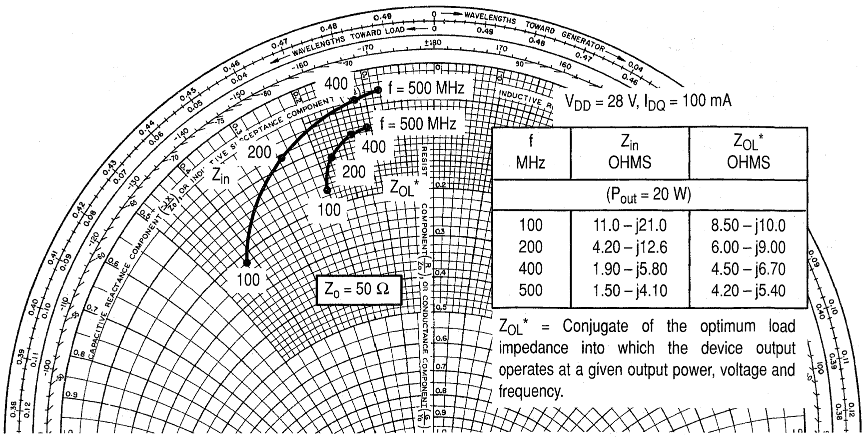


Figure 6. Output Power versus Voltage



f MHz	Z_{in} OHMS	Z_{OL}^* OHMS
	(P_{out} = 20 W)	
100	11.0 – j21.0	8.50 – j10.0
200	4.20 – j12.6	6.00 – j9.00
400	1.90 – j5.80	4.50 – j6.70
500	1.50 – j4.10	4.20 – j5.40

Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 7. Series Equivalent Input and Output Impedance

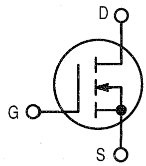
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement Mode MOSFETs

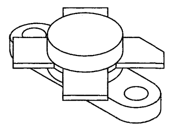
MRF173
MRF173CQ

80 W, 28 V, 175 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFETs

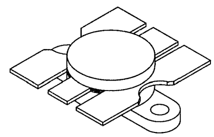
Designed for broadband commercial and military applications up to 200 MHz frequency range. The high–power, high–gain and broadband performance of these devices make possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance at 150 MHz, 28 V:
  Output Power = 80 W
  Gain = 11 dB (13 dB Typ)
  Efficiency = 55% Min. (60% Typ)
- Low Thermal Resistance
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- Low Noise Figure — 1.5 dB Typ at 2.0 A, 150 MHz
- Excellent Thermal Stability; Suited for Class A Operation





CASE 211–11, STYLE 2
(MRF173)



CASE 316–01, STYLE 2
(MRF173CQ)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage	V_{DGO}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	9.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	220 1.26	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Temperature Range	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{DS} = 0 V, V_{GS} = 0 V) I_D = 50 mA	$V_{(BR)DSS}$	65	—	—	V
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	2.0	mA
Gate–Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0 V)	I_{GSS}	—	—	1.0	μA
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.0	3.0	6.0	V
Drain–Source On–Voltage ($V_{DS(on)}$, V_{GS} = 10 V, I_D = 3.0 A)	$V_{DS(on)}$	—	—	1.4	V
Forward Transconductance (V_{DS} = 10 V, I_D = 2.0 A)	g_{fs}	1.8	2.2	—	mhos

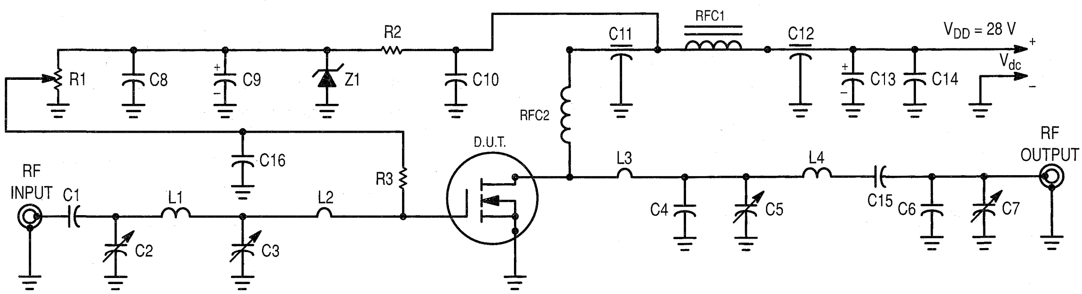
(continued)

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 8

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	110	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{oss}	—	105	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{rss}	—	10	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DD} = 28 V, f = 150 MHz, I_{DQ} = 50 mA)	NF	—	1.5	—	dB
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	G_{ps}	11	13	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	η	55	60	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA) Load VSWR 30:1 at all phase angles	ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA) MRF173	Z_{in}	—	2.99–j4.5	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA) MRF173	Z_{out}	—	2.68–j1.3	—	Ohms
Series Equivalent Input Impedance (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA) MRF173CQ	Z_{in}	—	1.35–j5.15	—	Ohms
Series Equivalent Output Impedance (V_{DD} = 28 V, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA) MRF173CQ	Z_{out}	—	2.72–j149	—	Ohms



C1, C15 — 470 pF Unelco
C2, C3, C5 — 9–180 pF, Arco 463
C4, C6 — 15 pF, Unelco
C7 — 5–80 pF, Arco 462
C8, C10, C14, C16 — 0.1 µF
C9, C13 — 50 µF, 50 Vdc
C11, C12 — 680 pF, Feed Through
L1 — #16 AWG, 1–1/4 Turns, 0.3″ ID
L2 — #16 AWG Hairpin 1″ long
L3 — #14 AWG Hairpin 0.8″ long
L4 — #14 AWG Hairpin 1.1″ long
RFC1 — Ferroxcube VK200–19/4B
RFC2 — 18 Turns #18 AWG Enameled, 0.3″ ID
R1 — 10 kΩ, 10 Turns Bourns
R2 — 1.8 kΩ, 1/4 W
R3 — 10 kΩ, 1/2 W
Z1 — 1N5925A Motorola Zener

Figure 1. 150 MHz Test Circuit

TYPICAL CHARACTERISTICS

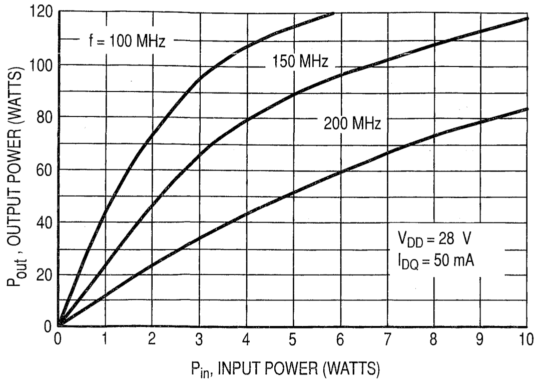


Figure 2. Output Power versus Input Power

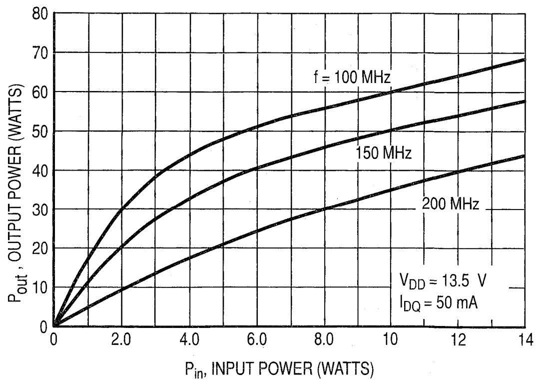


Figure 3. Output Power versus Input Power

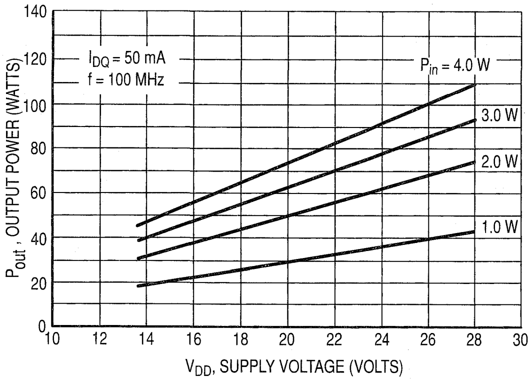


Figure 4. Output Power versus Supply Voltage

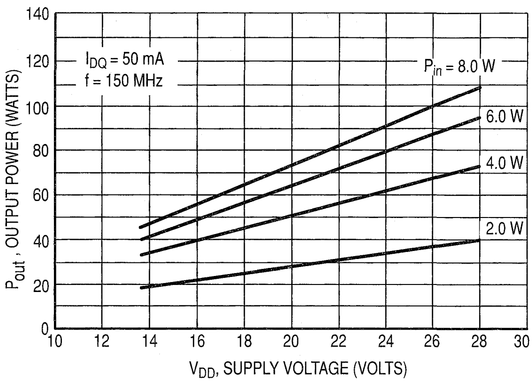


Figure 5. Output Power versus Supply Voltage

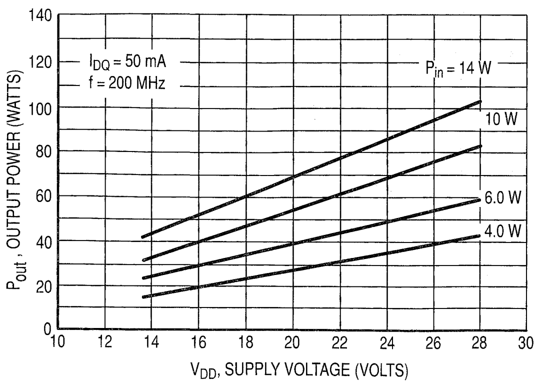


Figure 6. Output Power versus Supply Voltage

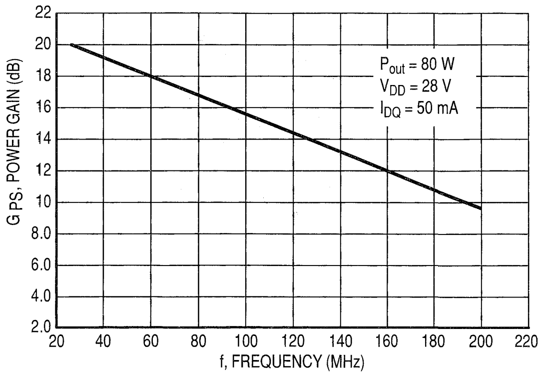


Figure 7. Power Gain versus Frequency

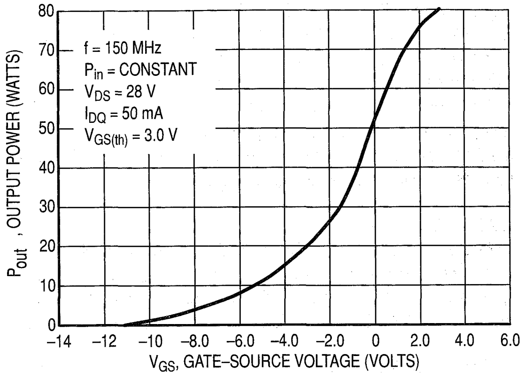


Figure 8. Output Power versus Gate Voltage

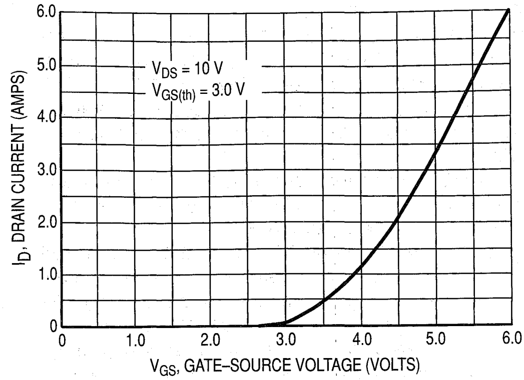


Figure 9. Drain Current versus Gate Voltage

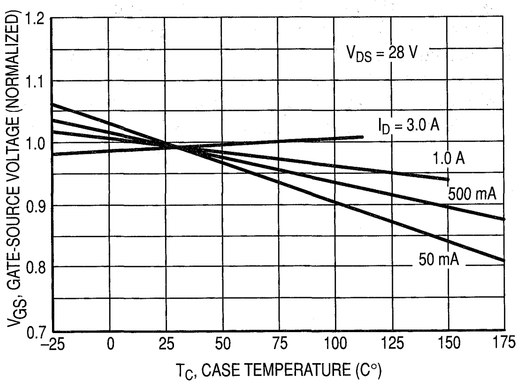


Figure 10. Gate–Source Voltage versus Case Temperature

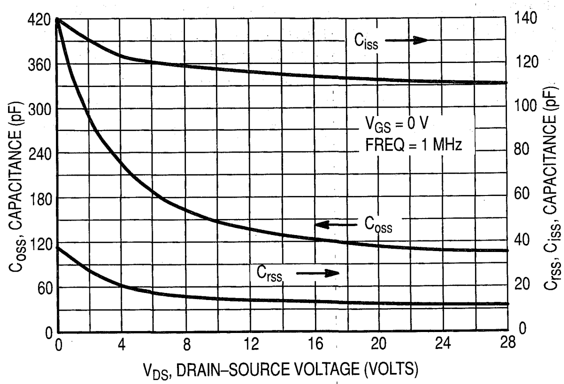


Figure 11. Capacitance versus Drain Voltage

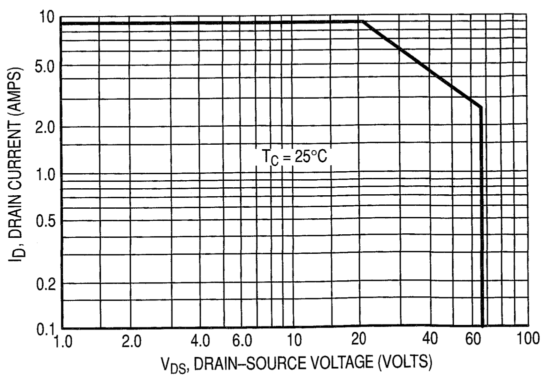


Figure 12. DC Safe Operating Area

DESIGN CONSIDERATIONS

The MRF173/CQ is a RF MOSFET power N–channel enhancement mode field–effect transistor (FET) designed for VHF power amplifier applications. Motorola's RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF173/CQ is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF173/CQ was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF173/CQ may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (see Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF173/CQ. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOSFETs helps ease the task of broadband network design. Both small–signal scattering parameters and large–signal impedances are provided. While the s–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

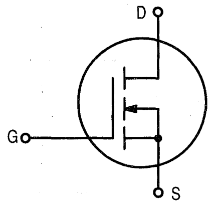
The RF MOSFET Line
RF Power Field Effect Transistor
N–Channel Enhancement–Mode

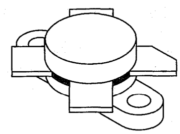
MRF174

. . . designed primarily for wideband large–signal output and driver stages up to 200 MHz frequency range.

- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 125 Watts
  Minimum Gain = 9.0 dB
  Efficiency = 50% (Min)
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 3.0 dB Typ at 2.0 A, 150 MHz

125 W, to 200 MHz
N–CHANNEL MOS
BROADBAND RF POWER
FET





CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	13	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

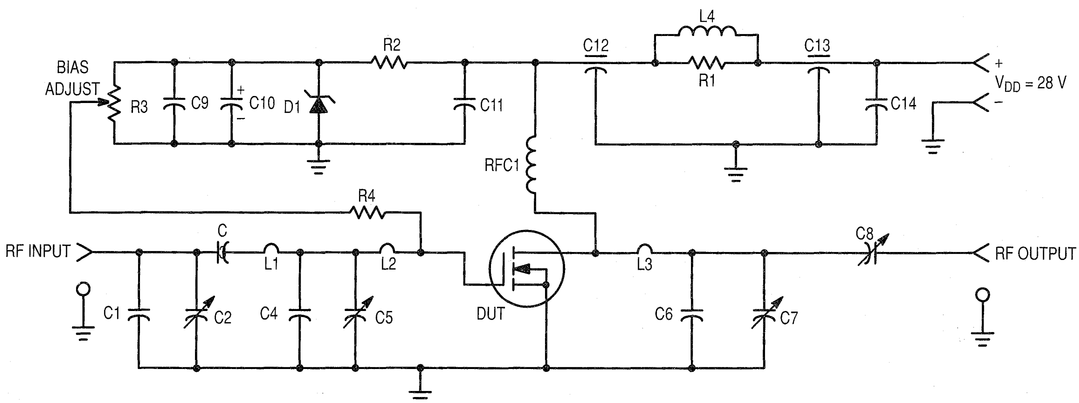
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	10	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3.0 A)	g_{fs}	1.75	2.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	175	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	190	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	40	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DD} = 28 Vdc, I_D = 2.0 A, f = 150 MHz)	NF	—	3.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA)	G_{ps}	9.0	11.8	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA)	η	50	60	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			



C1 — 15 pF Unelco
C2 — Arco 462, 5.0–80 pF
C3 — 100 pF Unelco
C4 — 25 pF Unelco
C6 — 40 pF Unelco
C7 — Arco 461, 2.7–30 pF
C5, C8 — Arco 463, 9.0–180 pF
C9, C11, C14 — 0.1 μF Erie Redcap
C10 — 50 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — #16 AWG, 1–1/4 Turns, 0.213″ ID
L2 — #16 AWG, Hairpin 0.25″ 0.062″
L3 — #14 AWG, Hairpin 0.47″ 0.2″
L4 — 10 Turns #16 AWG Enameled Wire on R1
RFC1 — 18 Turns #16 AWG Enameled Wire, 0.3″ ID
R1 — 10 Ω, 2.0 W
R2 — 1.8 kΩ, 1/2 W
R3 — 10 kΩ, 10 Turn Bourns
R4 — 10 kΩ, 1/4 W

Figure 1. 150 MHz Test Circuit

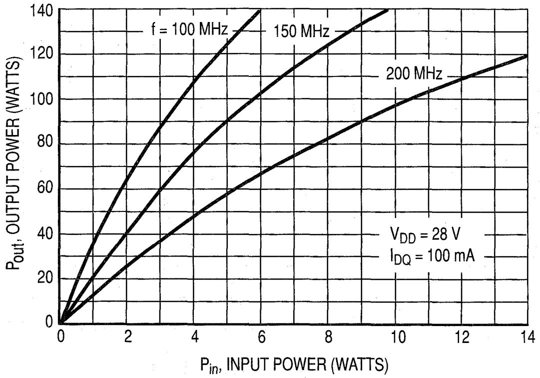


Figure 2. Output Power versus Input Power

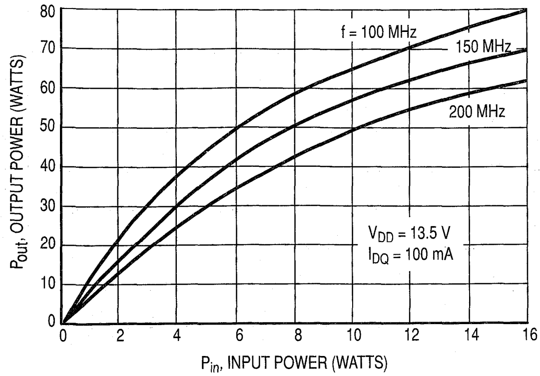


Figure 3. Output Power versus Input Power

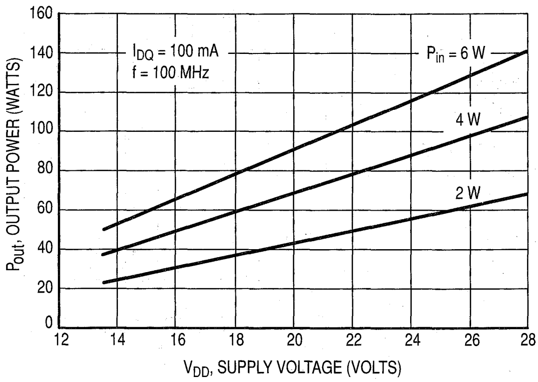


Figure 4. Output Power versus Supply Voltage

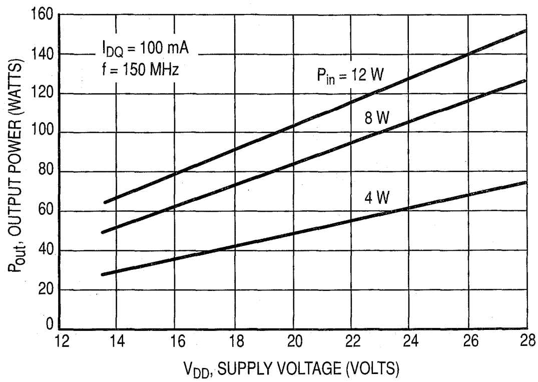


Figure 5. Output Power versus Supply Voltage

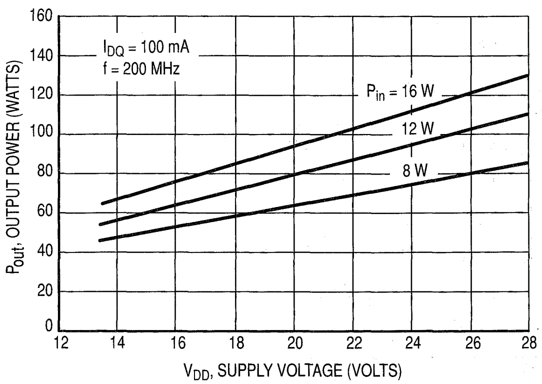


Figure 6. Output Power versus Supply Voltage

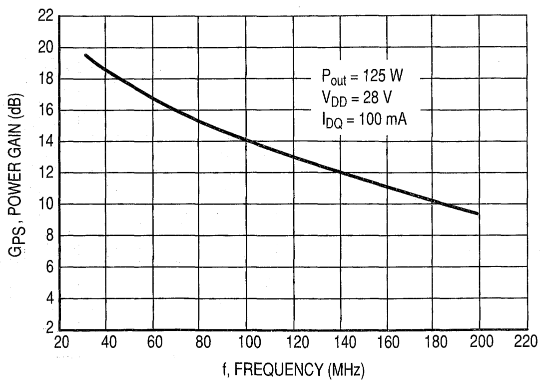


Figure 7. Power Gain versus Frequency

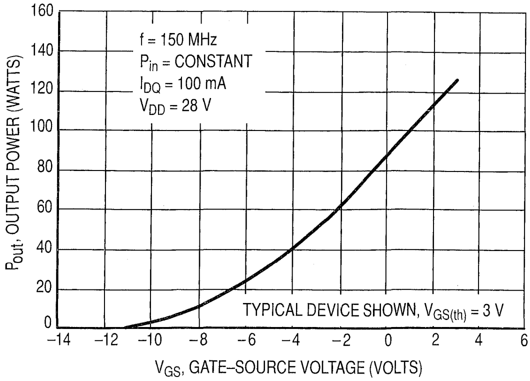


Figure 8. Output Power versus Gate Voltage

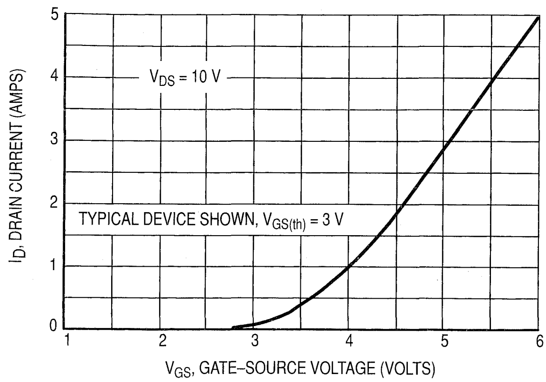


Figure 9. Drain Current versus Gate Voltage (Transfer Characteristics)

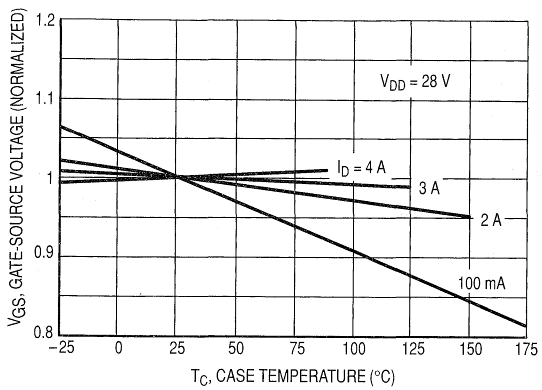


Figure 10. Gate–Source Voltage versus Case Temperature

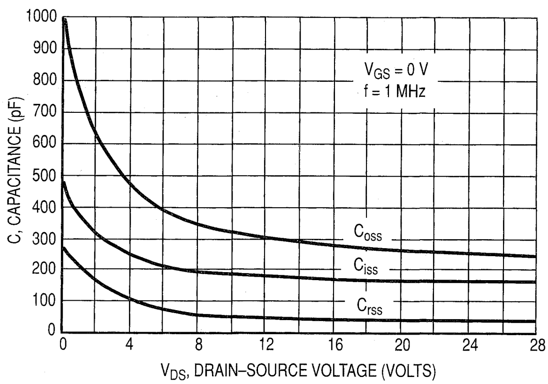


Figure 11. Capacitance versus Drain Voltage

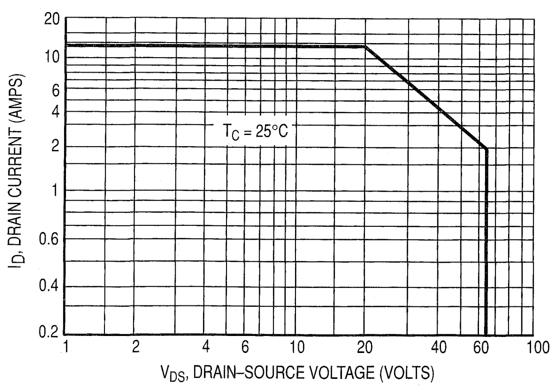


Figure 12. DC Safe Operating Area

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
2.0	0.932	−133	74.0	112	0.011	23	0.835	−151
5.0	0.923	−160	31.6	98	0.011	12	0.886	−168
10	0.921	−170	16.0	93	0.011	10	0.896	−174
20	0.921	−175	8.00	88	0.011	12	0.899	−177
30	0.921	−177	5.32	86	0.011	16	0.900	−178
40	0.921	−177	3.98	83	0.012	21	0.901	−178
50	0.922	−178	3.17	81	0.012	26	0.902	−178
60	0.923	−178	2.63	79	0.012	30	0.903	−178
70	0.924	−178	2.24	77	0.013	34	0.904	−178
80	0.925	−178	1.95	75	0.013	39	0.906	−178
90	0.927	−178	1.72	73	0.014	43	0.907	−178
100	0.930	−178	1.50	71	0.016	45	0.910	−178
110	0.930	−178	1.31	70	0.018	46	0.912	−178
120	0.931	−178	1.19	68	0.019	47	0.914	−178
130	0.942	−178	1.10	67	0.019	49	0.919	−178
140	0.936	−178	1.01	66	0.021	50	0.921	−178
150	0.938	−178	0.936	65	0.021	53	0.922	−178
160	0.938	−178	0.879	64	0.022	53	0.923	−178
170	0.940	−178	0.830	63	0.023	54	0.923	−177
180	0.942	−178	0.780	61	0.024	56	0.924	−177
190	0.942	−178	0.737	60	0.026	59	0.928	−177
200	0.952	−178	0.705	59	0.027	58	0.929	−177
210	0.950	−178	0.668	57	0.029	61	0.934	−177
220	0.942	−178	0.626	56	0.030	61	0.933	−177
230	0.943	−178	0.592	56	0.032	62	0.939	−177
240	0.946	−177	0.566	55	0.033	64	0.941	−177
250	0.952	−177	0.545	54	0.035	64	0.943	−177
260	0.958	−177	0.523	53	0.036	65	0.946	−177
270	0.956	−177	0.500	52	0.038	67	0.943	−177
280	0.960	−177	0.481	52	0.039	68	0.946	−177
290	0.956	−178	0.460	51	0.042	68	0.944	−177
300	0.955	−178	0.443	50	0.043	68	0.947	−177

Table 1. Common Source Scattering Parameters
V_{DS} = 28 V, I_D = 3.0 A

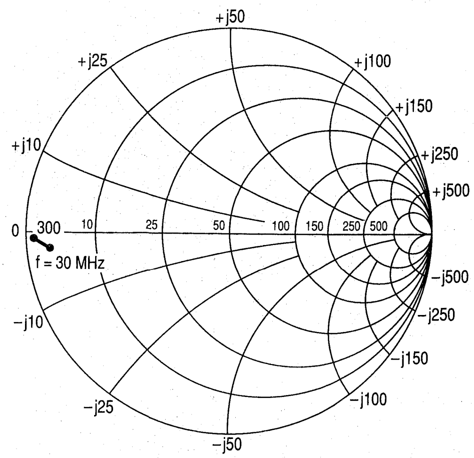


Figure 13. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A

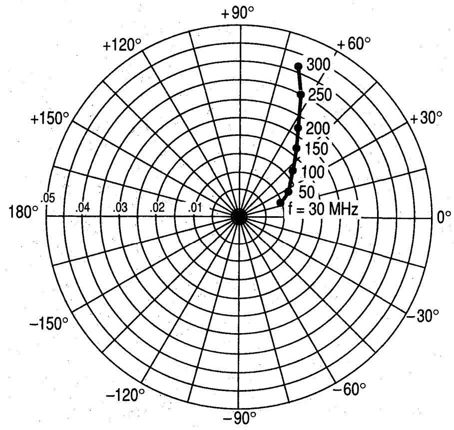


Figure 14. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A

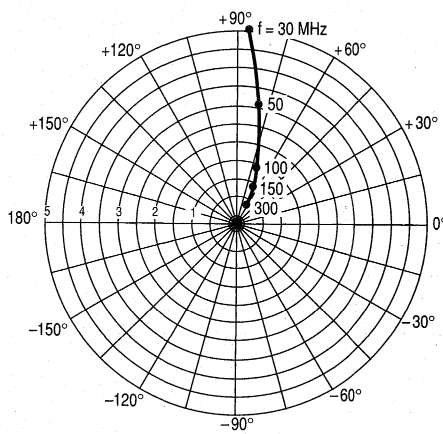


Figure 15. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A

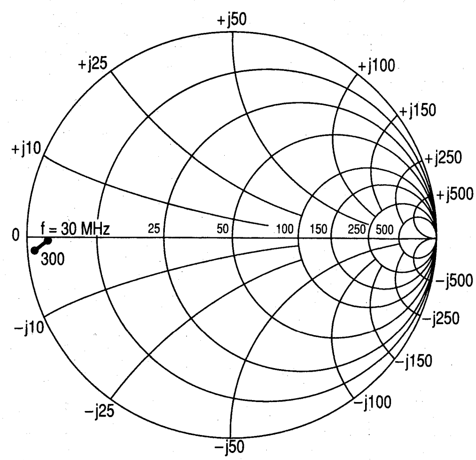
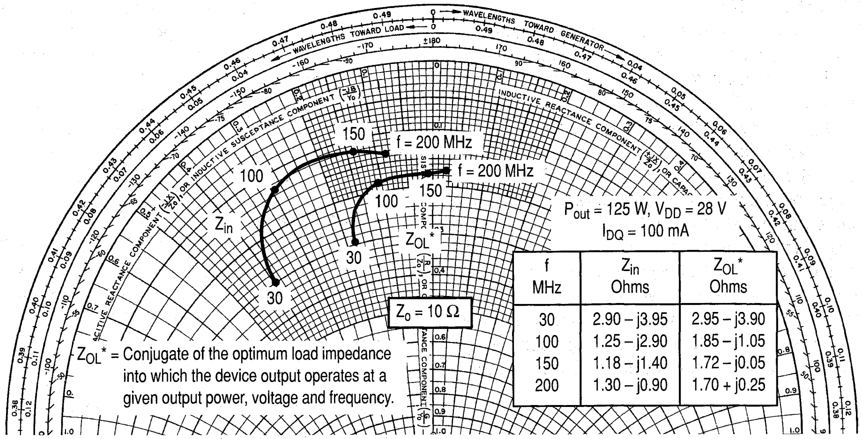


Figure 16. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V, I_D = 3.0 A



f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
30	2.90 – j3.95	2.95 – j3.90
100	1.25 – j2.90	1.85 – j1.05
150	1.18 – j1.40	1.72 – j0.05
200	1.30 – j0.90	1.70 + j0.25

Figure 17. Series Equivalent Input/Output Impedance, Z_{in}, Z_{OL}^*

DESIGN CONSIDERATIONS

The MRF174 is a RF power N–Channel enhancement mode field–effect transistor (FET) designed especially for UHF power amplifier and oscillator applications. Motorola RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove vertical power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF174 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF174 was characterized at I_{DQ} = 100 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF174 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

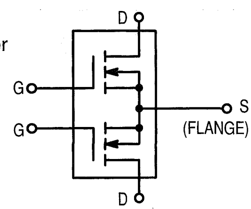
Impedance matching networks similar to those used with bipolar UHF transistors are suitable for MRF174. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOSFETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

The RF MOSFET Line
RF Power Field-Effect Transistors
N–Channel Enhancement–Mode

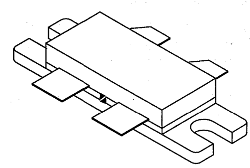
MRF175GU
MRF175GV

Designed for broadband commercial and military applications using push pull circuits at frequencies to 500 MHz. The high power, high gain and broadband performance of these devices makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance
  - MRF175GV @ 28 V, 225 MHz ("V" Suffix)
    - Output Power — 200 Watts
    - Power Gain — 14 dB Typ
    - Efficiency — 65% Typ
  - MRF175GU @ 28 V, 400 MHz ("U" Suffix)
    - Output Power — 150 Watts
    - Power Gain — 12 dB Typ
    - Efficiency — 55% Typ
- 100% Ruggedness Tested At Rated Output Power
- Low Thermal Resistance
- Low C_{rss} — 20 pF Typ @ V_{DS} = 28 V



200/150 WATTS, 28 V, 500 MHz
N–CHANNEL MOS
BROADBAND
RF POWER FETs



CASE 375–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	26	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	400 2.27	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.5	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc

(continued)

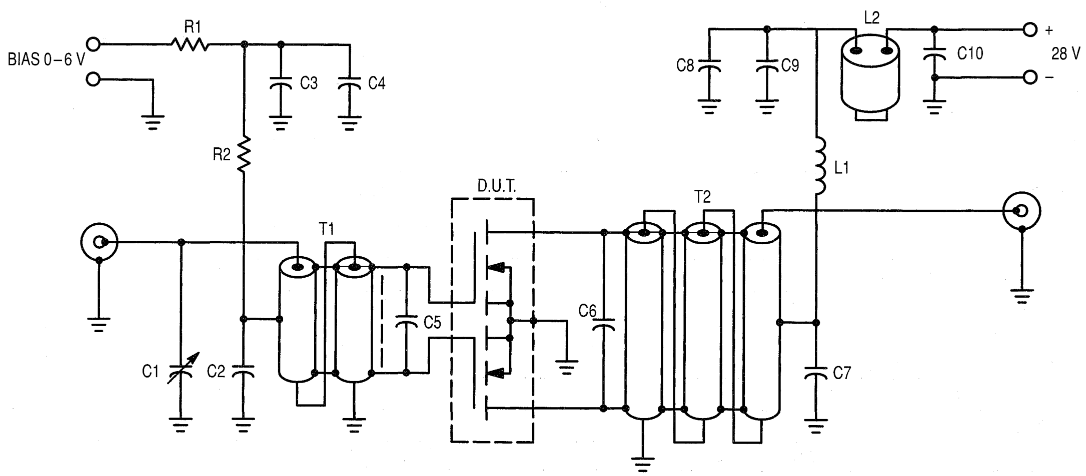
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 5.0 A)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	2.0	3.0	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	180	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	200	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	20	—	pF
FUNCTIONAL CHARACTERISTICS — MRF175GV (2) (Figure 1)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA)	G_{ps}	12	14	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA)	η	55	65	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each side of device measured separately.
2. Measured in push–pull configuration.



C1 — Arco 404, 8.0–60 pF
C2, C3, C7, C8 — 1000 pF Chip
C4, C9 — 0.1 µF Chip
C5 — 180 pF Chip
C6 — 100 pF and 130 pF Chips in Parallel
C10 — 0.47 µF Chip, Kemet 1215 or Equivalent
L1 — 10 Turns AWG #16 Enamel Wire, Close Wound, 1/4″ I.D.
L2 — Ferrite Beads of Suitable Material for 1.5–2.0 µH Total Inductance

Board material — .062″ fiberglass (G10), Two sided, 1 oz. copper, $\varepsilon_r \cong 5$

Unless otherwise noted, all chip capacitors are ATC Type 100 or Equivalent.

R1 — 100 Ohms, 1/2 W
R2 — 1.0 k Ohm, 1/2 W
T1 — 4:1 Impedance Ratio RF Transformer. Can Be Made of 25 Ohm Semirigid Coax, 47–52 Mils O.D.
T2 — 1:9 Impedance Ratio RF Transformer. Can Be Made of 15–18 Ohms Semirigid Coax, 62–90 Mils O.D.

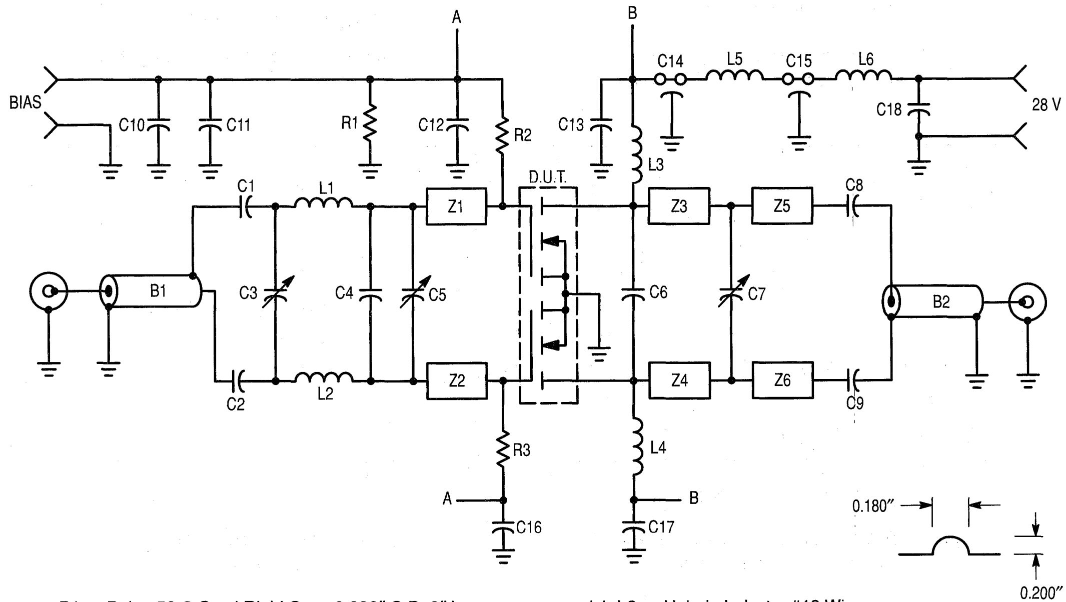
NOTE: For stability, the input transformer T1 should be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

Figure 1. 225 MHz Test Circuit

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS — MRF175GU (1) (Figure 2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA)	G_{ps}	10	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTE:
1. Measured in push–pull configuration.



B1 — Balun 50 Ω Semi Rigid Coax 0.086″ O.D. 2″ Long
B2 — Balun 50 Ω Semi Rigid Coax 0.141″ O.D. 2″ Long
C1, C2, C8, C9 — 270 pF ATC Chip Cap
C3, C5, C7 — 1.0–20 pF Trimmer Cap
C4 — 15 pF ATC Chip Cap
C6 — 33 pF ATC Chip Cap
C10, C12, C13, C16, C17 — 0.01 µF Ceramic Cap
C11 — 1.0 µF 50 V Tantalum
C14, C15 — 680 pF Feedthru Cap
C18 — 20 µF 50 V Tantalum

L1, L2 — Hairpin Inductor #18 Wire
L3, L4 — 12 Turns #18 Enameled Wire 0.340″ I.D.
L5 — Ferroxcube VK200 20/4B
L6 — 3 Turns #16 Enameled Wire 0.340″ I.D.
R1 — 1.0 kΩ 1/4 W Resistor
R2, R3 — 10 kΩ 1/4 W Resistor
Z1, Z2 — Microstrip Line 0.400″ x 0.250″
Z3, Z4 — Microstrip Line 0.870″ x 0.250″
Z5, Z6 — Microstrip Line 0.500″ x 0.250″
Board material — 0.060″ Teflon–fiberglass, ε_r = 2.55, copper clad both sides, 2 oz. copper.

Figure 2. 400 MHz Test Circuit

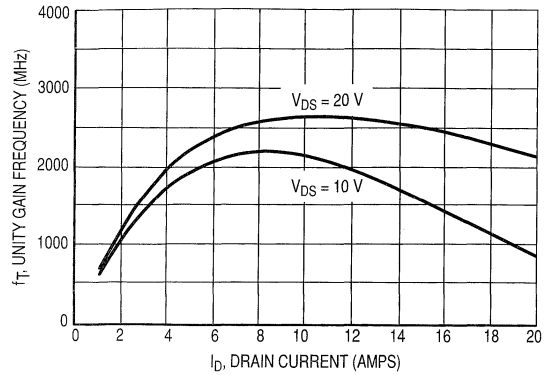


Figure 3. Common Source Unity Current Gain Frequency versus Drain Current

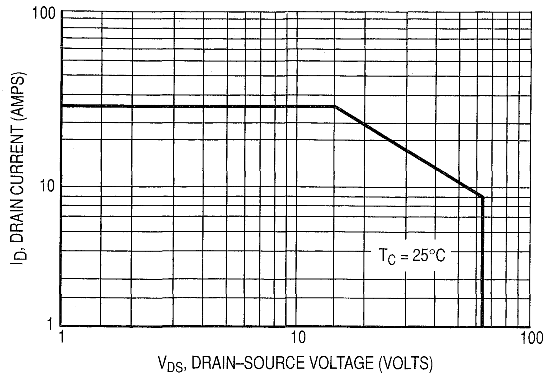


Figure 4. DC Safe Operating Area

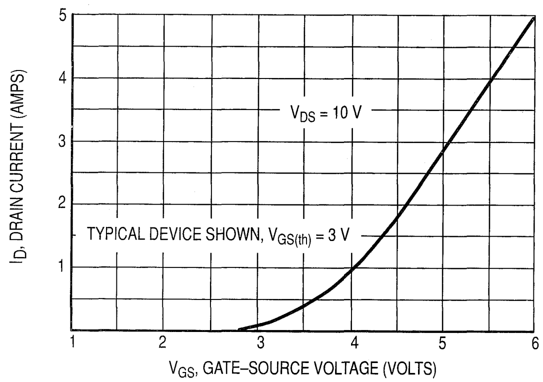


Figure 5. Drain Current versus Gate Voltage (Transfer Characteristics)

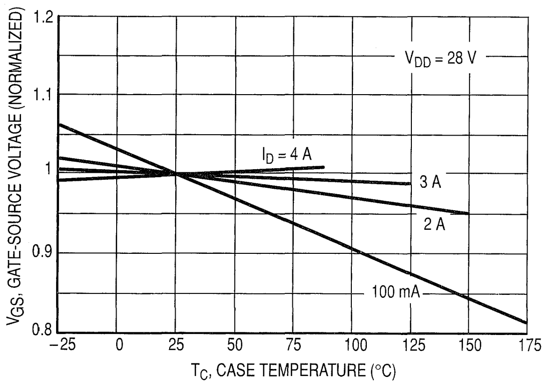


Figure 6. Gate–Source Voltage versus Case Temperature

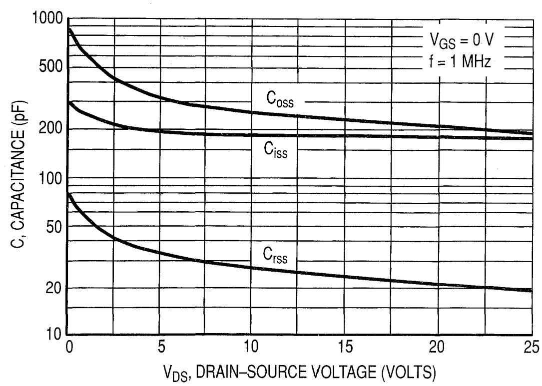


Figure 7. Capacitance versus Drain–Source Voltage*

* Data shown applies to each half of MRF175GU/GV.

TYPICAL CHARACTERISTICS
MRF175GV

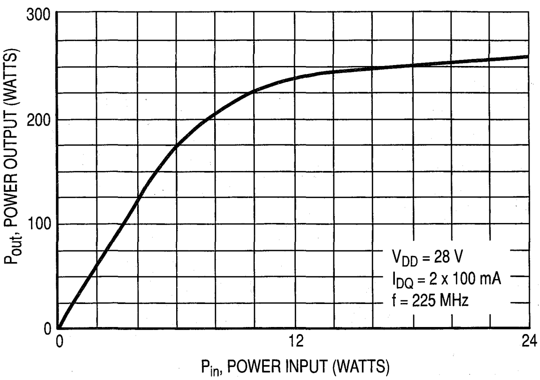


Figure 8. Power Input versus Power Output

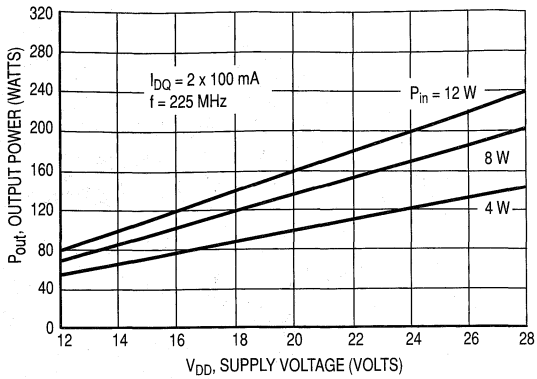


Figure 9. Output Power versus Supply Voltage

MRF175GU

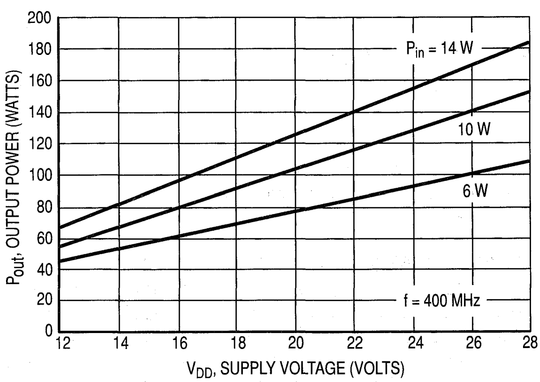


Figure 10. Output Power versus Supply Voltage

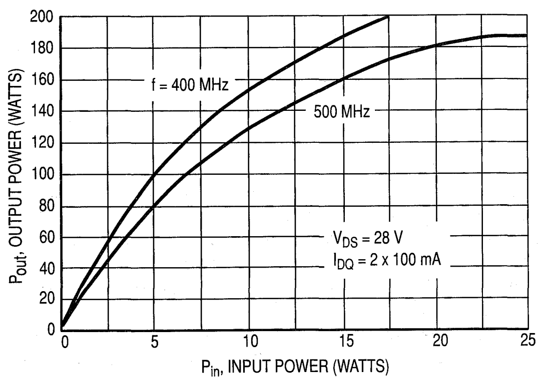


Figure 11. Output Power versus Input Power

MRF175GV

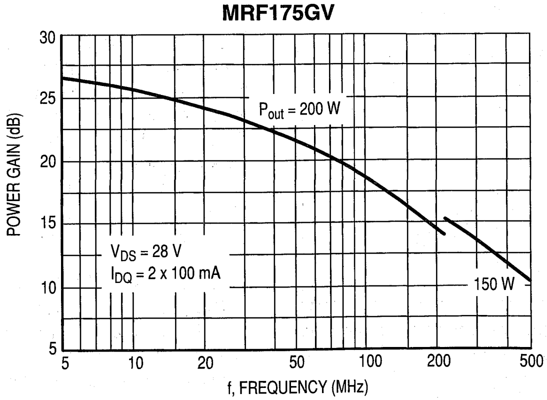
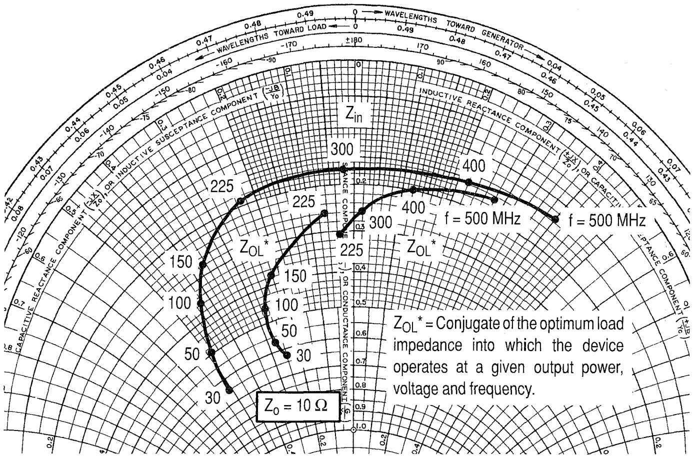


Figure 12. Power Gain versus Frequency

INPUT AND OUTPUT IMPEDANCE



V_{DD} = 28 V, I_{DQ} = 2 x 100 mA

f MHz	Z_{in} OHMS	Z_{OL}* OHMS
(P_{out} = 150 W)		
225	1.95 – j2.30	3.10 – j0.25
300	1.75 – j0.20	2.60 + j0.20
400	1.60 + j2.20	2.00 + j1.20
500	1.35 + j4.00	1.70 + j2.70
(P_{out} = 200 W)		
30	6.50 – j5.10	6.30 – j2.50
50	5.00 – j4.80	5.75 – j2.75
100	3.60 – j4.20	4.60 – j2.65
150	2.80 – j3.60	2.60 – j2.20
225	1.95 – j2.30	2.60 – j0.60

NOTE: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

Figure 13. Series Equivalent Input/Output Impedance

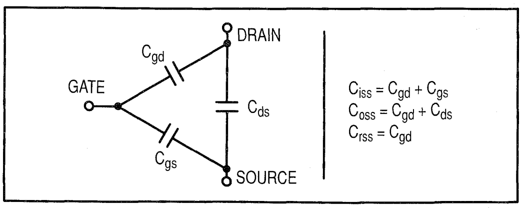
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



The C_{iss} given in the electrical characteristics table was measured using method 2 above. It should be noted that C_{iss}, C_{oss}, C_{rss} are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain, data presented in Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of this device are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

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The MRF175G is a RF power N–channel enhancement mode field–effect transistor (FETs) designed for HF, VHF and UHF power amplifier applications. Motorola RF MOSFETs feature a vertical structure with a planar design.

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The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF175G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF175G was characterized at I_{DQ} = 100 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

GAIN CONTROL

Power output of the MRF176 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

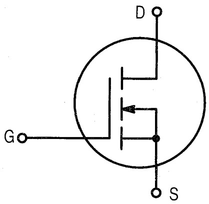
The RF MOSFET Line
RF Power Field-Effect Transistors
N–Channel Enhancement–Mode

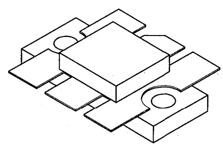
MRF175LU
MRF175LV

100 W, 28 V, 400 MHz
N–CHANNEL
BROADBAND
RF POWER FETs

Designed for broadband commercial and military applications using single ended circuits at frequencies to 400 MHz. The high power, high gain and broadband performance of each device makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Guaranteed Performance
  MRF175LU @ 28 V, 400 MHz ("U" Suffix)
    Output Power — 100 Watts
    Power Gain — 10 dB Typ
    Efficiency — 55% Typ
  MRF175LV @ 28 V, 225 MHz ("V" Suffix)
    Output Power — 100 Watts
    Power Gain — 14 dB Typ
    Efficiency — 65% Typ
- 100% Ruggedness Tested At Rated Output Power
- Low Thermal Resistance
- Low C_{rss} — 20 pF Typ @ V_{DS} = 28 V





CASE 333–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	13	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.5	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	µAdc

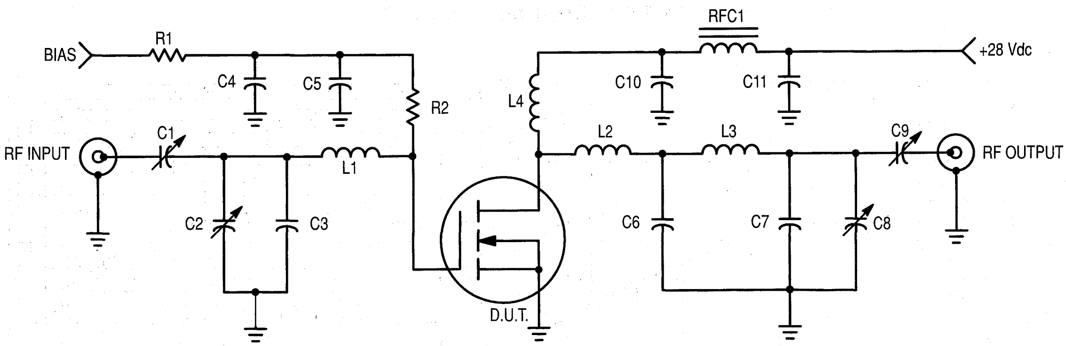
(continued)

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 8

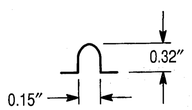
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 5.0 A)	$V_{DS(on)}$	0.1	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	2.0	3.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	180	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	200	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	20	—	pF
FUNCTIONAL CHARACTERISTICS — MRF175LV (Figure 1)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 225 MHz, I_{DQ} = 100 mA)	G_{ps}	12	14	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 225 MHz, I_{DQ} = 100 mA)	η	55	65	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 225 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
FUNCTIONAL CHARACTERISTICS — MRF175LU (Figure 2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 100 mA)	G_{ps}	8.0	10	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			



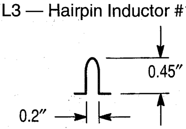
C1, C2, C8 — Arco 463 or Equivalent
C3, C7 — 25 pF Unelco Cap
C4 — 1000 pF Chip Cap
C5 — 0.01 µF Chip Cap
C6 — 250 pF Unelco Cap
C9 — Arco 462 or Equivalent
C10 — 1000 pF ATC Chip Cap
C11 — 10 µF 100 V Electrolytic

L1 — Hairpin Inductor #18 Wire



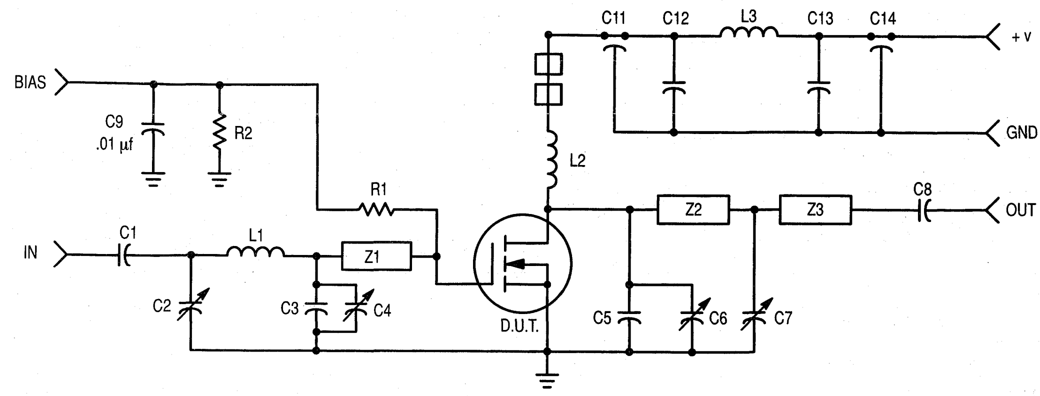
L2 — Stripline Inductor 0.200″ x 0.500″

L3 — Hairpin Inductor #16 Wire



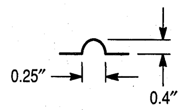
L4 — 2 Turns #16 Wire 5/16″ ID
RFC1 — VK200–4B
R1 — 1.0 k 1/4 W Resistor
R2 — 100 Ω Resistor

Figure 1. 225 MHz Test Circuit



C1, C8 — 270 pF ATC Chip Cap
C2, C4, C6, C7 — 1.0–20 pF Trimmer Cap
C3 — 15 pF Mini Unelco Cap
C5 — 33 pF Mini Unelco Cap
C9, C12 — 0.1 µF Ceramic Cap
C11, C14 — 680 pF Feed Thru Cap
C13 — 50 µF Tantalum Cap

L1 — Hairpin Inductor #18 Wire



L2 — 12 Turns #18 Wire 0.450″ ID
L3 — Ferroxcube VK200 20/4B

R1 — 10 k 1/4 W Resistor
R2 — 1 k 1/4 W Resistor
R3 — 1.5 k 1/4 W Resistor
Z1 — Microstrip Line 0.950″ x 0.250″
Z2 — Microstrip Line 1″ x 0.250″
Z3 — Microstrip Line 0.550″ x 0.250″
Board Material — 0.062″ Teflon — fiberglass, ε_r = 2.56, 1 oz. copper clad both sides

Figure 2. 400 MHz Test Circuit

TYPICAL CHARACTERISTICS

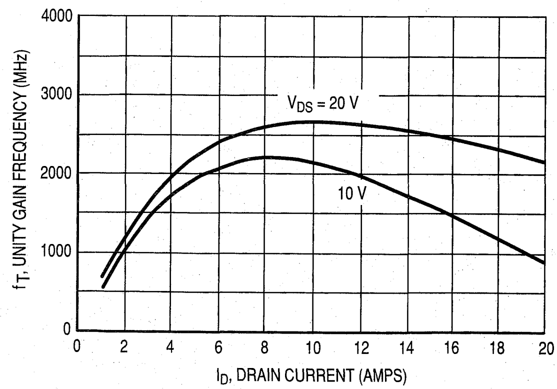


Figure 3. Common Source Unity Current Gain Frequency versus Drain Current

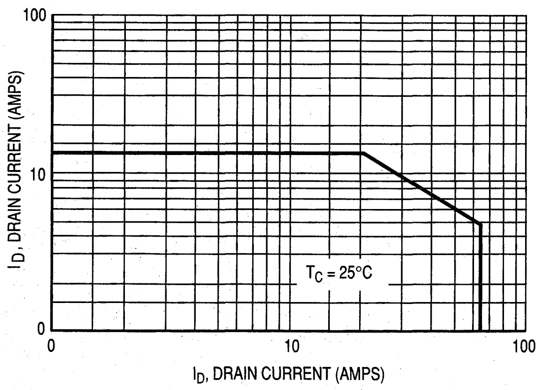


Figure 4. DC Safe Operating Area

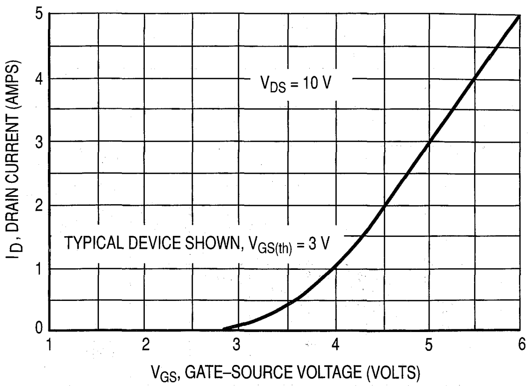


Figure 5. Drain Current versus Gate Voltage (Transfer Characteristics)

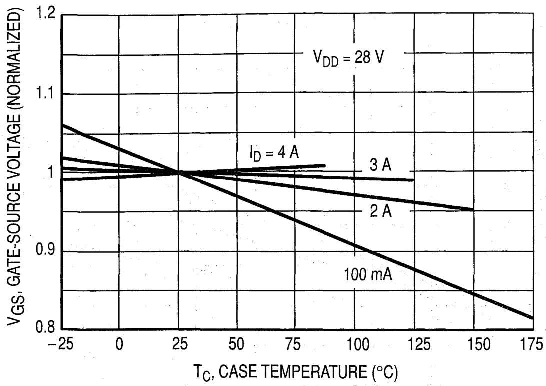


Figure 6. Gate–Source Voltage versus Case Temperature

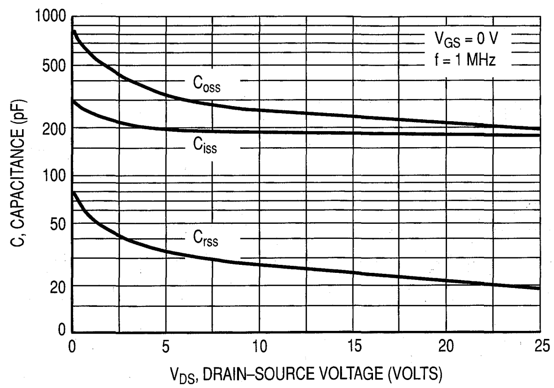


Figure 7. Capacitance versus Drain–Source Voltage

TYPICAL CHARACTERISTICS

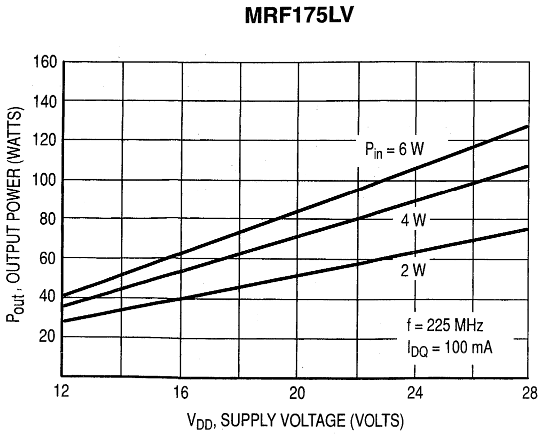


Figure 8. Output Power versus Supply Voltage

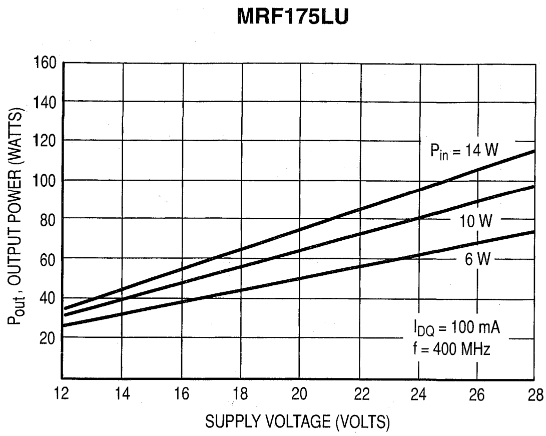


Figure 9. Output Power versus Supply Voltage

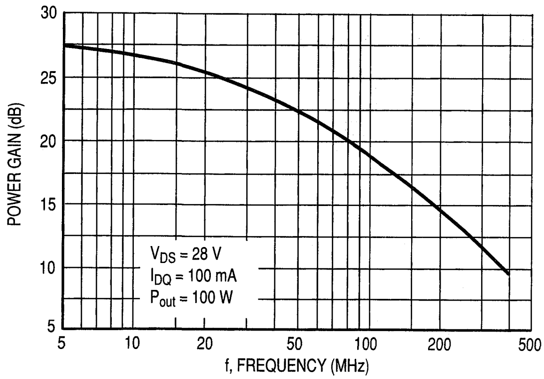
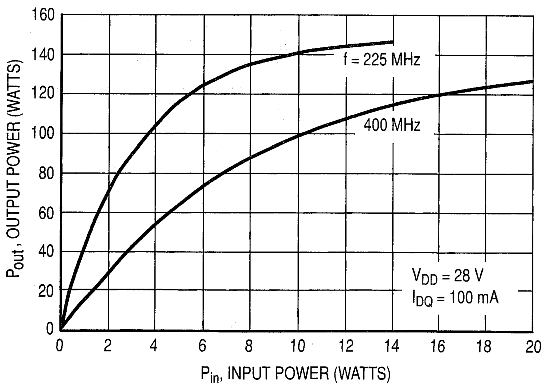


Figure 10. Power Gain versus Frequency



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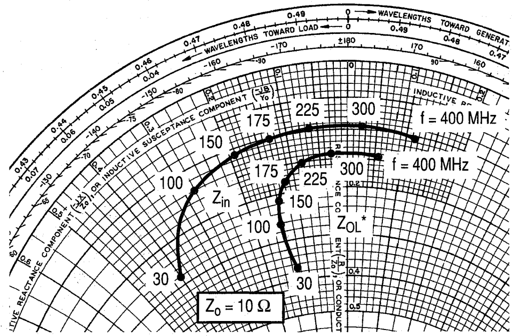
INPUT AND OUTPUT IMPEDANCE



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(P_{out} = 100 W)

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
30	2.80 – j4.00	3.65 – j1.30
100	1.40 – j2.80	2.60 – j1.50
150	1.10 – j1.90	2.10 – j1.40
175	1.00 – j1.25	1.80 – j1.20
225	0.95 – j0.65	1.50 – j0.80
300	0.95 + j0.20	1.35 – j0.30
400	1.05 + j1.15	1.45 + j0.55

Z_{OL}* = CONJUGATE OF THE OPTIMUM LOAD IMPEDANCE INTO WHICH THE DEVICE OUTPUT OPERATES AT A GIVEN OUTPUT POWER, VOLTAGE AND FREQUENCY.

RF POWER MOSFET CONSIDERATIONS

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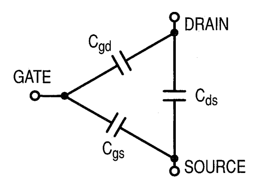

$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

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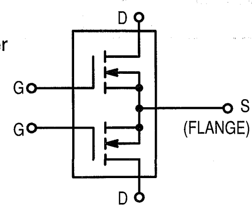
RF Power Field-Effect Transistors
N–Channel Enhancement–Mode

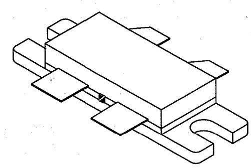
MRF176GU
MRF176GV

Designed for broadband commercial and military applications using push pull circuits at frequencies to 500 MHz. The high power, high gain and broadband performance of these devices makes possible solid state transmitters for FM broadcast or TV channel frequency bands.

- Electrical Performance
  MRF176GU @ 50 V, 400 MHz ("U" Suffix)
    Output Power — 150 Watts
    Power Gain — 14 dB Typ
    Efficiency — 50% Typ
  MRF176GV @ 50 V, 225 MHz ("V" Suffix)
    Output Power — 200 Watts
    Power Gain — 17 dB Typ
    Efficiency — 55% Typ
- 100% Ruggedness Tested At Rated Output Power
- Low Thermal Resistance
- Low C_{rss} — 7.0 pF Typ @ V_{DS} = 50 V

200/150 W, 50 V, 500 MHz
N–CHANNEL MOS
BROADBAND
RF POWER FETs





CASE 375–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	400 2.27	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	2.5	mAdc
Gate–Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc

NOTE:
1. Each side of device measured separately.

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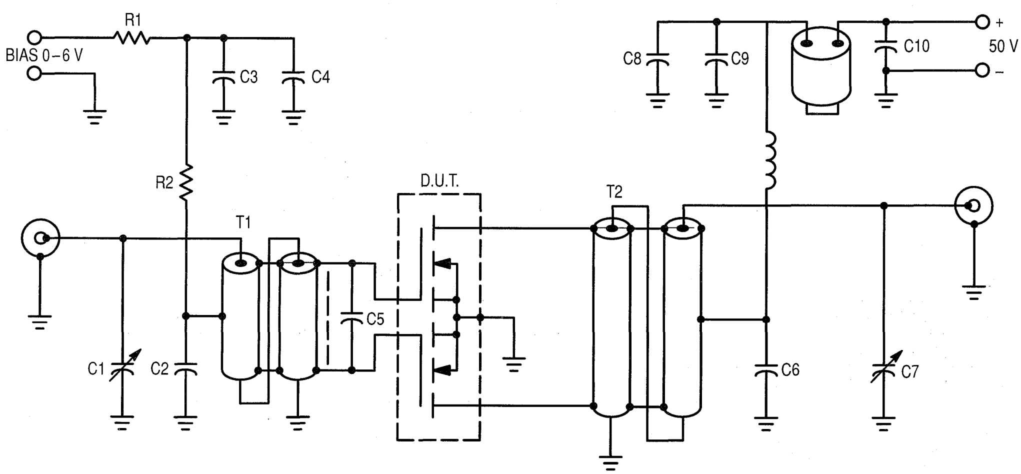
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 5.0 A)	$V_{DS(on)}$	1.0	3.0	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	2.0	3.0	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	180	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	100	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	6.0	—	pF
FUNCTIONAL CHARACTERISTICS — MRF176GV (2) (Figure 1)					
Common Source Power Gain (V_{DD} = 50 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA)	G_{ps}	15	17	—	dB
Drain Efficiency (V_{DD} = 50 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 50 Vdc, P_{out} = 200 W, f = 225 MHz, I_{DQ} = 2.0 x 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each side of device measured separately.
2. Measured in push–pull configuration.



C1 — Arco 404, 8.0–60 pF
C2, C3, C6, C8 — 1000 pF Chip
C4, C9 — 0.1 µF Chip
C5 — 180 pF Chip
C7 — Arco 403, 3.0–35 pF
C10 — 0.47 µF Chip, Kemet 1215 or Equivalent
L1 — 10 Turns AWG #16 Enameled Wire, Close Wound, 1/4″ I.D.

Board material — .062″ fiberglass (G10), Two sided, 1 oz. copper, $\varepsilon_r \cong 5$

Unless otherwise noted, all chip capacitors are ATC Type 100 or Equivalent

L2 — Ferrite Beads of Suitable Material for 1.5–2.0 µH, Total Inductance
R1 — 100 Ohms, 1/2 W
R2 — 1.0 kOhms, 1/2 W
T1 — 4:1 Impedance Ratio RF Transformer. Can Be Made of 25 Ohm Semirigid Co–Ax, 47–62 Mils O.D.
T2 — 1:4 Impedance Ratio RF Transformer. Can Be Made of 25 Ohm Semirigid Co–Ax, 62–90 Mils O.D.

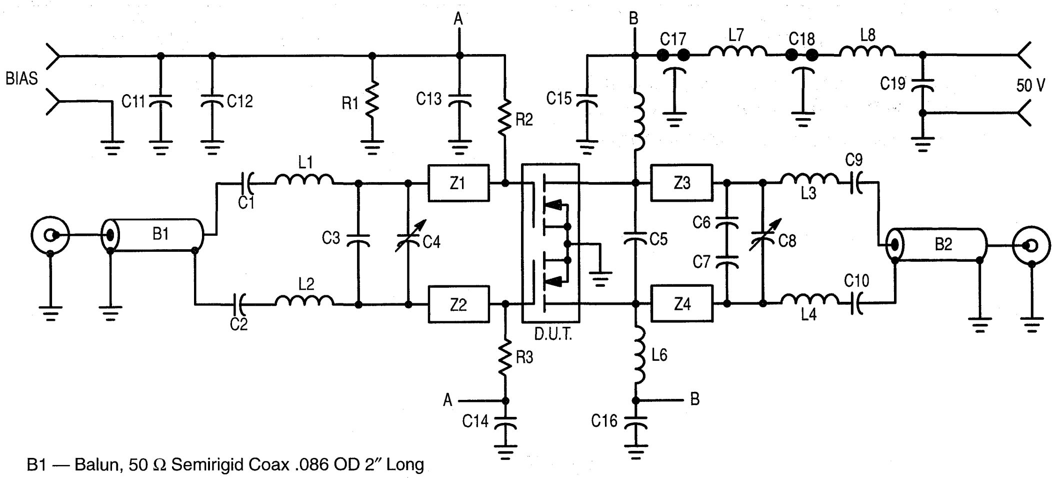
NOTE: For stability, the input transformer T1 should be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

Figure 1. 225 MHz Test Circuit

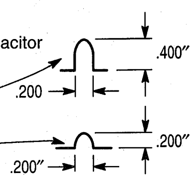
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS — MRF176GU (1) (Figure 2)					
Common Source Power Gain (V_{DD} = 50 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA)	G_{ps}	12	14	—	dB
Drain Efficiency (V_{DD} = 50 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 50 Vdc, P_{out} = 150 W, f = 400 MHz, I_{DQ} = 2.0 x 100 mA, VSWR 10:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTE:
1. Measured in push–pull configuration.



B1 — Balun, 50 Ω Semirigid Coax .086 OD 2″ Long
B2 — Balun, 50 Ω Semirigid Coax .141 OD 2″ Long
C1, C2, C9, C10 — 270 pF ATC Chip Capacitor
C3 — 15 pF ATC Chip Cap
C4, C8 — 1.0–20 pF Piston Trimmer Cap
C5 — 27 pF ATC Chip Cap
C6, C7 — 22 pF Mini Unelco Capacitor
C11, C13, C14, C15, C16 — 0.01 µF Ceramic Capacitor
C12 — 1.0 µF 50 V Tantalum Cap
C17, C18 — 680 pF Feedthru Capacitor
C19 — 10 µF 100 V Tantalum Cap
L1, L2 — Hairpin Inductor #18 W
L3, L4 — Hairpin Inductor #18 W



L5, L6 — 13T #18 W .250 ID
L7 — Ferroxcube VK–200 20/4B
L8 — 3T #18 W .340 ID
R1 — 1.0 kΩ 1/4 W Resistor
R2, R3 — 10 kΩ 1/4 W Resistor
Z1, Z2 — Microstrip Line .400L x .250W
Z3, Z4 — Microstrip Line .450L x .250W

Ckt Board Material — .060″ teflon–fiberglass, copper clad both sides, 2 oz. copper, ε_r = 2.55

Figure 2. 400 MHz Test Circuit

TYPICAL CHARACTERISTICS

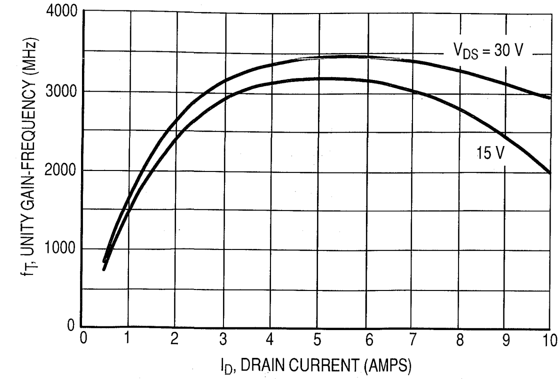


Figure 3. Common Source Unity Current Gain* Gain–Frequency versus Drain Current

* Data shown applies to each half of MRF176GU/GV

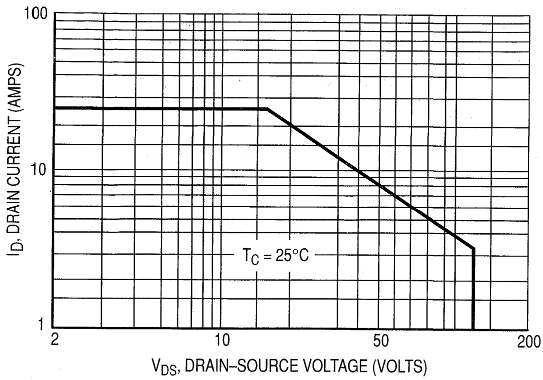
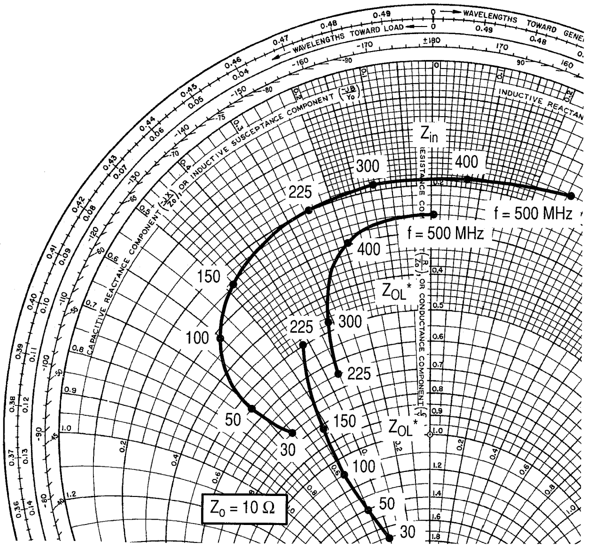


Figure 4. DC Safe Operating Area



INPUT AND OUTPUT IMPEDANCE
MRF176GU/GV
V_{DD} = 50 V, I_{DQ} = 2 x 100 mA

f MHz	Z_{in} OHMS	Z_{OL}* OHMS
(P_{out} = 150 W)		
225	2.05 – j2.50	6.50 – j3.50
300	2.00 – j1.10	4.80 – j3.10
400	1.85 + j0.75	3.00 – j1.90
500	1.60 + j2.70	2.60 + j0.10
(P_{out} = 200 W)		
30	7.50 – j6.50	17.00 – j4.00
50	5.50 – j7.00	14.00 – j5.00
100	3.20 – j6.00	11.00 – j5.20
150	2.50 – j4.80	8.20 – j5.00
225	2.05 – j2.50	5.00 – j4.20

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

NOTE: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

Figure 5. Series Equivalent Input/Output Impedance

TYPICAL CHARACTERISTICS

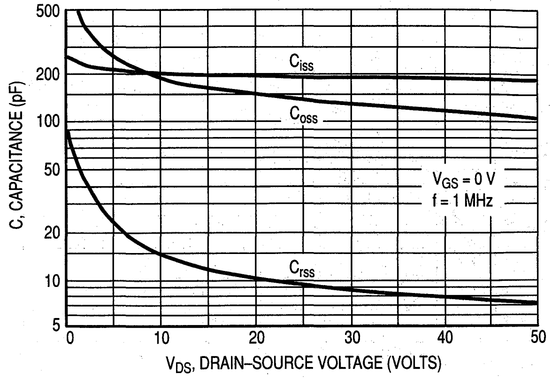


Figure 6. Capacitance versus Drain–Source Voltage*

* Data shown applies to each half of MRF176GU/GV

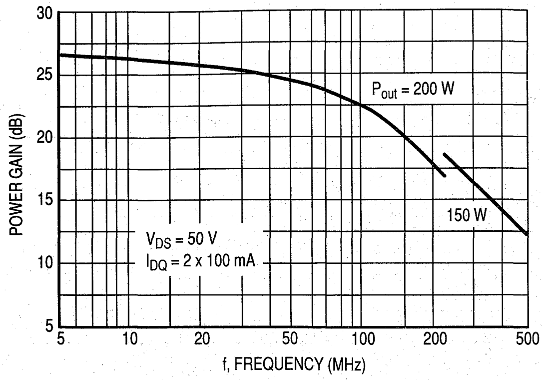


Figure 7. Power Gain versus Frequency

MRF176GV

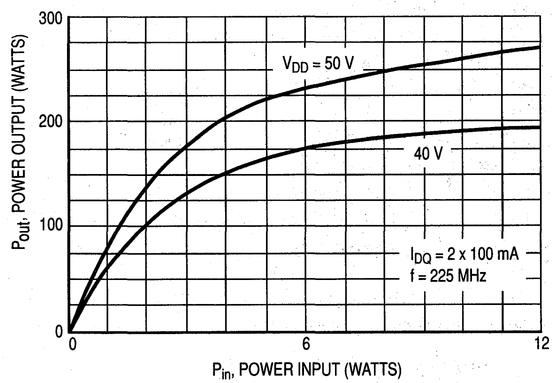


Figure 8. Power Input versus Power Output

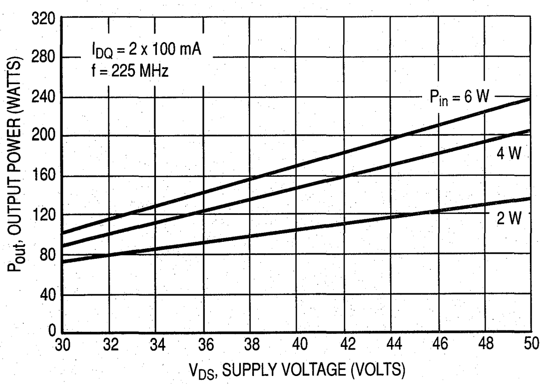


Figure 9. Output Power versus Supply Voltage

TYPICAL CHARACTERISTICS
MRF176GU

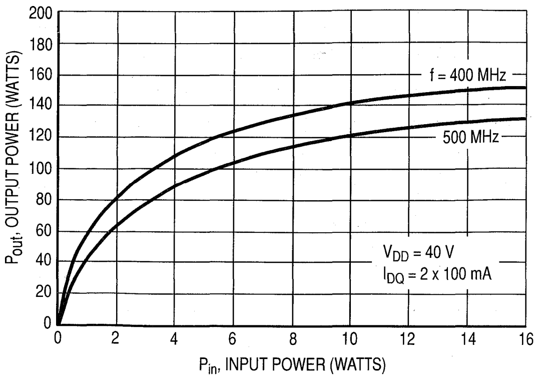


Figure 10. Output Power versus Input Power

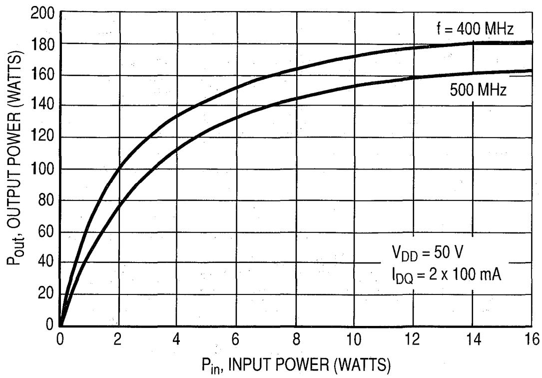


Figure 11. Output Power versus Input Power

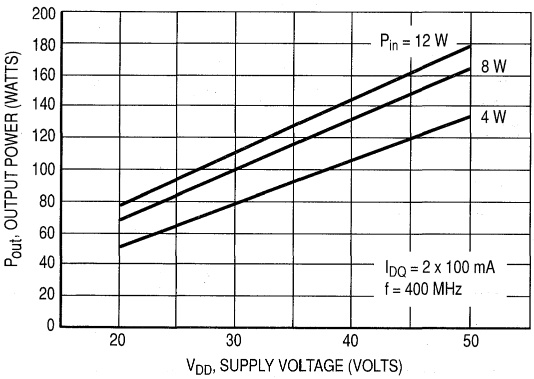


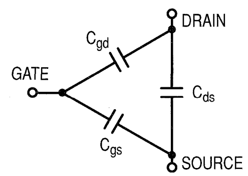
Figure 12. Output Power versus Supply Voltage

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

The C_{iss} given in the electrical characteristics table was measured using method 2 above. It should be noted that C_{iss}, C_{oss}, C_{rss} are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain, data presented in Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of this device are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — This device does not have an internal monolithic zener diode from gate–to–source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

HANDLING CONSIDERATIONS

The gate of the MOSFET, which is electrically isolated from the rest of the die by a very thin layer of SiO_2, may be damaged if the power MOSFET is handled or installed improperly. Exceeding the 40 V maximum gate–to–source voltage rating, $V_{GS(max)}$, can rupture the gate insulation and destroy the FET. RF Power MOSFETs are not nearly as susceptible as CMOS devices to damage due to static discharge because the input capacitances of power MOSFETs are much larger and absorb more energy before being charged to the gate breakdown voltage. However, once breakdown begins, there is enough energy stored in the gate–source capacitance to ensure the complete perforation of the gate oxide. To avoid the possibility of device failure caused by static discharge, precautions similar to those taken with small–signal MOSFET and CMOS devices apply to power MOSFETs.

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

The gate of the power MOSFET could still be in danger after the device is placed in the intended circuit. If the gate may see voltage transients which exceed $V_{GS(max)}$, the circuit designer should place a 40 V zener across the gate and source terminals to clamp any potentially destructive spikes. Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DESIGN CONSIDERATIONS

The MRF176G is a RF power N–channel enhancement mode field–effect transistor (FETs) designed for VHF and

UHF power amplifier applications. Motorola RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V–groove MOS power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF176G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF176G was characterized at I_{DQ} = 100 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

GAIN CONTROL

Power output of the MRF176 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

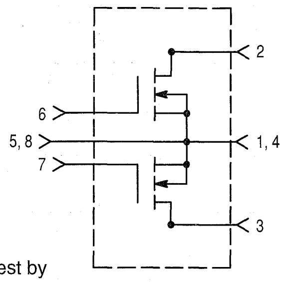
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement Mode MOSFET

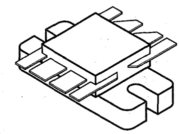
MRF177

**100 W, 28 V, 400 MHz
N–CHANNEL
BROADBAND
RF POWER MOSFET**

Designed for broadband commercial and military applications up to 400 MHz frequency range. Primarily used as a driver or output amplifier in push–pull configurations. Can be used in manual gain control, ALC and modulation circuits.

- Typical Performance at 400 MHz, 28 V:
  Output Power — 100 W
  Gain — 12 dB
  Efficiency — 60%
- Low Thermal Resistance
- Low C_{rss} — 10 pF Typ @ V_{DS} = 28 Volts
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- Excellent Thermal Stability; Suited for Class A Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.





CASE 744A–01, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Temperature Range	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	0.65	°C/W

(1) Total device dissipation rating applies only when the device is operated as an RF push–pull amplifier.

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 8

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic (1)	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3.0 A)	$V_{DS(on)}$	—	—	1.4	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.0 A)	g_{fs}	1.8	2.2	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	100	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	105	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	10	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 8) (2)					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 200 mA)	G_{PS}	10	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 200 mA)	η	55	60	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, I_{DQ} = 200 mA, Load VSWR = 30:1, All Phase Angles At Frequency of Test)	ψ	No Degradation in Output Power Before & After Test			

(1) Note each transistor chip measured separately
(2) Both transistor chips operating in push–pull amplifier

TYPICAL CHARACTERISTICS

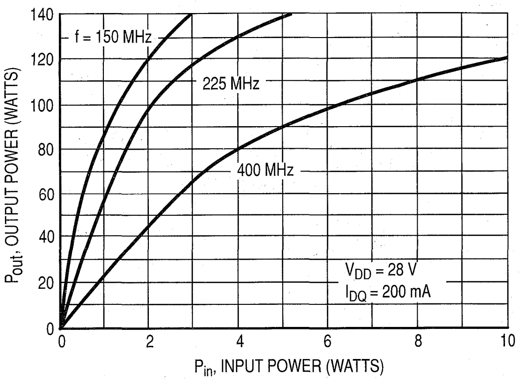


Figure 1. Output Power versus Input Power

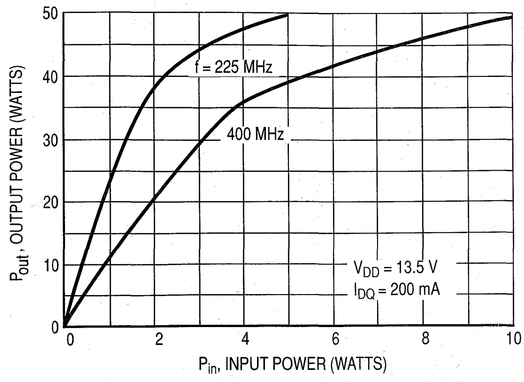


Figure 2. Output Power versus Input Power

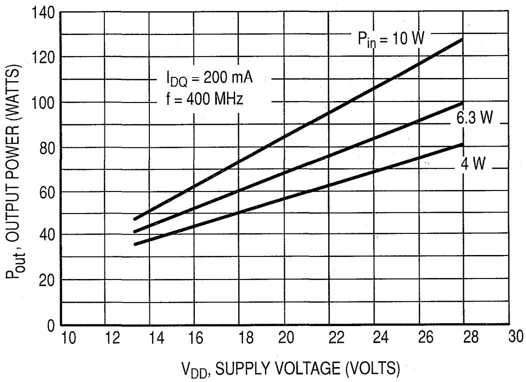


Figure 3. Output Power versus Supply Voltage

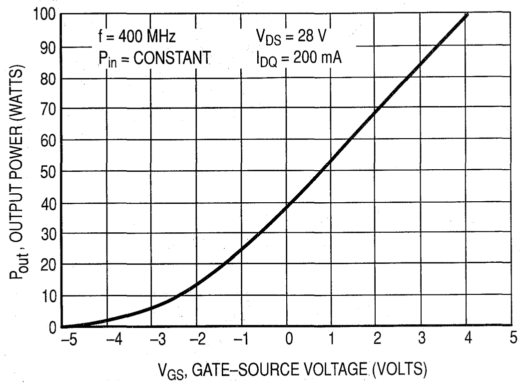


Figure 4. Output Power versus Gate Voltage

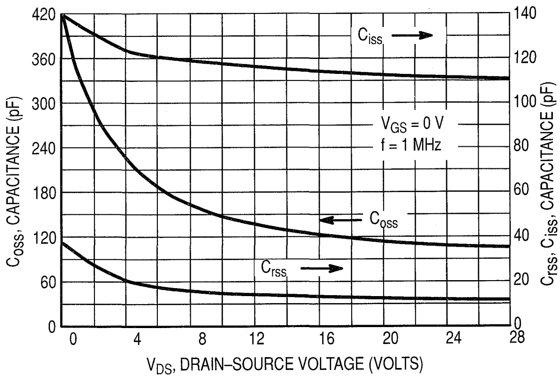


Figure 5. Capacitance versus Drain Voltage

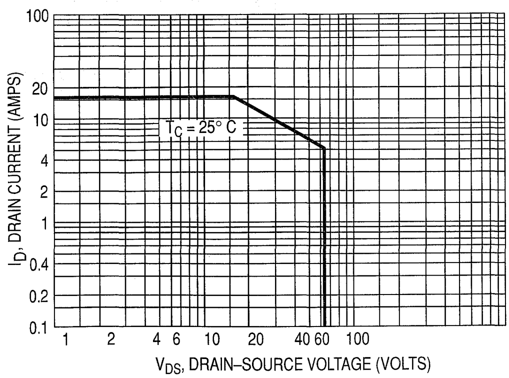
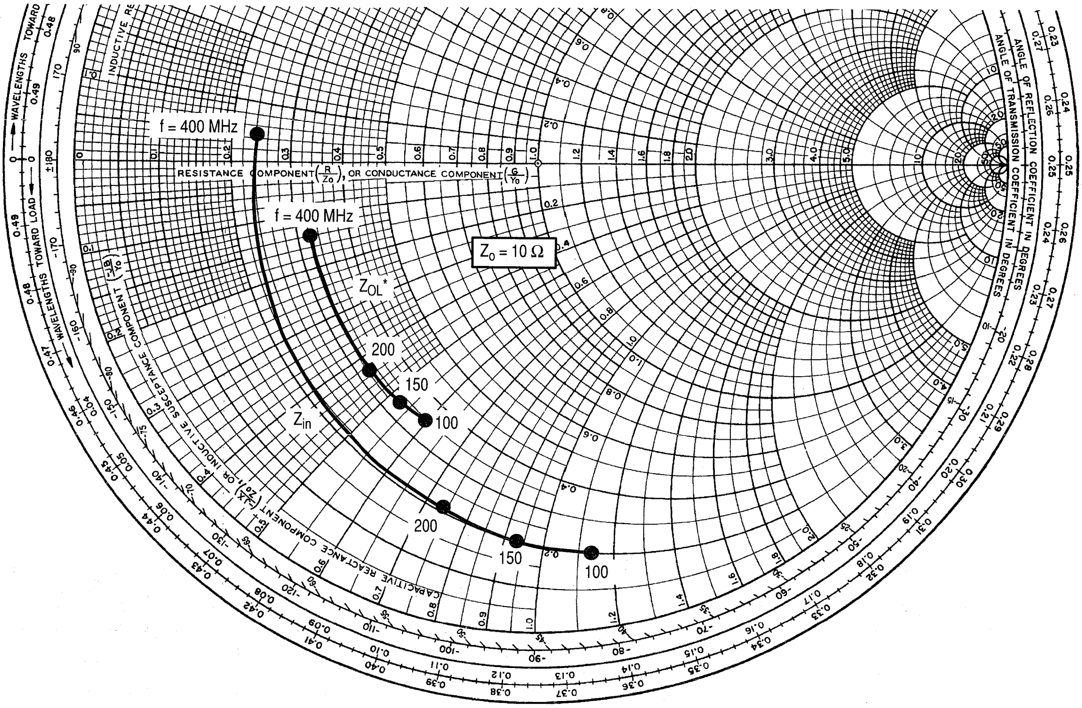


Figure 6. DC Safe Operating Area

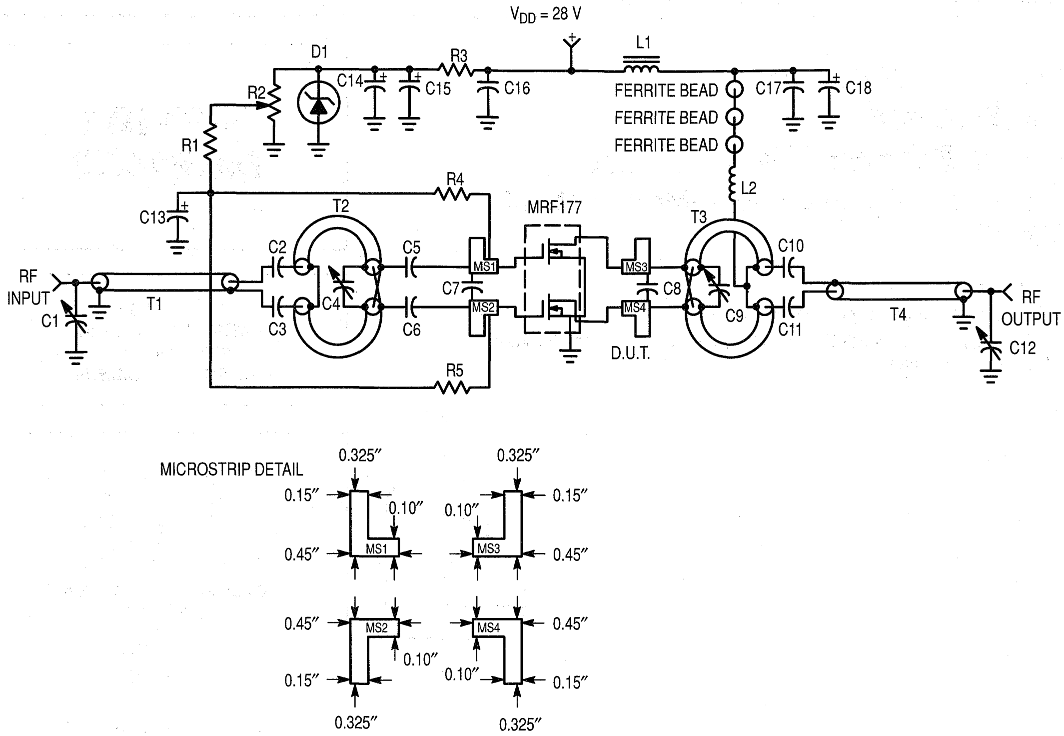


NOTE: Input and Output Impedance values given are measured gate–to–gate and drain–to–drain respectively.

V_{DD} = 28 V I_{DQ} = 200 mA P_{out} = 100 W		
f (MHz)	Z_{in} Ohms	Z_{OL}* Ohms
100	2.0 – j11.5	3.5 – j6
150	2.05 – j9.45	3.35 – j5.34
200	2.1 – j7.5	3.3 – j4.4
400	2.35 + j0.4	3.2 – j1.38

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 7. Impedance or Admittance Coordinates



C1, C12	1–10 pF JOHANSON OR EQUIVALENT	D1	1N5347B, 20 Vdc
C2, C3, C5, C6, C10, C11	270 pF ATC 100 MIL CHIP CAP	L1	1–TURN NO. 18, 0.25″, 2–HOLE FERRITE BEAD
C4, C9	1–20 pF	L2	8–1/2 TURNS NO. 18, CLOSE WOUND .375″ DIA.
C7	36 pF CHIP CAP	R1, R4, R5	10 kΩ @ 1/2 W RESISTOR
C8	10 pF CHIP CAP	R2	10 kΩ, 10 TURN RESISTOR
C13, C14	0.1 μFD @ 50 Vdc	R3	2.0 kΩ @ 1/2 W RESISTOR
C15, C18	10 μFD @ 50 Vdc	T1	1–1/2 T, 50 Ω COAX, .034″ DIA. ON DUAL 0.5″ FERRITE CORE
C16	500 pF BUTTON	T2	2.0″ 25 Ω COAX, .075″ DIA.
C17	1000 pF UNCASED MICA	T3	2.1″ 10 Ω COAX, .075″ DIA.
		T4	4.0″ 50 Ω COAX, .0865″ DIA.
		BOARD	Dielectric Thickness = 0.060″ 2oz Copper, Cu–Clad, Teflon Fiberglass, ε_r = 2.55

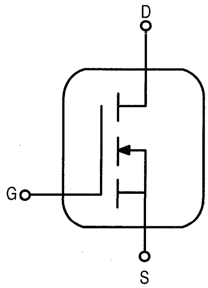
Figure 8. Test Circuit Electrical Schematic

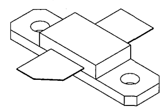
The RF MOSFET Line
RF Power
Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF182
MRF182S

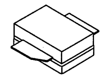
30 W, 1.0 GHz
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

- High Gain, Rugged Device
- Broadband Performance from HF to 1 GHz
- Bottom Side Source Eliminates DC Isolators, Reducing Common Mode Inductances





CASE 360B–01, STYLE 1
(MRF182)



CASE 360C–03, STYLE 1
(MRF182S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ T_C = 70°C Derate above 70°C	P_D	74 0.57	W W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

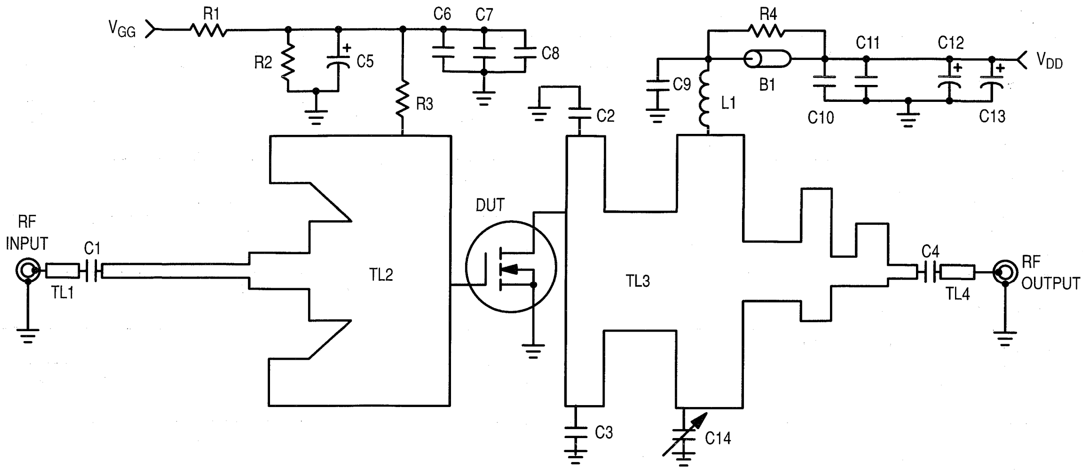
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 1.0 μAdc)	$V_{(BR)DSS}$	65	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	–	–	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	–	–	1	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 5

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 μA)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 50 mA)	$V_{GS(Q)}$	3	4	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	–	0.9	1.2	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A)	g_{fs}	1.6	1.8	–	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	56	–	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	–	28	–	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	–	2.5	–	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 945 MHz)	G_{ps}	11	14	–	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 945 MHz)	η	50	60	–	%
Load Mismatch (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 945 MHz, Load VSWR 5:1 at All Phase Angles)	Ψ	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 960 MHz)	Z_{in}	–	0.81 + j1.6	–	ohms
Series Equivalent Output Impedance (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 50 mA, f = 960 MHz)	Z_{out}	–	2.15 – j1.7	–	ohms



B1	Short RF Bead Fair Rite–274301944	L1	5 Turns, 20 AWG, IDIA 0.126
C1	18 pF Chip Capacitor	R1	10 kΩ, 1/4 W Resistor
C2, C3, C6, C9	43 pF Chip Capacitor	R2	13 kΩ, 1/4 W Resistor
C4	100 pF Chip Capacitor	R3	1.0 kΩ, 1/4 W Chip Resistor
C5, C12	10 μF, 50 Vdc Electrolytic Capacitor	R4	4 x 39 Ω, 1/8 W Chip Resistor
C7, C10	1000 pF Chip Capacitor	″TL1–TL4	Microstrip Line See Photomaster
C8, C11	0.1 μF, 50 Vdc Chip Capacitor	Ckt Board	1/32″ Glass Teflon, ε_r = 2.55
C13	250 μF, 50 Vdc Electrolytic Capacitor		ARLON–GX–0300–55–22
C14	0.6–4.5 pF Variable Capacitor		

Figure 1. MRF182 Schematic

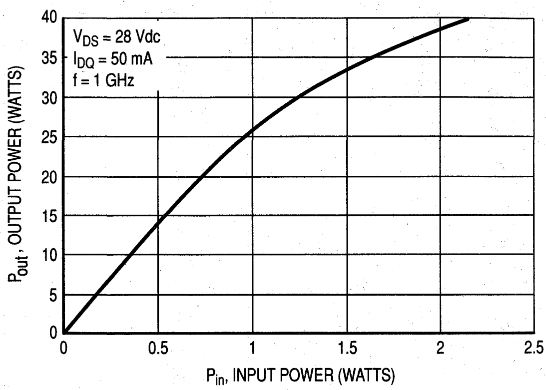


Figure 2. Output Power versus Input Power at 1 GHz

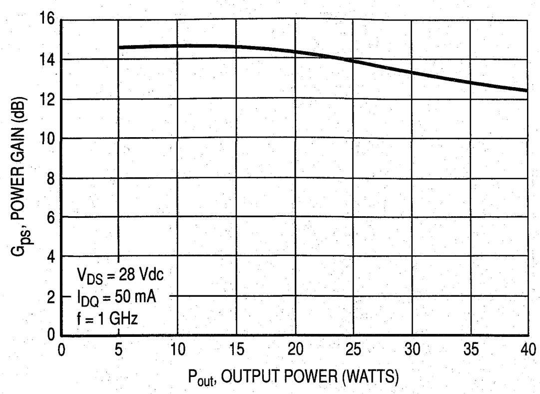


Figure 3. Power Gain versus Output Power at 1 GHz

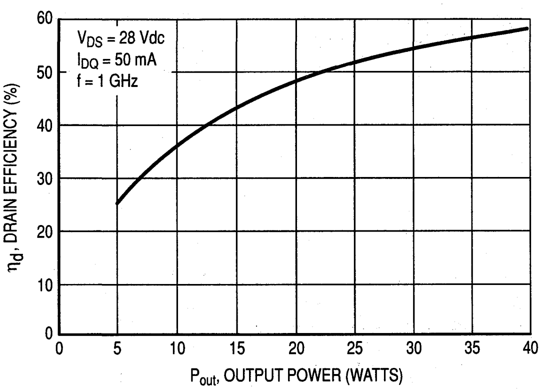


Figure 4. Drain Efficiency versus Output Power at 1 GHz

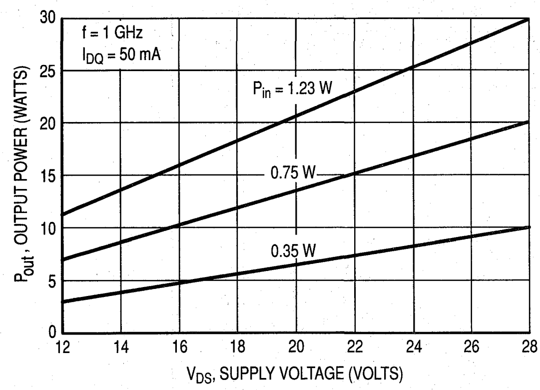


Figure 5. Output Power versus Supply Voltage

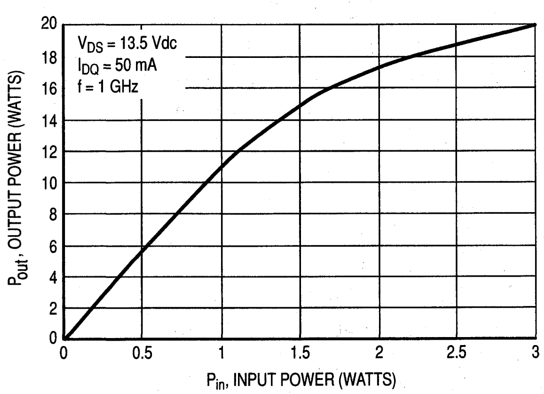


Figure 6. Output Power versus Input Power

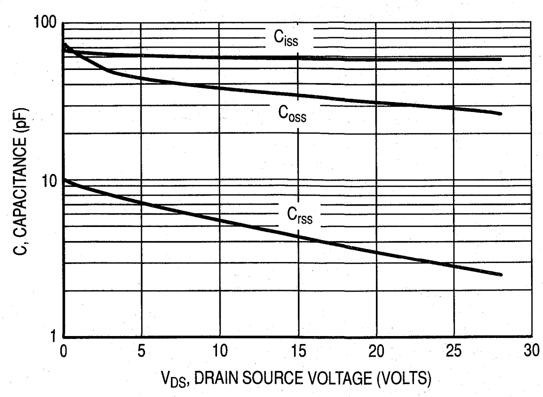


Figure 7. Capacitance versus Drain Source Voltage

Table 1. Typical Common Source S–Parameters (V_{DS} = 13.5 V)
I_D = 1.0 A

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
20	0.933	–131	40.81	112	0.021	22	0.664	–138
30	0.922	–148	29.31	104	0.022	15	0.700	–151
40	0.892	–156	22.19	99	0.022	10	0.718	–158
50	0.877	–161	17.91	95	0.023	7	0.725	–162
60	0.870	–164	14.67	92	0.023	4	0.732	–164
70	0.863	–166	12.57	90	0.022	2	0.735	–166
80	0.860	–168	11.00	89	0.022	1	0.738	–168
90	0.860	–169	9.79	87	0.022	0	0.740	–169
100	0.859	–170	8.79	86	0.022	–1	0.741	–169
150	0.859	–173	5.78	80	0.022	–7	0.750	–172
200	0.862	–175	4.29	74	0.022	–11	0.759	–172
250	0.868	–176	3.38	69	0.021	–14	0.770	–173
300	0.880	–177	2.77	65	0.020	–17	0.780	–173
350	0.877	–177	2.32	61	0.020	–19	0.793	–173
400	0.882	–178	1.98	56	0.019	–22	0.808	–173
450	0.892	–179	1.72	52	0.018	–24	0.816	–173
500	0.899	–180	1.51	49	0.017	–26	0.828	–174
550	0.898	180	1.33	45	0.017	–27	0.838	–174
600	0.907	179	1.19	42	0.016	–28	0.849	–175
650	0.914	179	1.07	38	0.015	–28	0.859	–175
700	0.916	177	0.95	35	0.014	–25	0.867	–176
750	0.920	177	0.88	34	0.015	–26	0.874	–176
800	0.924	176	0.80	30	0.015	–27	0.884	–177
850	0.929	175	0.74	27	0.015	–33	0.891	–178
900	0.929	174	0.68	25	0.013	–38	0.897	–178
950	0.933	173	0.63	22	0.011	–39	0.905	–179
1000	0.934	173	0.58	20	0.010	–37	0.912	–180
1050	0.930	172	0.54	17	0.009	–33	0.918	180
1100	0.938	171	0.52	15	0.009	–29	0.924	179
1150	0.933	170	0.48	13	0.008	–28	0.929	178
1200	0.930	169	0.45	10	0.008	–25	0.930	177
1250	0.939	168	0.42	8	0.007	–23	0.935	177
1300	0.936	168	0.40	6	0.007	–21	0.934	176
1350	0.933	167	0.38	4	0.006	–19	0.936	175
1400	0.937	166	0.35	2	0.005	–14	0.939	174
1450	0.937	165	0.33	0	0.005	–5	0.934	174
1500	0.927	164	0.32	–2	0.004	0	0.930	173

Table 2. Typical Common Emitter S–Parameters (V_{DS} = 28 V)

I_D = 1.0 A

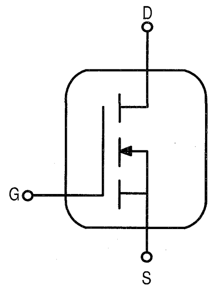
f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\lvert S_{11} \rvert$	∠ ϕ	$\lvert S_{21} \rvert$	∠ ϕ	$\lvert S_{12} \rvert$	∠ ϕ	$\lvert S_{22} \rvert$	∠ ϕ
20	0.964	–99	54.39	129	0.014	39	0.429	–108
30	0.949	–121	43.46	118	0.017	28	0.478	–125
40	0.909	–134	34.35	109	0.018	20	0.520	–137
50	0.884	–142	28.27	103	0.018	15	0.540	–144
60	0.875	–148	23.38	98	0.019	11	0.553	–149
70	0.862	–152	20.10	95	0.019	8	0.562	–152
80	0.861	–156	17.64	92	0.019	5	0.569	–154
90	0.858	–158	15.72	90	0.019	3	0.575	–156
100	0.858	–160	14.11	88	0.019	1	0.580	–157
150	0.856	–166	9.26	79	0.018	–7	0.606	–160
200	0.862	–169	6.80	71	0.018	–12	0.633	–161
250	0.871	–171	5.29	65	0.017	–16	0.661	–161
300	0.882	–173	4.27	59	0.016	–21	0.690	–162
350	0.883	–174	3.52	54	0.015	–23	0.718	–162
400	0.895	–175	2.97	49	0.014	–26	0.747	–163
450	0.904	–176	2.54	45	0.013	–28	0.767	–164
500	0.911	–177	2.20	41	0.012	–30	0.789	–165
550	0.911	–178	1.90	37	0.011	–30	0.807	–166
600	0.923	–179	1.69	33	0.010	–30	0.825	–167
650	0.929	–180	1.50	30	0.009	–29	0.841	–168
700	0.929	179	1.32	26	0.009	–22	0.855	–169
750	0.933	178	1.21	24	0.010	–22	0.865	–170
800	0.938	177	1.09	21	0.009	–20	0.877	–171
850	0.942	176	1.00	18	0.010	–31	0.886	–172
900	0.942	175	0.92	16	0.008	–37	0.894	–173
950	0.947	174	0.84	13	0.006	–38	0.904	–174
1000	0.946	173	0.77	11	0.005	–28	0.912	–175
1050	0.943	172	0.72	8	0.005	–18	0.919	–176
1100	0.948	171	0.67	6	0.004	–9	0.926	–177
1150	0.945	171	0.62	4	0.005	0	0.932	–178
1200	0.939	170	0.59	1	0.004	3	0.934	–179
1250	0.949	169	0.54	0	0.005	12	0.940	–180
1300	0.947	168	0.51	–3	0.005	18	0.939	180
1350	0.944	167	0.48	–4	0.005	22	0.941	179
1400	0.945	166	0.44	–7	0.004	34	0.943	178
1450	0.944	165	0.42	–9	0.005	45	0.940	177
1500	0.933	164	0.40	–10	0.005	55	0.936	176

The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

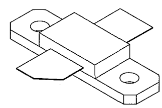
MRF183
MRF183S

Designed for broadband commercial and industrial applications at frequencies to 1.0 GHz. The high gain and broadband performance of these devices makes ithem ideal for large–signal, common source amplifier applications in 28 volt base station equipment.

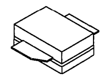
- Guaranteed Performance at 945 MHz, 28 Volts
  - Output Power – 45 Watts
  - Power Gain – 11 dB
  - Efficiency – 50%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Capable of Handling 30:1 VSWR @ 28 Vdc, 945 MHz



45 W, 1.0 GHz
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B–01, STYLE 1
(MRF183)



CASE 360C–03, STYLE 1
(MRF183S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current – Continuous	I_D	5	Adc
Total Device Dissipation @ T_C = 70°C Derate above 70°C	P_D	86 0.67	W W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

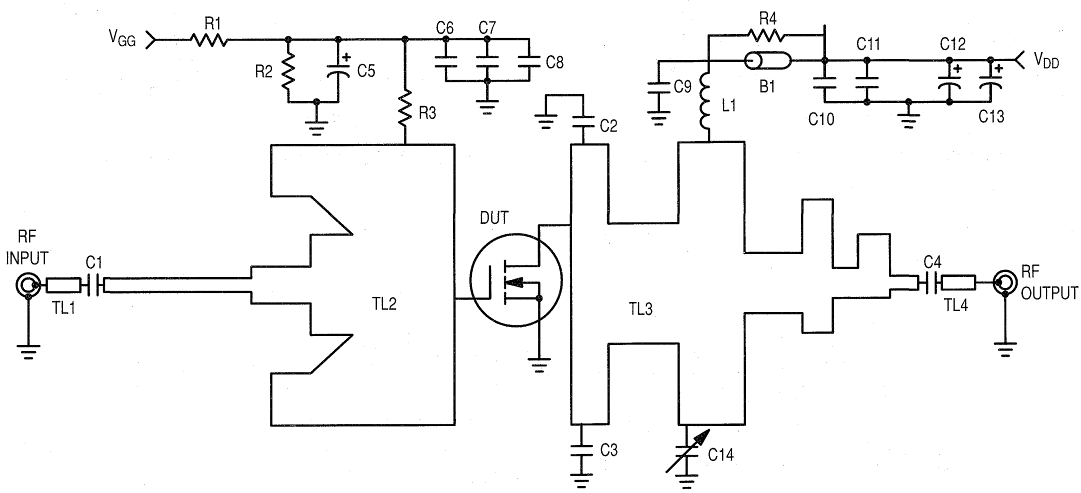
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 1 μAdc)	$V_{(BR)DSS}$	65	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	–	–	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	–	–	1	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 5

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 400 μA)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 75 mA)	$V_{GS(Q)}$	2.5	3.5	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	–	0.75	0.9	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A)	g_{fs}	2	2.6	–	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	82	–	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	–	38	–	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	–	3.8	–	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 45 W, I_{DQ} = 75 mA, f = 945 MHz)	G_{ps}	11	14	–	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 45 W, I_{DQ} = 75 mA, f = 945 MHz)	η	50	60	–	%
Load Mismatch (V_{DD} = 28 Vdc, P_{out} = 45 W, I_{DQ} = 100 mA, f = 945 MHz, Load VSWR 5:1 at All Phase Angles)	Ψ	No Degradation in Output Power			



B1	Short RF Bead Fair Rite–2743019447	L1	5 Turns, 20 AWG, IDIA 0.126″
C1	18 pF Chip Capacitor	R1	10 kΩ, 1/4 W Resistor
C2, C3, C6, C9	43 pF Chip Capacitor	R2	13 kΩ, 1/4 W Resistor
C4	100 pF Chip Capacitor	R3	1.0 kΩ, 1/4 W Chip Resistor
C5, C12	10 μF, 50 Vdc Electrolytic Capacitor	R4	4 x 39 Ω, 1/8 W Chip Resistor
C7, C10	1000 pF Chip Capacitor	TL1–TL4	Microstrip Line See Photomaster
C8, C11	0.1 μF, 50 Vdc Chip Capacitor	Ckt Board	1/32″ Glass Teflon, ε_r = 2.55 ARLON–GX–0300–55–22
C13	250 μF, 50 Vdc Electrolytic Capacitor		
C14	0.6–4.5 pF Variable Capacitor		

Figure 1. MRF183 Test Circuit Schematic

TYPICAL CHARACTERISTICS

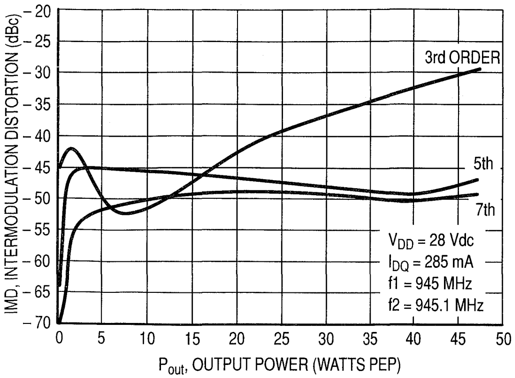


Figure 2. Intermodulation Distortion versus Output Power

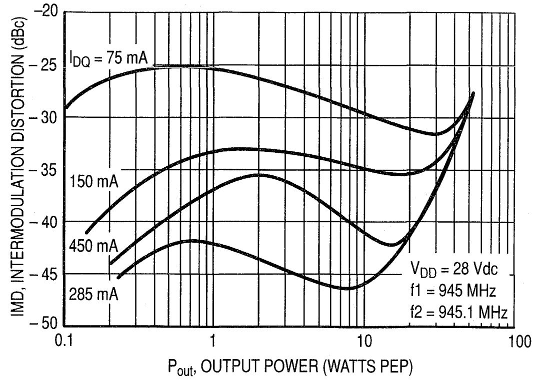


Figure 3. Intermodulation Distortion versus Output Power

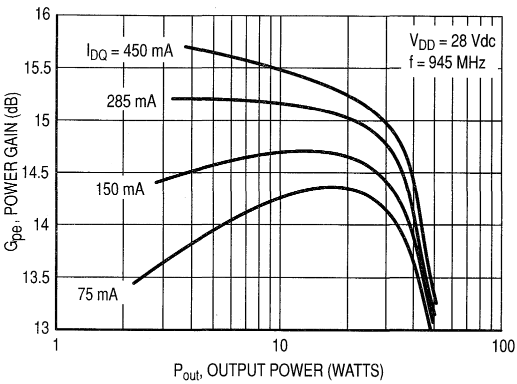


Figure 4. Power Gain versus Output Power

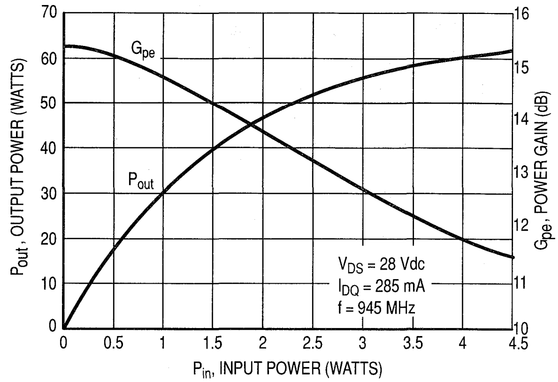


Figure 5. Output Power versus Input Power

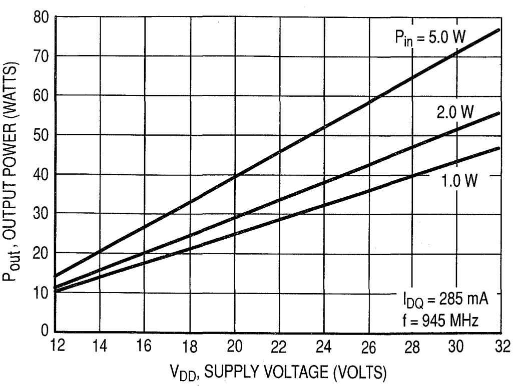


Figure 6. Output Power versus Supply Voltage

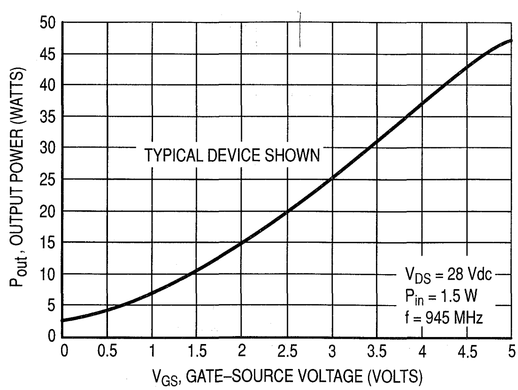


Figure 7. Output Power versus Gate Voltage

TYPICAL CHARACTERISTICS

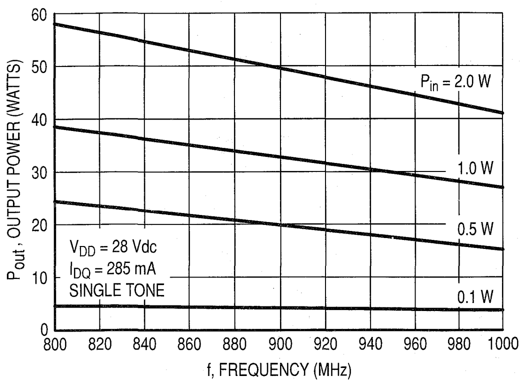


Figure 8. Output Power versus Frequency

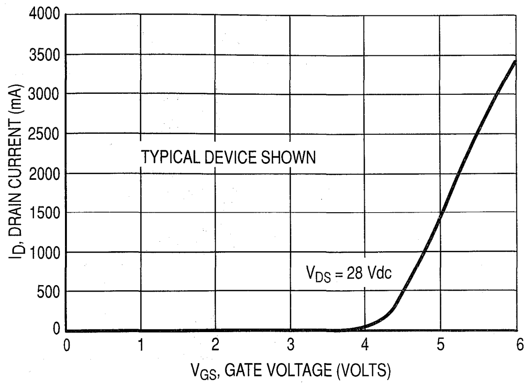


Figure 9. Drain Current versus Gate Voltage

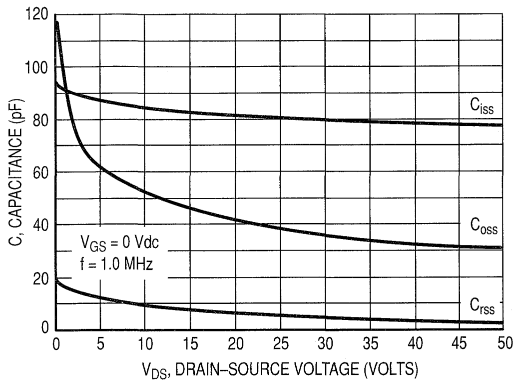


Figure 10. Capacitance versus Voltage

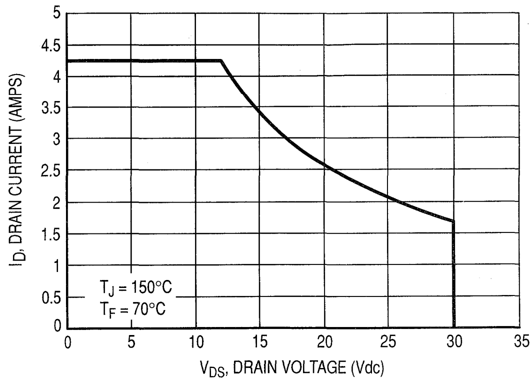


Figure 11. DC Safe Operating Area

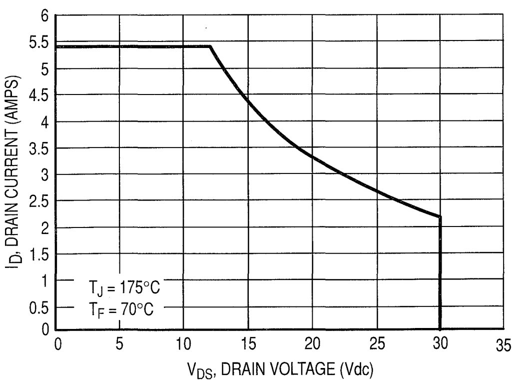


Figure 12. DC Safe Operating Area

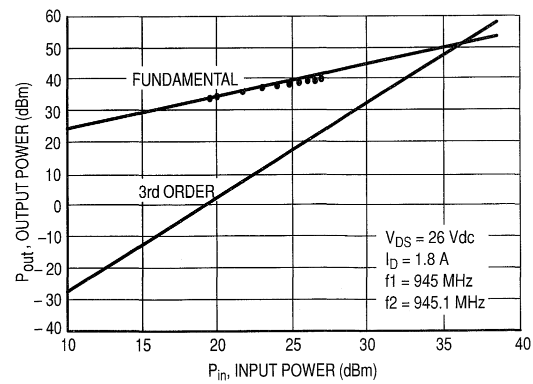


Figure 13. Class A Third Order Intercept Point

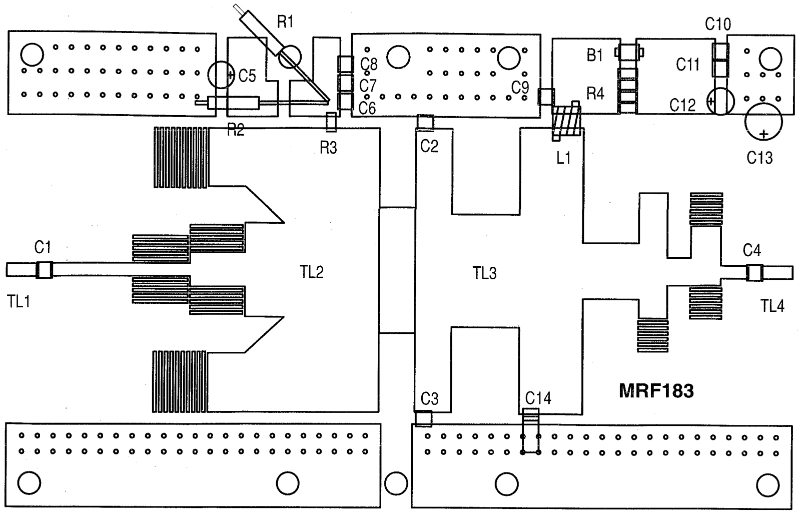
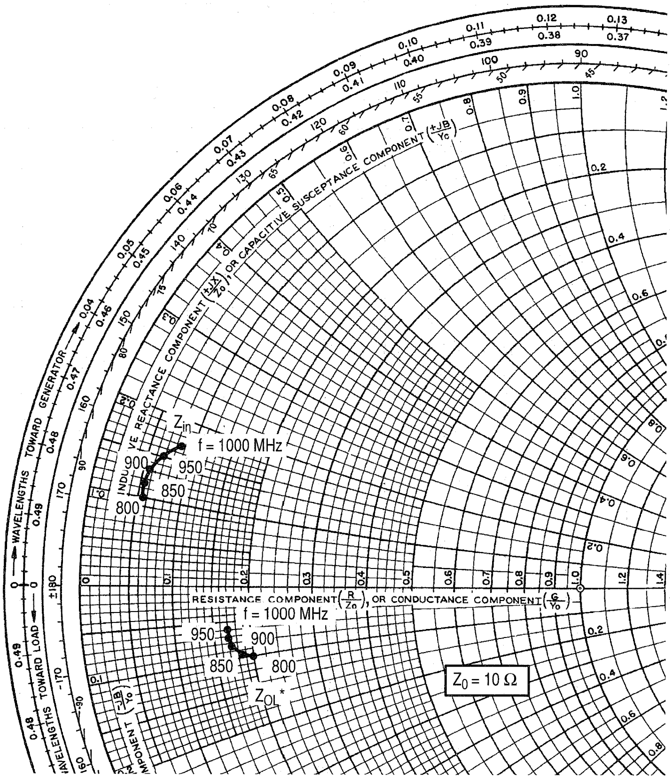


Figure 14. MRF183 Component Parts Layout



V_{DD} = 28 Vdc, I_{DQ} = 75 mA, P_{out} = 45 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	0.62 + j1.12	1.92 – j0.95
850	0.64 + j1.33	1.83 – j0.88
900	0.68 + j1.42	1.75 – j0.82
950	0.75 + j1.56	1.72 – j0.70
1000	0.82 + j1.64	1.69 – j0.60

Z_{in} = Conjugate of source impedance.

Z_{out} = Conjugate of the load impedance at given output power, voltage, frequency and efficiency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency and device stability.

Figure 15. Series Equivalent Input and Output Impedance

Table 1. Typical Common Source S–Parameters (V_{DS} = 13.5 V)

I_D = 1.5 A

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
20	0.954	–157	29.58	100	0.017	11	0.778	–161
30	0.941	–164	19.73	96	0.017	8	0.796	–168
40	0.922	–168	14.84	93	0.017	4	0.804	–170
50	0.907	–171	11.94	91	0.017	3	0.808	–172
60	0.903	–172	9.75	89	0.017	2	0.812	–173
70	0.899	–173	8.34	88	0.017	0	0.814	–174
80	0.898	–174	7.29	86	0.017	–1	0.816	–175
90	0.896	–175	6.49	85	0.017	–2	0.816	–175
100	0.897	–175	5.83	84	0.017	–2	0.817	–175
150	0.895	–177	3.82	79	0.017	–6	0.822	–176
200	0.898	–178	2.84	74	0.016	–9	0.828	–176
250	0.902	–178	2.24	70	0.016	–11	0.835	–176
300	0.908	–179	1.84	66	0.015	–14	0.842	–176
350	0.905	–179	1.55	62	0.015	–16	0.850	–176
400	0.913	–180	1.32	58	0.014	–18	0.861	–176
450	0.920	180	1.15	54	0.014	–18	0.865	–176
500	0.924	179	1.01	51	0.013	–20	0.874	–177
550	0.922	179	0.89	47	0.013	–21	0.881	–177
600	0.931	178	0.80	44	0.012	–21	0.889	–177
650	0.935	178	0.72	41	0.011	–20	0.895	–177
700	0.935	177	0.64	38	0.011	–17	0.901	–178
750	0.937	177	0.59	37	0.012	–18	0.905	–178
800	0.940	176	0.54	33	0.012	–20	0.913	–178
850	0.943	176	0.50	30	0.012	–29	0.919	–179
900	0.945	175	0.46	28	0.010	–33	0.924	–179
950	0.947	174	0.43	26	0.009	–34	0.930	–180
1000	0.947	174	0.40	24	0.008	–29	0.935	180
1050	0.947	173	0.37	21	0.007	–24	0.939	179
1100	0.952	172	0.35	19	0.007	–19	0.944	179
1150	0.949	172	0.32	17	0.007	–17	0.948	178
1200	0.946	171	0.30	14	0.006	–16	0.948	177
1250	0.954	170	0.28	12	0.006	–13	0.953	177
1300	0.952	170	0.27	9	0.006	–12	0.950	176
1350	0.949	169	0.26	9	0.006	–10	0.951	176
1400	0.948	168	0.23	8	0.005	–7	0.953	175
1450	0.948	168	0.22	6	0.004	4	0.948	174
1500	0.940	167	0.21	4	0.004	19	0.944	174

Table 2. Typical Common Source S–Parameters (V_{DS} = 28 V)

I_D = 1.5 A

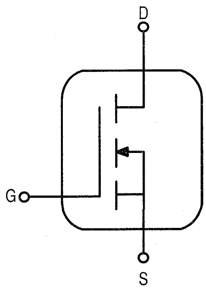
f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
20	0.968	–132	45.79	113	0.014	24	0.579	–145
30	0.953	–145	31.75	106	0.015	17	0.623	–157
40	0.921	–154	24.33	99	0.015	12	0.648	–161
50	0.904	–159	19.68	95	0.015	7	0.661	–164
60	0.898	–163	16.11	92	0.015	5	0.670	–166
70	0.890	–165	13.79	90	0.015	2	0.677	–167
80	0.886	–167	12.06	87	0.015	1	0.681	–168
90	0.886	–168	10.71	86	0.015	–1	0.684	–169
100	0.887	–169	9.61	84	0.015	–3	0.688	–169
150	0.886	–172	6.26	76	0.015	–9	0.706	–170
200	0.890	–174	4.59	69	0.014	–13	0.724	–170
250	0.898	–175	3.57	64	0.014	–17	0.744	–169
300	0.906	–176	2.88	59	0.013	–19	0.764	–169
350	0.908	–177	2.37	54	0.012	–23	0.785	–169
400	0.915	–178	2.00	49	0.011	–24	0.807	–170
450	0.924	–178	1.71	45	0.010	–25	0.821	–170
500	0.930	–179	1.48	41	0.010	–26	0.838	–171
550	0.928	–180	1.28	37	0.009	–26	0.851	–171
600	0.937	180	1.13	33	0.008	–25	0.865	–172
650	0.944	179	1.00	30	0.007	–22	0.878	–172
700	0.943	178	0.88	27	0.008	–14	0.888	–173
750	0.946	178	0.81	25	0.008	–15	0.895	–173
800	0.949	177	0.73	22	0.009	–17	0.906	–174
850	0.954	177	0.67	20	0.009	–28	0.912	–175
900	0.953	175	0.61	18	0.007	–34	0.919	–175
950	0.957	175	0.56	15	0.005	–32	0.927	–176
1000	0.957	174	0.51	13	0.004	–22	0.934	–177
1050	0.957	174	0.48	10	0.004	–11	0.939	–178
1100	0.962	173	0.45	8	0.004	–2	0.945	–178
1150	0.959	172	0.41	7	0.004	3	0.950	–179
1200	0.955	171	0.39	4	0.004	9	0.950	–180
1250	0.962	170	0.36	2	0.004	13	0.955	180
1300	0.959	170	0.33	0	0.004	17	0.953	179
1350	0.956	169	0.31	–1	0.004	25	0.954	178
1400	0.954	168	0.29	–4	0.004	32	0.957	177
1450	0.955	168	0.28	–6	0.004	46	0.952	177
1500	0.948	167	0.26	–7	0.004	56	0.948	176

The RF MOSFET Line
RF POWER Field-Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

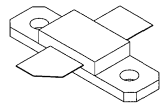
MRF184
MRF184S

Designed for broadband commercial and industrial applications at frequencies to 1.0 GHz. The high gain and broadband performance of these devices makes them ideal for large–signal, common source amplifier applications in 28 volt base station equipment.

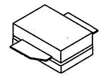
- Guaranteed Performance @ 945 MHz, 28 Volts
  Output Power = 60 Watts
  Power Gain = 11.5 dB
  Efficiency = 53%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Capable of Handling 30:1 VSWR @ 28 Vdc, 945 MHz



60 W, 1.0 GHz
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B–01, STYLE 1
(MRF184)



CASE 360C–03, STYLE 1
(MRF184S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	7	Adc
Total Device Dissipation @ T_C = 70°C Derate above 70°C	P_D	118 0.9	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

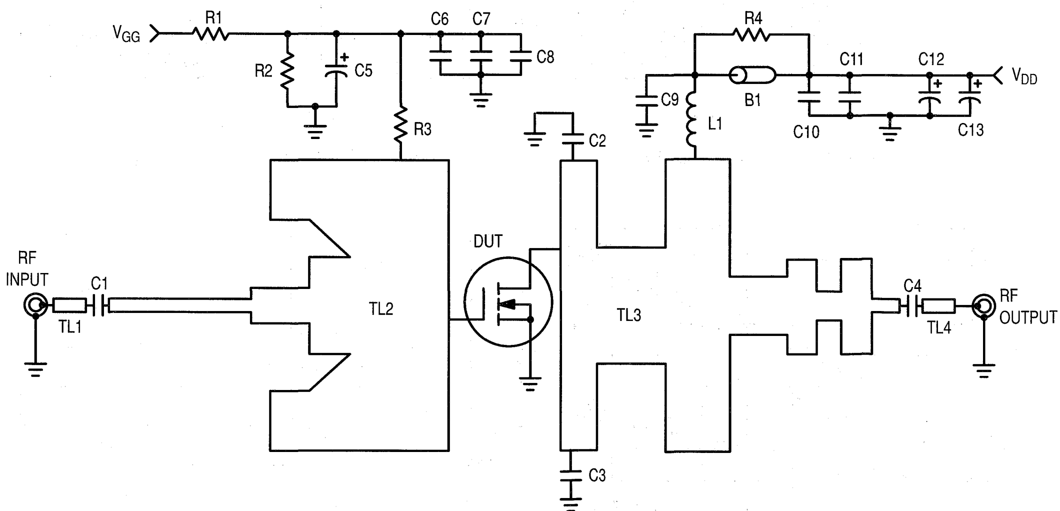
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 V, I_D = 1 μAdc)	$V_{(BR)DSS}$	65	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	–	–	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0 V)	I_{GSS}	–	–	1	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 2

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 200 μA)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 100 mA)	$V_{GS(Q)}$	3	4	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A)	$V_{DS(on)}$	–	0.65	0.8	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A)	g_{fs}	2.2	2.6	–	s
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	–	83	–	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	–	44	–	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	–	4.3	–	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 60 W, f = 945 MHz, I_{DQ} = 100 mA)	G_{ps}	11.5	15	–	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 60 W, f = 945 MHz, I_{DQ} = 100 mA)	η	53	60	–	%
Load Mismatch (V_{DD} = 28 V, P_{out} = 60 W, I_{DQ} = 100 mA, f = 945 MHz, Load VSWR 5:1 at all Phase Angles)	ψ	No Degradation in Output Power			



B1	Short RF Bead Fair Rite–2743019447	L1	5 Turns, 20 AWG, IDIA 0.126″
C1	18 pF Chip Capacitor	R1	10 kΩ, 1/4 W Resistor
C2, C3, C6, C9	43 pF Chip Capacitor	R2	13 kΩ, 1/4 W Resistor
C4	100 pF Chip Capacitor	R3	1.0 kΩ, 1/4 W Chip Resistor
C5, C12	10 μF, 50 Vdc Electrolytic Capacitor	R4	4 x 39 Ω, 1/8 W Chip Resistor
C7, C10	1000 pF Chip Capacitor	TL1–TL4	Microstrip Line See Photomaster
C8, C11	0.1 μF, 50 Vdc Chip Capacitor	Ckt Board	1/32″ Glass Teflon, ε_r = 2.55
C13	250 μF, 50 Vdc Electrolytic Capacitor		ARLON–GX–0300–55–22

Figure 1. MRF184 Test Circuit Schematic

TYPICAL CHARACTERISTICS

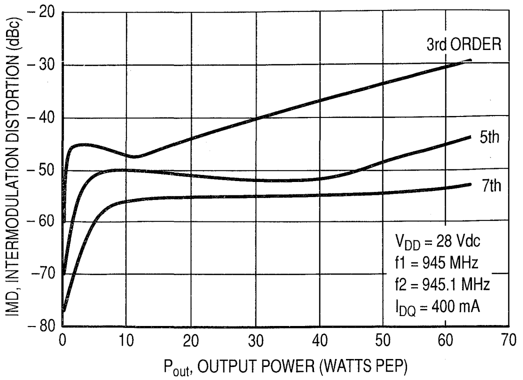


Figure 2. Intermodulation Distortion versus Output Power

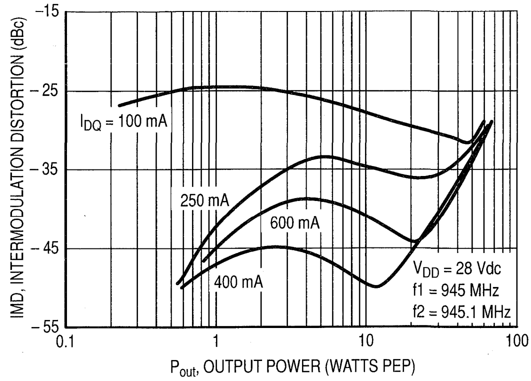


Figure 3. Intermodulation Distortion versus Output Power

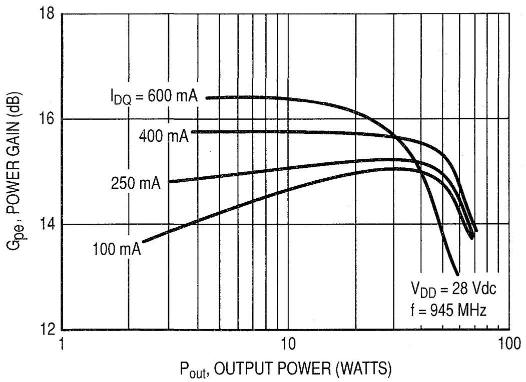


Figure 4. Power Gain versus Output Power

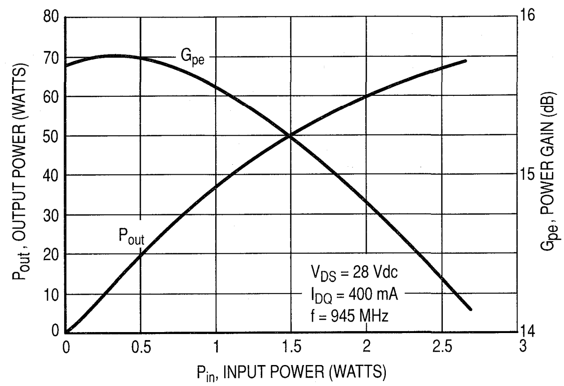


Figure 5. Output Power versus Input Power

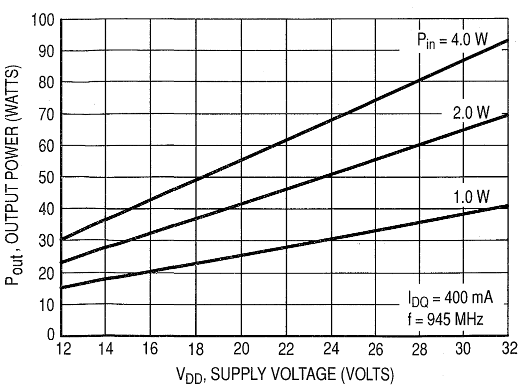


Figure 6. Output Power versus Supply Voltage

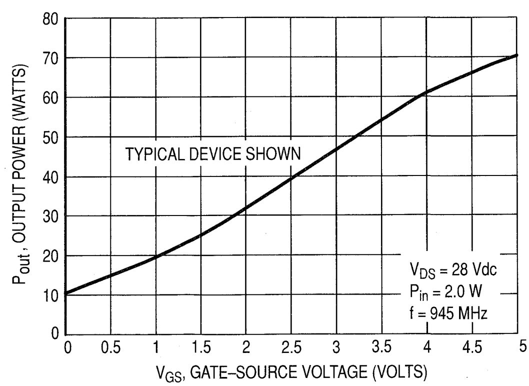


Figure 7. Output Power versus Gate Voltage

TYPICAL CHARACTERISTICS

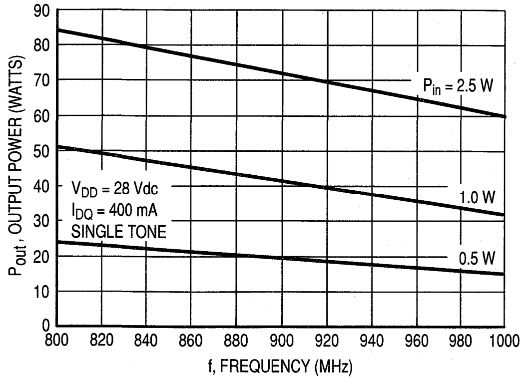


Figure 8. Output Power versus Frequency

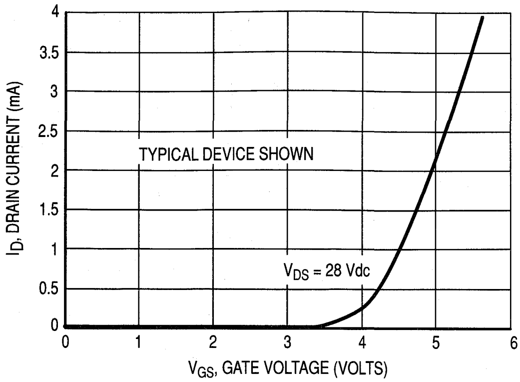


Figure 9. Drain Current versus Gate Voltage

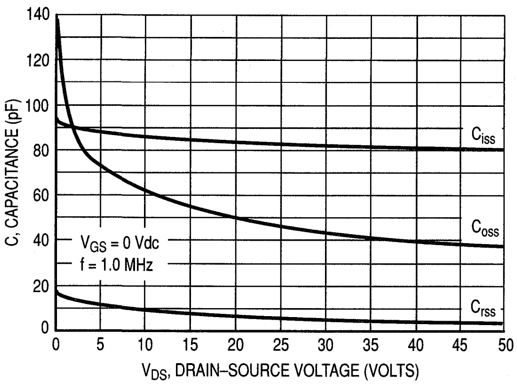


Figure 10. Capacitance versus Voltage

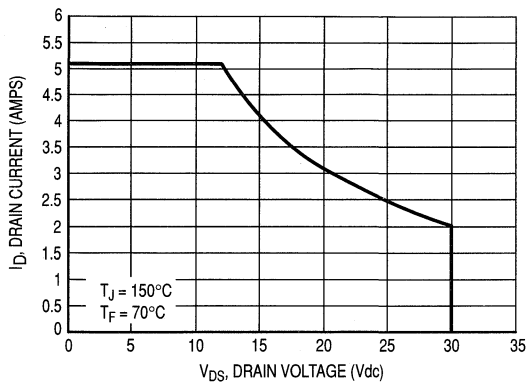


Figure 11. DC Safe Operating Area

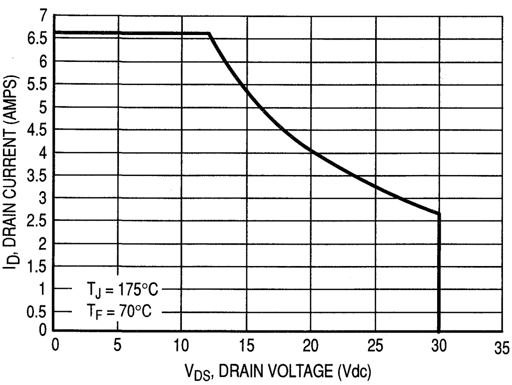


Figure 12. DC Safe Operating Area

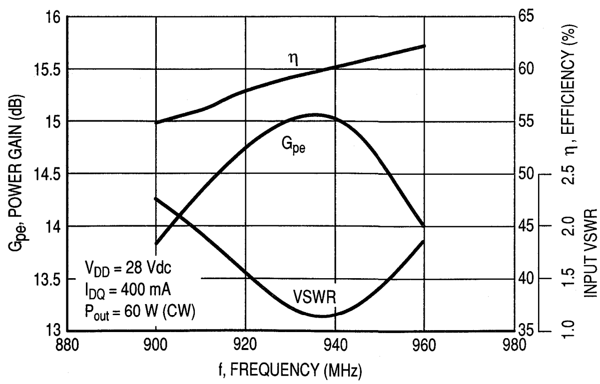


Figure 13. Performance in Broadband Circuit

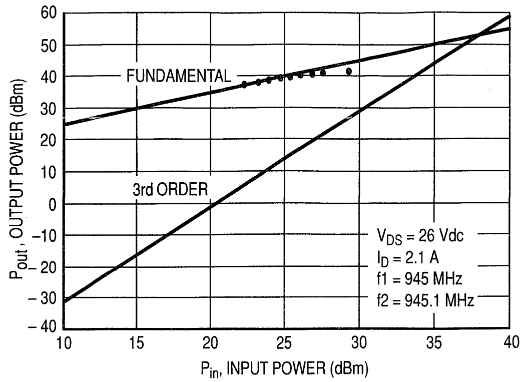


Figure 14. Class A Third Order Intercept Point

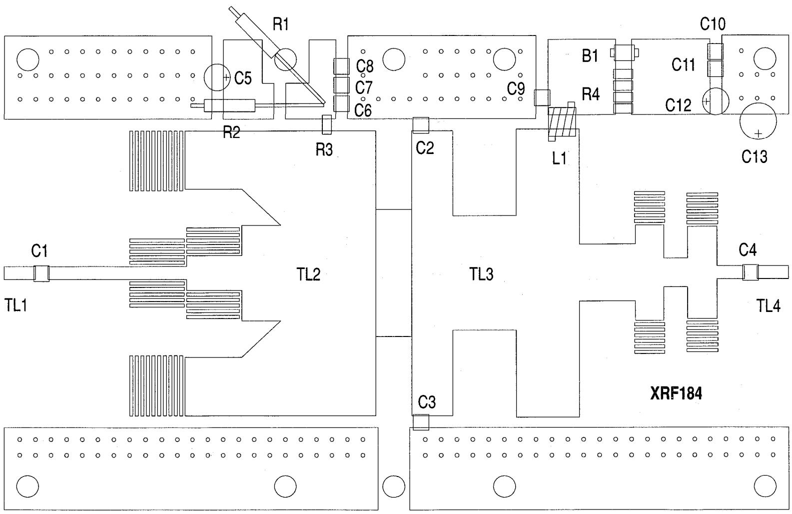
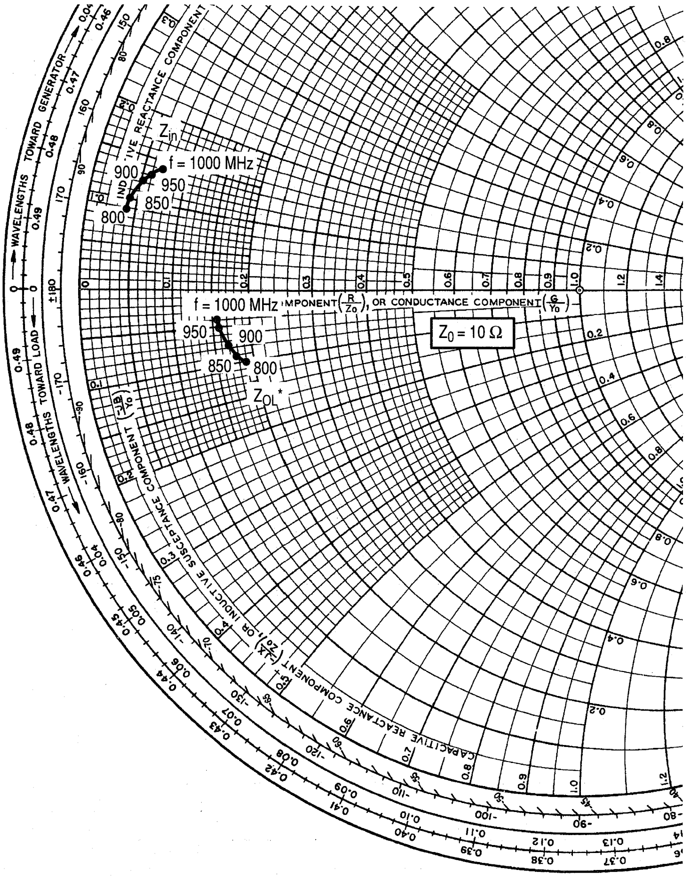


Figure 15. Component Parts Layout



V_{DD} = 28 Vdc, I_{DQ} = 100 mA, P_{out} = 60 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	0.40 + j0.90	1.85 – j1.00
850	0.45 + j1.10	1.75 – j0.90
900	0.52 + j1.20	1.70 – j0.75
950	0.60 + j1.30	1.60 – j0.50
1000	0.70 + j1.38	1.57 – j0.40

Z_{in} = Conjugate of source impedance.

Z_{out} = Conjugate of the load impedance at given output power, voltage, frequency and efficiency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency and device stability.

Figure 16. Series Equivalent Input and Output Impedance

Table 1. Common Source S–Parameters (V_{DS} = 13.5 V)

I_D = 2.0 A

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
20	0.916	179	10.88	80	0.014	–22	0.843	175
30	0.917	178	9.26	79	0.014	–25	0.847	174
40	0.918	177	8.10	78	0.015	–29	0.852	174
50	0.919	176	7.16	77	0.015	–33	0.853	174
100	0.919	175	4.57	75	0.015	–35	0.855	173
150	0.920	174	3.34	67	0.015	–38	0.865	173
200	0.921	173	2.60	62	0.014	–41	0.867	173
250	0.922	173	2.11	59	0.014	–45	0.877	173
300	0.928	172	1.77	55	0.014	–49	0.881	173
350	0.938	172	1.50	50	0.013	–55	0.887	173
400	0.941	171	1.28	47	0.013	–59	0.895	173
450	0.942	171	1.12	44	0.012	–62	0.896	173
500	0.943	171	1.00	41	0.012	–68	0.898	172
550	0.945	171	0.91	38	0.010	–75	0.899	172
600	0.947	171	0.80	35	0.010	–79	0.903	172
650	0.948	171	0.71	33	0.009	–85	0.905	172
700	0.955	170	0.65	30	0.008	–88	0.909	172
750	0.959	170	0.60	28	0.008	–95	0.919	172
800	0.962	169	0.55	25	0.007	–102	0.922	172
850	0.963	169	0.50	23	0.007	–111	0.923	171
900	0.964	169	0.45	21	0.007	–118	0.926	171
950	0.968	169	0.43	19	0.006	–125	0.929	171
1000	0.970	169	0.39	18	0.006	–129	0.933	171
1050	0.971	168	0.36	17	0.005	–134	0.935	171
1100	0.972	168	0.34	14	0.005	–142	0.936	170
1150	0.973	168	0.32	13	0.005	–149	0.938	170
1200	0.974	167	0.29	12	0.006	–156	0.940	169
1250	0.976	167	0.28	10	0.007	–162	0.943	169
1300	0.975	167	0.26	9	0.008	–173	0.945	168
1350	0.972	166	0.25	8	0.009	–178	0.946	167
1400	0.969	166	0.24	7	0.011	175	0.947	167
1450	0.965	165	0.22	6	0.012	172	0.948	167
1500	0.959	164	0.21	5	0.013	169	0.950	167

Table 2. Common Source S–Parameters (V_{DS} = 28 V)

I_D = 2.0 A

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
20	0.912	–170	16.01	84	0.016	–12	0.746	178
30	0.917	–173	13.73	82	0.015	–15	0.755	177
40	0.918	–174	12.02	80	0.014	–17	0.759	177
50	0.919	–176	10.62	78	0.013	–20	0.766	176
100	0.922	–178	6.76	71	0.012	–22	0.775	176
150	0.930	177	4.92	65	0.011	–25	0.791	176
200	0.931	176	3.82	60	0.010	–27	0.791	176
250	0.933	175	3.07	55	0.009	–29	0.793	176
300	0.941	174	2.53	51	0.009	–31	0.826	176
350	0.943	173	2.14	45	0.008	–35	0.834	176
400	0.945	172	1.83	41	0.008	–45	0.853	176
450	0.948	172	1.58	38	0.007	–52	0.858	176
500	0.950	172	1.39	35	0.007	–57	0.865	176
550	0.955	172	1.24	32	0.007	–61	0.876	176
600	0.960	172	1.10	29	0.006	–64	0.882	176
650	0.965	171	0.96	26	0.006	–68	0.888	175
700	0.967	171	0.89	24	0.006	–71	0.894	175
750	0.970	171	0.80	20	0.005	–73	0.904	175
800	0.973	170	0.73	18	0.005	–78	0.906	175
850	0.974	169	0.66	17	0.004	–83	0.908	174
900	0.975	169	0.61	13	0.004	–91	0.909	173
950	0.976	169	0.57	12	0.004	–94	0.915	173
1000	0.978	168	0.52	11	0.004	–96	0.916	173
1050	0.979	168	0.47	9	0.005	–102	0.919	172
1100	0.980	168	0.43	7	0.005	–115	0.924	172
1150	0.980	167	0.41	6	0.006	–119	0.931	171
1200	0.979	167	0.38	5	0.006	–125	0.934	170
1250	0.978	167	0.36	2	0.006	–139	0.935	170
1300	0.974	167	0.34	1	0.007	–148	0.936	170
1350	0.971	166	0.32	0	0.007	–156	0.937	169
1400	0.970	165	0.31	–1	0.007	–165	0.938	169
1450	0.969	165	0.30	–2	0.008	–171	0.939	169
1500	0.965	164	0.27	–3	0.008	–178	0.946	169

Advance Information

The RF MOSFET Line

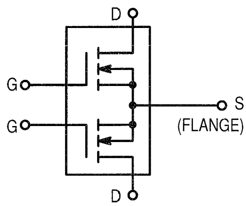
RF POWER Field-Effect Transistor

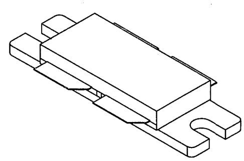
N–Channel Enhancement–Mode Lateral MOSFET

MRF185

85 WATTS, 1.0 GHz
28 VOLTS
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

- High Gain, Rugged Device
- Broadband Performance from HF to 1 GHz
- Bottom Side Source Eliminates DC Isolators, Reducing Common Mode Inductances





CASE 375B–02, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.45	Watts W/°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 V, I_D = 1 μAdc)	$V_{(BR)DSS}$	65	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	–	–	1	μAdc
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0 V)	I_{GSS}	–	–	1	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 1

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Quiescent Voltage (V_{DS} = 26 V, I_D = 300 mA per side)	$V_{GS(Q)}$	3	4	5	Vdc
Delta Quiescent Voltage between sides (V_{DS} = 26 V, I_D = 300 mA per side)	$\Delta V_{GS(Q)}$	–	0.15	0.3	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 3 A per side)	$V_{DS(on)}$	–	0.75	1	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A per side)	g_{fs}	1.6	2	–	s
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	–	38	–	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	–	4.6	6	pF
FUNCTIONAL CHARACTERISTICS					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 85 W, f = 960 MHz, I_{DQ} = 600 mA)	G_{ps}	11	14	–	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 85 W, f = 960 MHz, I_{DQ} = 600 mA)	η	45	55	–	%
Load Mismatch (V_{DD} = 28 Vdc, P_{out} = 85 W, f = 960 MHz, I_{DQ} = 600 mA, Load VSWR 5:1 at All Phase Angles)	Ψ	No Degradation in Output Power			

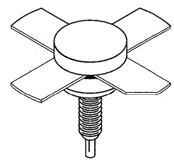
The RF Line
NPN Silicon RF Power Transistors

MRF240

40 W, 145–175 MHz
RF POWER
TRANSISTORS
NPN SILICON

. . . designed for 13.6 volt VHF large–signal class C and class AB linear power amplifier applications in commercial and industrial equipment.

- High Common Emitter Power Gain
- Specified 13.6 V, 160 MHz Performance:
  Output Power = 40 Watts
  Power Gain = 9.0 dB Min
  Efficiency = 55% Min
- Load Mismatch Capability at Rated Voltage and RF Drive
- Silicon Nitride Passivated
- Low Intermodulation Distortion, d_3 = –30 dB Typ



CASE 145A–09, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	100 0.57	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	70	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	90	125	pF

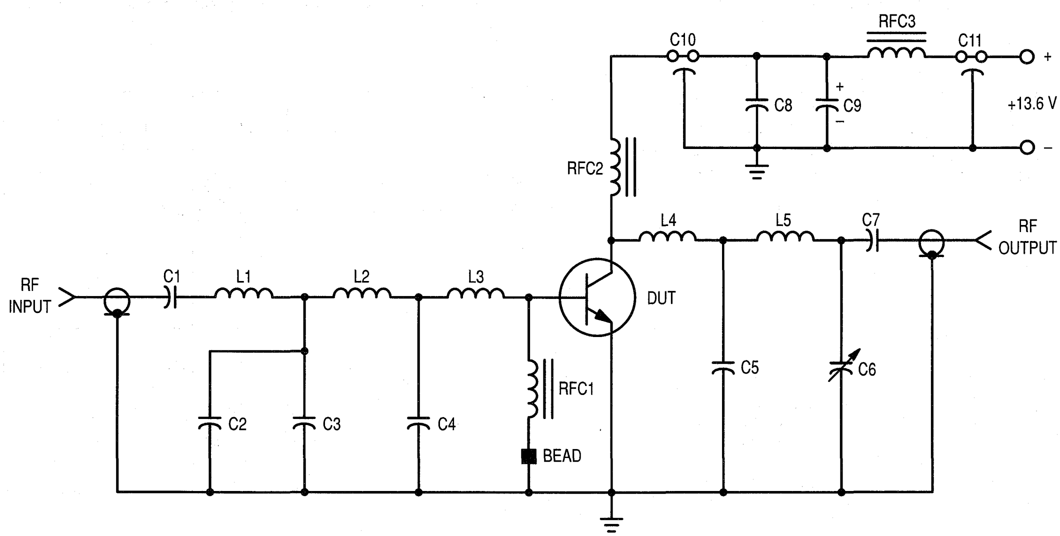
(continued)

NOTES:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 13.6 Vdc, P_{out} = 40 W, f = 160 MHz)	G_{PE}	9.0	10	—	dB
Collector Efficiency (V_{CC} = 13.6 Vdc, P_{out} = 40 W, f = 160 MHz)	η	55	—	—	%
TYPICAL SSB PERFORMANCE					
Intermodulation Distortion (3) (V_{CC} = 13.6 Vdc, P_{out} = 35 W (PEP), f1 = 146 MHz, f2 = 146.002 MHz, I_{CQ} = 50 mAdc)	IMD (d_3)	—	–30	—	dB

NOTE:
3. To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1 — 200 pF, 350 Vdc, UNELCO
C2 — 100 pF, 350 Vdc, UNELCO
C3 — 40 pF, 350 Vdc, UNELCO
C4, C5 — 80 pF, 350 Vdc, UNELCO
C6 — 1.0–20 pF, ARCO Trimmer
C7 — 100 pF 350 Vdc, UNELCO
C8 — 0.1 µF ERIE Disc Ceramic
C9 — 1.0 µF TANTALUM
C10, C11 — 680 pF ALLEN BRADLEY Feedthru
RFC1 — 0.15 µH Molded Choke
RFC2 — 10 Turns, #18 AWG on 470 Ohm, 1.0 Watt Resistor
Bead — FERROXCUBE Bead
RFC3 — FERROXCUBE Choke, VK200–4B
L1 — 3.3 x 0.2 cm AIRLINE Inductor
L2 — 1.0 x 0.2 cm AIRLINE Inductor
L3 — 1.2 x 0.6 cm Brass Pad
L4 — 1.2 x 0.6 cm Brass Pad and 2.0 x 0.2 cm AIRLINE Inductor
Board — G10, ε_r = 5, t = 62 mils 2 sided, 2 oz. Clad
Connectors: Type N

Figure 1. 160 MHz Test Circuit Schematic

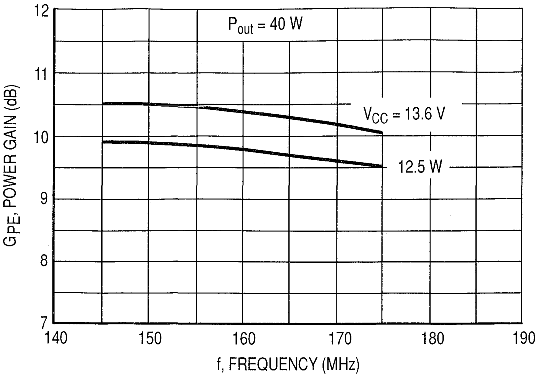


Figure 2. Power Gain versus Frequency

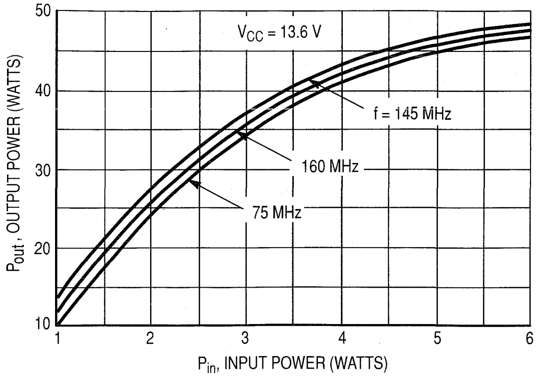


Figure 3. Output Power versus Input Power

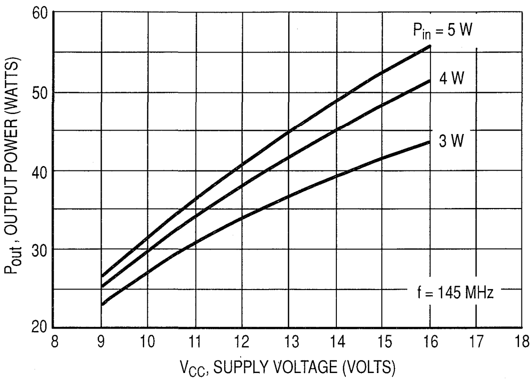


Figure 4. Output Power versus Supply Voltage

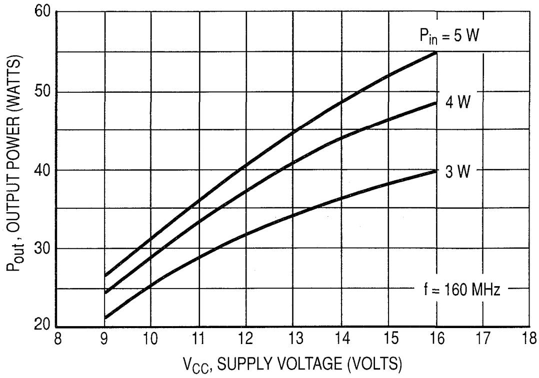


Figure 5. Output Power versus Supply Voltage

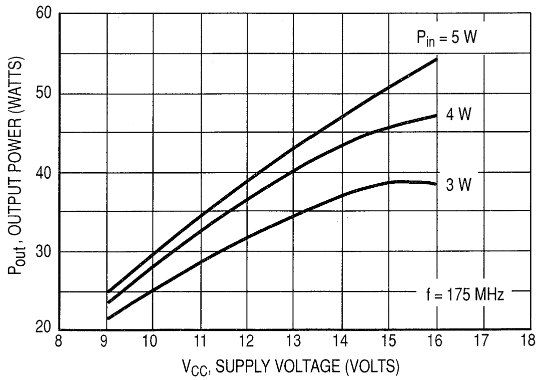
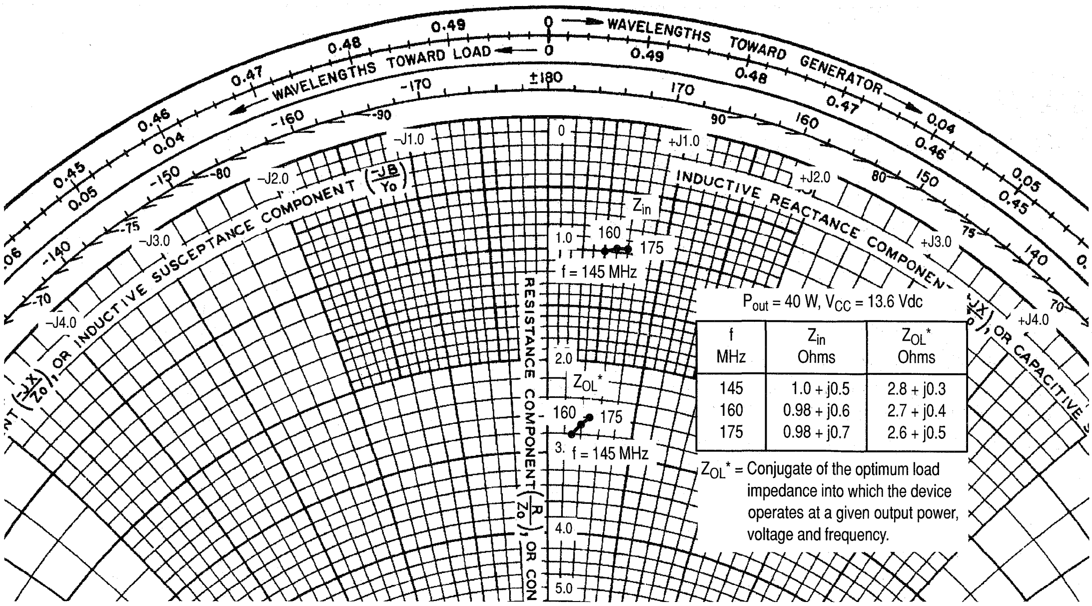


Figure 6. Output Power versus Supply Voltage



P_{out} = 40 W, V_{CC} = 13.6 Vdc

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
145	1.0 + j0.5	2.8 + j0.3
160	0.98 + j0.6	2.7 + j0.4
175	0.98 + j0.7	2.6 + j0.5

Z_{OL}^* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 7. Series Equivalent Input/Output Impedances

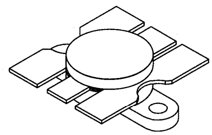
The RF Line
NPN Silicon RF Power Transistor

MRF247

The MRF247 is designed for 12.5 Volt VHF large–signal amplifier applications in industrial and commercial FM equipment operating to 175 MHz.

- Specified 12.5 Volt, 175 MHz Characteristics —
  Output Power = 75 Watts
  Power Gain = 7.0 dB Min
  Efficiency = 55% Min
- Characterized With Series Equivalent Large–Signal Impedance Parameters
- Internal Matching Network Optimized for Minimum Gain Frequency Slope Response Over the Range 136 to 175 MHz
- Load Mismatch Capability at Rated P_{out} and Supply Voltage

**75 W, 175 MHz
CONTROLLED Q
RF POWER
TRANSISTOR
NPN SILICON**



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	18	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Peak	I_C	20	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

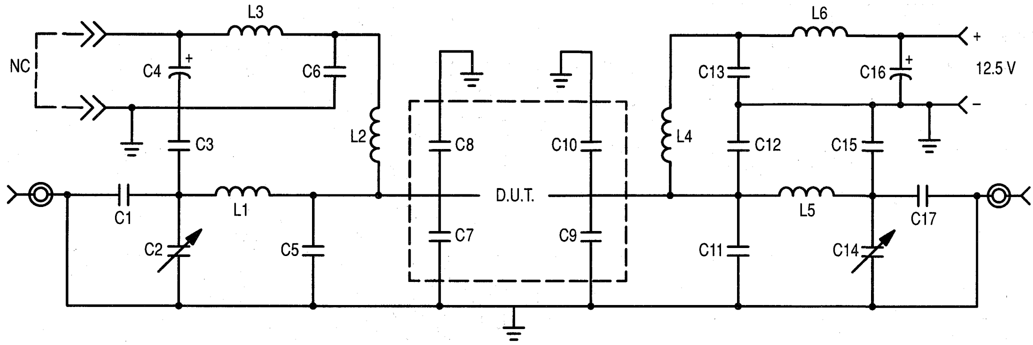
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc

(1) This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	75	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	235	300	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 75 Watts, f = 175 MHz)	G_{PE}	7.0	8.5	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 75 Watts, f = 175 MHz)	η	55	60	—	%
Load Mismatch (V_{CC} = 12.5 Vdc, P_{out} = 75 Watts, f = 175 MHz, VSWR = 30:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1, C17	330 pF ATC 100 mil Ceramic Capacitor	C11	150 pF Standard Unelco Clamped Mica Capacitor
C2, C14	Johansen 1–20 pF Trimmer Capacitor	C12	33 pF Mini–Unelco Clamped Mica Capacitor
C3	40 pF Standard Unelco Clamped Mica Capacitor	C15	27 pF Mini–Unelco Clamped Mica Capacitor
C4, C16	Sprague 10 µF – 35 Vdc Electrolytic Capacitor	L1	2 Turns, 16 AWG Enameled, IDIA 0.13″
C5	80 pF Standard Unelco Clamped Mica Capacitor	L2, L4	4 Turns, 18 AWG Enameled, IDIA 0.18″
C6, C13	91 pF Mini–Unelco Clamped Mica Capacitor	L3, L6	VK 200 with Ferrite Bead
C7, C8	240 pF ATC 100 mil Ceramic Capacitor	L5	2 Turns, 16 AWG Enameled, IDIA 0.15″
C9, C10	180 pF ATC 100 mil Ceramic Capacitor		

Figure 1. Output Power versus Input Power

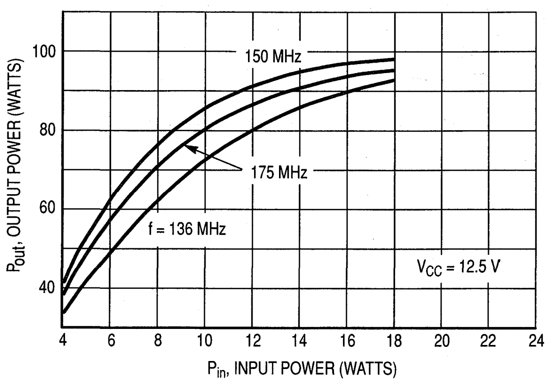


Figure 2. Output Power versus Input Power

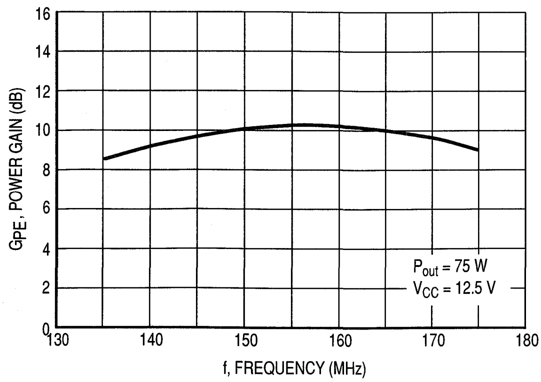


Figure 3. Power Gain versus Frequency

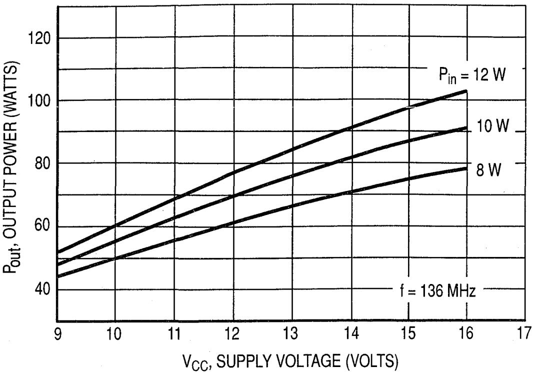


Figure 4. Output Power versus Supply Voltage

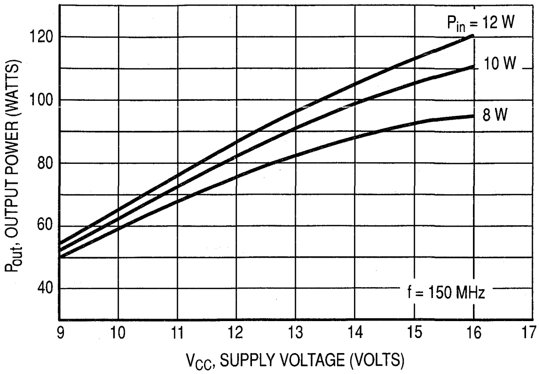


Figure 5. Output Power versus Supply Voltage

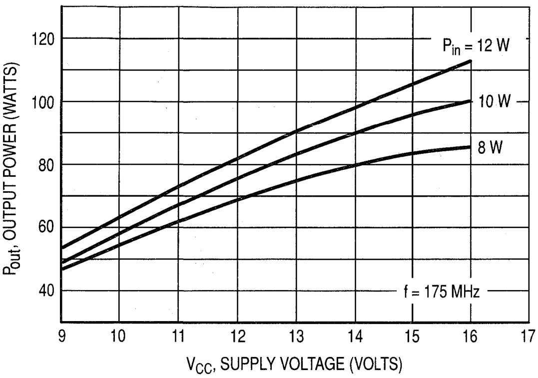
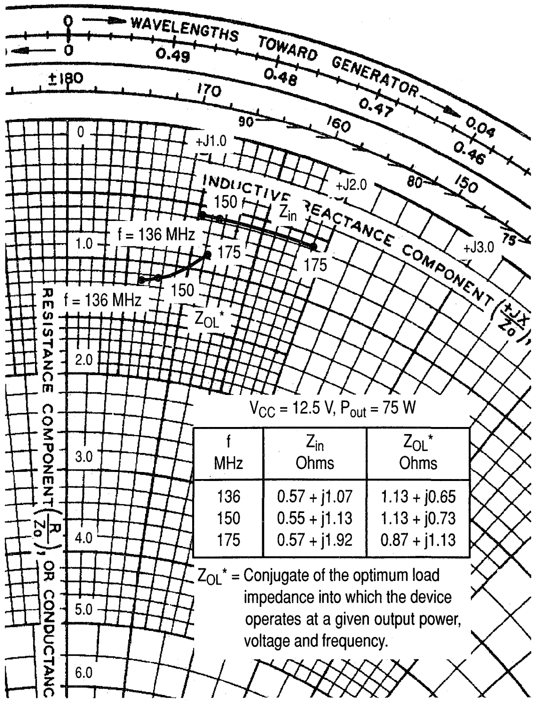


Figure 6. Output Power versus Supply Voltage



V_{CC} = 12.5 V, P_{out} = 75 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
136	0.57 + j1.07	1.13 + j0.65
150	0.55 + j1.13	1.13 + j0.73
175	0.57 + j1.92	0.87 + j1.13

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 7. Series Equivalent Impedances

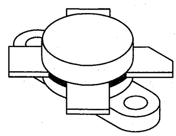
The RF MOSFET Line
RF Power
Field-Effect Transistor
N–Channel Enhancement–Mode

MRF255

Designed for broadband commercial and industrial applications at frequencies to 54 MHz. The high gain, broadband performance and linear characterization of this device makes it ideal for large–signal, common source amplifier applications in 12.5 Volt mobile and base station equipment.

- Guaranteed Performance at 54 MHz, 12.5 Volts
  Output Power — 55 Watts PEP
  Power Gain — 13 dB Min
  Two–Tone IMD — –25 dBc Max
  Efficiency — 40% Min, Two–Tone Test
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Aluminum Nitride Package Electrical Insulator
- Circuit Board Photomaster Available by Ordering Document MRF255PHT/D from Motorola Literature Distribution.

**55 W, 12.5 Vdc, 54 MHz
N–CHANNEL
BROADBAND
RF POWER FET**



CASE 211–11, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	36	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	36	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	22	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	175 1.0	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

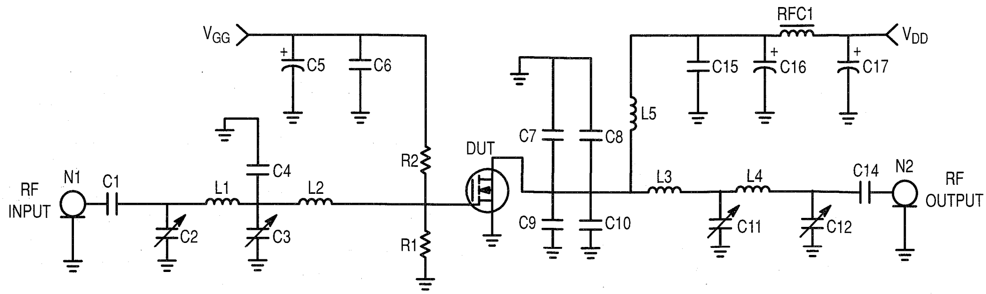
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 20 mAdc)	$V_{(BR)DSS}$	36	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 25 mAdc)	$V_{GS(th)}$	1.25	2.3	3.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 4.0 Adc)	$V_{DS(on)}$	—	—	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3.0 Adc)	g_{fs}	4.2	—	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	140	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	285	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	38	44	pF
FUNCTIONAL TESTS (In Motorola Test Fixture.)					
Common Source Amplifier Power Gain, f_1 = 54, f_2 = 54.001 MHz (V_{DD} = 12.5 Vdc, P_{out} = 55 W (PEP), I_{DQ} = 400 mA)	G_{ps}	13	16	—	dB
Intermodulation Distortion (1), f_1 = 54.000 MHz, f_2 = 54.001 MHz (V_{DD} = 12.5 Vdc, P_{out} = 55 W (PEP), I_{DQ} = 400 mA)	$IMD_{(d3,d5)}$	—	−30	−25	dBc
Drain Efficiency, f_1 = 54; f_2 = 54.001 MHz (V_{DD} = 12.5 Vdc, P_{out} = 55 W (PEP), I_{DQ} = 400 mA)	η	40	45	—	%
Drain Efficiency, f = 54 MHz (V_{DD} = 12.5 Vdc, P_{out} = 55 W CW, I_{DQ} = 400 mA)	η	—	60	—	%
Output Mismatch Stress, f_1 = 54; f_2 = 54.001 MHz (V_{DD} = 12.5 Vdc, P_{out} = 55 W (PEP), I_{DQ} = 400 mA, VSWR = 20:1, at all phase angles)	ψ	No Degradation in Output Power Before and After Test			

(1) To MIL–STD–1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1 — 470 pF, Chip Capacitor
C2, C3, C11, C12 — 20–200 pF, Trimmer, ARCO #464
C4 — 100 pF, Chip Capacitor
C5, C17 — 100 μF, 15 V, Electrolytic
C6 — 0.001 μF, Disc Ceramic
C7, C8, C9, C10 — 330 pF, Chip Capacitor
C14 — 1200 pF, ATC Chip Capacitor
C15 — 910 pF, 500 V, Dipped Mica
C16 — 47 μF, 16 V, Electrolytic

L1 — 8 Turns, #20 AWG, 0.126″ ID
L2 — 5 Turns, #18 AWG, 0.142″ ID
L3 — 3 Turns, #20 AWG, 0.102″ ID
L4 — 7 Turns, #24 AWG, 0.070″ ID
L5 — 6.5 Turns, #18 AWG, 0.230″ ID, 0.5″ Long
N1, N2 — Type N Flange Mount
RFC1 — Ferroxcube VK–200–19/4B
R1 — 39 kΩ, 1/4 W Carbon
R2 — 150 Ω, 1/4 W Carbon
Board — G–10 .060″

Figure 1. 54 MHz Linear RF Test Circuit Electrical Schematic

TYPICAL CHARACTERISTICS

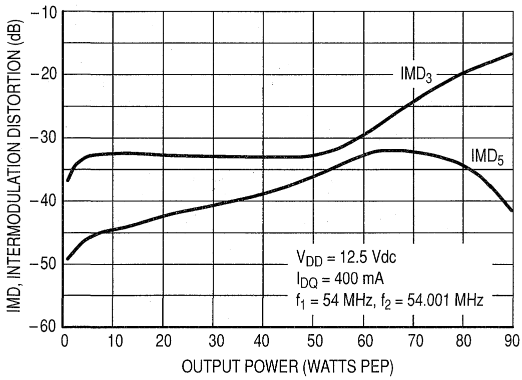


Figure 2. IMD versus Output Power

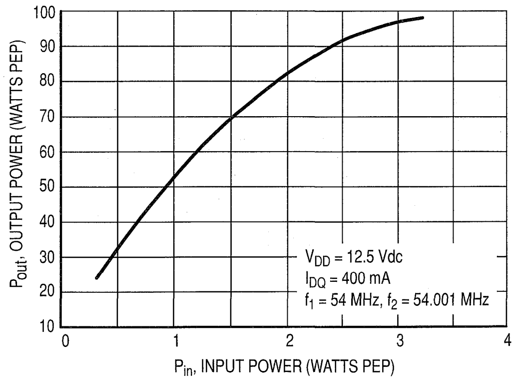


Figure 3. Output Power versus Input Power

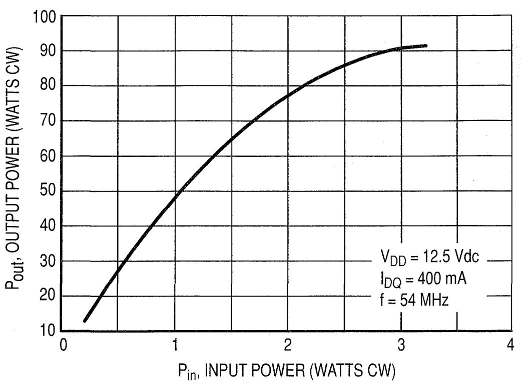


Figure 4. Output Power versus Input Power

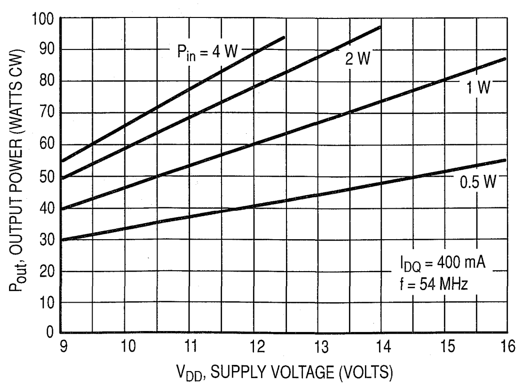


Figure 5. Output Power versus Supply Voltage

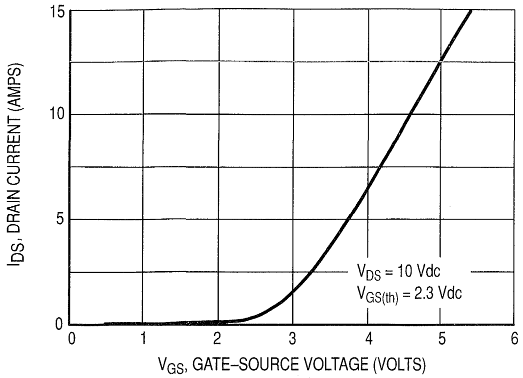


Figure 6. Drain Current versus Gate Voltage

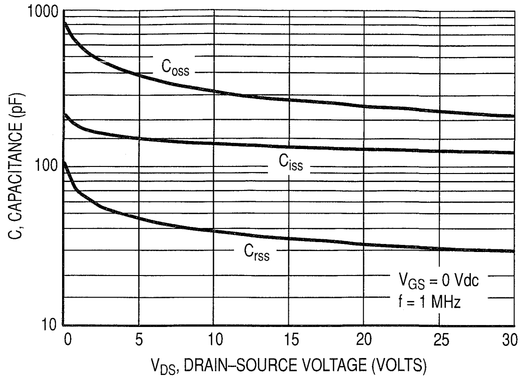


Figure 7. Capacitance versus Voltage

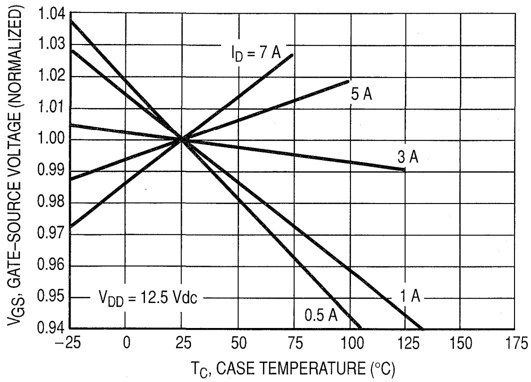


Figure 8. Gate–Source Voltage versus Case Temperature

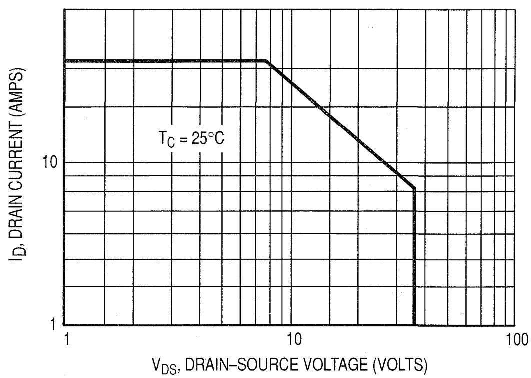


Figure 9. DC Safe Operating Area

Table 1. Series Equivalent Input and Output Impedance

V_{DD} = 12.5 Vdc, I_{DQ} = 400 mA, P_{out} = 55 W PEP
Optimized for Efficiency and IM Performance

f MHz	Z_{in} Ohms	Z_{OL^*} Ohms
54	6.50 + j7.96	1.27 + j1.54

Z_{OL^*} = Conjugate of the optimum load impedance into which the device operates at a given power, voltage and frequency.

Table 2. Common Source Scattering Parameters
(V_{DS} = 12.5 Vdc)

I_D = 100 mA

f (MHz)	S11		S21		S12		S22	
	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
1	0.98	−32	39.6	161	0.013	71	0.32	−80
2	0.92	−60	34.6	145	0.023	56	0.50	−108
5	0.81	−110	21.3	118	0.035	29	0.75	−143
10	0.76	−140	11.9	102	0.039	14	0.83	−160
20	0.74	−158	6.08	90	0.040	4	0.86	−169
30	0.75	−163	4.03	82	0.039	−2	0.87	−173
40	0.75	−166	2.98	77	0.038	−5	0.87	−174
50	0.76	−167	2.35	72	0.037	−8	0.88	−175
60	0.78	−168	1.91	67	0.036	−10	0.89	−176
70	0.79	−168	1.60	63	0.034	−12	0.89	−176
80	0.80	−169	1.36	59	0.032	−13	0.90	−177
90	0.81	−169	1.18	56	0.031	−14	0.90	−177
100	0.82	−169	1.03	52	0.029	−15	0.91	−177
120	0.85	−170	0.81	46	0.025	−14	0.92	−178
140	0.87	−171	0.65	41	0.022	−11	0.93	−179
160	0.88	−172	0.54	37	0.019	−6	0.94	180
180	0.90	−173	0.45	33	0.017	2	0.95	179
200	0.91	−174	0.38	30	0.016	12	0.95	178
220	0.92	−175	0.33	27	0.016	23	0.96	177
240	0.93	−176	0.29	25	0.016	34	0.96	176
260	0.94	−177	0.25	23	0.018	44	0.97	175

I_D = 400 mA

f (MHz)	S11		S21		S12		S22	
	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
1	0.98	−46	56.6	155	0.008	66	0.45	−148
2	0.95	−80	46.1	137	0.013	48	0.64	−151
5	0.90	−129	25.1	113	0.017	25	0.84	−164
10	0.88	−153	13.4	100	0.019	14	0.89	−172
20	0.88	−167	6.82	91	0.019	10	0.91	−176
30	0.88	−171	4.55	87	0.019	9	0.91	−178
40	0.88	−173	3.41	83	0.019	10	0.91	−178
50	0.88	−175	2.72	80	0.019	11	0.91	−179
60	0.88	−176	2.25	78	0.019	12	0.91	−179
70	0.88	−176	1.92	75	0.019	14	0.92	−180
80	0.88	−177	1.67	72	0.019	16	0.92	180
90	0.89	−177	1.47	70	0.019	18	0.92	179
100	0.89	−178	1.31	68	0.019	20	0.92	179
120	0.89	−178	1.08	63	0.019	24	0.92	179
140	0.89	−179	0.90	59	0.019	29	0.93	178
160	0.90	−179	0.77	55	0.020	34	0.93	177
180	0.90	−180	0.67	52	0.021	38	0.93	177
200	0.91	180	0.59	48	0.022	43	0.94	176
220	0.91	179	0.53	45	0.023	47	0.94	175
240	0.91	179	0.47	42	0.025	50	0.95	175
260	0.92	178	0.43	40	0.026	53	0.95	174

Table 2. Common Source Scattering Parameters (continued)
(V_{DS} = 12.5 Vdc)

I_D = 1 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1	0.98	−54	65.5	152	0.006	63	0.60	−162
2	0.96	−91	50.9	133	0.009	44	0.75	−163
5	0.93	−137	26.2	110	0.011	23	0.88	−170
10	0.93	−158	13.7	99	0.012	15	0.91	−175
20	0.92	−169	6.96	92	0.012	15	0.92	−178
30	0.92	−173	4.65	89	0.012	18	0.93	−179
40	0.92	−175	3.49	86	0.013	21	0.93	−180
50	0.92	−176	2.79	84	0.013	25	0.93	180
60	0.92	−177	2.32	82	0.013	28	0.93	179
70	0.92	−178	1.99	80	0.014	31	0.93	179
80	0.92	−179	1.74	78	0.014	34	0.93	179
90	0.92	−179	1.54	76	0.015	37	0.93	178
100	0.92	−180	1.39	74	0.016	40	0.93	178
120	0.92	180	1.15	71	0.017	44	0.93	177
140	0.92	179	0.98	68	0.019	48	0.93	177
160	0.92	178	0.86	65	0.020	51	0.93	176
180	0.92	178	0.76	62	0.022	54	0.93	176
200	0.92	177	0.68	59	0.024	56	0.94	175
220	0.92	177	0.61	56	0.026	58	0.94	175
240	0.92	176	0.56	53	0.028	59	0.94	174
260	0.92	176	0.51	51	0.030	61	0.94	173

DESIGN CONSIDERATIONS

The MRF255 is a common–surce, RF power, N–channel enhancement mode Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

This device was designed primarily for HF 12.5 V mobile linear power amplifier applications. The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

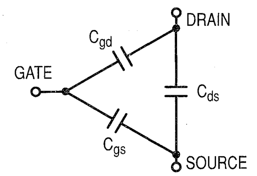
MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since the MRF255 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 8 for a typial plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. The MRF255 was characterized for linear and CW operation at I_{DQ} = 400 mA, which is the suggested value of bias current for typical applications.

The gate is a dc open circuit and draws essentially no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some applications may require a more elaborate bias sytem.

GAIN CONTROL

For CW applications, power output of the MRF255 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, AGC/ALC and modulation systems. The characteristic is very dependent on frequency and load line.

The RF MOSFET Line
Power Field-Effect Transistor
N–Channel Enhancement–Mode

MRF275G

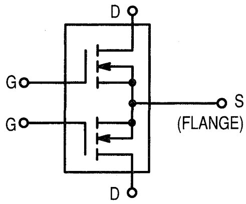
**150 W, 28 V, 500 MHz
N–CHANNEL MOS
BROADBAND
100 – 500 MHz
RF POWER FET**

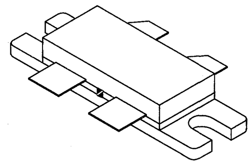
Designed primarily for wideband large–signal output and driver stages from 100 – 500 MHz.

- Guaranteed Performance @ 500 MHz, 28 Vdc
  Output Power — 150 Watts
  Power Gain — 10 dB (Min)
  Efficiency — 50% (Min)
  100% Tested for Load Mismatch at all Phase Angles with VSWR 30:1
- Overall Lower Capacitance @ 28 V
  C_{iss} — 135 pF
  C_{oss} — 140 pF
  C_{rss} — 17 pF
- Simplified AVC, ALC and Modulation

Typical data for power amplifiers in industrial and commercial applications:

- Typical Performance @ 400 MHz, 28 Vdc
  Output Power — 150 Watts
  Power Gain — 12.5 dB
  Efficiency — 60%
- Typical Performance @ 225 MHz, 28 Vdc
  Output Power — 200 Watts
  Power Gain — 15 dB
  Efficiency — 65%





CASE 375–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Adc
Drain Current — Continuous	I_D	26	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	400 2.27	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

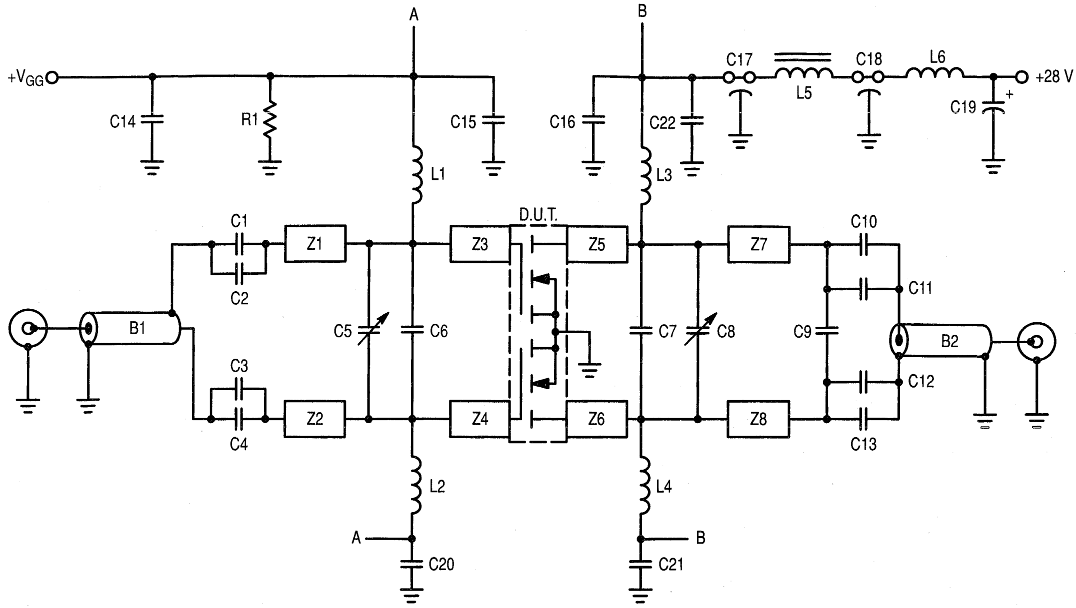
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1	mA
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1	µA
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.5	2.5	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 5 A)	$V_{DS(on)}$	0.5	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	3	3.75	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	135	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	140	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	17	—	pF
FUNCTIONAL CHARACTERISTICS (2) (Figure 1)					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 150 W, f = 500 MHz, I_{DQ} = 2 x 100 mA)	G_{ps}	10	11.2	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 150 W, f = 500 MHz, I_{DQ} = 2 x 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 150 W, f = 500 MHz, I_{DQ} = 2 x 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

1. Each side of device measured separately.
2. Measured in push–pull configuration.



B1	Balun, 50 Ω, 0.086″ O.D. 2″ Long, Semi Rigid Coax	L5	Ferroxcube VK200 20/4B
B2	Balun, 50 Ω, Coax 0.141″ O.D. 2″ Long, Semi Rigid	L6	4 Turns #16, 0.340″ I.D., Enameled Wire
C1, C2, C3, C4, C10, C11, C12, C13	270 pF, ATC Chip Capacitor	R1	1.0 kΩ,1/4 W Resistor
C5, C8	1.0–20 pF, Trimmer Capacitor, Johanson	W1 – W4	20 x 200 x 250 mils, Wear Pads, Beryllium–Copper, (See Component Location Diagram)
C6	22 pF, Mini–Unelco Capacitor		
C7	15 pF, Unelco Capacitor		
C9	2.1 pF, ATC Chip Capacitor	Z1, Z2	1.10″ x 0.245″, Microstrip Line
C14, C15, C16, C20, C21, C22	0.1 μF, Ceramic Capacitor	Z3, Z4, Z5, Z6	0.300″ x 0.245″, Microstrip Line
		Z7, Z8	1.00″ x 0.245″, Microstrip Line
C17, C18	680 pF, Feedthru Capacitor	Board material	0.060″ Teflon–fiberglass,
C19	10 μF, 50 V, Electrolytic Capacitor, Tantalum		
L1, L2	10 Turns AWG #24, 0.145″ O.D., 106 nH Taylor–Spring Inductor		
L3, L4	10 Turns AWG #18, 0.340″ I.D., Enameled Wire		

ε_r = 2.55, copper clad both sides, 2 oz. copper.
Points A are connected together on PCB.
Points B are connected together on PCB.

Figure 1. 500 MHz Test Circuit

TYPICAL CHARACTERISTICS

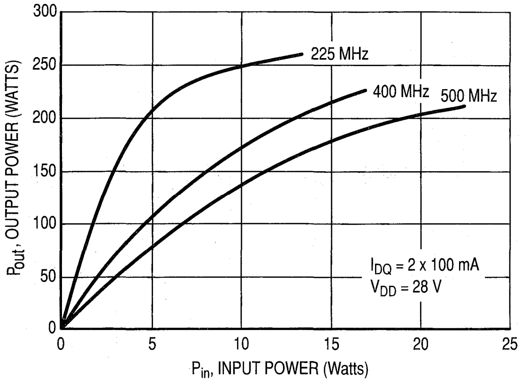


Figure 2. Output Power versus Input Power

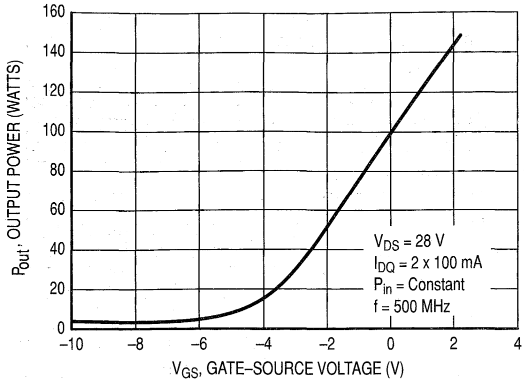


Figure 3. Output Power versus Gate Voltage

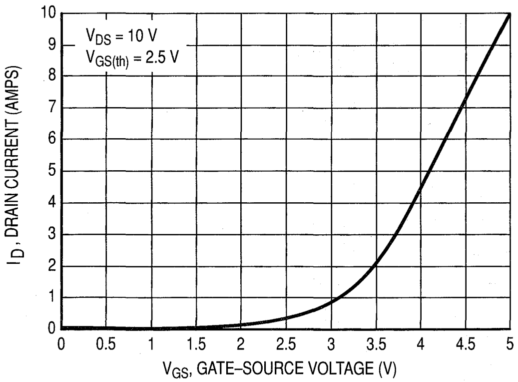


Figure 4. Drain Current versus Gate Voltage (Transfer Characteristics)

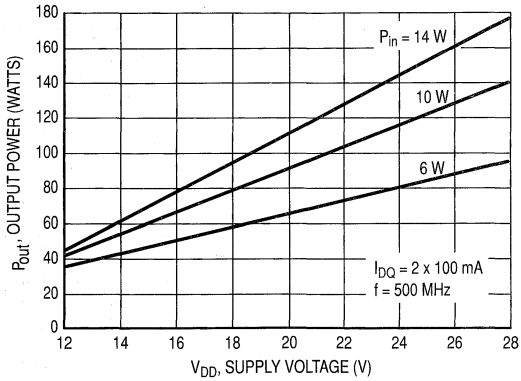


Figure 5. Output Power versus Supply Voltage

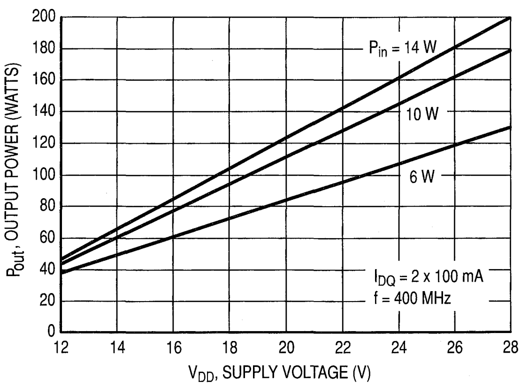


Figure 6. Output Power versus Supply Voltage

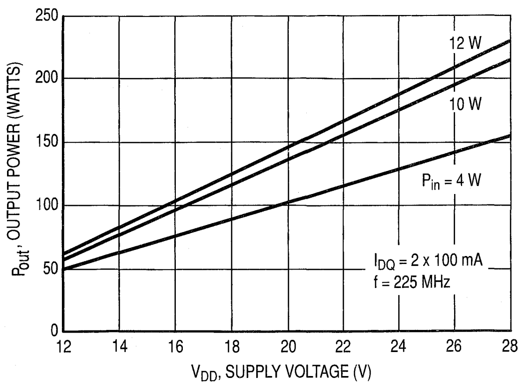


Figure 7. Output Power versus Supply Voltage

TYPICAL CHARACTERISTICS

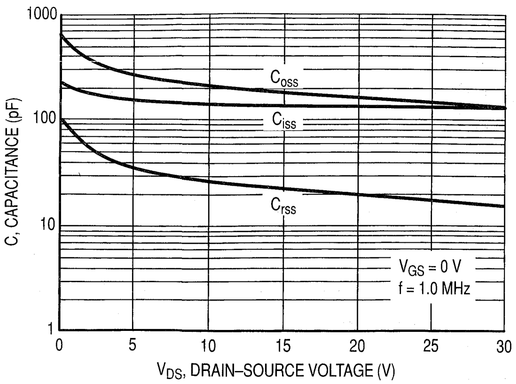


Figure 8. Capacitance versus Drain–Source Voltage*
*Data shown applies only to one half of device, MRF275G

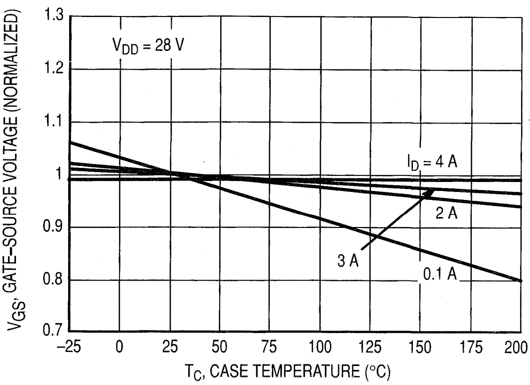


Figure 9. Gate–Source Voltage versus Case Temperature

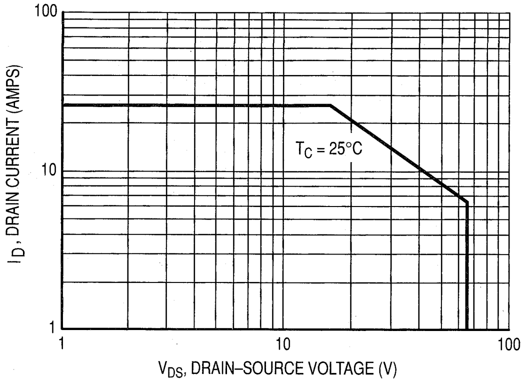
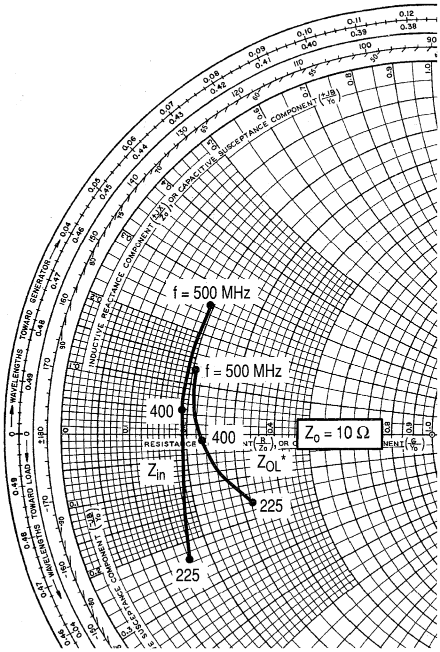


Figure 10. DC Safe Operating Area



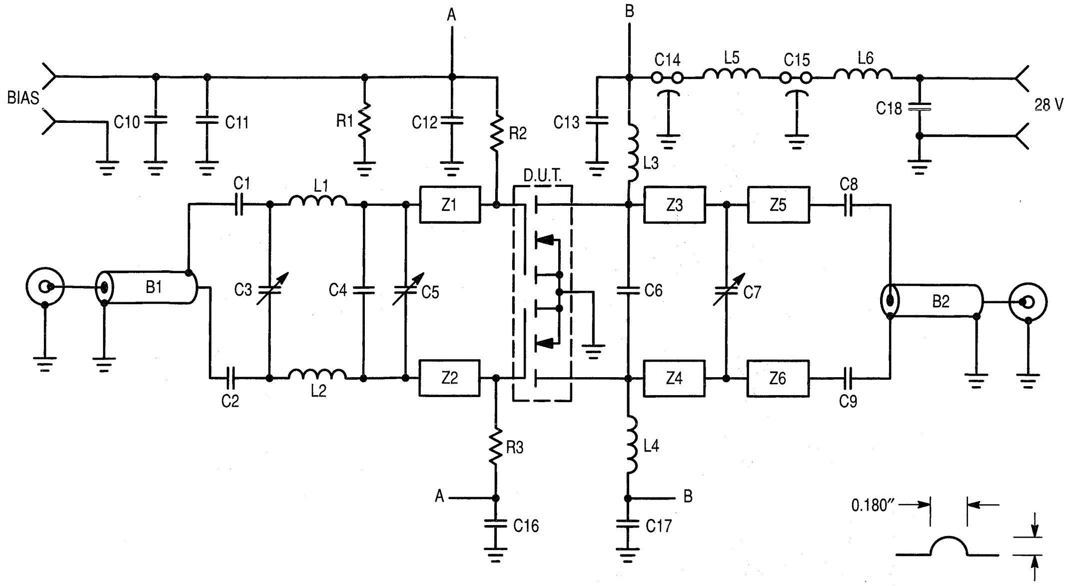
V_{DD} = 28 V, I_{DQ} = 2 x 100 mA, P_{out} = 150 W

f (MHz)	Z_{in} Ohms	Z_{OL}* Ohms
225	1.6 – j2.30	3.2 – j1.50
400	1.9 + j0.48	2.3 – j0.19
500	1.9 + j2.60	2.0 + j1.30

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

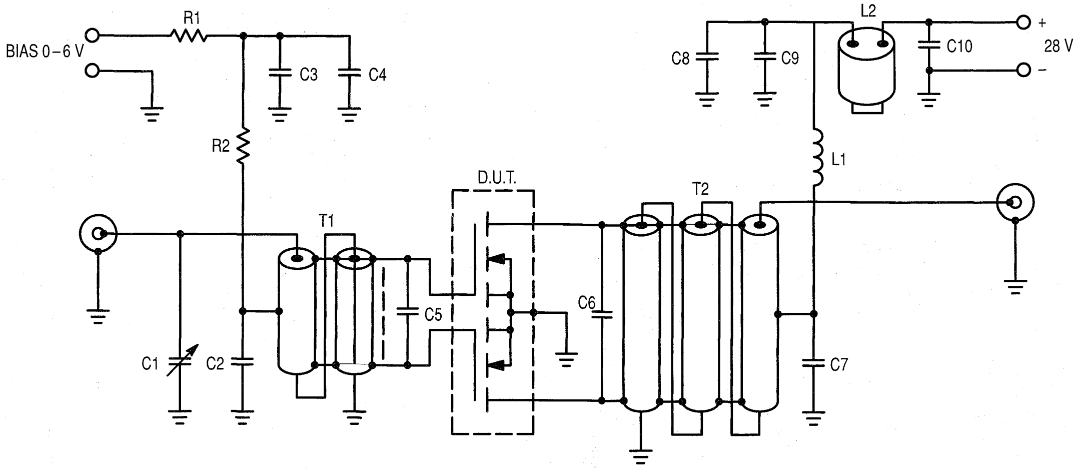
Note: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

Figure 11. Series Equivalent Input/Output Impedance



B1	Balun, 50 Ω, 0.086″ O.D. 2″ Long, Semi Rigid Coax	L1, L2	#18 Wire, Hairpin Inductor
B2	Balun, 50 Ω, 0.141″ O.D. 2″ Long, Semi Rigid Coax	L3, L4	12 Turns #18, 0.340″ I.D., Enameled Wire
C1, C2, C8, C9	270 pF, ATC Chip Capacitor	L5	Ferroxcube VK200 20/4B
C3, C5, C7	1.0–20 pF, Trimmer Capacitor	L6	3 Turns #16, 0.340″ I.D., Enameled Wire
C4	15 pF, ATC Chip Capacitor	R1	1.0 kΩ, 1/4 W Resistor
C6	33 pF, ATC Chip Capacitor	R2, R3	10 kΩ, 1/4 W Resistor
C10, C12, C13, C16, C17	0.01 µF, Ceramic Capacitor	Z1, Z2	0.400″ x 0.250″, Microstrip Line
C11	1.0 µF, 50 V, Tantalum	Z3, Z4	0.870″ x 0.250″, Microstrip Line
C14, C15	680 pF, Feedthru Capacitor	Z5, Z6	0.500″ x 0.250″, Microstrip Line
C18	20 µF, 50 V, Tantalum	Board material	0.060″ Teflon–fiberglass, ε_r = 2.55, copper clad both sides, 2 oz. copper.

Figure 12. 400 MHz Test Circuit



C1	8.0–60 pF, Arco 404	R1	100 Ω, 1/2 W
C2, C3, C7, C8	1000 pF, Chip Capacitor	R2	1.0 k Ω, 1/2 W
C4, C9	0.1 μF, Chip Capacitor	T1	4:1 Impedance Ratio, RF Transformer Can Be Made of 25 Ω, Semi Rigid Coax, 47–52 Mils O.D.
C5	180 pF, Chip Capacitor	T2	1:9 Impedance Ratio, RF Transformer. Can Be Made of 15–18 Ω, Semi Rigid Coax, 62–90 Mils O.D.
C6	100 pF and 130 pF, Chips in Parallel		
C10	0.47 μF, Chip Capacitor, 1215 or Equivalent, Kemet		
L1	10 Turns AWG #16, 1/4″ I.D., Enamel Wire, Close Wound		
L2	Ferrite Beads of Suitable Material for 1.5–2.0 μH Total Inductance		

Board material 062″ fiberglass (G10), $\varepsilon_r \cong 5$, Two sided, 1 oz. Copper.

Unless otherwise noted, all chip capacitors are ATC Type 100 or Equivalent.

NOTE: For stability, the input transformer T1 should be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

Figure 13. 225 MHz Test Circuit

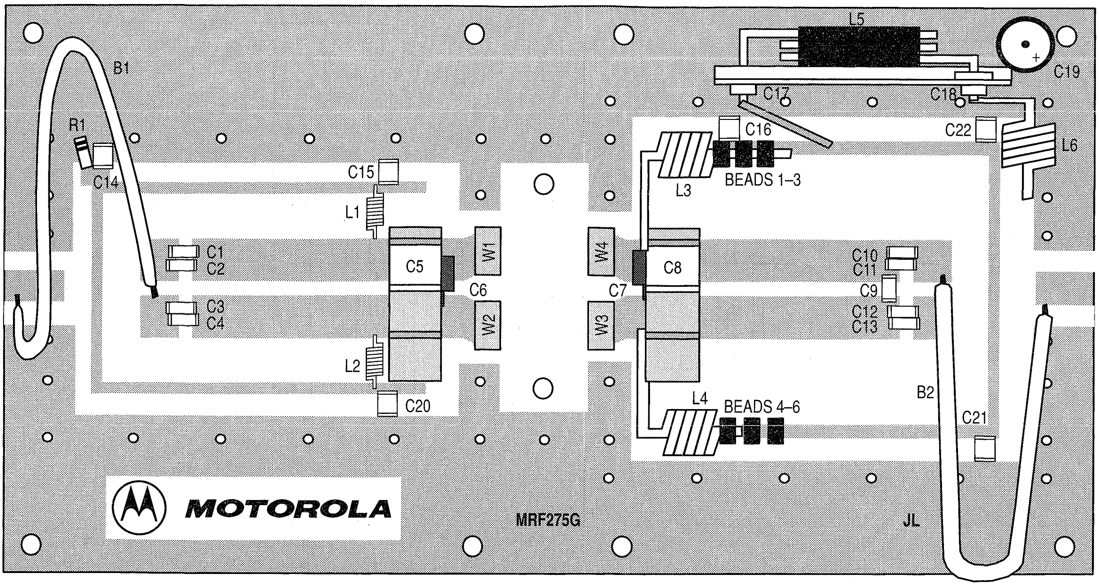


Figure 14. MRF275G Component Location (500 MHz)
(Not to Scale)

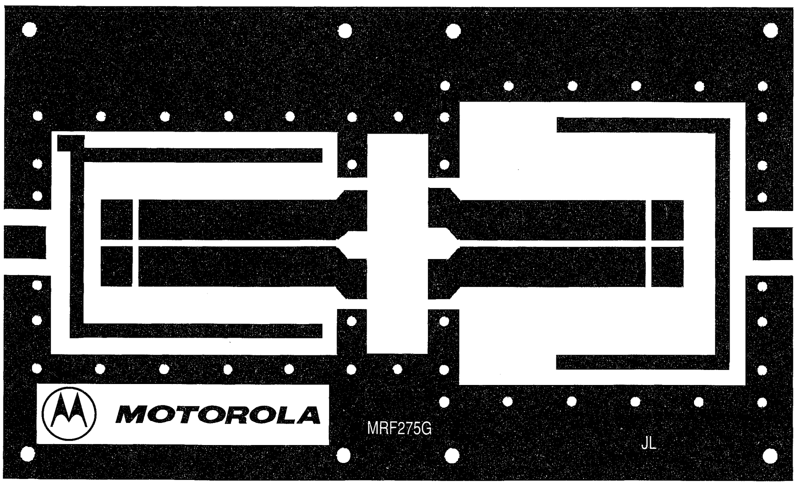


Figure 15. MRF275G Circuit Board Photo Master (500 MHz) Scale 1:1
(Reduced 25% in printed data book, DL110/D)

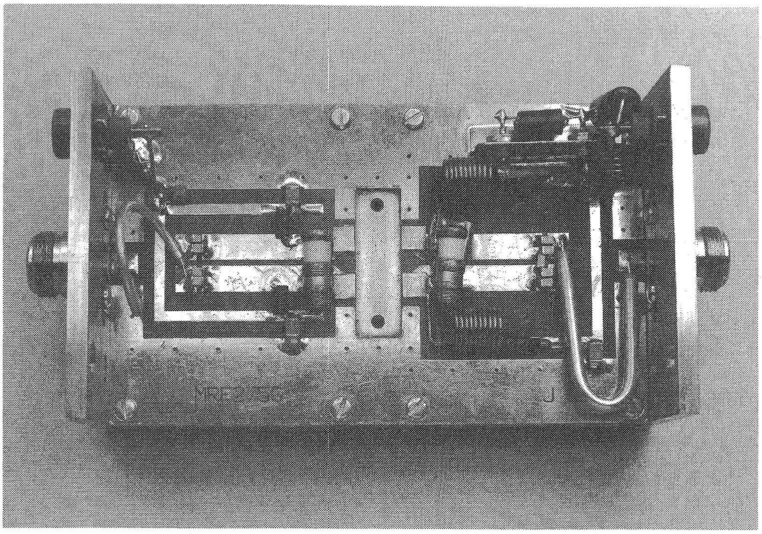


Figure 16. MRF275G Test Fixture

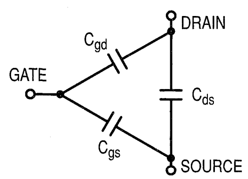
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

The C_{iss} given in the electrical characteristics table was measured using method 2 above. It should be noted that C_{iss}, C_{oss}, C_{rss} are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain, data presented in Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of this device are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

DESIGN CONSIDERATIONS

The MRF275G is a RF power N–channel enhancement mode field–effect transistor (FETs) designed for HF, VHF and UHF power amplifier applications. Motorola RF MOSFETs feature a vertical structure with a planar design.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

The MRF275G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF275G was characterized at I_{DQ} = 100 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

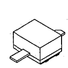
GAIN CONTROL

Power output of the MRF275G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

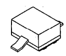
The RF Sub–Micron MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF282S
MRF282Z

10 W, 2000 MHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 458–03, STYLE 1
(MRF282S)



CASE 458A–01, STYLE 1
(MRF282Z)

Designed for class A and class AB PCN and PCS base station applications at frequencies up to 2600 MHz. Suitable for FM, TDMA, CDMA, and multicarrier amplifier applications.

- Specified Two–Tone Performance @ 2000 MHz, 26 Volts
  Output Power = 10 Watts (PEP)
  Power Gain = 11 dB
  Efficiency = 30%
  Intermodulation Distortion = –30 dBc
- Specified Single–Tone Performance @ 2000 MHz, 26 Volts
  Output Power = 10 Watts (CW)
  Power Gain = 11 dB
  Efficiency = 40%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 10 Watts (CW) Output Power
- Gold Metallization for Improved Reliability

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 0.34	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.9	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

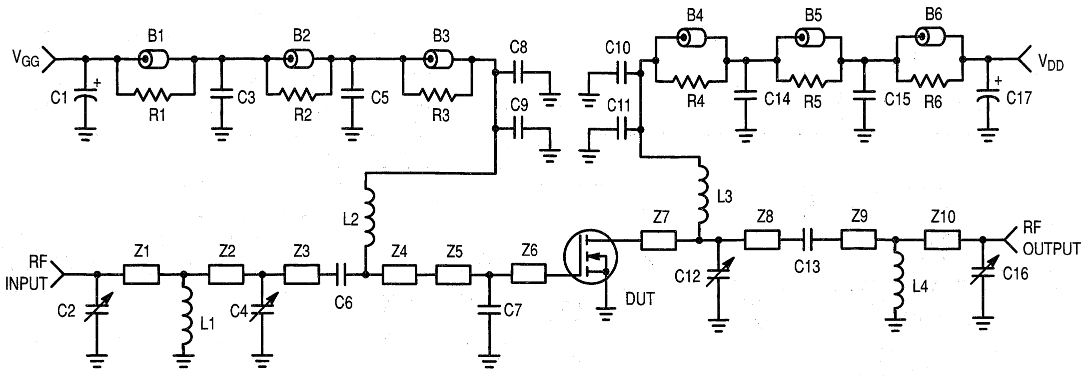
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1.0	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 1

ELECTRICAL CHARACTERISTICS continued (T_C = 25°C unless otherwise noted)

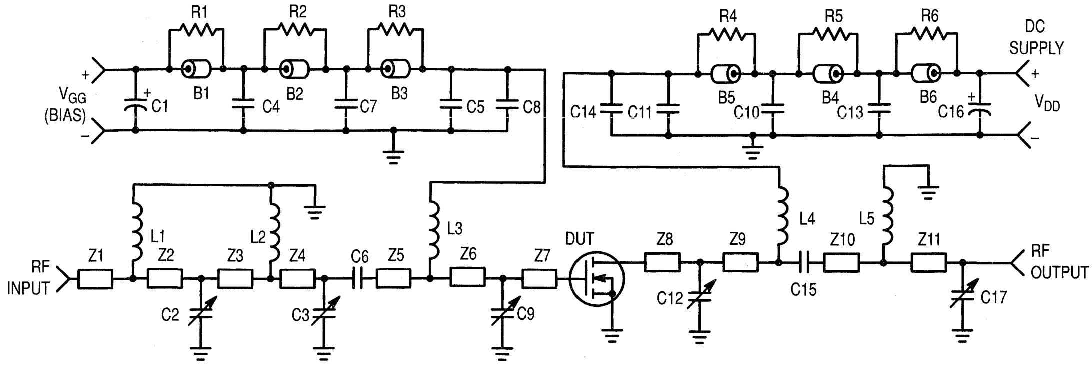
Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 50 μAdc)	$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.5 Adc)	$V_{DS(on)}$	—	0.4	0.6	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 0.5 Adc)	g_{fs}	0.5	0.7	—	S
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 75 mAdc)	$V_{GS(q)}$	3.0	4.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	15	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	8.0	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	0.45	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	G_{ps}	11	12.6	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	η	30	34	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	I_{MD}	—	–32.5	–30	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	I_{RL}	10	14	—	dB
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	G_{ps}	11	12.6	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	η	—	30	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	I_{MD}	—	–32.5	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 10 W (PEP), I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	I_{RL}	10	14	—	dB
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f = 2000.0 MHz)	G_{ps}	11	12.3	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f = 2000.0 MHz)	η	40	45	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz, Load VSWR = 10:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power			



B1, B2, B3, B4, B5, B6	Ferrite Bead, Ferroxcube, 56–590–65–3B	R1, R2, R3, R4, R5, R6	12 Ω, 0.2 W Chip Resistor, Rohm
C1, C17	470 μF, Electrolytic Capacitor, Mallory	Z1	0.155″ x 0.08″ Microstrip
C2, C4, C12	0.6–4.5 pF, Variable Capacitor, Johanson	Z2	0.280″ x 0.08″ Microstrip
C3, C15	0.1 μF, Chip Capacitor, Kemet	Z3	0.855″ x 0.08″ Microstrip
C5, C14	1000 pF, B Case Chip Capacitor, ATC	Z4	0.483″ x 0.08″ Microstrip
C6, C8, C10, C13	12 pF, B Case Chip Capacitor, ATC	Z5	0.200″ x 0.330″ Microstrip
C7	1.8 pF, B Case Chip Capacitor, ATC	Z6	0.220″ x 0.330″ Microstrip
C9, C11	100 pF, B Case Chip Capacitor, ATC	Z7	0.490″ x 0.330″ Microstrip
C16	0.4–2.5 pF, Variable Capacitor, Johanson	Z8	0.510″ x 0.08″ Microstrip
L1	Straight Wire, 21 AWG, 0.3″	Z9	0.990″ x 0.08″ Microstrip
L2	8 Turns, 0.042″ ID, 24 AWG, Enamel	Z10	0.295″ x 0.08″ Microstrip
L3	9 Turns, 0.046″ ID, 26 AWG, Enamel	Board	35 Mils Glass Teflon®, Arlon GX–300, $\varepsilon_r = 2.55$
L4	3 Turns, 0.048″ ID, 25 AWG, Enamel		

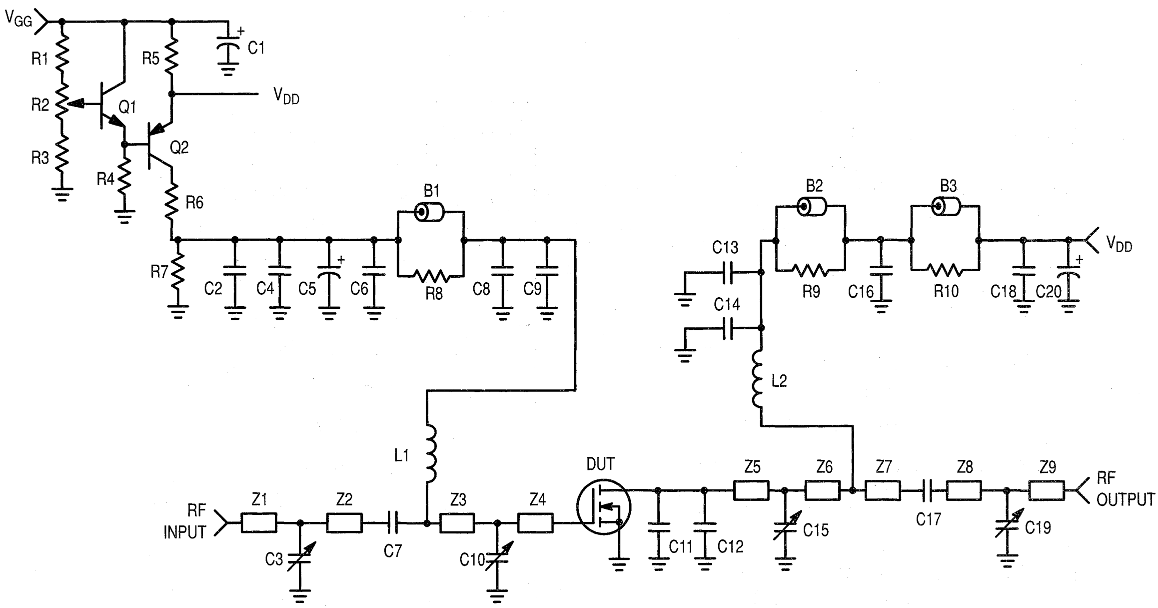
Input/Output Connectors Type N Flange Mount

Figure 1. Schematic of 1.93 – 2.0 GHz Broadband Test Circuit



B1, B2, B3, B4, B5, B6	Ferrite Bead, Fair Rite, (2743021446)	R1, R2, R3, R4, R5, R6	12 Ω, 1/8 W Fixed Film Chip Resistor, 0.08″ x 0.13″
C1, C16	470 µF, 63 V, Electrolytic Capacitor, Mallory	W1, W2	Berrylium Copper, 0.010″ x 0.110″ x 0.210″
C2, C9, C12	0.6–4.5 pF, Variable Capacitor, Johanson Gigatrim	Z1	0.122″ x 0.08″ Microstrip
C3	0.8–4.5 pF, Variable Capacitor, Johanson Gigatrim	Z2	0.650″ x 0.08″ Microstrip
C4, C13	0.1 µF, Chip Capacitor	Z3	0.160″ x 0.08″ Microstrip
C5, C14	100 pF, B Case Chip Capacitor, ATC	Z4	0.030″ x 0.08″ Microstrip
C6, C8, C11, C15	12 pF, B Case Chip Capacitor, ATC	Z5	0.045″ x 0.08″ Microstrip
C7, C10	1000 pF, B Case Chip Capacitor, ATC	Z6	0.291″ x 0.08″ Microstrip
C17	0.1 pF, B Case Chip Capacitor, ATC	Z7	0.483″ x 0.330″ Microstrip
L1	3 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.053″ Long, 6.0 nH	Z8	0.414″ x 0.330″ Microstrip
		Z9	0.392″ x 0.08″ Microstrip
L2	5 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.091″ Long, 15 nH	Z10	0.070″ x 0.08″ Microstrip
		Z11	1.110″ x 0.08″ Microstrip
L3, L4	9 Turns, 26 AWG, 0.080″ OD, 0.046″ ID, 0.170″ Long, 30.8 nH	Board	1 = 0.03 Glass Teflon®, Arlon GX–0300–55–22, 2 oz Copper, 3 x 5″ Dimenson, 0.030″, ε_r = 2.55
L5	4 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.078″ Long, 10 nH		

Figure 2. Schematic of 1.81 – 1.88 GHz Broadband Test Circuit



B1, B2, B3,	Ferrite Bead, Ferroxcube, 56–590–65–3B	R2	1.0 kΩ, 1/2 W Potentiometer
C1, C20	470 µF, 63 V, Electrolytic Capacitor, Mallory	R3	13 kΩ, Axial, 1/4 W Resistor
C2	0.01 µF, B Case Chip Capacitor, ATC	R4, R6, R7	390 Ω, 1/8 W Chip Resistor, Rohm
C3, C10, C15	0.6–4.5 pF, Variable Capacitor, Johanson	R5	1.0 Ω, 10 W 1% Resistor, DALE
C4, C16	0.02 µF, B Case Chip Capacitor, ATC	R8, R9, R10	12 Ω, 1/8 W Chip Resistor, Rohm
C5	100 µF, 50 V, Electrolytic Capacitor, Sprague	Z1	0.624″ x 0.08″ Microstrip
C6, C7, C9, C14, C17	12 pF, B Case Chip Capacitor, ATC	Z2	0.725″ x 0.08″ Microstrip
		Z3	0.455″ x 0.08″ Microstrip
C8, C13	51 pF, B Case Chip Capacitor, ATC	Z4	0.530″ x 0.330″ Microstrip
C11, C12	0.3 pF, B Case Chip Capacitor, ATC	Z5	0.280″ x 0.330″ Microstrip
C18	0.1 µF, Chip Capacitor, Kemet	Z6	0.212″ x 0.330″ Microstrip
C19	0.4–2.5 pF, Variable Capacitor, Johanson	Z7	0.408″ x 0.08″ Microstrip
L1	8 Turns, 0.042″ ID, 24 AWG, Enamel	Z8	0.990″ x 0.08″ Microstrip
L2	9 Turns, 0.046″ ID, 26 AWG, Enamel	Z9	0.295″ x 0.08″ Microstrip
Q1	NPN, 15 W, Bipolar Transistor, MJD310	Board	35 Mils Glass Teflon®, Arlon GX–0300, $\varepsilon_r = 2.55$
Q2	PNP, 15 W, Bipolar Transistor, MJD320	Input/Output	Type N Flange Mount RF55–22, Connectors, Omni Spectra
R1	200 Ω, Axial, 1/4 W Resistor		

Figure 3. Schematic of Class A Test Circuit

TYPICAL CHARACTERISTICS

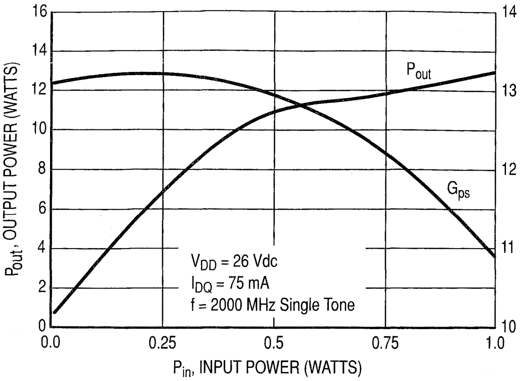


Figure 4. Output Power & Power Gain versus Input Power

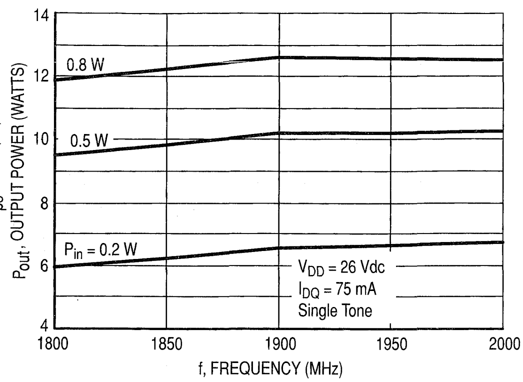


Figure 5. Output Power versus Frequency

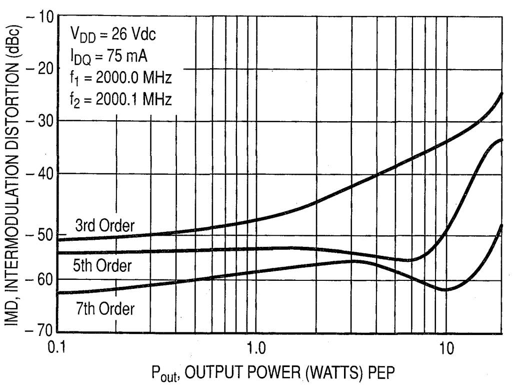


Figure 6. Intermodulation Distortion versus Output Power

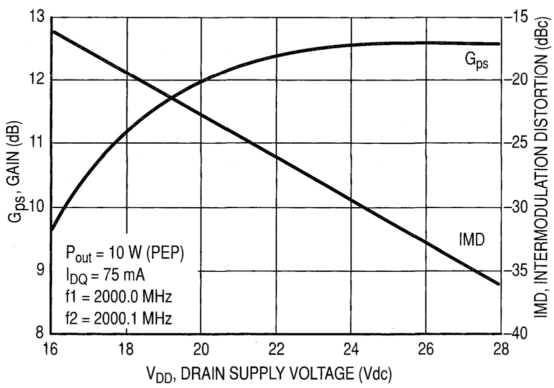


Figure 7. Power Gain and Intermodulation Distortion versus Supply Voltage

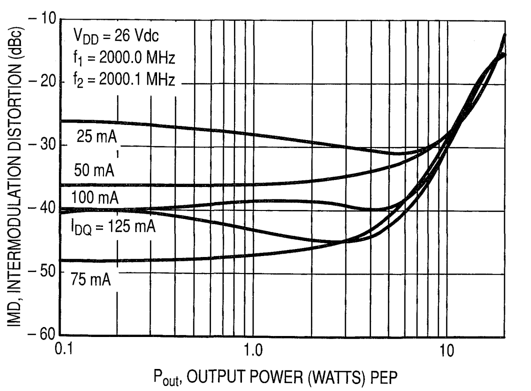


Figure 8. Intermodulation Distortion versus Output Power

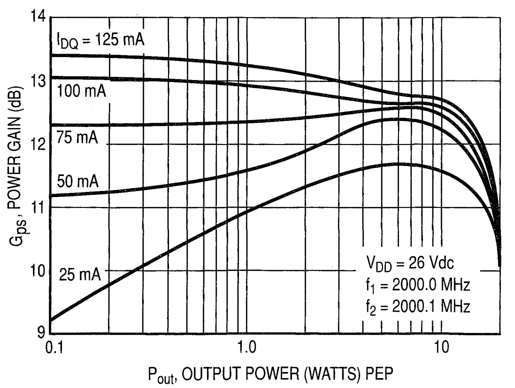


Figure 9. Power Gain versus Output Power

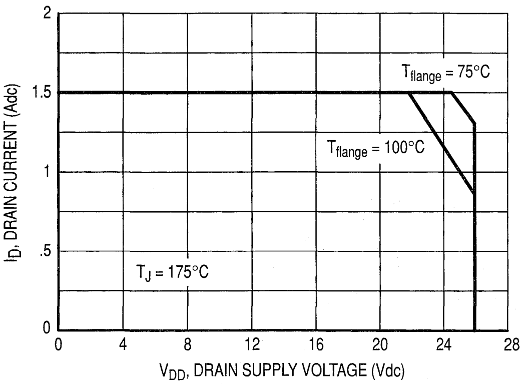


Figure 10. Class A DC Safe Operating Area

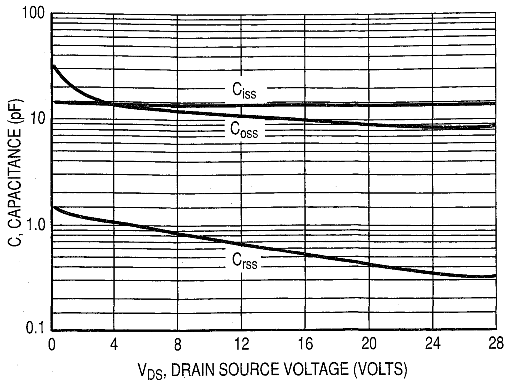


Figure 11. Capacitance versus Drain Source Voltage

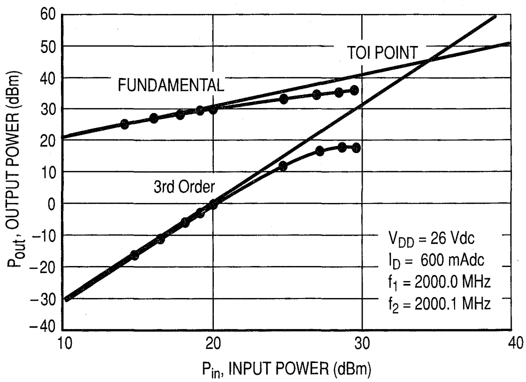


Figure 12. Class A Third Order Intercept Point

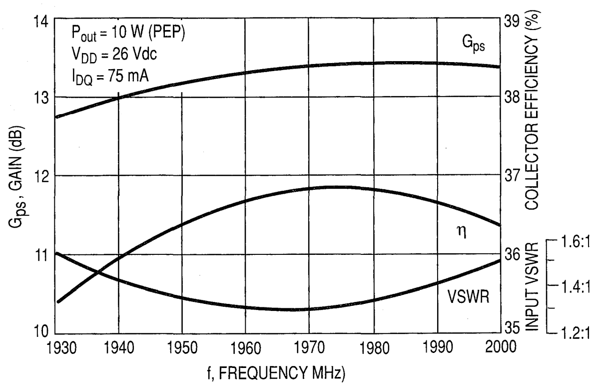
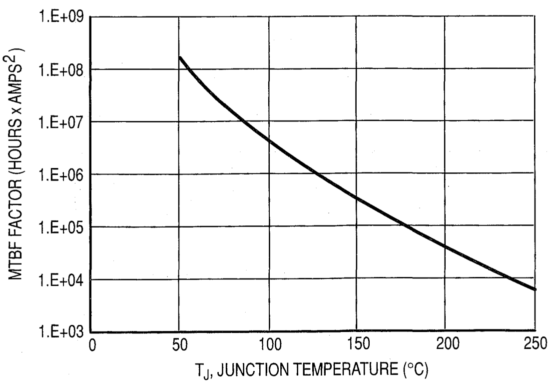
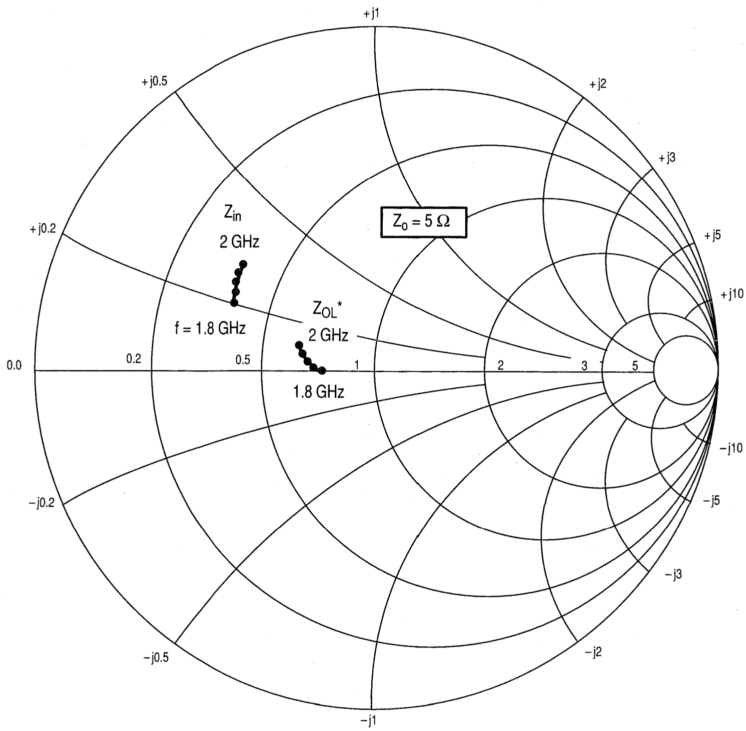


Figure 13. Performance in Broadband Circuit



This graph displays calculated MTBF in hours x ampere^2 drain current. Life tests at elevated temperature have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 14. MTBF Factor versus Junction Temperature



V_{CC} = 26 V, I_{CQ} = 75 mA, P_{out} = 10 W (PEP)

f MHz	Z_{in}(1) Ω	Z_{OL}* Ω
1800	2.1 + j1.0	3.8 − j0.15
1860	2.05 + j1.15	3.77 − j0.13
1900	2.0 + j1.2	3.75 − j0.1
1960	1.9 + j1.4	3.65 + j0.1
2000	1.85 + j1.6	3.55 + j0.2

Z_{in}(1) = Conjugate of fixture gate terminal impedance.

Z_{OL}* = Conjugate of the optimum load impedance at given output power, voltage, IMD, bias current and frequency.

Figure 15. Series Equivalent Input and Output Impedence

Table 1. Common Source S–Parameters at V_{DS} = 24 Vdc, I_D = 600 mAdc

f GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
0.1	0.916	-81	33.41	128	0.016	41	0.498	-60
0.2	0.850	-118	20.81	101	0.020	16	0.499	-88
0.3	0.843	-135	14.45	84	0.020	2	0.532	-106
0.4	0.848	-144	10.61	73	0.019	-7	0.552	-117
0.5	0.861	-151	8.34	63	0.017	-15	0.609	-125
0.6	0.872	-154	6.61	55	0.015	-19	0.647	-132
0.7	0.882	-158	5.43	47	0.013	-23	0.675	-139
0.8	0.895	-160	4.54	41	0.011	-24	0.728	-145
0.9	0.901	-163	3.82	34	0.009	-24	0.740	-150
1.0	0.902	-164	3.27	29	0.008	-18	0.773	-160
1.1	0.909	-166	2.83	24	0.006	-6	0.794	-164
1.2	0.917	-168	2.48	19	0.006	10	0.813	-168
1.3	0.923	-169	2.18	14	0.006	14	0.826	-172
1.4	0.931	-171	1.94	10	0.006	15	0.842	-176
1.5	0.933	-172	1.73	6	0.005	43	0.853	-179
1.6	0.934	-174	1.55	2	0.007	60	0.859	177
1.7	0.937	-175	1.40	-1	0.009	60	0.869	174
1.8	0.938	-176	1.27	-4	0.010	63	0.869	171
1.9	0.942	-177	1.16	-7	0.011	71	0.874	169
2.0	0.943	-178	1.06	-10	0.014	73	0.876	166
2.1	0.946	-178	0.98	-12	0.016	71	0.884	163
2.2	0.950	-179	0.92	-15	0.019	67	0.897	160
2.3	0.953	-180	0.86	-18	0.019	63	0.903	157
2.4	0.954	179	0.80	-21	0.020	62	0.907	154
2.5	0.955	178	0.76	-24	0.020	65	0.907	151
2.6	0.961	177	0.71	-26	0.024	69	0.912	149

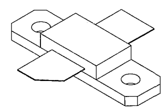
MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Advance Information

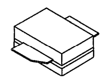
The RF Sub–Micron MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF284
MRF284S

30 W, 2000 MHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 360B–01, STYLE 1
(MRF284)



CASE 360C–03, STYLE 1
(MRF284S)

Designed for PCN and PCS base station applications at frequencies from 1000 to 2600 MHz. Suitable for FM, TDMA, CDMA, and multicarrier amplifier applications. To be used in class A and class AB for PCN–PCS/cellular radio and wireless local loop.

- Specified Two–Tone Performance @ 2000 MHz, 26 Volts
  Output Power = 30 Watts (PEP)
  Power Gain = 10 dB
  Efficiency = 30%
  Intermodulation Distortion = –30 dBc
- Typical Single–Tone Performance at 2000 MHz, 26 Volts
  Output Power = 30 Watts (CW)
  Power Gain = 9 dB
  Efficiency = 45%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 30 Watts (CW) Output Power
- Gold Metallization for Improved Reliability

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	87.5 0.5	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1.0	μAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	10	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 150 μAdc)	$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 200 mAdc)	$V_{GS(q)}$	3.0	4.0	5.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	—	0.3	0.6	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1.0 Adc)	g_{fs}	1.0	1.5	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	37	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	23	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	1.2	—	pF
FUNCTIONAL TESTS (in Motorola Test Fixture)					
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	G_{ps}	9	10.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	η	30	33	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	I_{MD}	—	–33	–29	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W, I_{DQ} = 200 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	I_{RL}	9	24	—	dB
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	G_{ps}	9	10.7	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	η	—	33	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	I_{MD}	—	–33	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 200 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	I_{RL}	9	15	—	dB
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 200 mA, f1 = 2000.0 MHz)	G_{ps}	8.5	10.7	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 200 mA, f1 = 2000.0 MHz)	η	35	—	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 200 mA, f1 = 2000.0 MHz, VSWR = 10:1, at All Phase Angles)	Ψ	No Degradation In Output Power			

TYPICAL CHARACTERISTICS

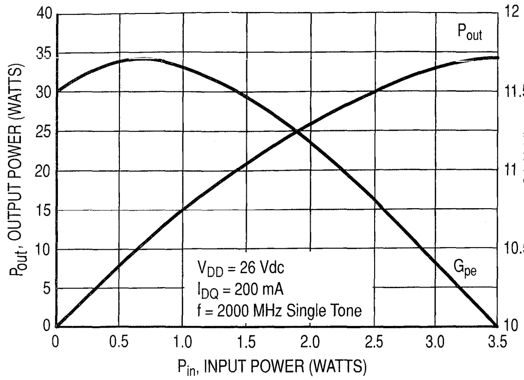


Figure 1. Output Power & Power Gain versus Input Power

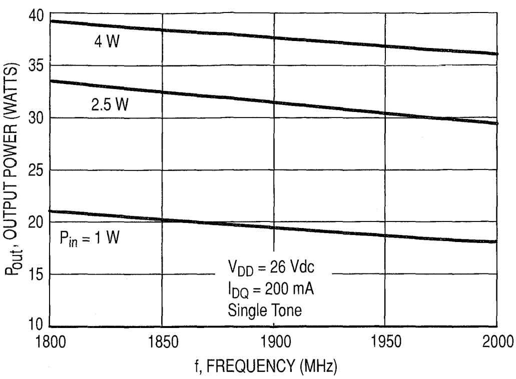


Figure 2. Output Power versus Frequency

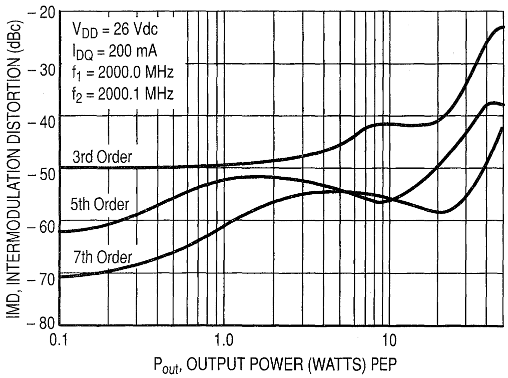


Figure 3. Intermodulation Distortion versus Output Power

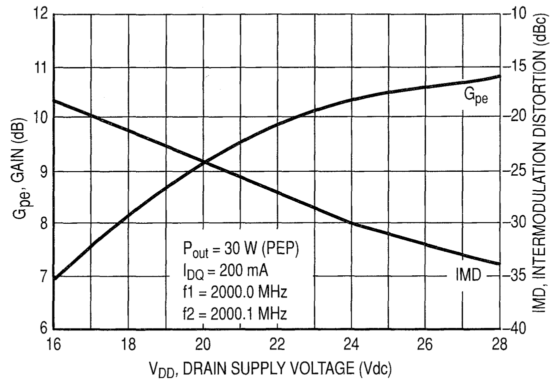


Figure 4. Power Gain and Intermodulation Distortion versus Supply Voltage

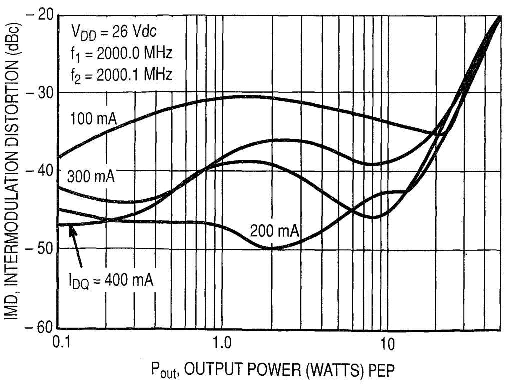


Figure 5. Intermodulation Distortion versus Output Power

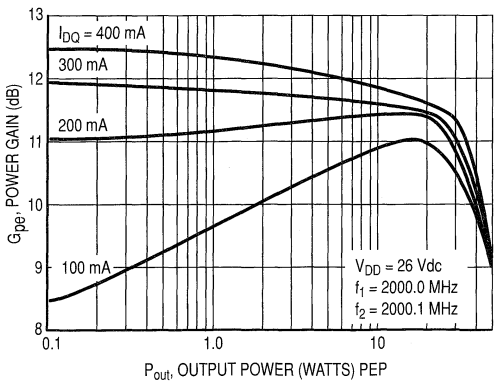


Figure 6. Power Gain versus Output Power

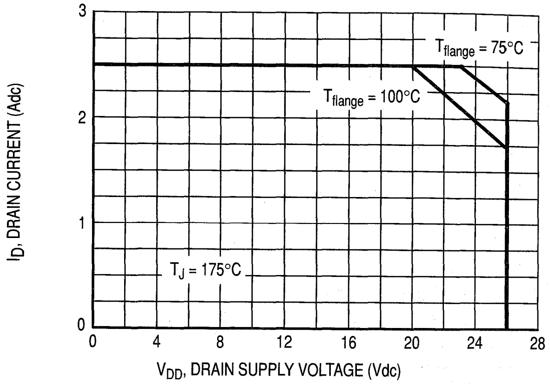


Figure 7. DC Safe Operating Area

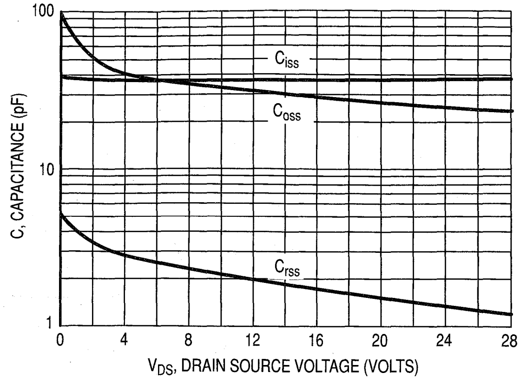


Figure 8. Capacitance versus Drain Source Voltage

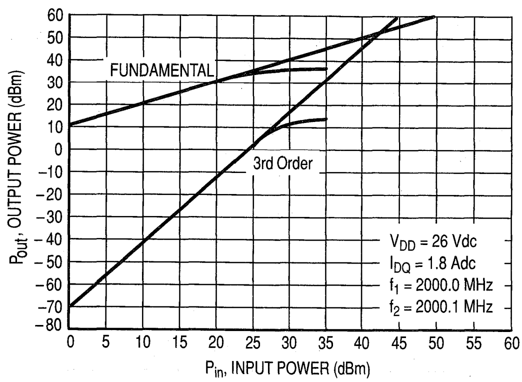
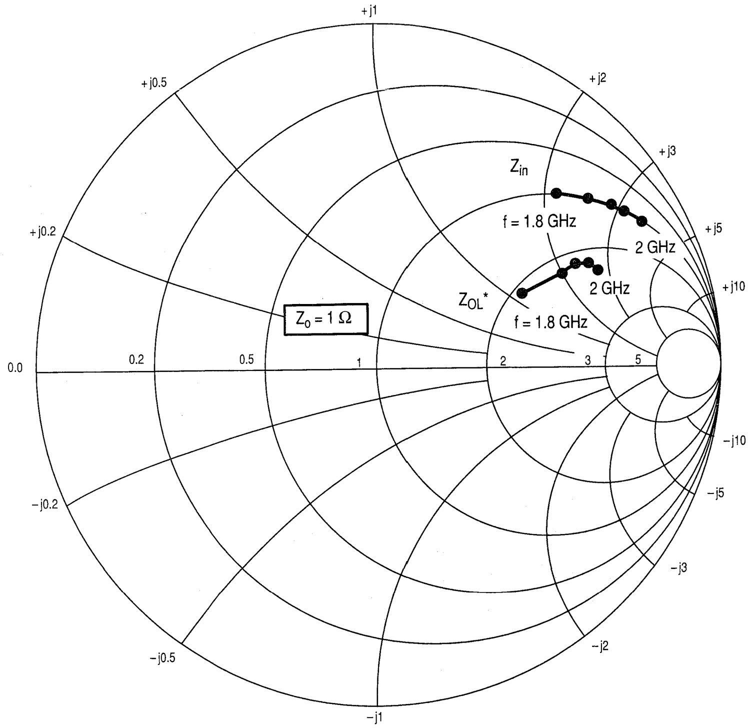


Figure 9. Class A Third Order Intercept Point



V_{CC} = 26 V, I_{CQ} = 200 mA, P_{out} = 15 W_{avg}

f MHz	Z_{in}(1) Ω	Z_{OL}* Ω
1800	1.0 + j2.2	2.1 + j1.4
1860	1.0 + j2.6	2.2 + j2.0
1900	1.0 + j2.9	2.3 + j2.3
1960	1.0 + j3.2	2.5 + j2.7
2000	1.0 + j3.7	2.6 + j2.72

Z_{in}(1) = Conjugate of fixture base terminal impedance.

Z_{OL}* = Conjugate of the optimum load impedance at given output power, voltage, bias current and frequency.

Figure 10. Series Equivalent Input and Output Impedence

Table 1. Common Source S–Parameters at V_{DS} = 26 Vdc, I_D = 1.8 Adc

f GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1.0	0.902	–170	1.10	28	0.005	60	0.913	–162
1.1	0.934	–167	0.92	26	0.006	82	0.921	–163
1.2	0.948	–167	0.85	24	0.007	89	0.924	–164
1.3	0.957	–169	0.73	21	0.009	94	0.929	–165
1.4	0.959	–169	0.68	19	0.011	94	0.931	–165
1.5	0.960	–170	0.59	17	0.014	94	0.933	–167
1.6	0.958	–172	0.53	14	0.015	92	0.936	–168
1.7	0.958	–172	0.50	13	0.016	93	0.936	–169
1.8	0.956	–174	0.45	10	0.019	92	0.937	–170
1.9	0.954	–175	0.43	8	0.020	90	0.937	–171
2	0.944	–177	0.39	6	0.023	82	0.937	–173
2.1	0.934	–177	0.38	4	0.023	72	0.935	–174
2.2	0.935	–178	0.35	–1	0.013	72	0.932	–176
2.3	0.945	180	0.31	–4	0.016	116	0.925	–179
2.4	0.944	178	0.30	–5	0.023	112	0.930	–179
2.5	0.946	177	0.29	–7	0.024	105	0.935	179
2.6	0.941	174	0.25	–11	0.025	112	0.930	176

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

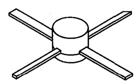
The RF Line
NPN Silicon High-Frequency Transistor

MRF313

1.0 W, 400 MHz
HIGH–FREQUENCY
TRANSISTOR
NPN SILICON

. . . designed for wideband amplifier, driver or oscillator applications in military, mobile, and aircraft radio.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 1.0 Watt
  Power Gain = 15 dB Min
  Efficiency = 45% Typ
- Emitter Ballast and Low Current Density for Improved MTBF
- Common Emitter for Improved Stability



CASE 305A–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	40	Vdc
Emitter–Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	150	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	6.1 35	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	28.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

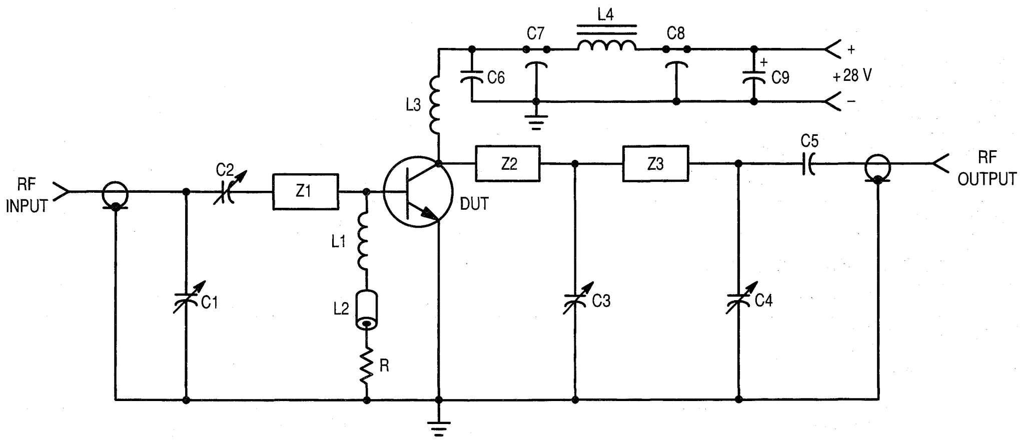
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	35	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	35	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	I_{CEO}	—	—	1.0	mAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	60	150	—
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 20 Vdc, f = 200 MHz)	f_T	—	2.5	—	GHz
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.5	5.0	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (1) (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	G_{pe}	15	16	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	η	—	45	—	%
Series Equivalent Input Impedance (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	Z_{in}	—	6.4 – j4.8	—	Ohms
Series Equivalent Output Impedance (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	Z_{out}	—	75 – j45	—	Ohms

NOTE:
1. Class C



C1, C2, C4 — 1.0–20 pF JOHANSON 9063
C3 — 1.0–10 pF JOHANSON
C5 — 150 pF Chip
C6 — 0.1 µF
C7, C8 — 680 pF Feedthru
C9 — 1.0 µF TANTALUM

L1, L3 — 5 Turns, AWG #20, 1/4″ I.D.
L2 — Ferrite Bead, FERROXCUBE No. 56–590–65/4B
L4 — FERROXCUBE VK200–20/4B
Input/Output Connectors — Type N
Board — Glass Teflon, ε = 2.56, t = 0.062″

R — 4.7 Ohms, 1/4 W
Z1 — 2.0″ x 0.1″ MICROSTRIP LINE
Z2, Z3 — 2.6″ x 0.1″ MICROSTRIP LINE

Figure 1. 400 MHz Power Gain Test Circuit

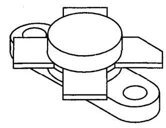
The RF Line
NPN Silicon RF Power Transistors

MRF314

. . . designed primarily for wideband large–signal driver and output amplifier stages in the 30–200 MHz frequency range.

- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 30 Watts
  Minimum Gain = 10 dB
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications

**30 W, 30–200 MHz
RF POWER
TRANSISTORS
NPN SILICON**



CASE 211–07, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	35	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.4	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	82 0.47	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.13	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 30 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 30 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 30 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 3.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	3.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	80	—

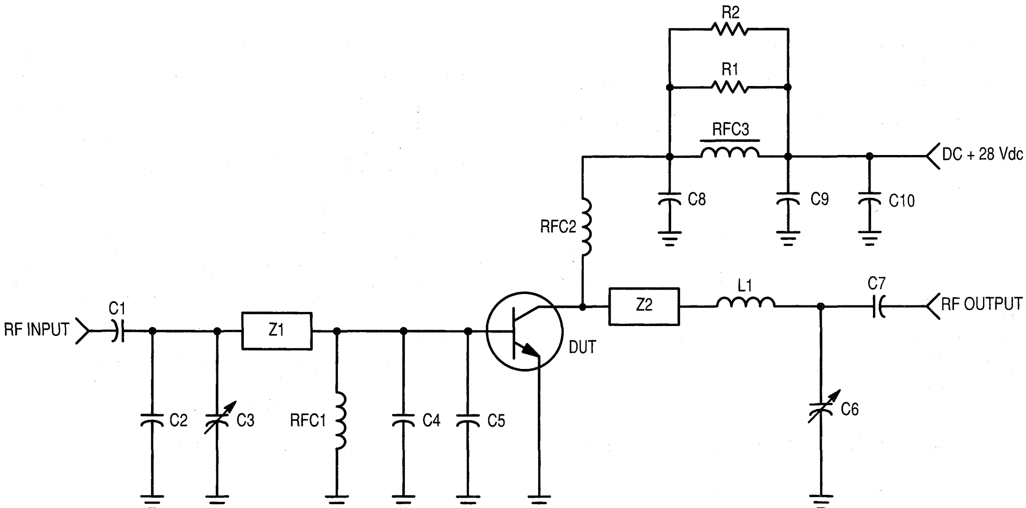
NOTE:

(continued)

1. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	30	40	pF
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 150 MHz)	G_{PE}	10	13.5	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 150 MHz)	η	50	—	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, VSWR = 30:1 all phase angles)	ψ	No Degradation in Power Output			



C1, C7 — 18 pF, 100 mil ATC
C2 — 68 pF, 100 mil ATC
C3, C6 — Johanson #JMC 5501
C4 — 270 pF, 100 mil ATC
C5 — 240 pF, 100 mil ATC
C8, C9 — 100 pF Underwood
C10 — 1.0 µF Tantalum
L1 — 2 Turns, 2.5″ #20 Wire, ID = 0.275″

R1, R2 — 10 Ω, 1.0 W
RFC1 — 15 µH Molded Coil
RFC2 — 2 Turns, 2.5″ #20 Wire, ID = 0.2″
RFC3 — Ferroxcube VK200–19/4B
Z1 — Microstrip, 0.168″ W x 1.6″ L
Z2 — Microstrip, 0.168″ W x 1.2″ L
Board — Glass Teflon ε_r = 2.55

Figure 1. 150 MHz Test Circuit

TYPICAL PERFORMANCE CURVES

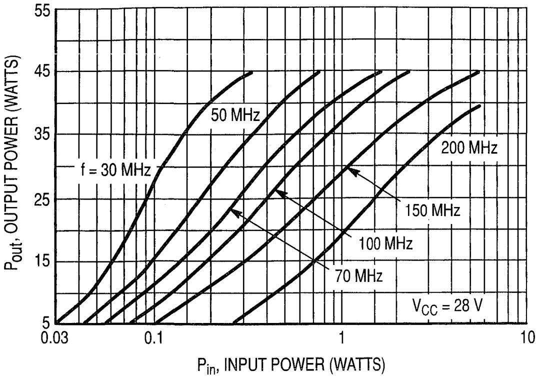


Figure 2. Output Power versus Input Power

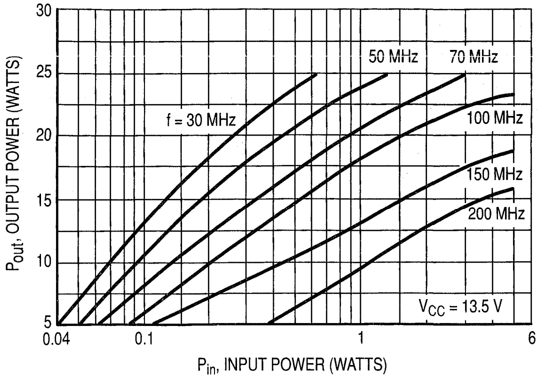


Figure 3. Output Power versus Input Power

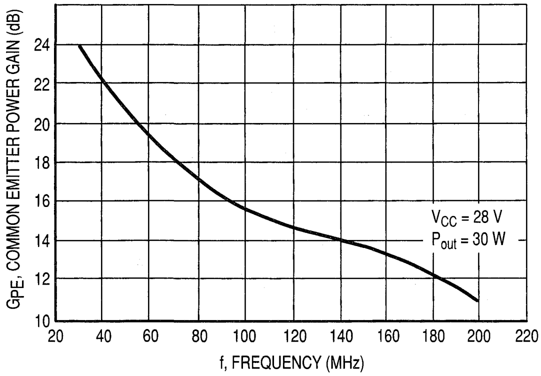


Figure 4. Power Gain versus Frequency

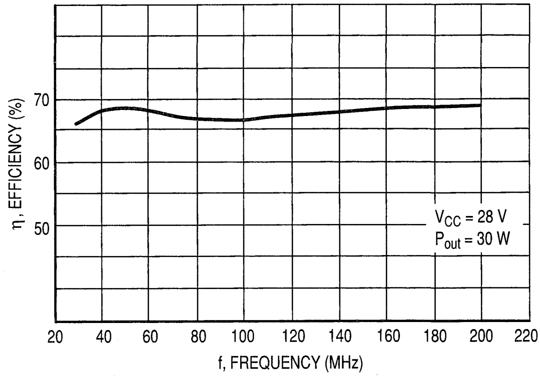
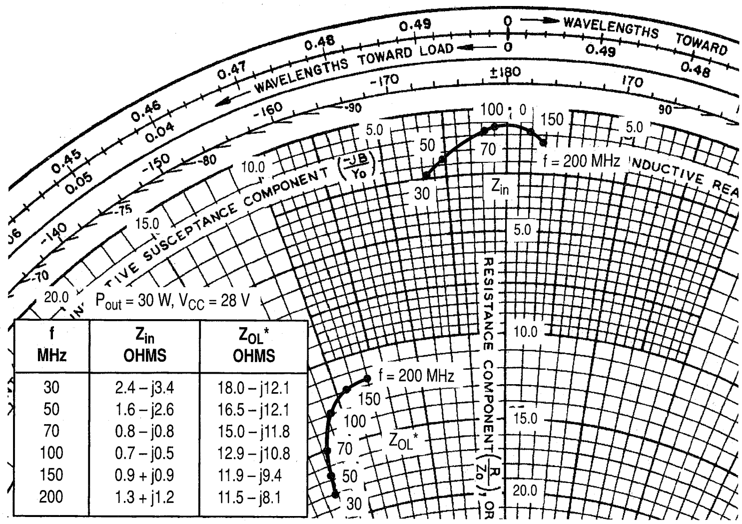


Figure 5. Efficiency versus Frequency



f MHz	Z_{in} OHMS	Z_{OL}* OHMS
30	2.4 – j3.4	18.0 – j12.1
50	1.6 – j2.6	16.5 – j12.1
70	0.8 – j0.8	15.0 – j11.8
100	0.7 – j0.5	12.9 – j10.8
150	0.9 + j0.9	11.9 – j9.4
200	1.3 + j1.2	11.5 – j8.1

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Input/Output Impedance

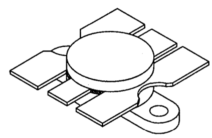
The RF Line
NPN Silicon RF Power Transistor

. . . designed primarily for wideband large–signal output amplifier stages in the 30–200 MHz frequency range.

- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 80 Watts
  Minimum Gain = 10 dB
- Built–In Matching Network for Broadband Operation
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications

MRF316

**80 W, 3.0–200 MHz
CONTROLLED "Q"
BROADBAND RF POWER
TRANSISTOR
NPN SILICON**



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	35	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous Peak	I_C	9.0 13.5	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	220 1.26	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	100	130	pF

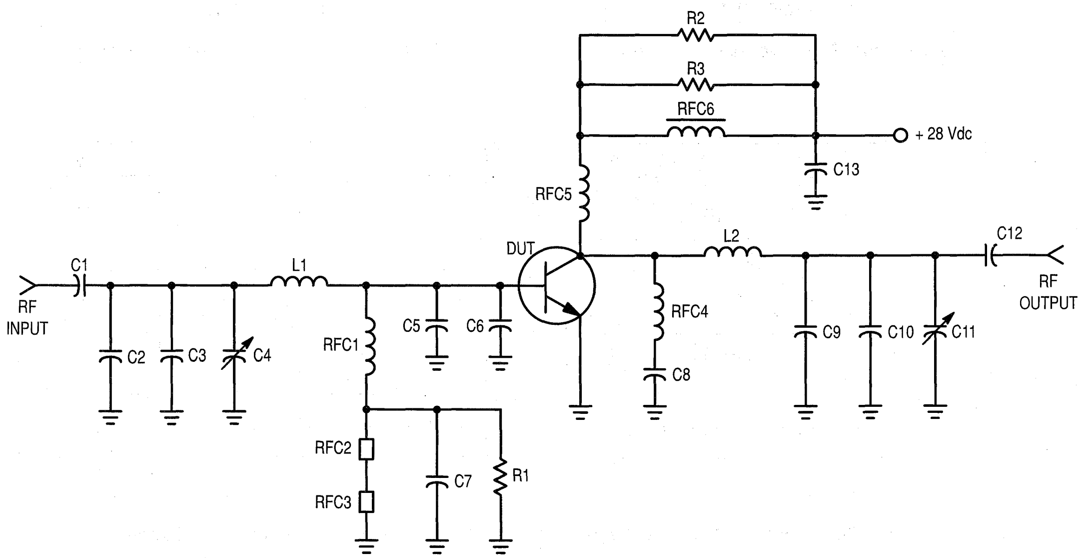
NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
NARROW BAND FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 150 MHz)	G_{PE}	10	13	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 150 MHz)	η	55	—	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 80 W CW, f = 150 MHz, VSWR = 30:1 all phase angles)	ψ	No Degradation in Output Power			



C1 — 22 pF 100 mil ATC
C2, C3 — 24 pF 100 mil ATC
C4, C11 — 0.8–20 pF JMC #5501 Johanson
C5 — 200 pF 100 mil ATC
C6 — 240 pF 100 mil ATC
C7 — Dipped Mica 1000 pF
C8 — 0.1 µF Erie Red Cap
C9, C10, C12 — 30 pF 100 mil ATC
C13 — 1.0 µF Tantalum

L1 — 0.8″, #20 Wire
L2 — 1.0″, #20 Wire
RFC1, RFC4 — 0.15 µH Molded Coil
RFC2, RFC3 — Ferroxcube Bead 56–590–65–3B
RFC5 — 2.5″, #20 Wire, 1.5 Turns
RFC6 — Ferroxcube VK200–19/4B
R1 — 10 Ω, 1/2 W
R2, R3 — 10 Ω, 1.0 W

Figure 1. 150 MHz Test Amplifier

TYPICAL PERFORMANCE CURVES

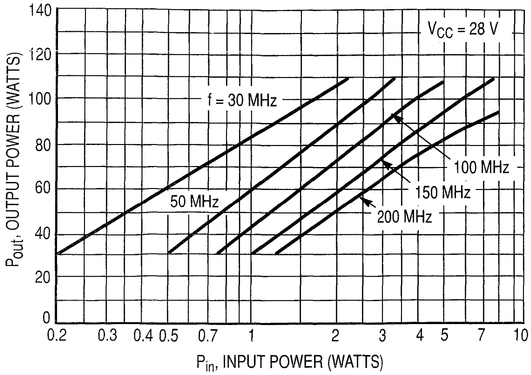


Figure 2. Output Power versus Input Power

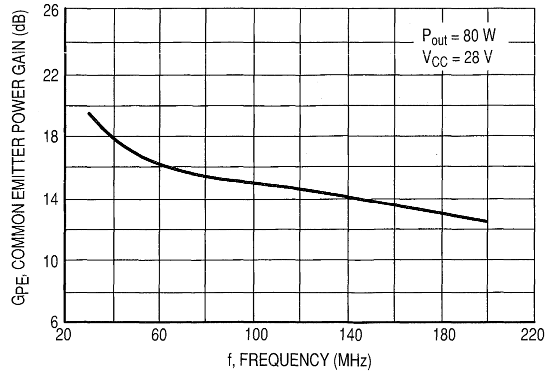


Figure 3. Power Gain versus Frequency

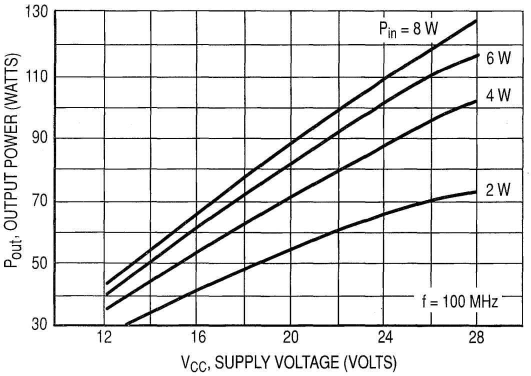


Figure 4. Output Power versus Supply Voltage

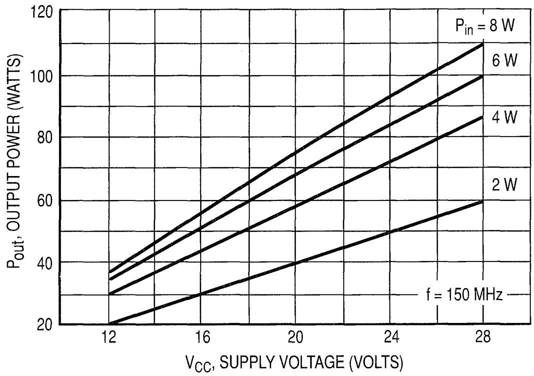


Figure 5. Output Power versus Supply Voltage

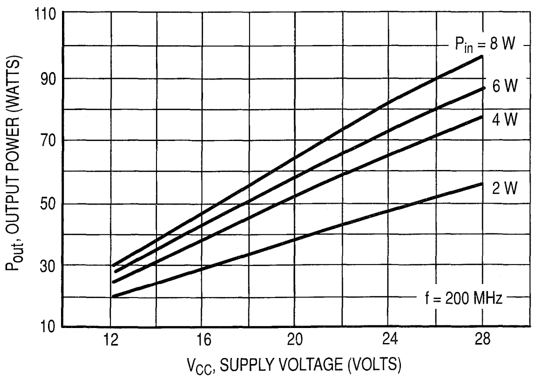
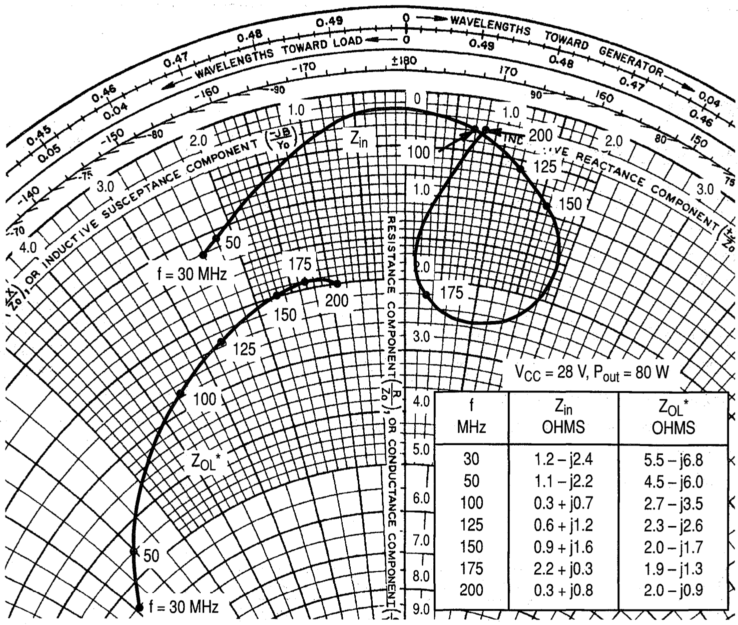


Figure 6. Output Power versus Supply Voltage



V_{CC} = 28 V, P_{out} = 80 W

f MHz	Z_{in} OHMS	Z_{OL}* OHMS
30	1.2 – j2.4	5.5 – j6.8
50	1.1 – j2.2	4.5 – j6.0
100	0.3 + j0.7	2.7 – j3.5
125	0.6 + j1.2	2.3 – j2.6
150	0.9 + j1.6	2.0 – j1.7
175	2.2 + j0.3	1.9 – j1.3
200	0.3 + j0.8	2.0 – j0.9

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 7. Series Equivalent Input–Output Impedance

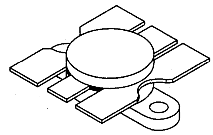
The RF Line
NPN Silicon RF Power Transistor

MRF317

. . . designed primarily for wideband large–signal output amplifier stages in 30–200 MHz frequency range.

- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 100 W
  Minimum Gain = 9.0 dB
- Built–In Matching Network for Broadband Operation
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability
- High Output Saturation Power — Ideally Suited for 30 W Carrier/120 W Peak AM Amplifier Service
- Guaranteed Performance in Broadband Test Fixture

**100 W, 30–200 MHz
CONTROLLED Q
BROADBAND RF POWER
TRANSISTOR
NPN SILICON**



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	35	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak (10 seconds)	I_C	12 18	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	25	80	—

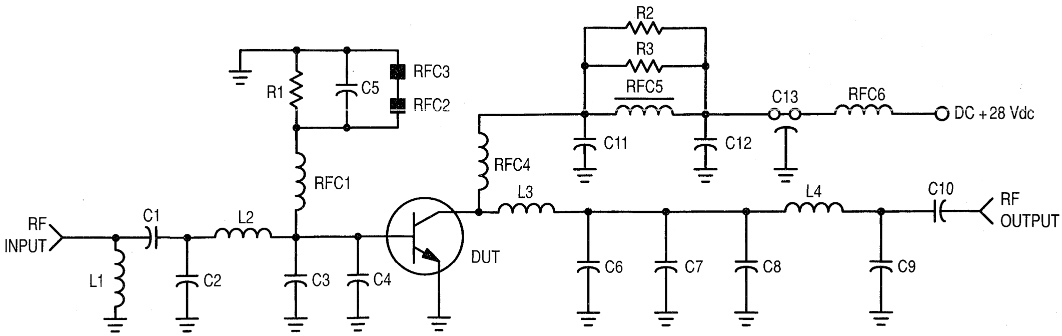
NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	150	175	pF
FUNCTIONAL TESTS (Figure 2)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 150 MHz, I_C (Max) = 6.5 Adc)	G_{PE}	9.0	10	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 150 MHz, I_C (Max) = 6.5 Adc)	η	55	60	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 100 W CW, f = 150 MHz, VSWR = 30:1 all phase angles)	ψ	No Degradation in Output Power			



C1, C9 — 39 pF, 100 mil ATC
C2 — 120 pF, 100 mil ATC
C3, C4 — 360 pF, 100 mil ATC
C5 — 1000 pF Dipped Mica
C6, C7 — 100 pF, 100 mil ATC*
C8 — 18 pF, 100 mil ATC*
C10 — 43 pF, 100 mil ATC

C11 — 60 pF, Underwood
C12 — 0.1 µF Erie Redcap
C13 — 1000 pF, Underwood J102
L1 — 50 nH
L2 — 6.0 nH
L3 — 8.0 nH
L4 — 32 nH

RFC1 — 0.15 µH Molded Coil
RFC2, RFC3 — Ferroxcube Bead 56–590–65/3B
RFC4 — 1 Turn, #18 Wire, 2.0″ L
RFC5 — Ferroxcube VK200 19/4B
RFC6 — 7 Turns, #18 Wire, 0.3″ ID
R1 — 10 Ω 1/2 W
R2, R3 — 10 Ω 1.0 W
*Combination of C6, C7, C8 equals 220 pF.

Figure 1. 110–160 MHz Broadband Amplifier — Test Fixture Schematic

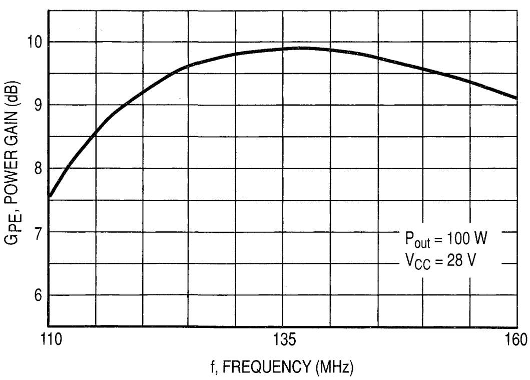


Figure 2. Power Gain versus Frequency Broadband Test Fixture

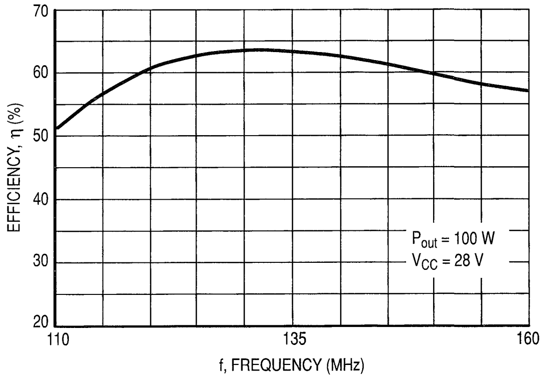


Figure 3. Efficiency versus Frequency Broadband Test Fixture

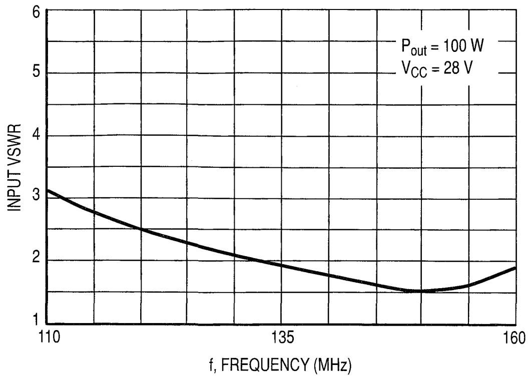


Figure 4. Input VSWR versus Frequency Broadband Test Fixture

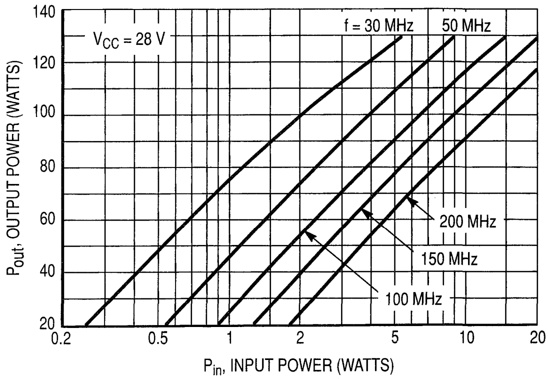


Figure 5. Output Power versus Input Power

TYPICAL PERFORMANCE CURVES

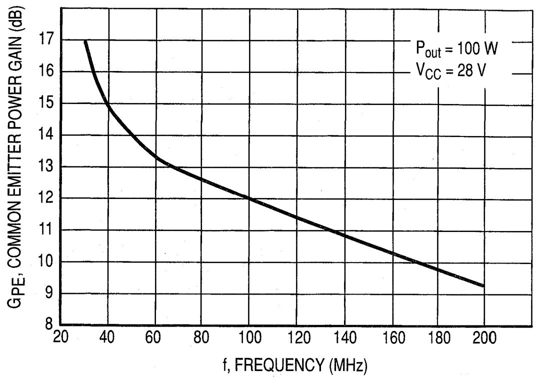


Figure 6. Power Gain versus Frequency

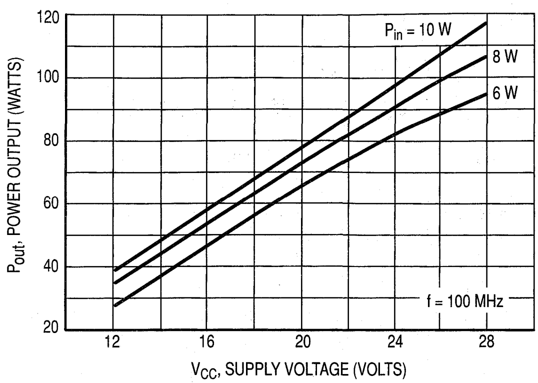


Figure 7. Power Output versus Supply Voltage

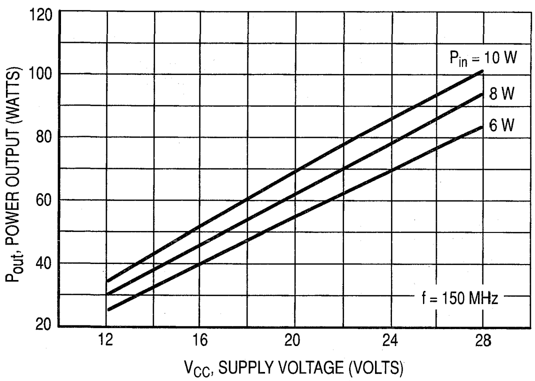


Figure 8. Power Output versus Supply Voltage

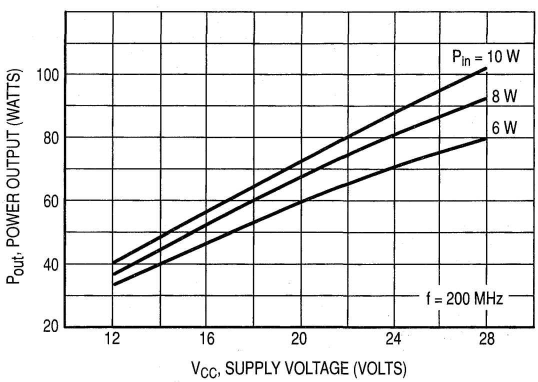
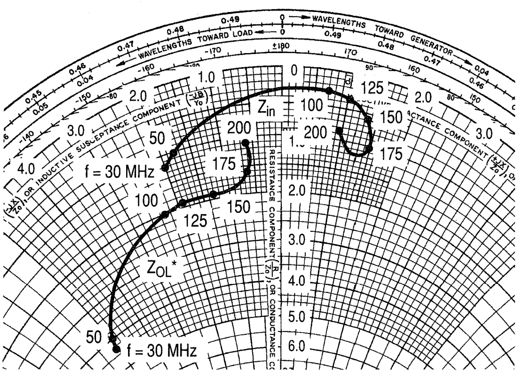


Figure 9. Power Output versus Supply Voltage



V_{CC} = 28 V, P_{out} = 100 W

f MHz	Z_{in} OHMS	Z_{OL}* OHMS
30	1.2 – j2.0	4.3 – j5.0
50	1.0 – j1.8	4.0 – j4.9
100	0.3 + j0.7	2.0 – j2.3
125	0.3 + j1.0	1.9 – j1.9
150	0.6 + j1.3	1.9 – j1.3
175	1.0 + j1.5	1.6 – j0.6
200	0.9 + j1.0	1.1 – j0.6

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 10. Series Equivalent Input–Output Impedance

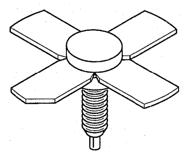
The RF Line
NPN Silicon RF Power Transistor

MRF321

10 W, 400 MHz RF POWER TRANSISTOR NPN SILICON

. . . designed primarily for wideband large–signal driver and predriver amplifier stages in 200–500 MHz frequency range.

- Guaranteed Performance at 400 MHz, 28 Vdc
  Output Power = 10 Watts
  Power Gain = 12 dB Min
  Efficiency = 50% Min
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability
- Computer–Controlled Wirebonding Gives Consistent Input Impedance



CASE 244–04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	33	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	1.1 1.5	Adc
Total Device Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	27 160	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

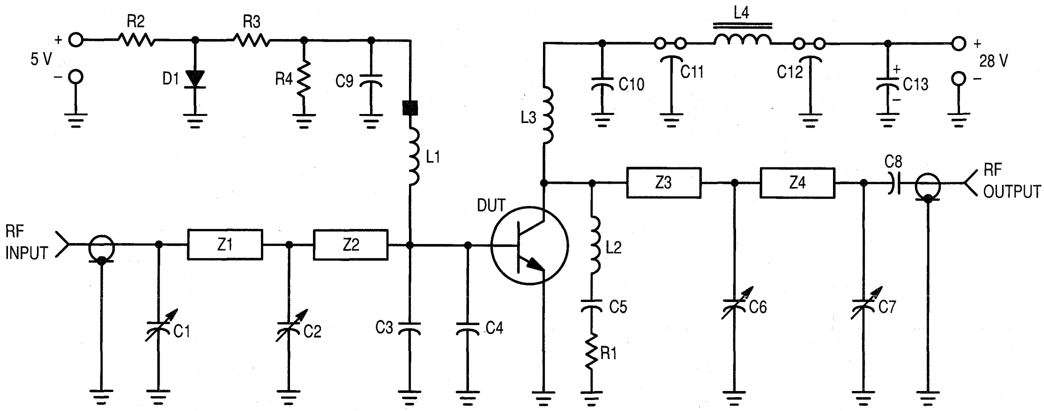
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mA, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	80	—

NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	10	12	pF
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 10 W, f = 400 MHz)	G_{PE}	12	13	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 10 W, f = 400 MHz)	η	50	60	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 10 W, f = 400 MHz, VSWR = 30:1 all phase angles)	ψ	No Degradation in Output Power			



C1, C2, C3 — 1.0–20 pF Johanson Trimmer (JMC 5501)
C3, C4 — 47 pF ATC Chip Capacitor
C5, C10 — 0.1 µF Erie Redcap
C7 — 0.5–10 pF Johanson Trimmer (JMC 5201)
C8 — 0.018 µF Vitramon Chip Capacitor
C9 — 200 pF UNELCO Capacitor
C11, C12 — 680 pF Feedthru
C13 — 1.0 µF, 50 Volt Tantalum Capacitor
D1 — 1N4001
L1 — 0.33 µH Molded Choke with Ferroxcube Bead (Ferroxcube 56–590–65/4B) on Ground End of Coil
L2 — 4 Turns #20 Enamel, 1/8″ ID
L3 — 6 Turns #20 Enamel, 1/4″ ID
L4 — Ferroxcube VK200–19/4B
R1 — 5.1 Ω, 1/4 Watt
R2 — 120 Ω, 1.0 Watt
R3 — 20 Ω, 1/2 Watt
R4 — 47 Ω, 1/2 Watt
Z1 — Microstrip 0.1″ W x 1.35″ L
Z2 — Microstrip 0.1″ W x 0.55″ L
Z3 — Microstrip 0.1″ W x 0.8″ L
Z4 — Microstrip 0.1″ W x 1.75″ L
Board — Glass Teflon, ε_R = 2.56, t = 0.062″
Input/Output Connectors — Type N

Figure 1. 400 MHz Test Circuit Schematic

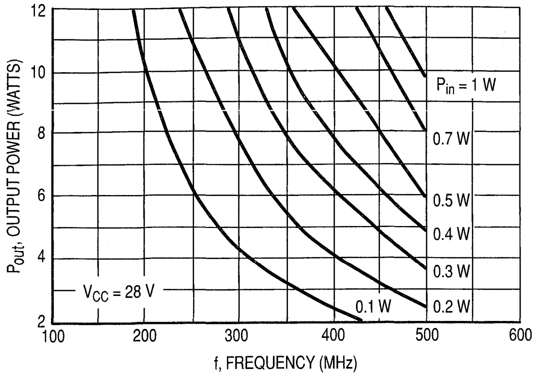


Figure 2. Output Power versus Frequency

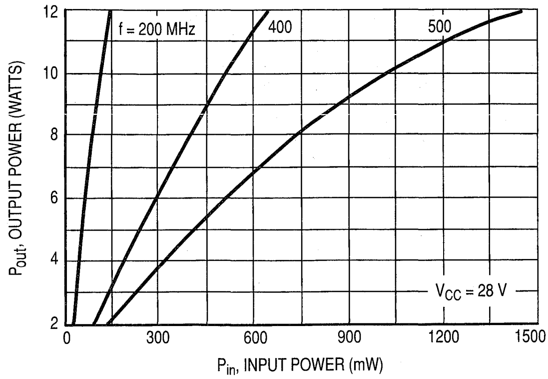


Figure 3. Output Power versus Input Power

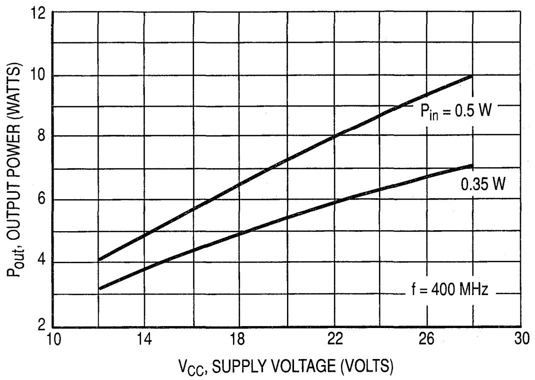


Figure 4. Output Power versus Supply Voltage

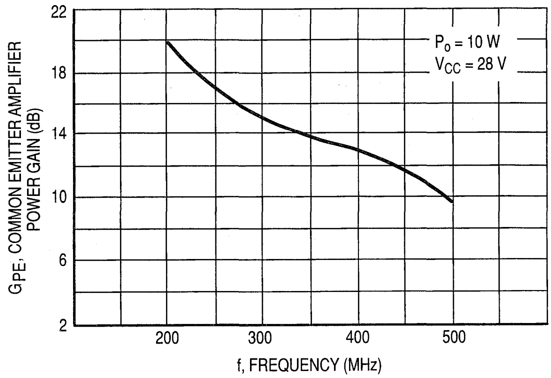
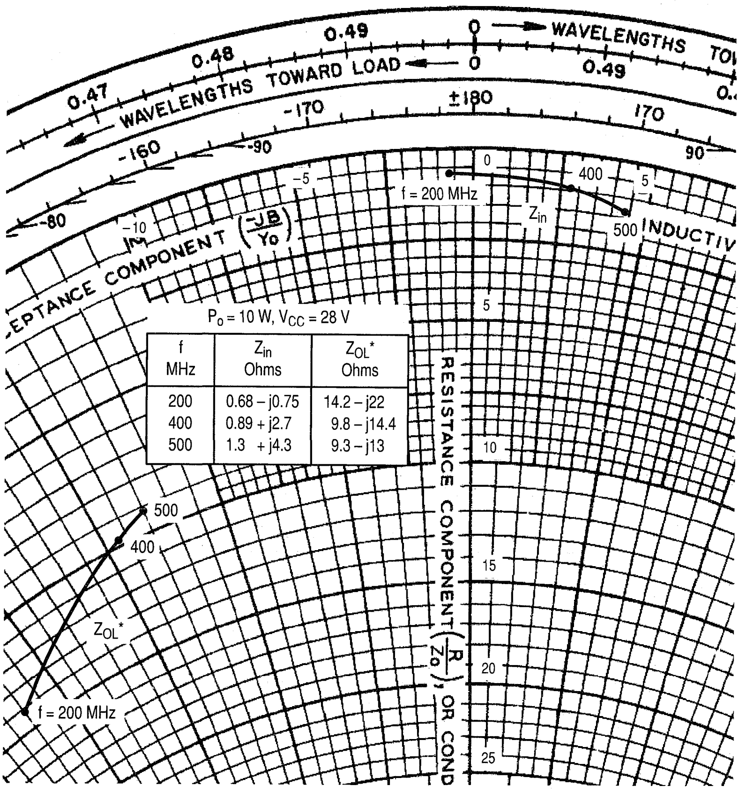


Figure 5. Power Gain versus Frequency



P_o = 10 W, V_{CC} = 28 V

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
200	0.68 – j0.75	14.2 – j22
400	0.89 + j2.7	9.8 – j14.4
500	1.3 + j4.3	9.3 – j13

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Impedance

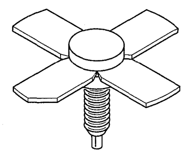
The RF Line
NPN Silicon RF Power Transistor

MRF323

. . . designed primarily for wideband large–signal driver and predriver amplifier stages in the 200–500 MHz frequency range.

- Guaranteed Performance at 400 MHz, 28 V
  Output Power = 20 Watts
  Power Gain = 10 dB Min
  Efficiency = 50% Min
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability
- Computer–Controlled Wirebonding Gives Consistent Input Impedance

20 W, 400 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 244–04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	33	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	2.2 3.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	55 310	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

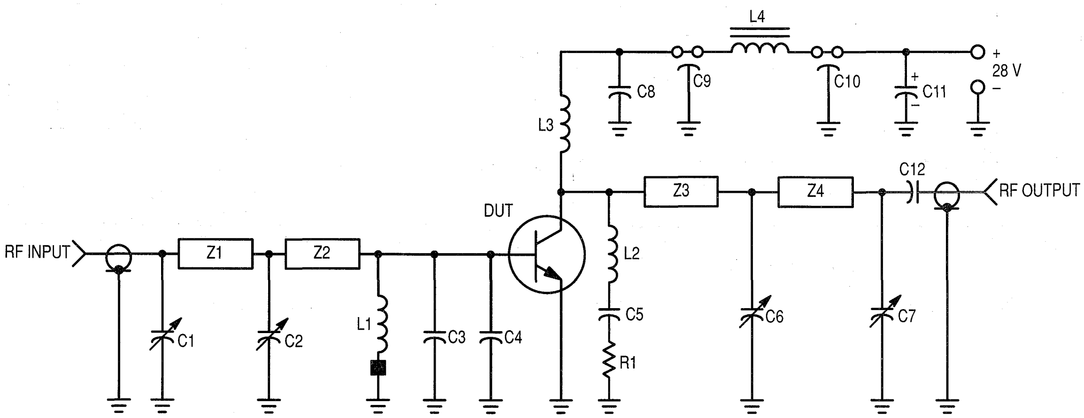
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	80	—

NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	20	24	pF
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 20 W, f = 400 MHz)	G_{PE}	10	11	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 20 W, f = 400 MHz)	η	50	60	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 20 W, f = 400 MHz, VSWR = 30:1 all phase angles)	ψ	No Degradation in Output Power			



C1, C2, C6 — 1.0–20 pF Johanson Trimmer (JMC 5501)
C3, C4 — 47 pF ATC Chip Capacitor
C5, C8 — 0.1 µF Erie Redcap
C7 — 0.5–10 pF Johanson Trimmer (JMC 5201)
C9, C10 — 680 pF Feedthru
C11 — 1.0 µF 50 Volt Tantalum
C12 — 0.018 µF Vitramon Chip Capacitor
L1 — 0.33 µH Molded Choke with Ferroxcube Bead (Ferroxcube 56–590–65/4B) on Ground End

L2 — 6 Turns #20 Enamel, 1/4″ ID, Closewound
L3 — 4 Turns #20 Enamel, 1/8″ ID, Closewound
L4 — Ferroxcube VK200–19/4B
R1 — 5.1 Ω 1/4 Watt
Z1 — Microstrip 0.1″ W x 1.35″ L
Z2 — Microstrip 0.1″ W x 0.55″ L
Z3 — Microstrip 0.1″ W x 0.8″ L
Z4 — Microstrip 0.1″ W x 1.75″ L
Board — Glass Teflon ε_r = 2.56, t = 0.062″
Input/Output Connectors — Type N

Figure 1. 400 MHz Test Circuit Schematic

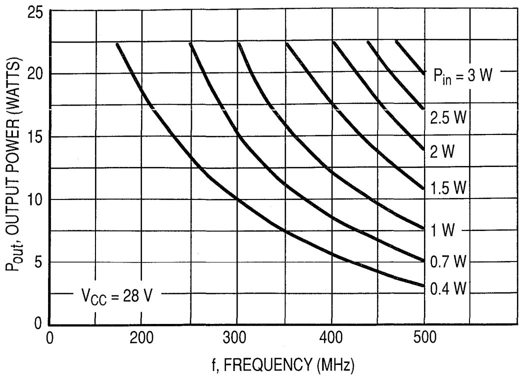


Figure 2. Output Power versus Frequency

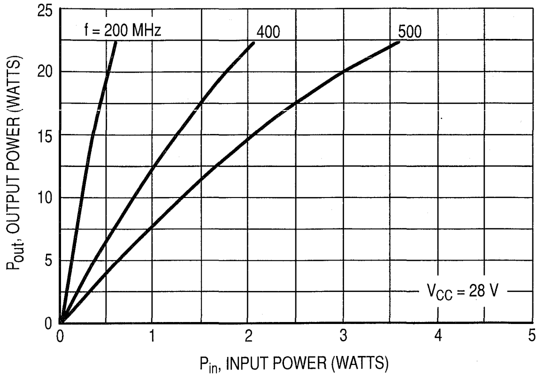


Figure 3. Output Power versus Input Power

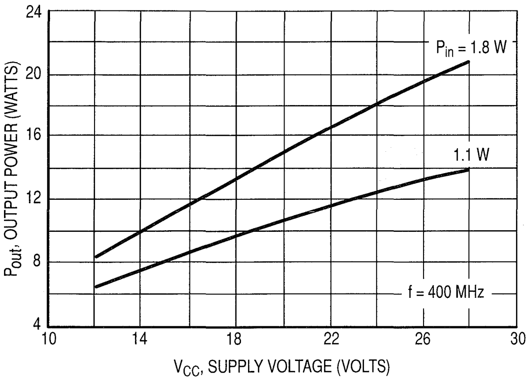


Figure 4. Output Power versus Supply Voltage

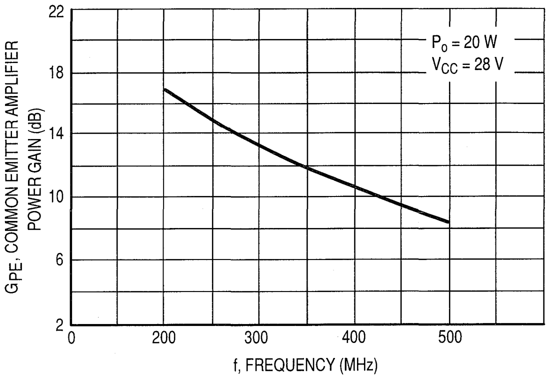
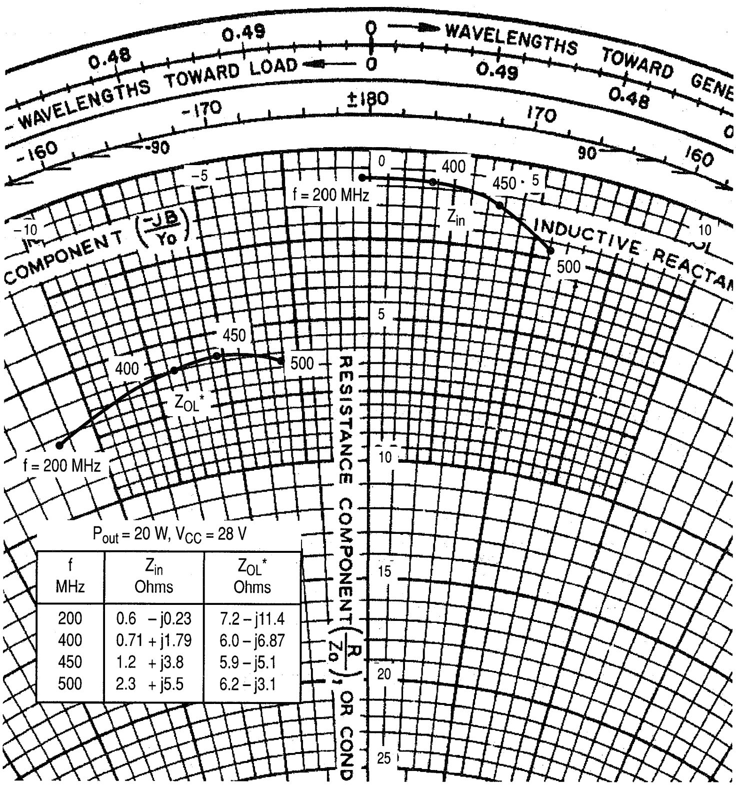


Figure 5. Power Gain versus Frequency



P_{out} = 20 W, V_{CC} = 28 V

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
200	0.6 − j0.23	7.2 − j11.4
400	0.71 + j1.79	6.0 − j6.87
450	1.2 + j3.8	5.9 − j5.1
500	2.3 + j5.5	6.2 − j3.1

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Impedance

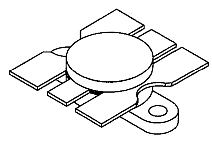
The RF Line
NPN Silicon RF Power Transistor

MRF325

. . . designed primarily for wideband large–signal output and driver amplifier stages in 100 to 500 MHz frequency range.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 30 Watts
  Minimum Gain = 8.5 dB
  Efficiency = 54% (Min)
- Built–In Matching Network for Broadband Operation Using Internal Matching Techniques
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization for High Reliability Applications

30 W, 225 to 400 MHz CONTROLLED "Q" BROADBAND RF POWER TRANSISTOR NPN SILICON



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	33	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	3.4 4.5	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	82 0.47	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.13	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

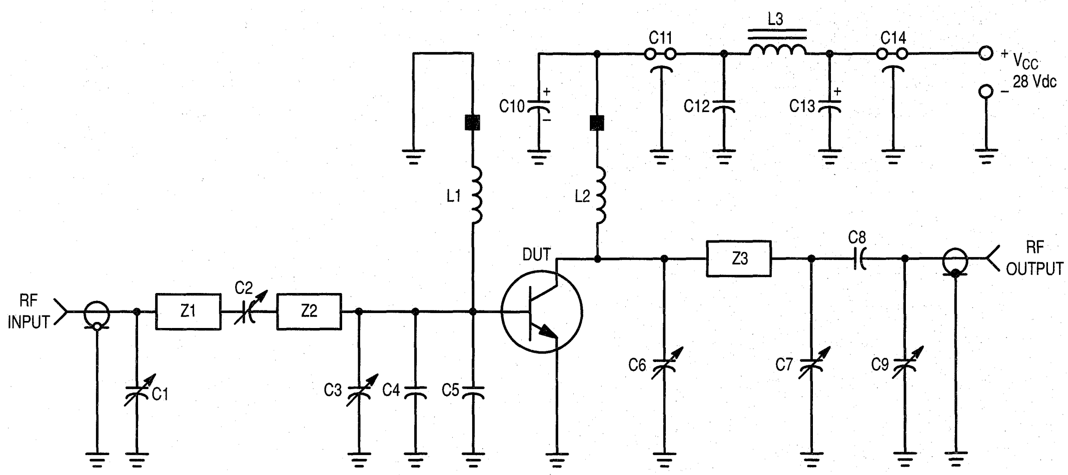
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 30 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 30 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 3.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 30 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	3.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	80	—

NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	30	40	pF
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 400 MHz)	G_{PE}	8.5	9.5	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 400 MHz)	η	50	60	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 400 MHz, VSWR = 30:1 all angles)	ψ	No Degradation in Output Power			



C1, C9 — 1.0–10 pF Johanson Capacitor (JMC 5201)
C2, C3, C6, C7 — 1.0–20 pF Johanson Capacitor (JMC 5501)
C4, C5 — 36 pF ATC 100–mil Chip Capacitor
C8 — 100 pF UNELCO
C10, C13 — 1.0 μF 50 V Tantalum
C11, C14 — 680 pF Feedthru
C12 — 0.1 μF Erie Redcap
L1 — 8 Turns #26 AWG Enameled, 1/16″ ID Closewound with Ferroxcube Bead (#56–590–65/4B) on Ground End
L2 — 14 Turns, #22 AWG Enameled, Closewound on a 470 Ω, 2.0 Watt Resistor with Ferroxcube Bead (#56–590–65/4B) on Cold End of L2
L3 — Ferroxcube VK200–19/4B Ferrite Choke
Z1 — Microstrip 0.19″ W x 0.88″ L
Z2 — Microstrip 0.28″ W x 1.0″ L
Z3 — Microstrip 0.31″ W x 1.25″ L
Board — Glass Teflon ε_r = 2.56, t = 0.062″
Input/Output Connectors — Type N

DUT Socket Lead Frame Etched from 80–mil–Thick Copper

Figure 1. 400 MHz Test Circuit

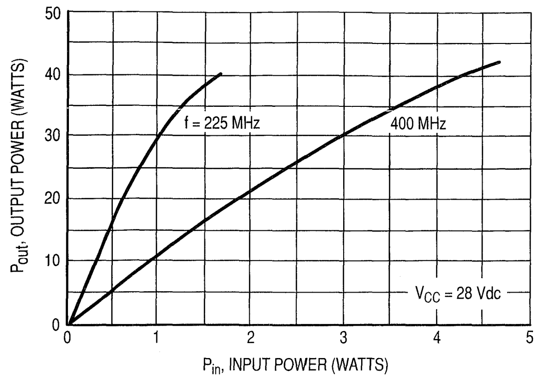


Figure 2. Output Power versus Input Power

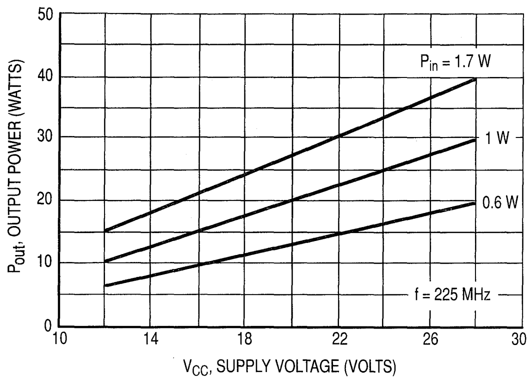


Figure 3. Output Power versus Supply Voltage

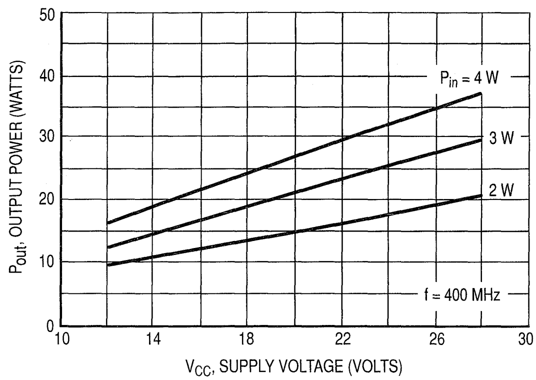
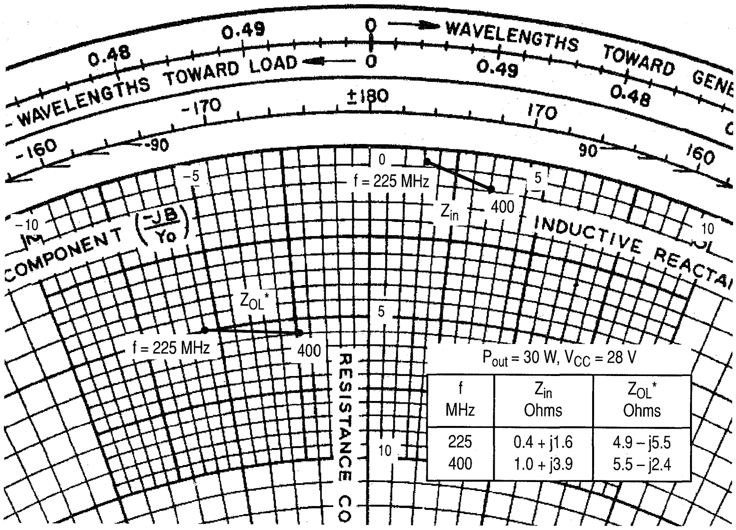


Figure 4. Output Power versus Supply Voltage



P_{out} = 30 W, V_{CC} = 28 V		
f MHz	Z_{in} Ohms	Z_{OL}* Ohms
225	0.4 + j1.6	4.9 – j5.5
400	1.0 + j3.9	5.5 – j2.4

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 5. Series Equivalent Impedance

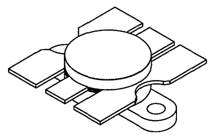
The RF Line
NPN Silicon RF Power Transistor

MRF326

. . . designed primarily for wideband large–signal output amplifier stages in the 100 to 500 MHz frequency range.

- Guaranteed Performance @ 400 MHz, 28 Vdc
  Output Power = 40 Watts
  Minimum Gain = 9.0 dB
- Built–In Matching Network for Broadband Operation
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications

40 W, 225 to 400 MHz CONTROLLED "Q" BROADBAND RF POWER TRANSISTOR NPN SILICON



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	33	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	4.5 6.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	110 0.63	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.6	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

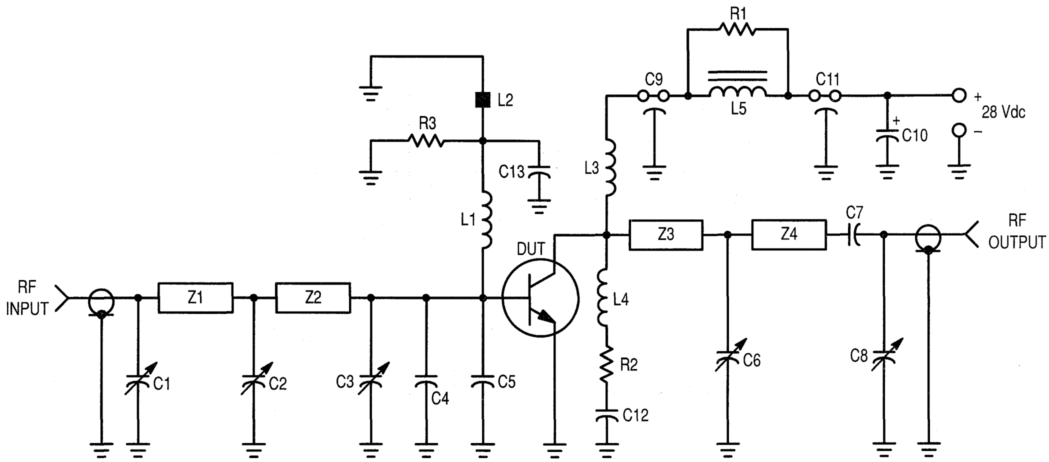
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 40 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 40 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 4.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 40 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	4.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	50	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	45	60	pF

NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 40 W, f = 400 MHz, I_C Max = 2.85 Adc)	G_{PE}	9.0	11	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 40 W, f = 400 MHz, I_C Max = 2.85 Adc)	η	50	—	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 40 W CW, f = 400 MHz, VSWR = 30:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 1.0–10 pF Johanson, Capacitor (JMC 5201)
C2, C3, C6, C8 — 1.0–20 pF Johanson Capacitor
C4, C5 — 36 pF ATC "B" Style Chip Capacitor
C7, C9, C13 — 100 pF UNELCO Capacitor
C11 — 680 pF Feedthru
C10 — 1.0 μF 50 V Tantalum
C12 — 0.1 μF Erie Redcap
L1 — 8 Turns #26 AWG Enameled, 1/16″ ID Closewound
L2, L5 — Ferroxcube VK200–19/4B Ferrite Choke
L3 — 8 Turns #20 AWG Enameled, 1/4″ ID Closewound
L4 — 4 Turns #26 AWG 0.1″ ID
R1 — 10 Ohm 2.0 W Carbon
R2, R3 — 10 Ohm 1.0 W Carbon
Z1 — Microstrip 0.19″ W x 1.28″ L
Z2 — Microstrip 0.28″ W x 1.0″ L
Z3 — Microstrip 0.31″ W x 1.0″ L
Z4 — Microstrip 0.31″ W x 0.9″ L
Board — Glass Teflon ε_r = 2.56 t = 0.062″
Input/Output Connectors — Type N UG58 A/U

Figure 1. 400 MHz Test Amplifier

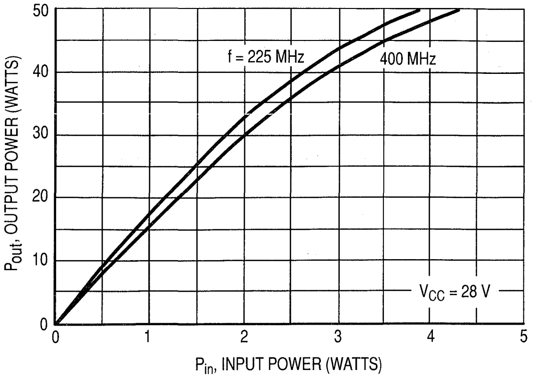


Figure 2. Output Power versus Input Power

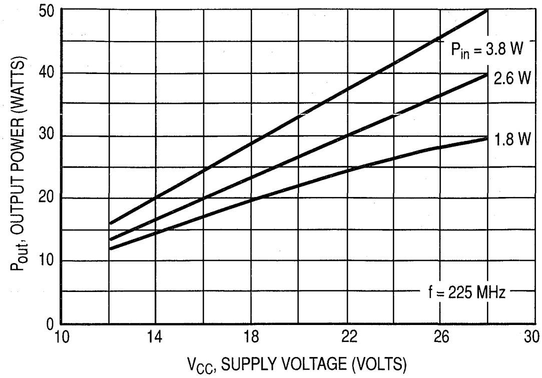


Figure 3. Output Power versus Supply Voltage

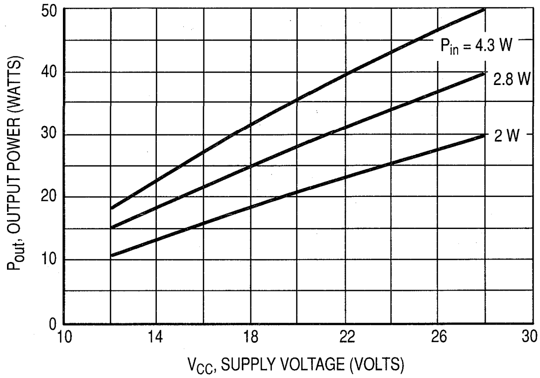
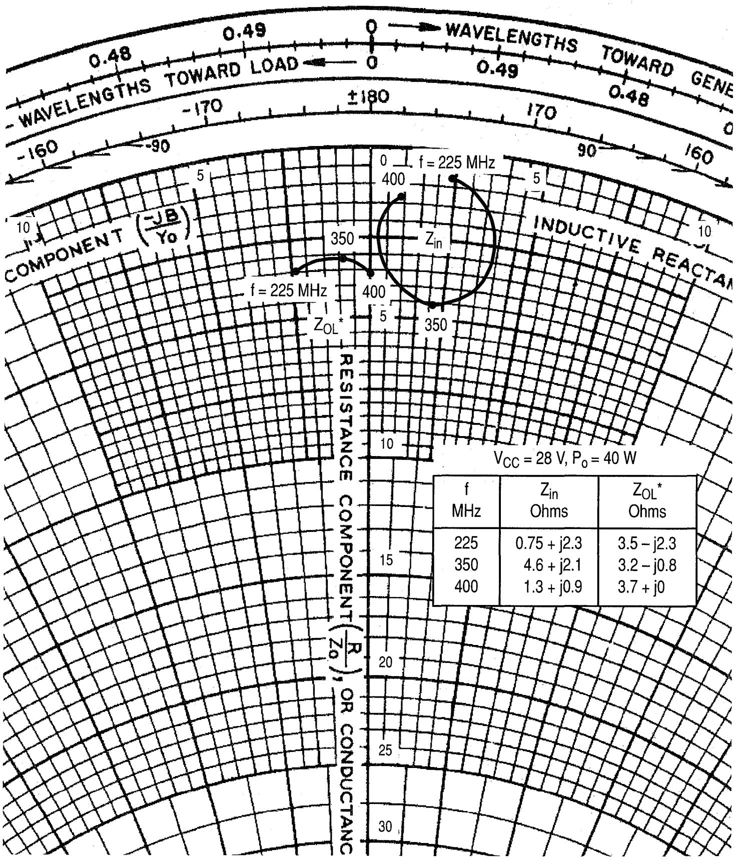


Figure 4. Output Power versus Supply Voltage
f = 400 MHz



V_{CC} = 28 V, P_o = 40 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
225	0.75 + j2.3	3.5 – j2.3
350	4.6 + j2.1	3.2 – j0.8
400	1.3 + j0.9	3.7 + j0

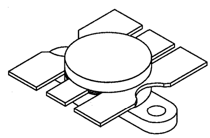
Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 5. Series Equivalent Input–Output Impedance

The RF Line
NPN Silicon RF Power Transistor

MRF327

80 W, 100 to 500 MHz
CONTROLLED "Q"
BROADBAND RF POWER TRANSISTOR
NPN SILICON



CASE 316–01, STYLE 1

. . . designed primarily for wideband large–signal output amplifier stages in the 100 to 500 MHz frequency range.

- Guaranteed Performance @ 400 MHz, 28 Vdc
  Output Power = 80 Watts over 225 to 400 MHz Band
  Minimum Gain = 7.3 dB @ 400 MHz
- Built–In Matching Network for Broadband Operation Using Double Match Technique
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications
- Characterized for 100 to 500 MHz

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	33	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	9.0 12	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 80 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 80 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 8.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 80 mAdc, I_C = 0)	$V_{(BR)CBO}$	60	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	95	125	pF

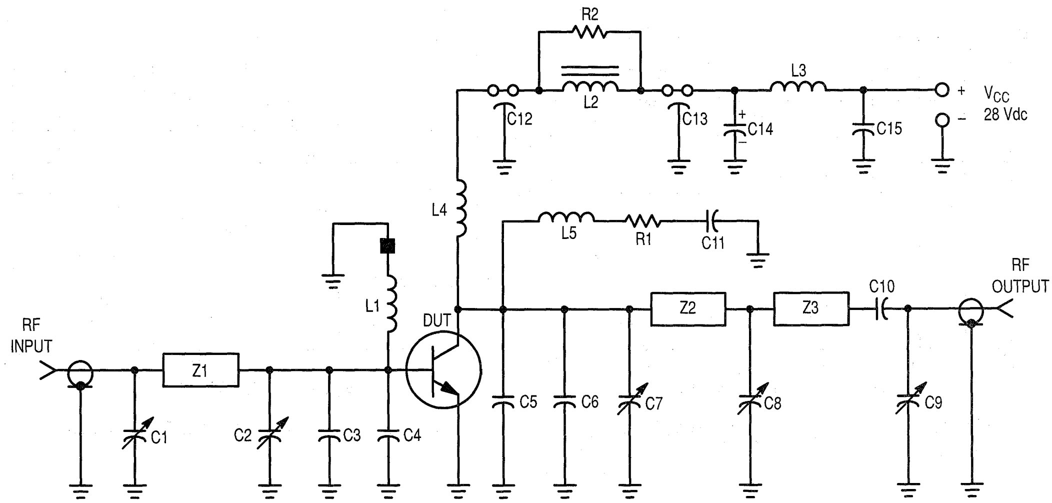
(continued)

NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

REV 1

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 400 MHz)	G_{PE}	7.3	9.0	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 400 MHz)	η	50	60	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 400 MHz, VSWR = 30:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1, C2, C7, C8, C9 — 1.0–20 pF Piston Trimmer (Johanson JMC 5501)
C3, C4 — 36 pF ATC 100 mil Chip Capacitor
C5, C6 — 43 pF ATC 100 mil Chip Capacitor
C10 — 100 pF UNELCO
C11, C15 — 0.1 μF Erie Redcap
C12, C13 — 680 pF Feedthru
C14 — 1.0 μF 50 V Tantalum
L1 — 4 Turns #22 AWG Enameled, 3/16″ ID Closewound with Ferroxcube Bead (#56–590–65/4B) on Ground End of Coil
L2 — Ferroxcube VK200–19/4B Ferrite Choke
L3 — 7 Turns #18 AWG, 11/16″ Long, Wound on a 100 kΩ 2.0 Watt Resistor
L4 — 6 Turns #20 AWG Enameled, 3/16″ ID Closewound
L5 — 4 Turns #22 AWG Enameled, 1/8″ ID Closewound
Z1 — Microstrip 0.2″ W x 1.5″ L
Z2 — Microstrip 0.17″ W x 1.16″ L
Z3 — Microstrip 0.17″ W x 0.63″ L
R1, R2 — 10 Ω 2.0 Watt
Board — Glass Teflon ε_r = 2.56, t = 0.062″
Input/Output Connectors Type N
DUT Socket Lead Frame Etched from 80–mil–Thick Copper

Figure 1. 400 MHz Test Circuit

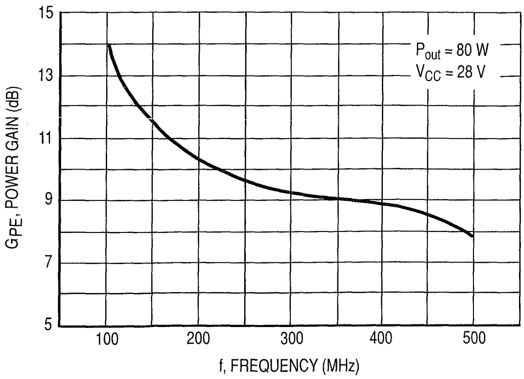


Figure 2. Power Gain versus Frequency

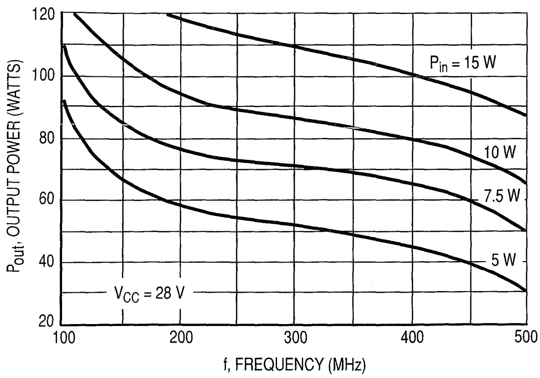


Figure 3. Output Power versus Frequency

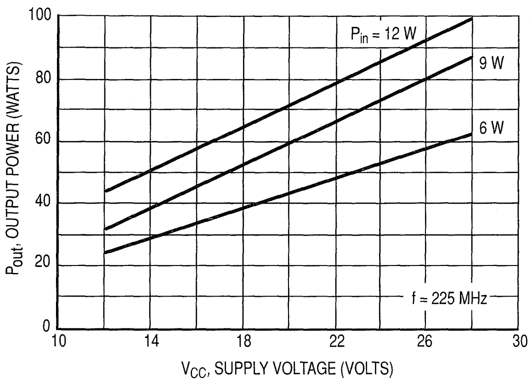


Figure 4. Output Power versus Supply Voltage

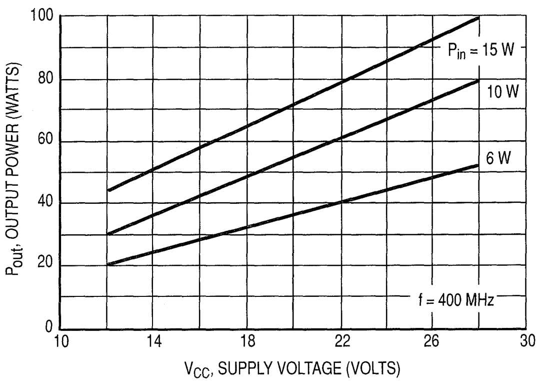


Figure 5. Output Power versus Supply Voltage

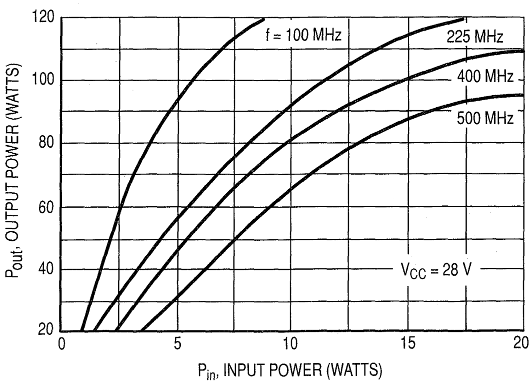
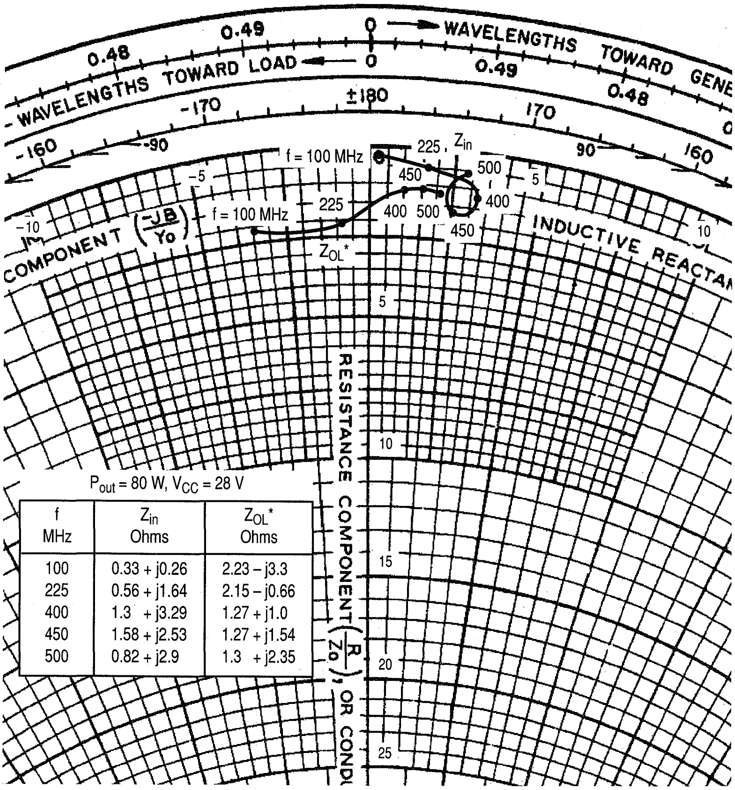


Figure 6. Output Power versus Input Power



P_{out} = 80 W, V_{CC} = 28 V

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
100	0.33 + j0.26	2.23 – j3.3
225	0.56 + j1.64	2.15 – j0.66
400	1.3 + j3.29	1.27 + j1.0
450	1.58 + j2.53	1.27 + j1.54
500	0.82 + j2.9	1.3 + j2.35

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 7. Series Equivalent Input–Output Impedance

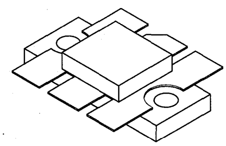
The RF Line
NPN Silicon RF Power Transistor

MRF329

. . . designed primarily for wideband large–signal output and driver amplifier stages in the 100 to 500 MHz frequency range.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 100 Watts
  Minimum Gain = 7.0 dB
  Efficiency = 50% (Min)
- Built–In Matching Network for Broadband Operation Using Double Match Technique
- 100% Tested for Load Mismatch at all Phase Angles with 3:1 VSWR
- Gold Metallization System for High Reliability

100 W, 100 to 500 MHz
CONTROLLED "Q"
BROADBAND RF POWER TRANSISTOR
NPN SILICON



CASE 333–04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	9.0 12	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	0.65	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 80 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 80 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 8.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc

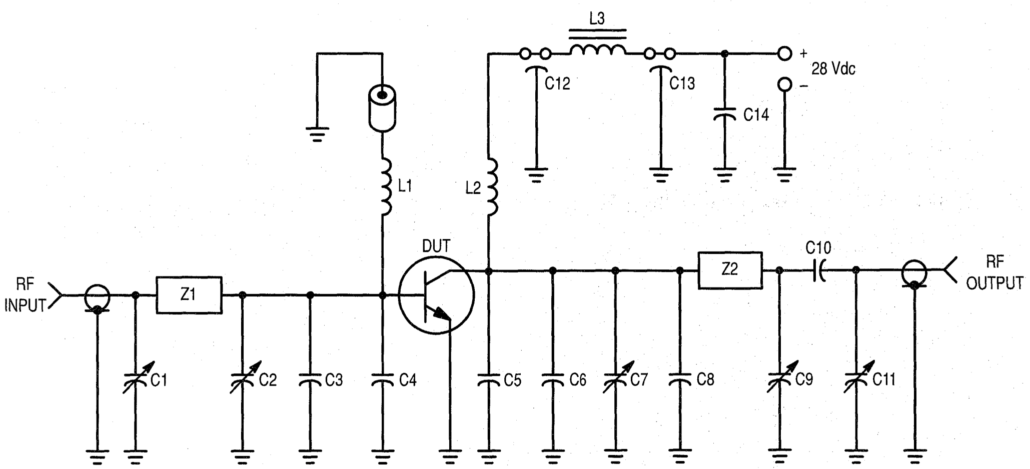
(continued)

NOTES:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (continued)					
Collector–Base Breakdown Voltage (I_C = 80 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	95	125	pF
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 400 MHz)	G_{PE}	7.0	9.7	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 400 MHz)	η	50	60	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 400 MHz, VSWR = 3:1 all angles)	ψ	No Degradation in Output Power			



C1, C2, C7, C9 — 1.0–20 pF Johanson (JMC 5501)
C3, C4 — 36 pF 100 mil Chip Cap (ATC)
C5, C6 — 50 pF 100 mil Chip Cap (ATC)
C8 — 30 pF 100 mil Chip Cap (ATC)
C10 — 2.0–150 pF 100 mil Chip Caps in Parallel (ATC)
C11 — 1.0–10 pF Johanson (JMC 5201)
C12, C13 — 1000 pF UNELCO Feedthru
C14 — 0.1 µF Erie Redcap

L1 — 0.15 µH Molded Choke with Ferrite Bead (Ferroxcube #56–590–65/4B) on Ground End
L2 — 4 Turns #18 AWG, 1/4″ ID
L3 — Ferroxcube VK200–19/4B
Z1 — Microstrip Line 2300 mils L x 210 mils W
Z2 — Microstrip Line 2300 mils L x 280 mils W
Board — Glass Teflon, t = 0.062″, ε_r = 2.56

Figure 1. 400 MHz Test Circuit

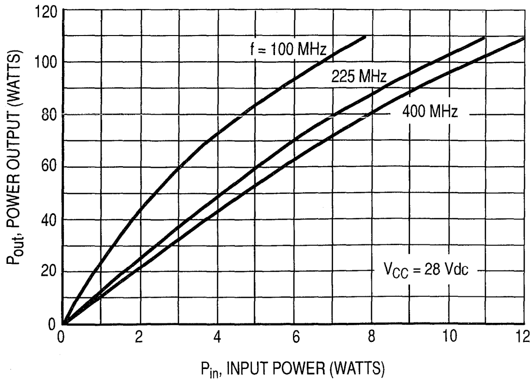


Figure 2. Output Power versus Input Power

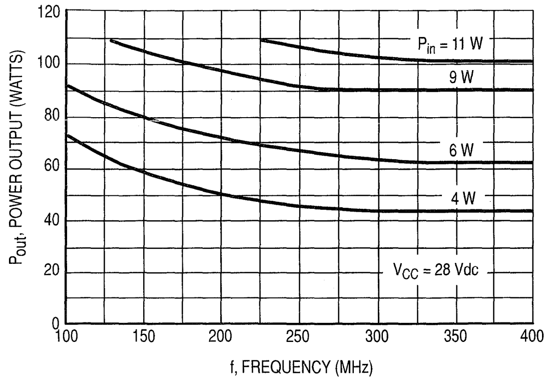


Figure 3. Output Power versus Frequency

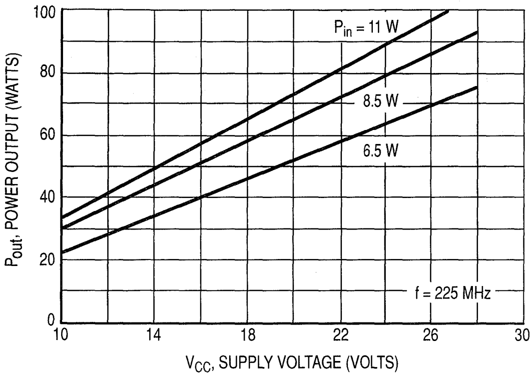


Figure 4. Output Power versus Supply Voltage

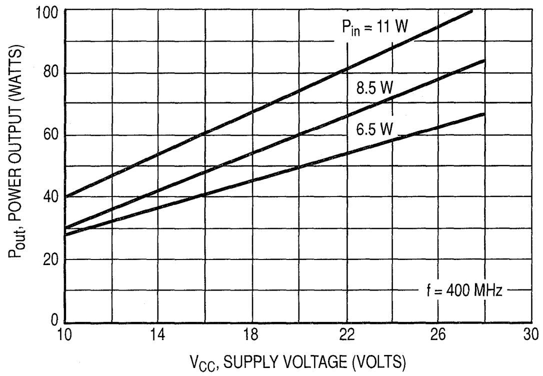


Figure 5. Output Power versus Supply Voltage

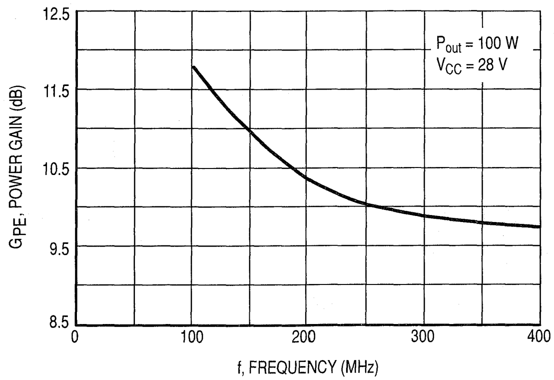
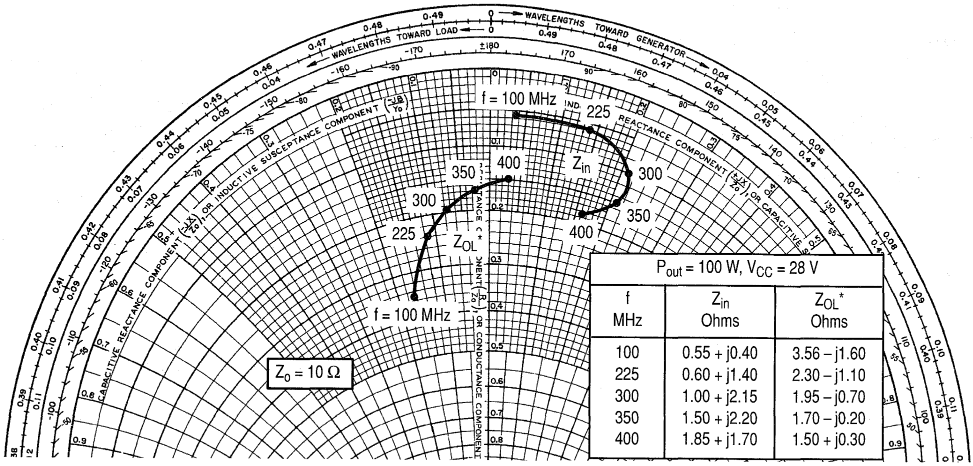


Figure 6. Power Gain versus Frequency



P_{out} = 100 W, V_{CC} = 28 V		
f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
100	0.55 + j0.40	3.56 – j1.60
225	0.60 + j1.40	2.30 – j1.10
300	1.00 + j2.15	1.95 – j0.70
350	1.50 + j2.20	1.70 – j0.20
400	1.85 + j1.70	1.50 + j0.30

Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 7. Series Equivalent Input/Output Impedance

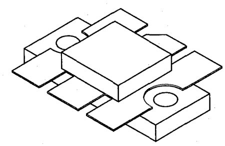
The RF Line
NPN Silicon RF Power Transistor

MRF338

Designed primarily for wideband large–signal output and driver amplifier stages in the 400 to 512 MHz frequency range.

- Specified 28 Volt, 470 MHz Characteristics
  Output Power = 80 Watts
  Minimum Gain = 7.3 dB
  Efficiency = 50% (Min)
- Built–In Matching Network for Broadband Operation
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications

**80 W, 400 to 512 MHz
CONTROLLED "Q"
BROADBAND RF POWER
TRANSISTOR
NPN SILICON**



CASE 333–04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Collector Current — Continuous — Peak	I_C	9 12	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

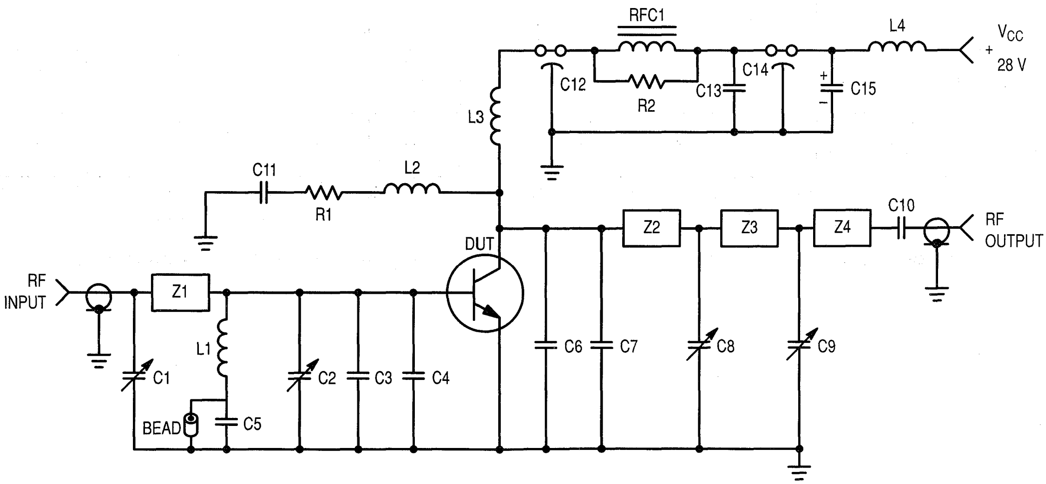
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 80 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 80 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 8 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc

(1) This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

REV 2

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Base Breakdown Voltage (I_C = 80 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	—	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	95	125	pF
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 470 MHz)	G_{PE}	7.3	8.8	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 470 MHz)	η	50	60	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 470 MHz, VSWR = 30:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			



Bead	Ferroxcube #56–590–65/3B	L3	3 Turns #18 AWG, 0.185″ ID, Close Wound
C1, C2, C8, C9	0.8–20 pF, Johanson (JMC 5501)	L4	4 Turns #18 AWG, 0.185″ ID, Close Wound
C3, C4, C6, C7	25 pF, 100 V, Underwood	RFC1	Ferroxcube VK200 19/4B
C5, C10	100 pF, 100 V, Underwood	R1, R2	10 Ω, 2.0 Watt Carbon
C11, C13	0.1 µF, Erie Redcap	Z1	0.190″ W x 2.5″ L, Microstrip Lin
C12, C14	680 pF, Feedthru	Z2	0.190″ W x 0.289″ L, Microstrip Line
C15	1.0 µF, Tantalum	Z3	0.190″ W x 0.55″ L, Microstrip Line
L1	0.15 µH, Molded Choke	Z4	0.190″ W x 0.325″ L, Microstrip Line
L2	5 Turns #20 AWG, 0.185″ ID, Close Wound	Board	Glass Teflon, t = 0.062″, ε_r = 2.56

Figure 1. 470 MHz Test Circuit

TYPICAL CHARACTERISTICS

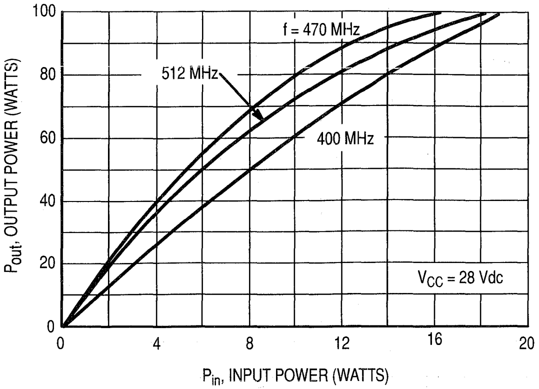


Figure 2. Output Power versus Input Power

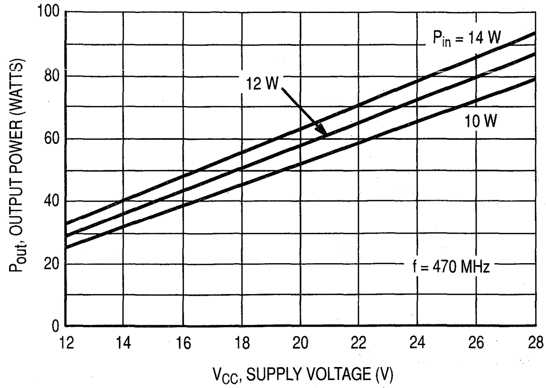


Figure 3. Output Power versus Supply Voltage

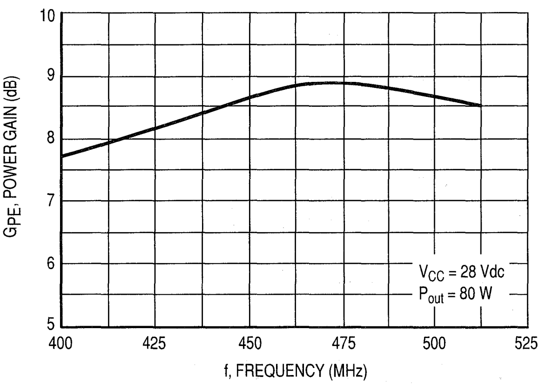


Figure 4. Power Gain versus Frequency

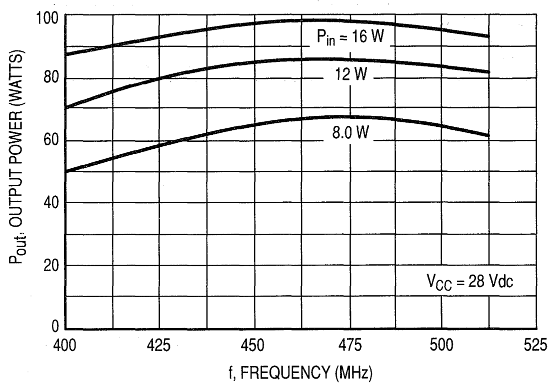
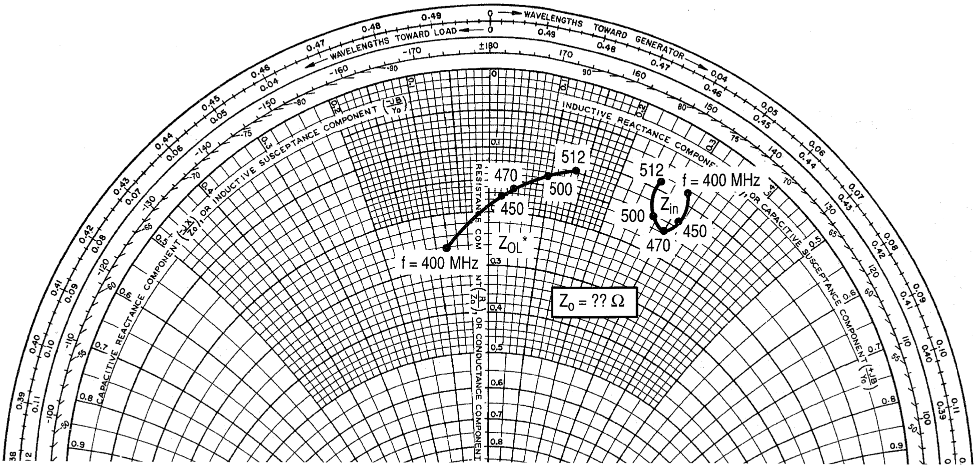


Figure 5. Output Power versus Frequency



V_{CC} = 28 V, P_{out} = 80 W		
f MHz	Z_{in} Ohms	Z_{OL}* Ohms
512	0.91 + j2.61	1.19 + j1.34
500	1.47 + j2.71	1.33 + j0.96
470	1.53 + j2.98	1.60 + j0.45
450	1.27 + j3.09	1.70 + j0.25
400	0.86 + j3.01	2.58 – j0.79

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Input/Output Impedance

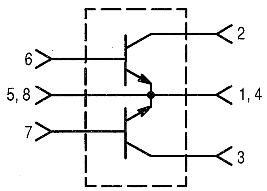
The RF Line
NPN Silicon Push-Pull RF Power Transistor

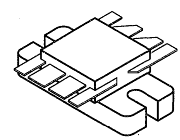
MRF392

**125 W, 30 to 500 MHz
CONTROLLED "Q"
BROADBAND PUSH–PULL
RF POWER TRANSISTOR
NPN SILICON**

Designed primarily for wideband large–signal output and driver amplifier stages in the 30 to 500 MHz frequency range.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 125 W
  Typical Gain = 10 dB
  Efficiency = 55% (Typ)
- Built–In Input Impedance Matching Networks for Broadband Operation
- Push–Pull Configuration Reduces Even Numbered Harmonics
- Gold Metallization System for High Reliability
- 100% Tested for Load Mismatch
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.





CASE 744A–01, STYLE 1

The MRF392 is two transistors in a single package with separate base and collector leads and emitters common. This arrangement provides the designer with a space saving device capable of operation in a push–pull configuration.

PUSH–PULL TRANSISTORS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	16	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

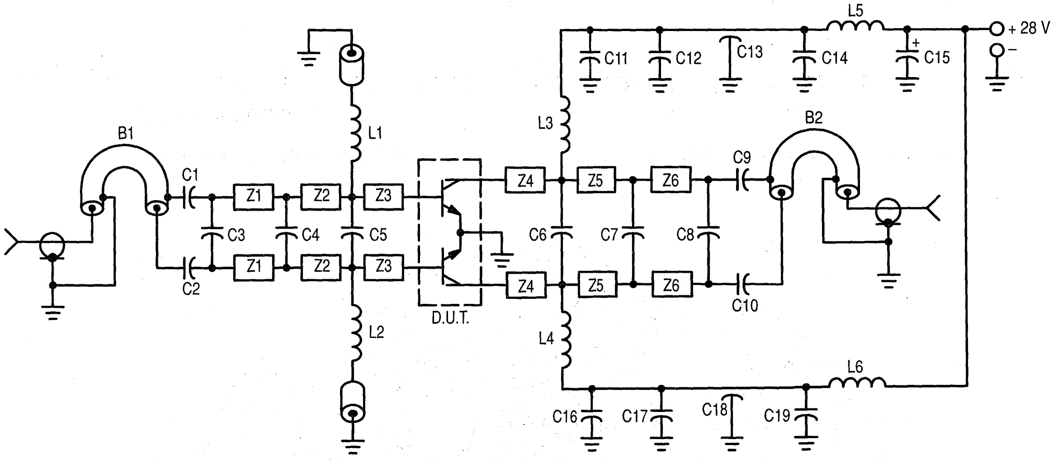
NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF push–pull amplifier.

REV 8

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	60	100	—
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	75	95	pF
FUNCTIONAL TESTS (2) — **See Figure 1**					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz)	G_{pe}	8.0	10	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz)	η	50	55	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz, VSWR = 30:1, all phase angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each transistor chip measured separately.
2. Both transistor chips operating in push–pull amplifier.



C1, C2 — 240 pF, 100 Mil Chip Cap (ATC) or Equivalent
C3 — 3.6 pF, 100 Mil Chip Cap (ATC) or Equivalent
C4, C8 — 8.2 pF, 100 Mil Chip Cap (ATC) or Equivalent
C5, C6 — 20 pF, 100 Mil Chip Cap (ATC) or Equivalent
C7 — 18 pF, Mini Unelco or Equivalent
C9, C10 — 270 pF, 100 Mil Chip Cap (ATC) or Equivalent
C11, C12, C16, C17 — 470 pF 100 Mil Chip Cap (ATC) or Equivalent
C13, C18 — 680 pF Feedthru
C14, C19 — 0.1 µF Erie Redcap or Equivalent
C15 — 20 µF, 50 V
L1, L2 — 0.15 µH Molded Choke With Ferrite Bead
L3, L4 — 2–1/2 Turns #20 AWG, 0.200 ID
L5, L6 — 3–1/2 Turns #18 AWG, 0.200 ID

B1 — Balun, 50 Ω Semi–Rigid Coaxial Cable 86 Mil OD, 2″ L
B2 — Balun, 50 Ω Semi–Rigid Coaxial Cable 86 Mil OD, 2″ L
Z1 — Microstrip Line 270 Mil L x 125 Mil W
Z2 — Microstrip Line 375 Mil L x 125 Mil W
Z3 — Microstrip Line 280 Mil L x 125 Mil W
Z4 — Microstrip Line 300 Mil L x 125 Mil W
Z5 — Microstrip Line 350 Mil L x 125 Mil W
Z6 — Microstrip Line 365 Mil L x 125 Mil W
Board Material — 0.0625″ Teflon Fiberglass ε_r = 2.5 ± 0.05 1 oz. Cu. CLAD, Double Sided

Figure 1. 400 MHz Test Fixture

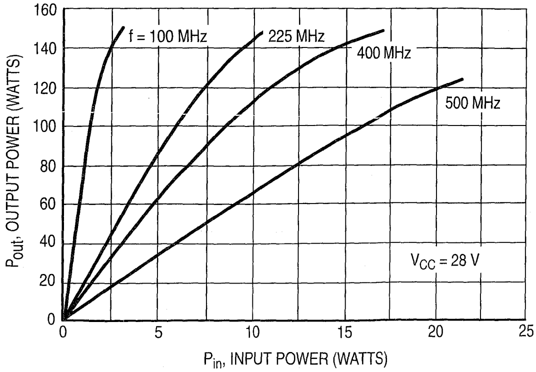


Figure 2. Output Power versus Input Power

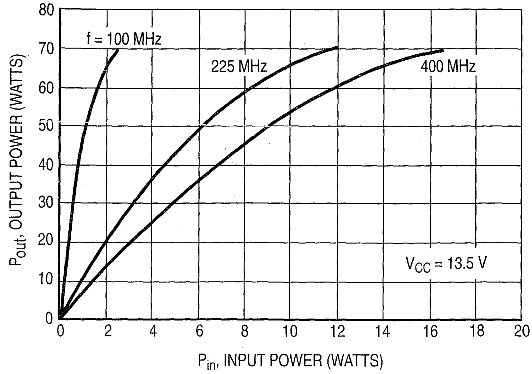


Figure 3. Output Power versus Input Power

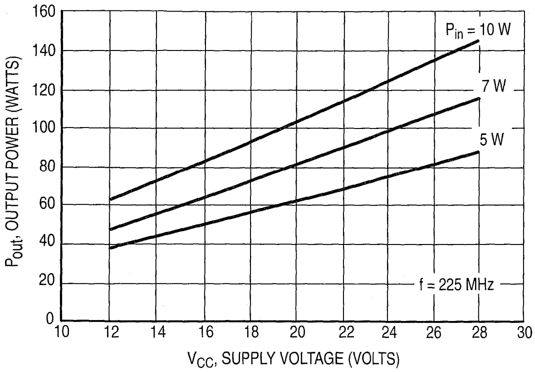


Figure 4. Output Power versus Supply Voltage

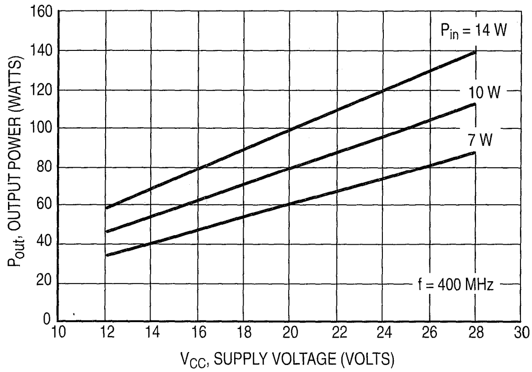
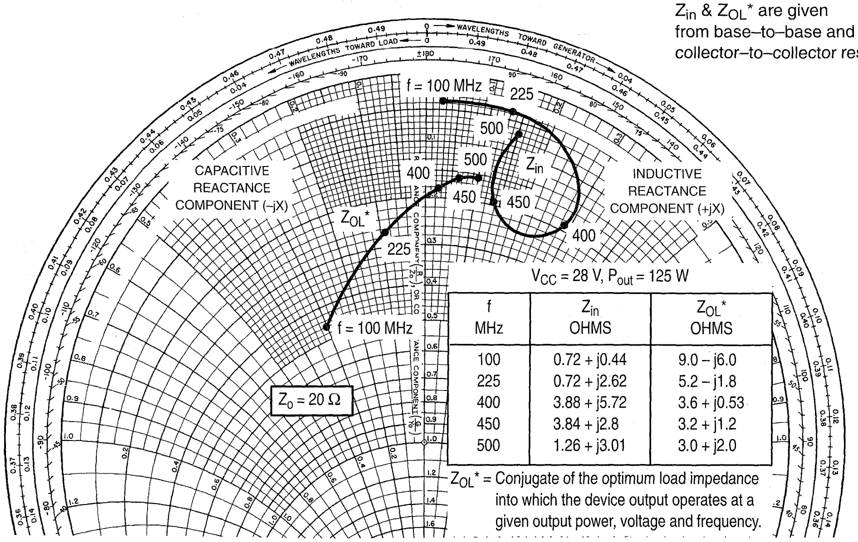


Figure 5. Output Power versus Supply Voltage

Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively.



V_{CC} = 28 V, P_{out} = 125 W

f MHz	Z_{in} OHMS	Z_{OL}* OHMS
100	0.72 + j0.44	9.0 – j6.0
225	0.72 + j2.62	5.2 – j1.8
400	3.88 + j5.72	3.6 + j0.53
450	3.84 + j2.8	3.2 + j1.2
500	1.26 + j3.01	3.0 + j2.0

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Input/Output Impedance

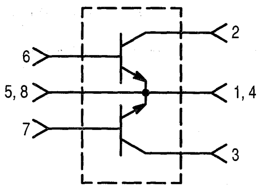
The RF Line
NPN Silicon Push-Pull RF Power Transistor

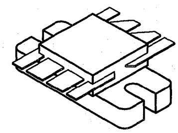
MRF393

. . . designed primarily for wideband large–signal output and driver amplifier stages in the 30 to 500 MHz frequency range.

- Specified 28 Volt, 500 MHz Characteristics —
  Output Power = 100 W
  Typical Gain = 9.5 dB (Class AB); 8.5 dB (Class C)
  Efficiency = 55% (Typ)
- Built–In Input Impedance Matching Networks for Broadband Operation
- Push–Pull Configuration Reduces Even Numbered Harmonics
- Gold Metallization System for High Reliability
- 100% Tested for Load Mismatch
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

100 W, 30 to 500 MHz
CONTROLLED "Q"
BROADBAND PUSH–PULL
RF POWER TRANSISTOR
NPN SILICON





CASE 744A–01, STYLE 1

The MRF393 is two transistors in a single package with separate base and collector leads and emitters common. This arrangement provides the designer with a space saving device capable of operation in a push–pull configuration.

PUSH–PULL TRANSISTORS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	16	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

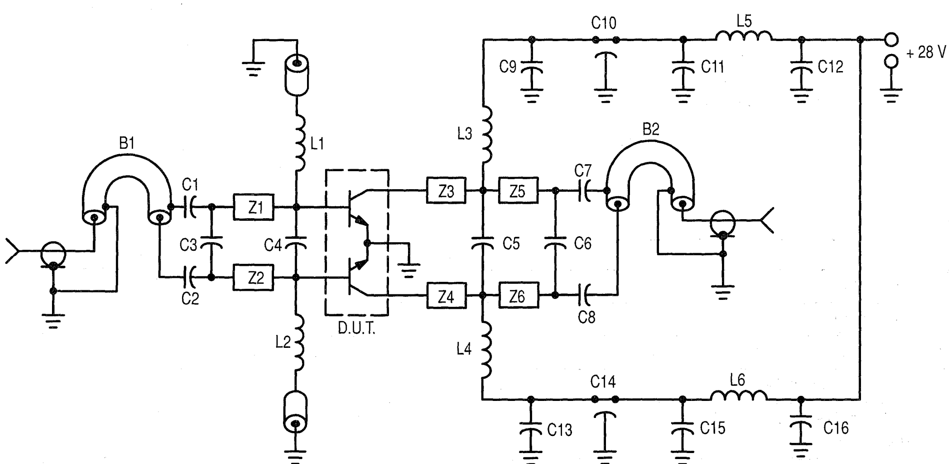
NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF push–pull amplifier.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	100	—
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	40	75	95	pF
FUNCTIONAL TESTS (2) — **See Figure 1**					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 500 MHz)	G_{pe}	7.5	8.5	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 500 MHz)	η	50	55	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 500 MHz, VSWR = 30:1, all phase angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each transistor chip measured separately.
2. Both transistor chips operating in push–pull amplifier.



C1, C2, C7, C8 — 240 pF 100 mil Chip Cap
C3 — 15 pF 100 mil Chip Cap
C4 — 24 pF 100 mil Chip Cap
C5 — 33 pF 100 mil Chip Cap
C6 — 12 pF 100 mil Chip Cap
C9, C13 — 1000 pF 100 mil Chip Cap
C10, C14 — 680 pF Feedthru Cap
C11, C15 — 0.1 µF Ceramic Disc Cap
C12, C16 — 50 µF 50 V

L1, L2 — 0.15 µH Molded Choke with Ferrite Bead
L3, L4 — 2–1/2 Turns #20 AWG 0.200″ ID
L5, L6 — 3–1/2 Turns #18 AWG 0.200″ ID
B1, B2 — Balun 50 Ω Semi Rigid Coax, 86 mil OD, 4″ Long
Z1, Z2 — 850 mil Long x 125 mil W. Microstrip
Z3, Z4 — 200 mil Long x 125 mil W. Microstrip
Z5, Z6 — 800 mil Long x 125 mil W. Microstrip
Board Material — 0.0325″ Teflon–Fiberglass, ε_r = 2.56,
1 oz. Copper Clad both sides.

Figure 1. 500 MHz Test Fixture

CLASS C

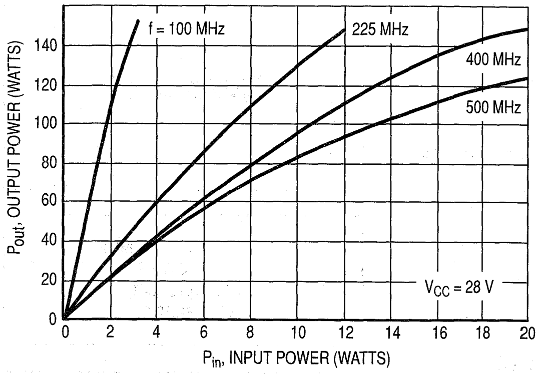


Figure 2. Output Power versus Input Power

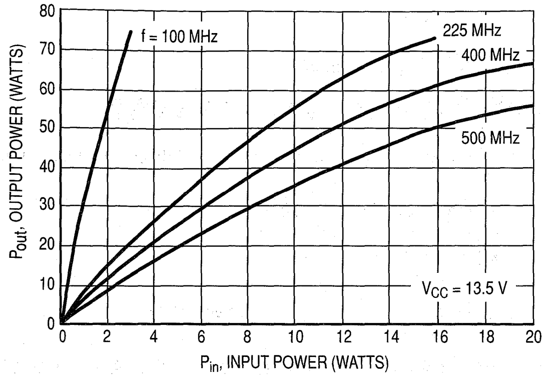


Figure 3. Output Power versus Input Power

CLASS C

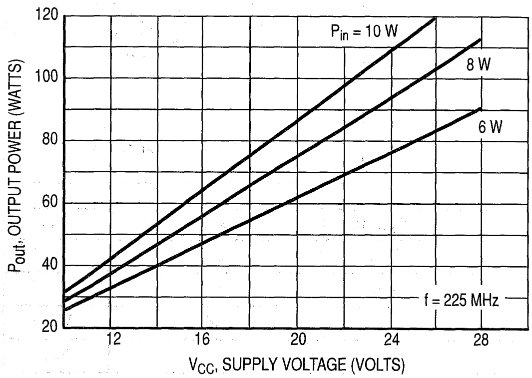


Figure 4. Output Power versus Supply Voltage

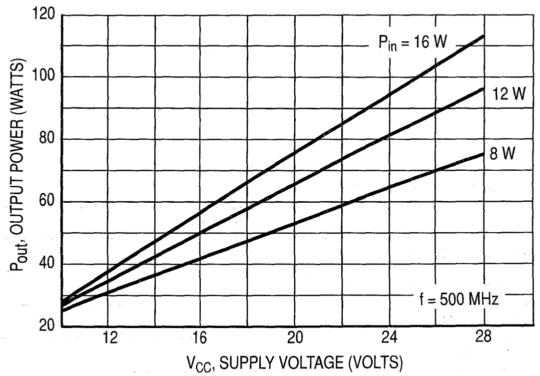
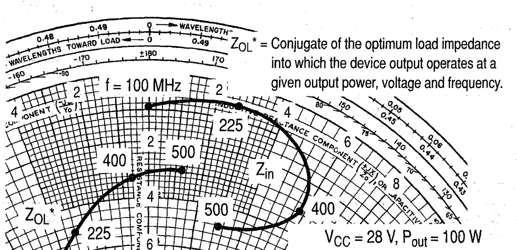


Figure 5. Output Power versus Supply Voltage



f MHz	Z_{in}	Z_{OL}*
100	0.85 + j0	7.8 – j5.6
225	0.58 + j2.6	5.0 – j3.2
400	3.00 + j5.9	3.2 – j0.6
500	4.80 + j3.0	2.9 + j1.2

NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively.

Figure 6. Series Equivalent Input/Output Impedance

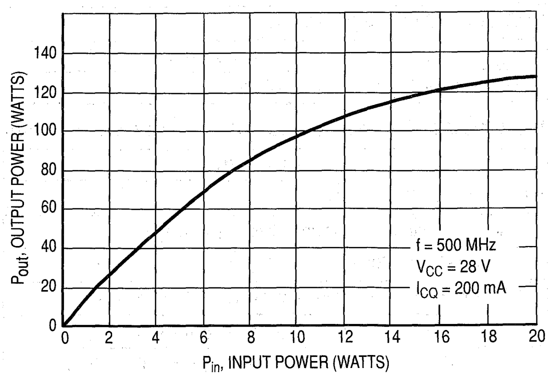


Figure 7. Class AB Output Power versus Input Power

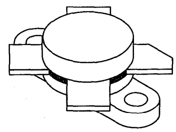
The RF Line
NPN Silicon RF Power Transistor

MRF421

Designed primarily for application as a high–power linear amplifier from 2.0 to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics —
  Output Power = 100 W (PEP)
  Minimum Gain = 10 dB
  Efficiency = 40%
- Intermodulation Distortion @ 100 W (PEP) —
  IMD = −30 dB (Min)
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR

100 W (PEP), 30 MHz
RF POWER
TRANSISTORS
NPN SILICON



CASE 211–11, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	20	Vdc
Collector–Base Voltage	V_{CBO}	45	Vdc
Emitter–Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	20	Adc
Withstand Current — 10 s	—	30	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	290 1.66	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	45	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 200 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 16 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	10	mAdc

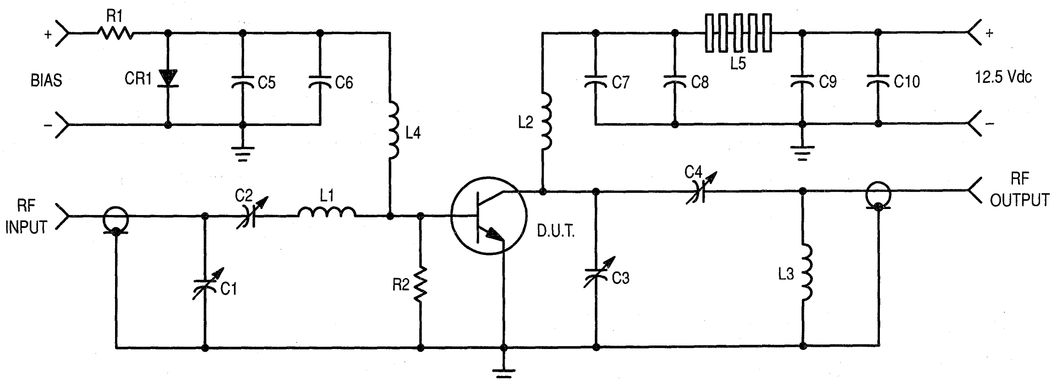
(continued)

REV 1

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	70	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	550	800	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 100 W, $I_{C(max)}$ = 10 Adc, I_{CQ} = 150 mAdc, f = 30, 30.001 MHz)	G_{PE}	10	12	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 100 W, $I_{C(max)}$ = 10 Adc, I_{CQ} = 150 mA, f = 30, 30.001 MHz)	η	40	—	—	%
Intermodulation Distortion (1) (V_{CE} = 12.5 Vdc, P_{out} = 100 W, I_C = 10 Adc, I_{CQ} = 150 mA, f = 30, 30.001 MHz)	IMD	—	−33	−30	dB

NOTE:
1. To proposed EIA method of measurement. Reference peak envelope power.



C1, C2, C4 — 170–780 pF, ARCO 469
C3 — 80–480 pF, ARCO 466
C5, C7, C10 — ERIE 0.1 µF, 100 V
C6 — MALLORY 500 µF @ 15 V Electrolytic
C9 — 100 µF, 15 V Electrolytic
C8 — 1000 pF, 350 V UNDERWOOD
R1 — 10 Ω, 25 Watt Wirewound
R2 — 10 Ω, 1.0 Watt Carbon
CR1 — 1N4997
L1 — 3 Turns, #16 Wire, 5/16″ I.D., 5/16″ Long
L2 — 12 Turns, #16 Enameled Wire Closewound, 1/4″ I.D.
L3 — 1-3/4 Turns, 1/8″ Tubing, 3/8″ I.D., 3/8″ Long
L4 — 10 µH Molded Choke
L5 — 10 Ferrite Beads — FERROXCUBE #56–590–65/3B

Figure 1. 30 MHz Test Circuit Schematic

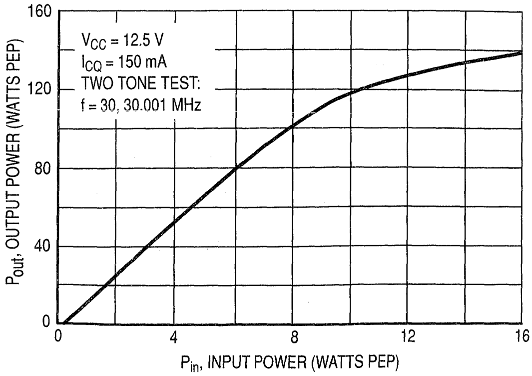


Figure 2. Output Power versus Input Power

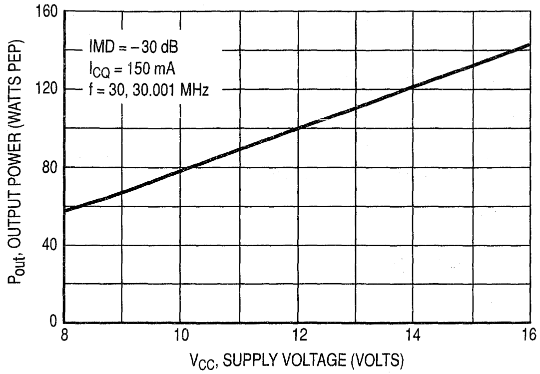


Figure 3. Output Power versus Supply Voltage

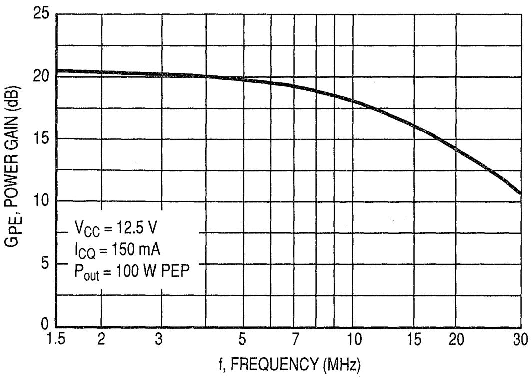


Figure 4. Power Gain versus Frequency

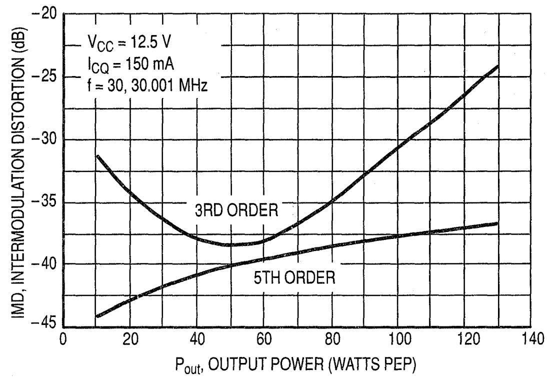


Figure 5. Intermodulation Distortion versus Output Power

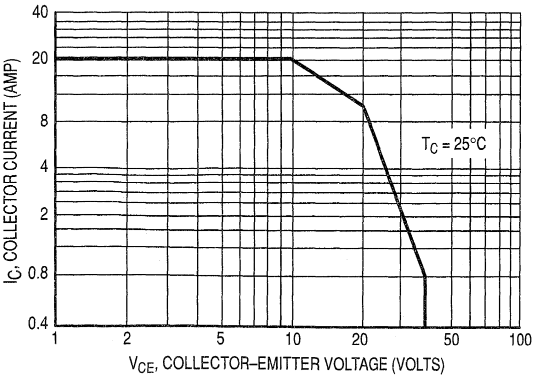
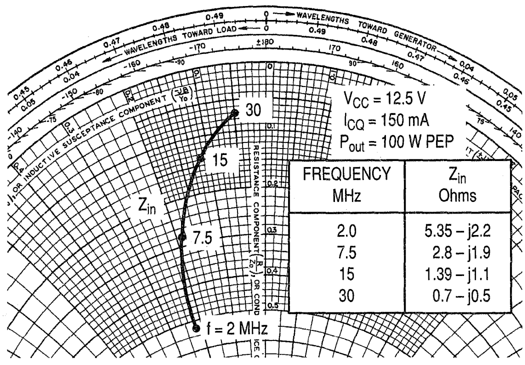


Figure 6. DC Safe Operating Area



FREQUENCY MHz	Z_{in} Ohms
2.0	5.35 – j2.2
7.5	2.8 – j1.9
15	1.39 – j1.1
30	0.7 – j0.5

Figure 7. Series Equivalent Impedance

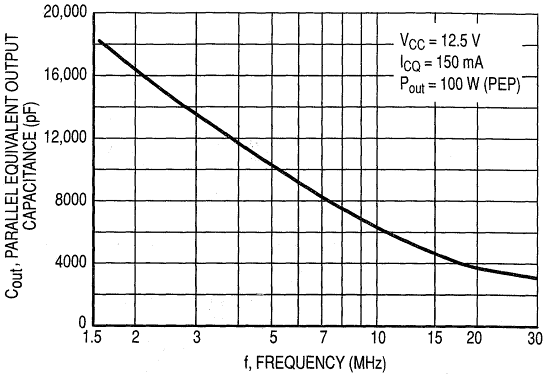


Figure 8. Output Capacitance versus Frequency

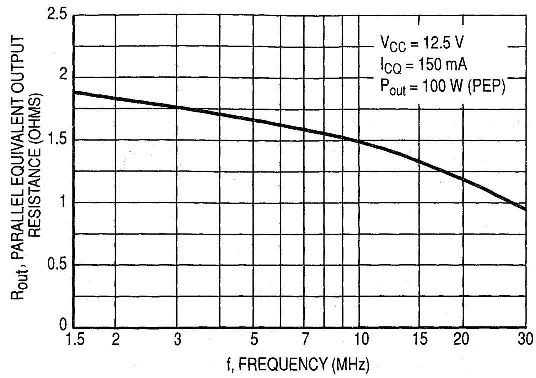


Figure 9. Output Resistance versus Frequency

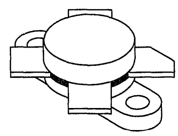
The RF Line
NPN Silicon RF Power Transistor

Designed primarily for applications as a high–power linear amplifier from 2.0 to 30 MHz.

- Specified 28 Volt, 30 MHz Characteristics —
  Output Power = 150 W (PEP)
  Minimum Gain = 10 dB
  Efficiency = 40%
- Intermodulation Distortion @ 150 W (PEP) —
  IMD = –30 dB (Min)
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR

MRF422

150 W (PEP), 30 MHz
RF POWER
TRANSISTORS
NPN SILICON



CASE 211–11, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CBO}	85	Vdc
Emitter–Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	20	Adc
Withstanding Current — 10 s	—	30	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	290 1.66	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	85	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	85	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	20	mAdc

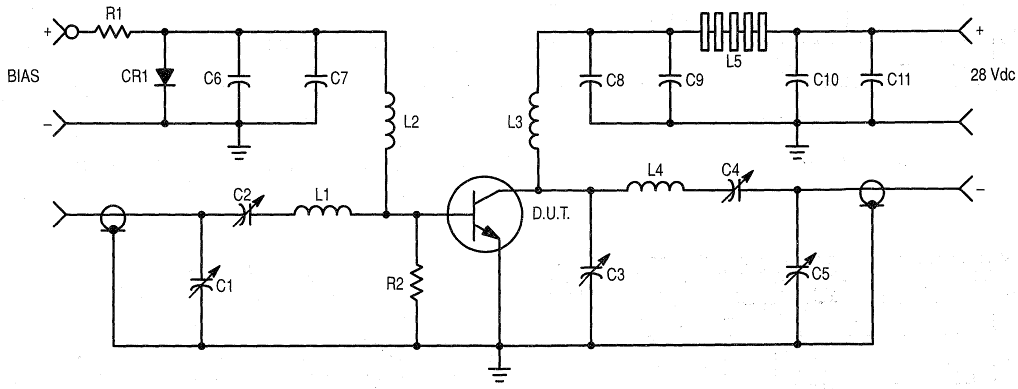
(continued)

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	15	30	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	420	—	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 150 W (PEP), $I_{C(max)}$ = 6.7 Adc, I_{CQ} = 150 mAdc, f = 30, 30.001 MHz)	G_{PE}	10	13	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 150 W (PEP), $I_{C(max)}$ = 6.7 Adc, I_{CQ} = 150 mAdc, f = 30, 30.001 MHz)	η	—	45	—	%
Intermodulation Distortion (1) (V_{CE} = 28 Vdc, P_{out} = 150 W (PEP), I_C = 6.7 Adc, I_{CQ} = 150 mAdc, f = 30, 30.001 MHz)	IMD	—	−33	−30	dB
Output Power (V_{CE} = 28 Vdc, f = 30 MHz)	P_{out}	150	—	—	Watts (PEP)

NOTE:
1. To Mil–Std–1311 Version A, Test Method 2204, Two Tone, Reference each Tone.



C1, C2, C3, C5 — 170–680 pF, ARCO 469
C4 — 80–480 pF, ARCO 466
C6, C8, C11 — ERIE 0.1 µF, 100 V
C7 — MALLORY 500 µF, 15 V Electrolytic
C9 — UNDERWOOD 1000 pF, 350 V
C10 — 10 µF, 50 V Electrolytic
R1 — 10 Ω, 25 Watt Wire Wound
R2 — 10 Ω, 1.0 Watt Carbon
CR1 — 1N4997

L1 — 3 Turns, #16 Wire, 5/16″ I.D., 5/16″ Long
L2 — 10 µH Molded Choke
L3 — 12 Turns, #16 Enameled Wire, Close Wound, 1/4″ Dia.
L4 — 5 Turns, 1/8″ Copper Tubing
L5 — 10 Ferrite Beads — FERROXCUBE #56–590–65/3B

Figure 1. 30 MHz Test Circuit Schematic

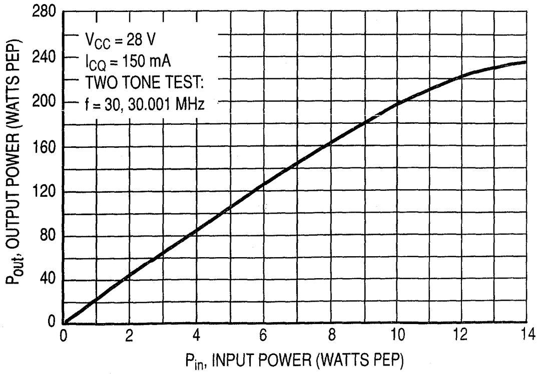


Figure 2. Output Power versus Input Power

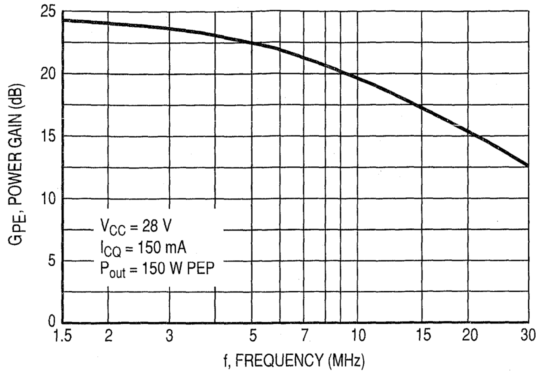


Figure 3. Power Gain versus Frequency

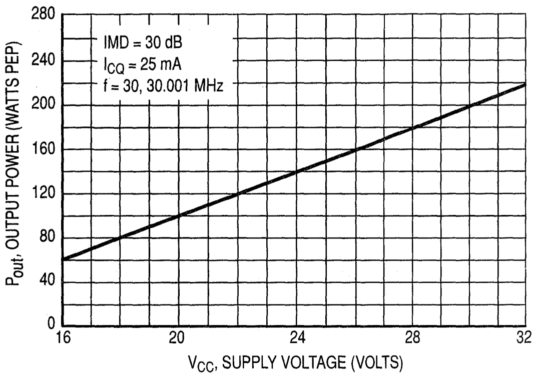


Figure 4. Linear Output Power versus Supply Voltage

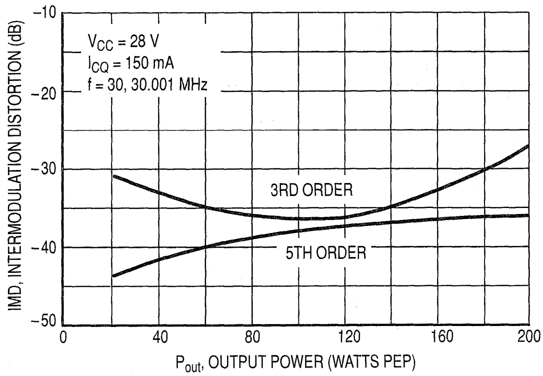


Figure 5. Intermodulation Distortion versus Output Power

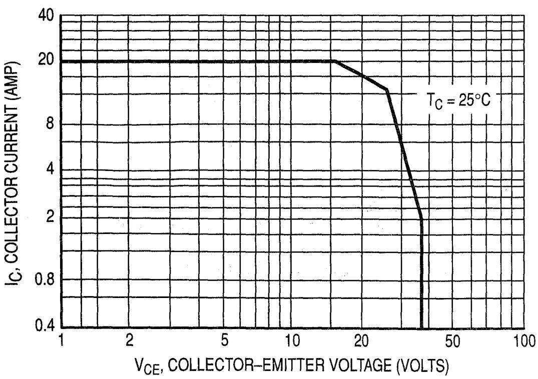


Figure 6. DC Safe Operating Area

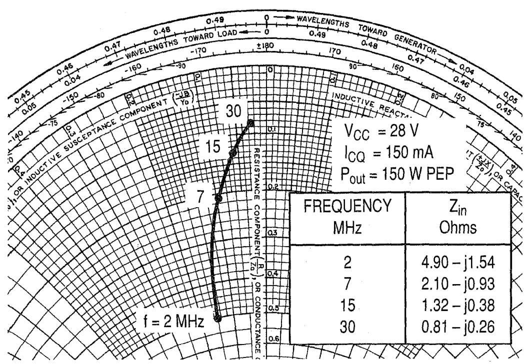


Figure 7. Series Input Impedance

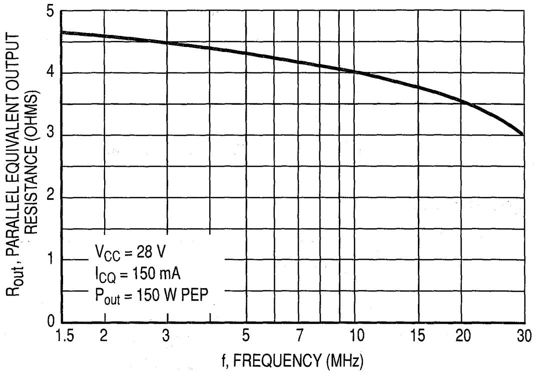


Figure 8. Output Resistance versus Frequency

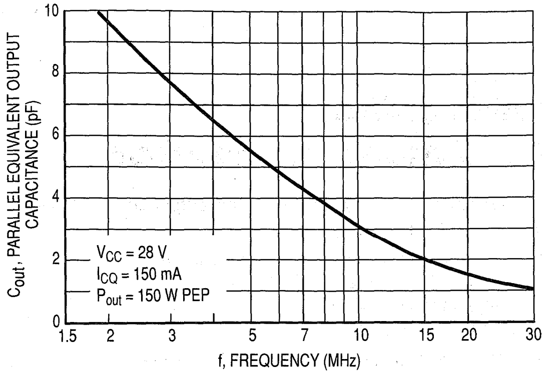


Figure 9. Output Capacitance versus Frequency

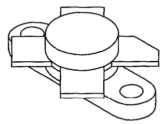
The RF Line
NPN Silicon RF Power Transistor

MRF426

. . . designed for high gain driver and output linear amplifier stages in 1.5 to 30 MHz HF/SSB equipment.

- Specified 28 Volt, 30 MHz Characteristics —
  Output Power = 25 W (PEP)
  Minimum Gain = 22 dB
  Efficiency = 35%
- Intermodulation Distortion @ 25 W (PEP) —
  IMD = −30 dB (Max)
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Class A and AB Characterization
- BLX 13 Equivalent

25 W (PEP), 30 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 211–07, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	35	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.0	Adc
Withstand Current — 5 s	—	6.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	70 0.4	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc

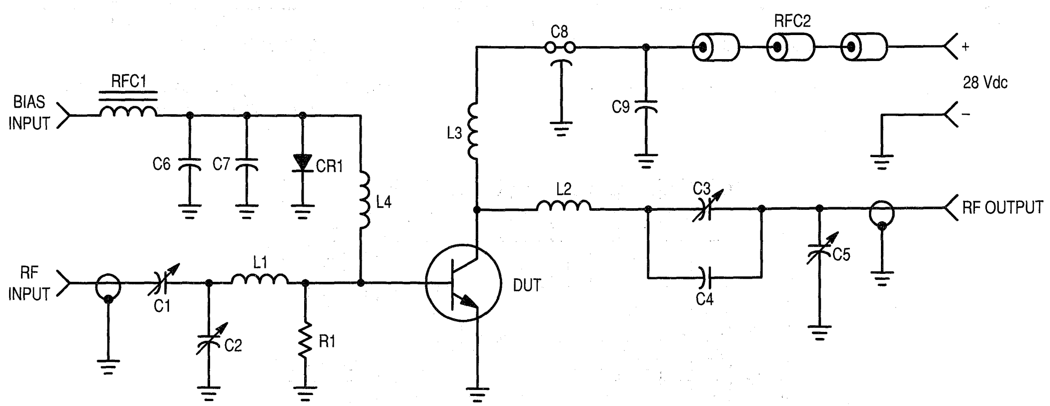
NOTE:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	35	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	60	80	pF
FUNCTIONAL TESTS (SSB)					
Common–Emitter Amplifier Gain (V_{CC} = 28 Vdc, P_{out} = 25 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA)	G_{PE}	22	25	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 25 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA)	η	35	—	—	%
Intermodulation Distortion (2) (V_{CC} = 28 Vdc, P_{out} = 25 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA)	$IMD_{(d3)}$	—	−35	−30	dB
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 25 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (2) and Power Gain (V_{CC} = 28 Vdc, P_{out} = 8.0 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 1.2 Adc)	G_{PE} $IMD_{(d3)}$ $IMD_{(d5)}$	— — —	23.5 −40 −55	— — —	dB

NOTE:
2. To Mil–Std–1311 Version A, Test Method 2204B, Two Tone, Reference each Tone.



C1, C2 — ARCO 469, 190−780 pF
C3, C4 — ARCO 464, 25−280 pF
C5 — 120 pF Dipped Mica
C6, C7 — 100 µF, 15 Vdc
C8 — 680 pF F.T. Allen Bradley
C9 — 1.0 µF 35 V Tantalum
CR1 — 1N4997

L1 — 3 Turns #16 0.25″ ID
L2 — 6 Turns #16 0.5″ ID
L3 — 7 Turns #20 0.38″ ID
L4 — 10 µH Molded Choke Delevan
RFC1 — Ferroxcube VK200/20–4B
RFC2 — 3–Ferroxcube 5653065–3B
RF — Input/Output Connectors UG53 A/µ
R1 — 10 Ω 1/2 Watt 10%

Adjust Bias (Base) for I_{CQ} = 20 mA with No RF Applied

Figure 1. 30 MHz Linear Test Circuit

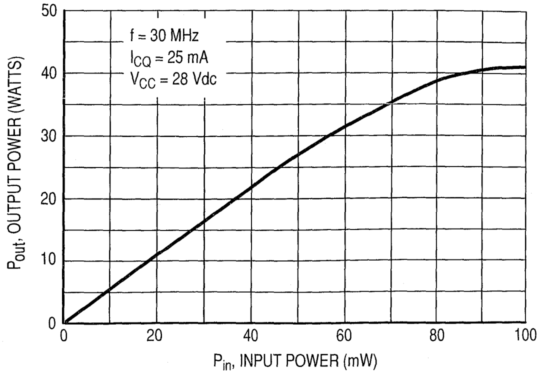


Figure 2. Output Power versus Input Power

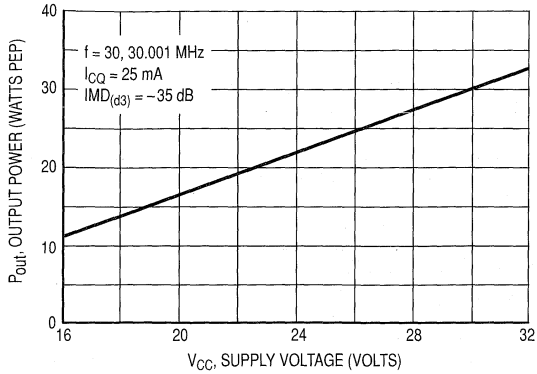


Figure 3. Output Power versus Supply Voltage

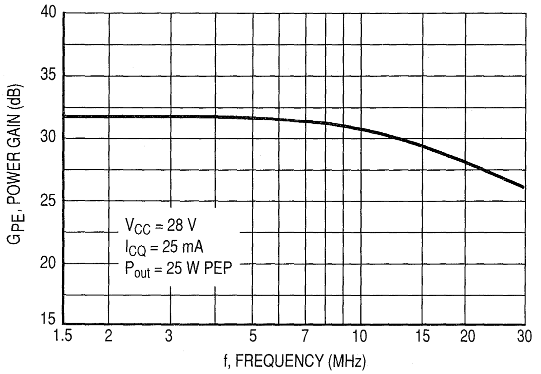


Figure 4. Power Gain versus Frequency

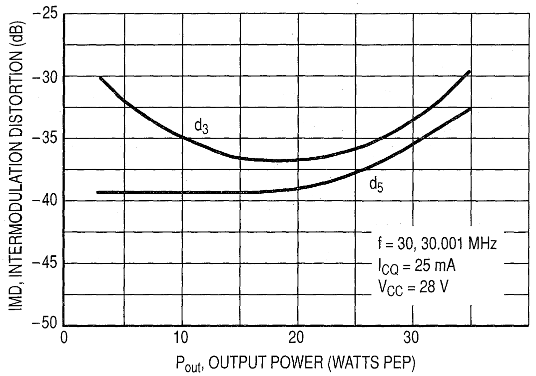


Figure 5. Intermodulation Distortion versus Output Power

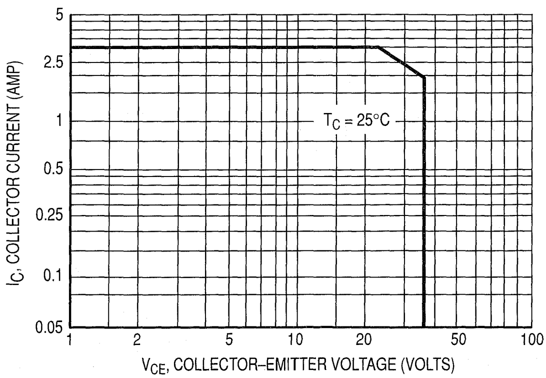


Figure 6. DC Safe Operating Area

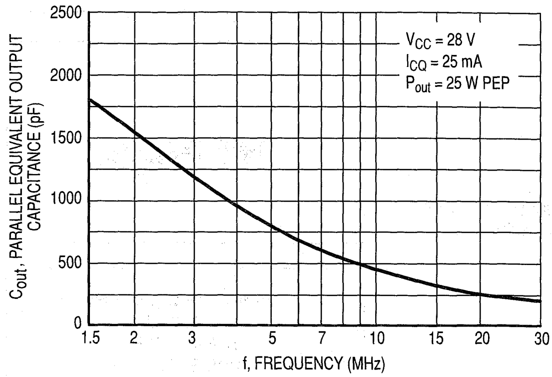


Figure 7. Output Capacitance versus Frequency

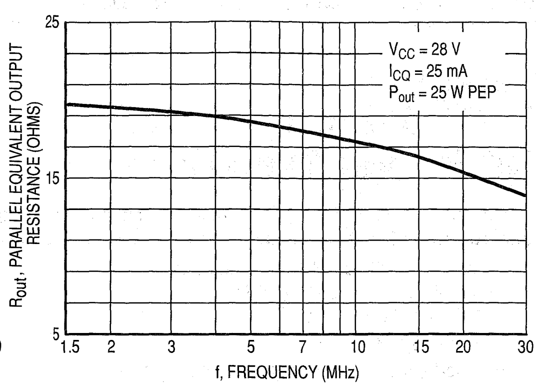
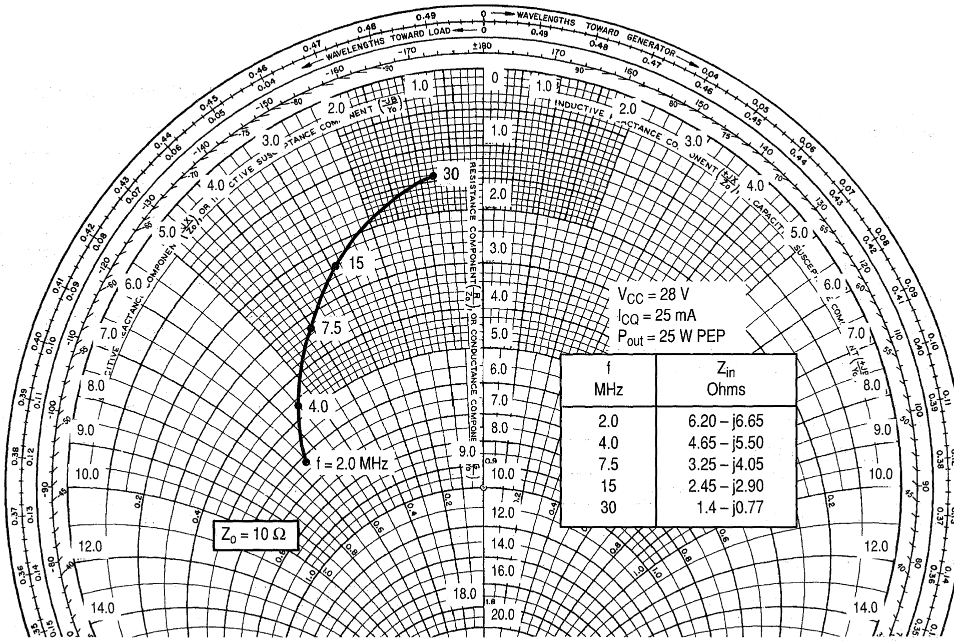


Figure 8. Output Resistance versus Frequency



f MHz	Z_{in} Ohms
2.0	6.20 – j6.65
4.0	4.65 – j5.50
7.5	3.25 – j4.05
15	2.45 – j2.90
30	1.4 – j0.77

Figure 9. Series Equivalent Input Impedance

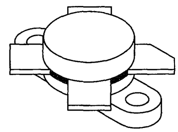
The RF Line
NPN Silicon RF Power Transistor

MRF429

Designed primarily for high–voltage applications as a high–power linear amplifier from 2.0 to 30 MHz. Ideal for marine and base station equipment.

- Specified 50 Volt, 30 MHz Characteristics —
  Output Power = 150 W (PEP)
  Minimum Gain = 13 dB
  Efficiency = 45%
- Intermodulation Distortion @ 150 W (PEP) —
  IMD = −32 dB (Max)
- Diffused Emitter Resistors for Superior Ruggedness
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR @ 150 W CW

150 W (LINEAR), 30 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 211–11, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	50	Vdc
Collector–Base Voltage	V_{CBO}	100	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	16	Adc
Withstand Current — 10 s	—	20	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	233 1.33	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

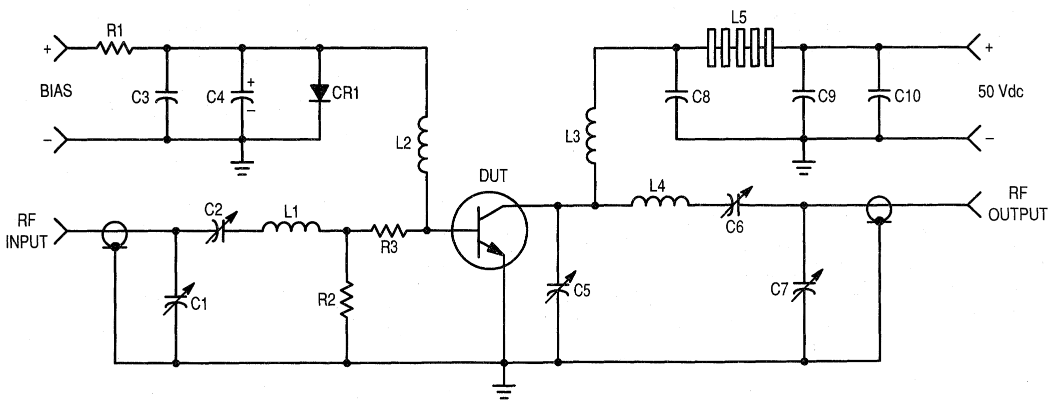
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	50	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	100	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	100	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	220	300	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Gain (V_{CC} = 50 Vdc, P_{out} = 150 W (PEP), I_C(max) = 3.32 Adc, f = 30; 30.001 MHz)	G_{PE}	13	15	—	dB
Output Power (V_{CE} = 50 Vdc, f = 30; 30.001 MHz)	P_{out}	150	—	—	W (PEP)
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 150 W (PEP), I_C(max) = 3.32 Adc, f = 30, 30.001 MHz)	η	45	—	—	%
Intermodulation Distortion (1) (V_{CE} = 50 Vdc, P_{out} = 150 W (PEP), I_C = 3.32 Adc)	IMD	—	−35	−32	dB
Electrical Ruggedness (V_{CC} = 50 Vdc, P_{out} = 150 W CW, f = 30 MHz, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTE:
1. To Mil–Std–1311 Version A, Test Method 2204, Two Tone, Reference each Tone.



C1, C2, C7 — 170–780 pF, Arco 469
C3, C8, C9 — 0.1 μF, 100 V Erie
C4 — 500 μF @ 6.0 V
C5 — 9.0–180 pF, Arco 463
C6 — 80–480 pF, Arco 466
C10 — 30 μF, 100 V
R1 — 10 Ω, 10 Watt
R2 — 10 Ω, 1.0 Watt
R3 — 5.0 – 3.3 Ω 1/2 Watt Carbon Resistors in Parallel
CR1 — 1N4997
L1 — 3 Turns, #16 Wire, 5/16″ I.D., 5/16″ Long
L2 — 10 μH Molded Choke
L3 — 12 Turns, #16 Enameled Wire Closewound, 1/4″ I.D.
L4 — 5 Turns, 1/8″ Copper Tubing, 9/16″ I.D., 3/4″ Long
L5 — 10 Ferrite Beads — Ferroxcube #56–590–65/3B

Figure 1. 30 MHz Test Circuit Schematic

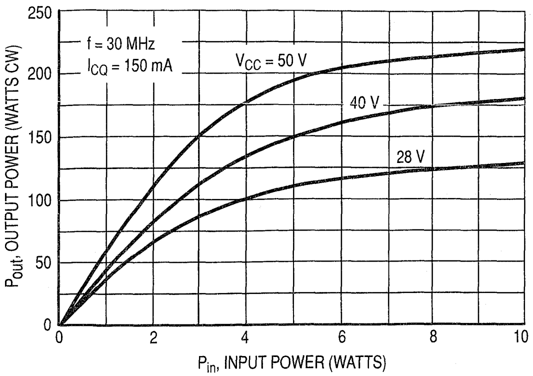


Figure 2. Output Power versus Input Power

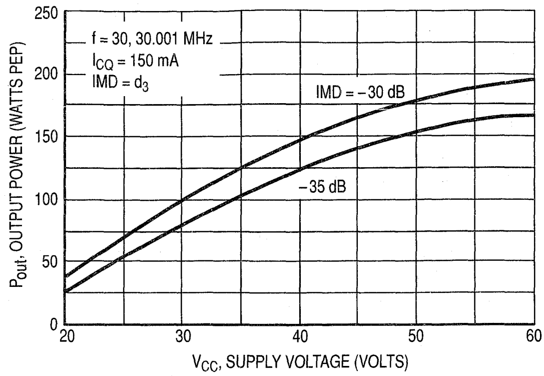


Figure 3. Output Power versus Supply Voltage

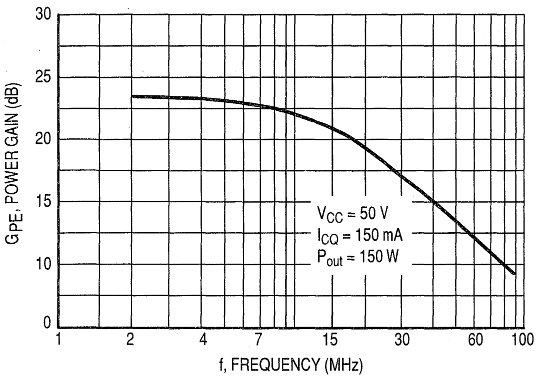


Figure 4. Power Gain versus Frequency

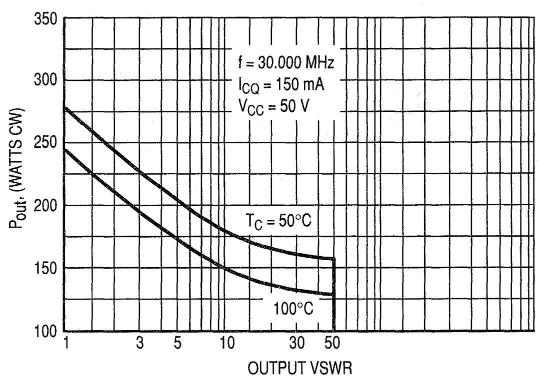


Figure 5. RF Safe Operating Area (SOAR)

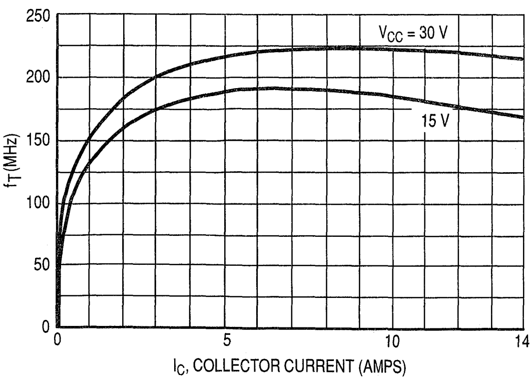


Figure 6. f_T versus Collector Current

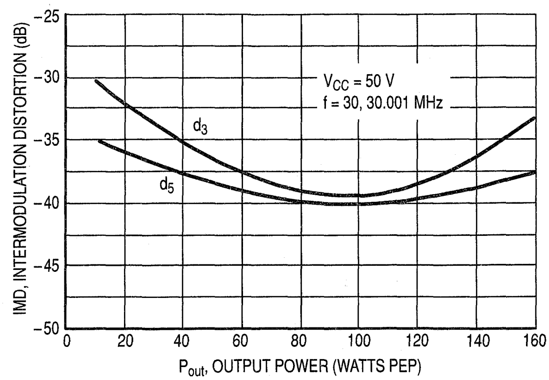


Figure 7. IMD versus P_{out}

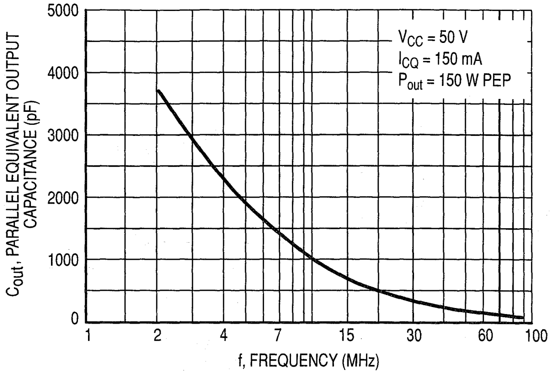


Figure 8. Output Capacitance versus Frequency

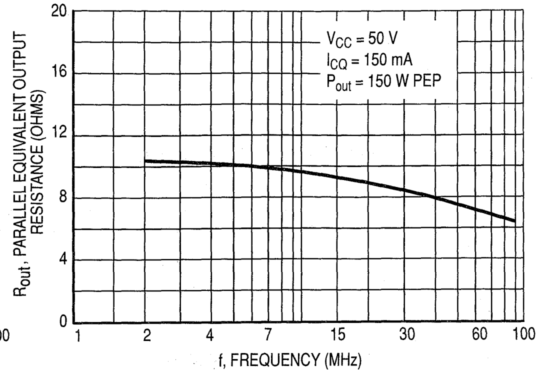
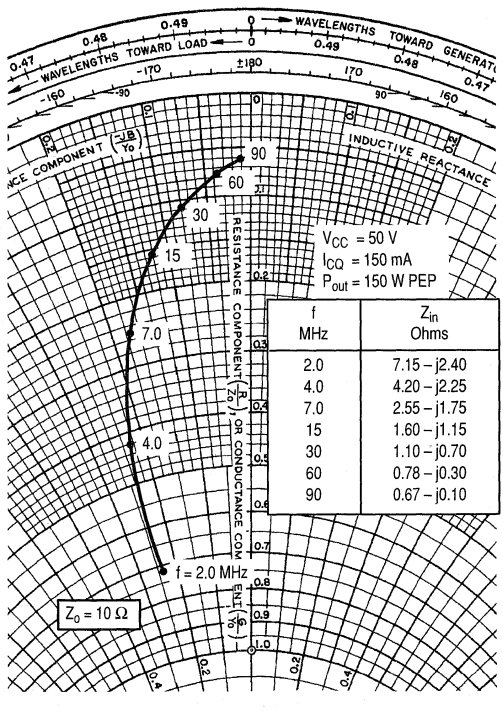


Figure 9. Output Resistance versus Frequency



f MHz	Z_{in} Ohms
2.0	7.15 – j2.40
4.0	4.20 – j2.25
7.0	2.55 – j1.75
15	1.60 – j1.15
30	1.10 – j0.70
60	0.78 – j0.30
90	0.67 – j0.10

Figure 10. Series Equivalent Impedance

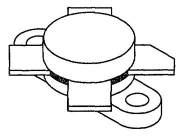
The RF Line
NPN Silicon RF Power Transistor

MRF448

Designed primarily for high–voltage applications as a high–power linear amplifier from 2.0 to 30 MHz. Ideal for marine and base station equipment.

- Specified 50 Volt, 30 MHz Characteristics
  Output Power = 250 W
  Minimum Gain = 12 dB
  Efficiency = 45%
- Intermodulation Distortion @ 250 W (PEP) —
  IMD = −30 dB (Max)
- 100% Tested for Load Mismatch at all Phase Angles with 3:1 VSWR

250 W, 30 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 211–11, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	50	Vdc
Collector–Base Voltage	V_{CBO}	100	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	16	Adc
Withstand Current — 10 s	—	20	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	290 1.67	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	50	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	100	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	100	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc

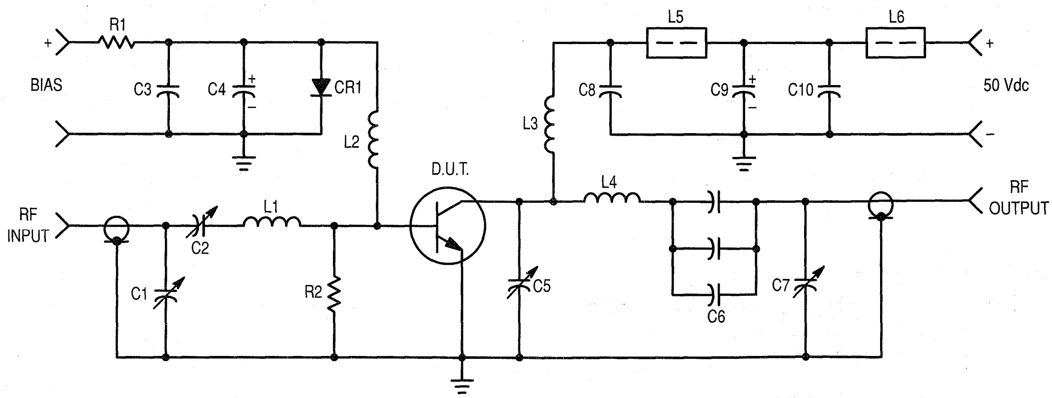
NOTE:
1. P_D is a measurement reflecting short term maximum condition. See SOAR curve for operating conditions.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 10 Vdc)	h_{FE}	10	30	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	350	450	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 250 W CW, f = 30 MHz, I_{CQ} = 250 mA)	G_{PE}	12	14	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 250 W, f = 30 MHz, I_{CQ} = 250 mA)	η	— —	45 65	— —	% (PEP) % (CW)
Intermodulation Distortion (2) (V_{CE} = 50 Vdc, P_{out} = 250 W (PEP), I_{CQ} = 250 mA, f = 30 MHz)	IMD	—	–33	–30	dB
Electrical Ruggedness (V_{CC} = 50 Vdc, P_{out} = 250 W CW, f = 30 MHz, VSWR 3:1 at all Phase Angles)	ψ	No Degradation in Output Power			

NOTE:
2. To Mil–Std–1311 Version A, Test Method 2204, Two Tone, Reference each Tone.



C1, C2, C5, C7 — 170–780 pF, Arco 469
C3, C8, C9 — 0.1 µF, 100 V Erie
C4 — 500 µF @ 6.0 V
C6 — 360 pF, 3 x 120 pF 3.0 kV in parallel
C10 — 10 µF, 100 V
R1 — 10 Ω, 10 Watt
R2 — 10 Ω, 1.0 Watt
CR1 — 1N4997 or equivalent
L1 — 3 Turns, #16 Wire, 0.4″ I.D., 0.3″ Long
L2 — 0.8 µH, Ohmite Z–235 or equivalent
L3 — 12 Turns, #16 Enameled Wire Closewound 0.25″ I.D.
L4 — 4 Turns, 1/8″ Copper Tubing, 0.6″ I.D., 1.0″ Long
L5, L6 — 2.0 µH, Fair–Rite 2643021801 Ferrite bead each or equivalent

Figure 1. 30 MHz Test Circuit Schematic

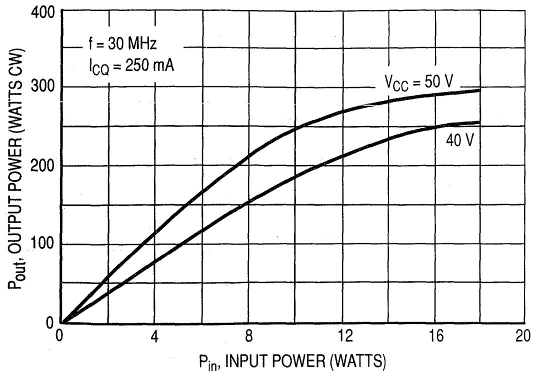


Figure 2. Output Power versus Input Power

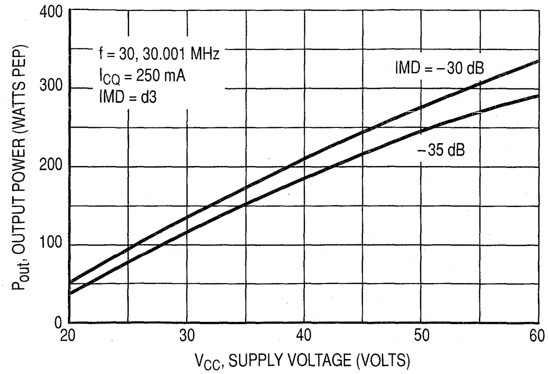


Figure 3. Output Power versus Supply Voltage

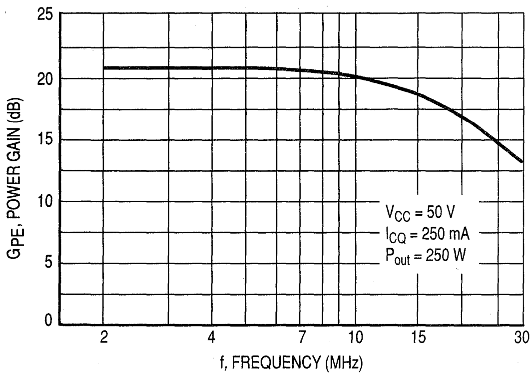


Figure 4. Power Gain versus Frequency

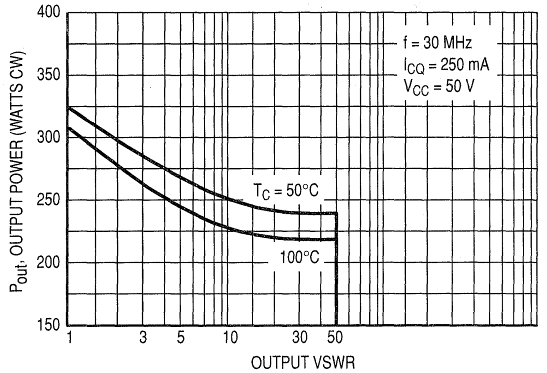


Figure 5. RF SOAR (Class AB) P_{out} versus Output VSWR

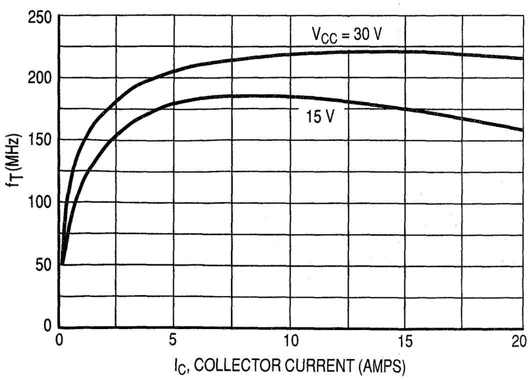


Figure 6. f_T versus Collector Current

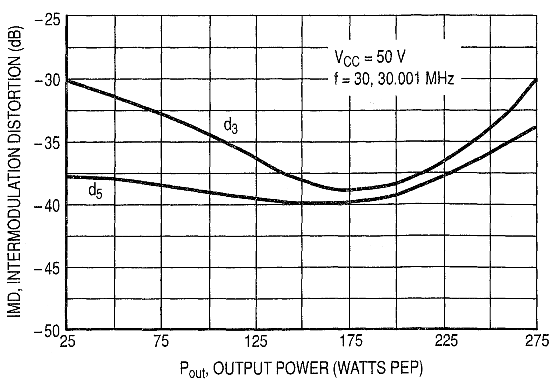


Figure 7. IMD versus P_{out}

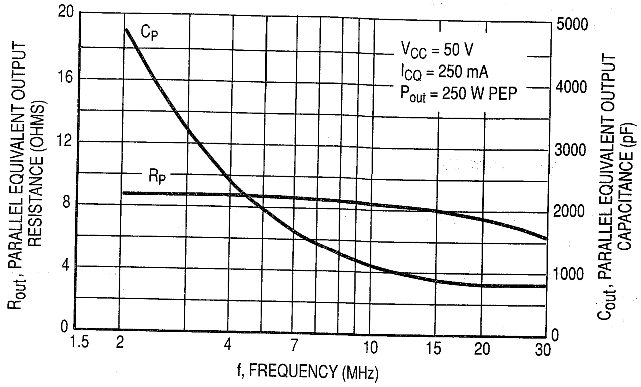
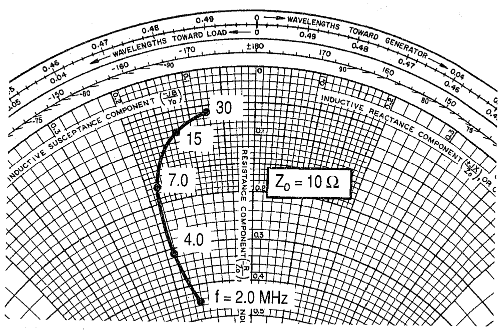


Figure 8. Output Resistance and Capacitance versus Frequency



V_{CC} = 50 V
I_{CQ} = 150 mA
P_{out} = 250 W PEP

f MHz	Z_{in} Ohms
2.0	4.50 – j1.40
4.0	3.10 – j1.80
7.0	1.70 – j1.75
15	0.80 – j1.25
30	0.60 – j0.75

Figure 9. Series Equivalent Impedance

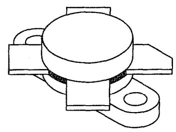
The RF Line
NPN Silicon
RF Power Transistor

MRF454

Designed for power amplifier applications in industrial, commercial and amateur radio equipment to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics —
  Output Power = 80 Watts
  Minimum Gain = 12 dB
  Efficiency = 50%

80 W, 30 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 211–11, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Collector–Base Voltage	V_{CBO}	45	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	20	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

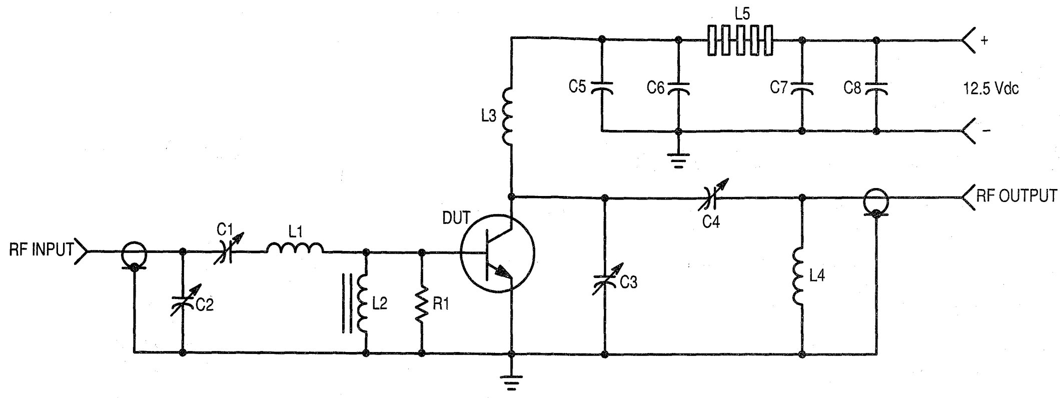
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	—	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	250	pF
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	G_{pe}	12	—	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	η	50	—	—	%
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	Z_{in}	—	.938–j.341	—	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	Z_{out}	—	1.16–j.201	—	Ohms
Parallel Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	—	—	1.06 Ω 1817 pF	—	—
Parallel Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	—	—	1.19 Ω 777 pF	—	—

REV 1



C1, C2, C4 — ARCO 469	L1 — 3 Turns, #18 AWG, 5/16″ I.D., 5/16″ Long
C3 — ARCO 466	L2 — VK200–20/4B, FERROXCUBE
C5 — 1000 pF, UNELCO	L3 — 12 Turns, #18 AWG Enameled Wire, 1/4″ I.D., Close Wound
C6, C7 — 0.1 μF Disc Ceramic	L4 — 3 Turns 1/8″ O.D. Copper Tubing, 3/8″ I.D., 3/4″ Long
C8 — 1000 μF/15 V Electrolytic	L5 — 7 FERRITE Beads, FERROXCUBE #56–590–65/3B
R1 — 10 Ohm/1.0 Watt, Carbon	

Figure 1. 30 MHz Test Circuit Schematic

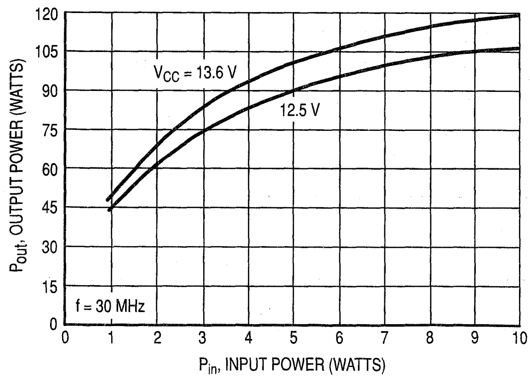


Figure 2. Output Power versus Input Power

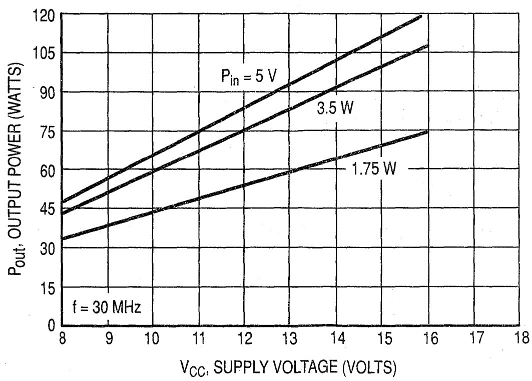


Figure 3. Output Power versus Supply Voltage

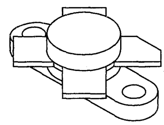
The RF Line
NPN Silicon RF Power Transistor

MRF455

. . . designed for power amplifier applications in industrial, commercial and amateur radio equipment to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics —
  Output Power = 60 Watts
  Minimum Gain = 13 dB
  Efficiency = 55%

60 W, 30 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 211–07, STYLE 1

MATCHING PROCEDURE

In the push–pull circuit configuration it is preferred that the transistors are used as matched pairs to obtain optimum performance.

The matching procedure used by Motorola consists of measuring h_{FE} at the data sheet conditions and color coding the device to predetermined h_{FE} ranges within the normal h_{FE} limits. A color dot is added to the marking on top of the cap. Any two devices with the same color dot can be paired together to form a matched set of units.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	18	Vdc
Collector–Emitter Voltage	V_{CES}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	175 1.0	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

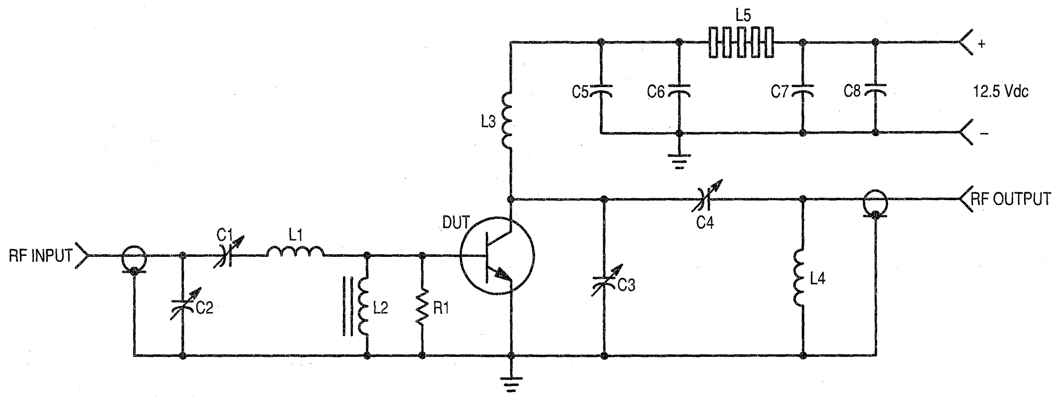
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	250	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	G_{pe}	13	—	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	η	55	—	—	%
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{in}	—	1.66–j.844	—	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{out}	—	1.73–j.188	—	Ohms
Parallel Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{in}	—	2.09/1030	—	Ω/pF
Parallel Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{out}	—	1.75/330	—	Ω/pF



C1, C2, C4 — ARCO 469
C3 — ARCO 466
C5 — 1000 pF, UNELCO
C6, C7 — 0.1 μF Disc Ceramic
C8 — 1000 μF/15 V Electrolytic
R1 — 10 Ohm/1.0 Watt, Carbon

L1 — 3 Turns, #18 AWG, 5/16″ I.D., 5/16″ Long
L2 — VK200–20/4B, FERROXCUBE
L3 — 12 Turns, #18 AWG Enameled Wire, 1/4″ I.D., Close Wound
L4 — 3 Turns 1/8″ O.D. Copper Tubing, 3/8″ I.D., 3/4″ Long
L5 — 7 FERRITE Beads, FERROXCUBE #56–590–65/3B

Figure 1. 30 MHz Test Circuit Schematic

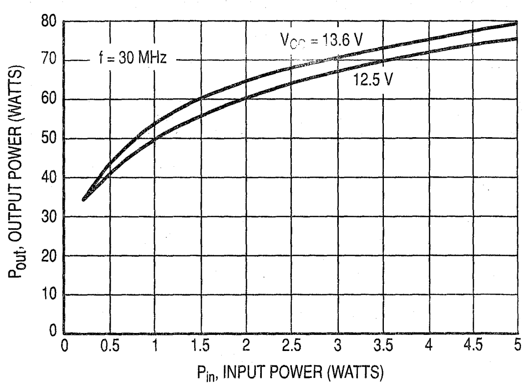


Figure 2. Output Power versus Input Power

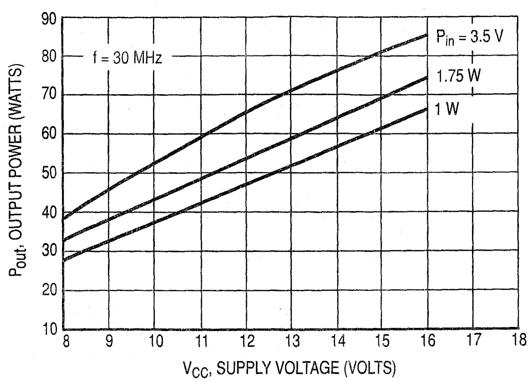


Figure 3. Output Power versus Supply Voltage

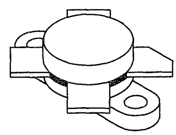
The RF Line
NPN Silicon RF Power Transistor

MRF492

Designed for 12.5 volt low band VHF large–signal power amplifier applications in commercial and industrial FM equipment.

- Specified 12.5 V, 50 MHz Characteristics —
  Output Power = 70 W
  Minimum Gain = 11 dB
  Efficiency = 50%
- Load Mismatch Capability at High Line and RF Overdrive

70 W, 50 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 211–11, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	18	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	20	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

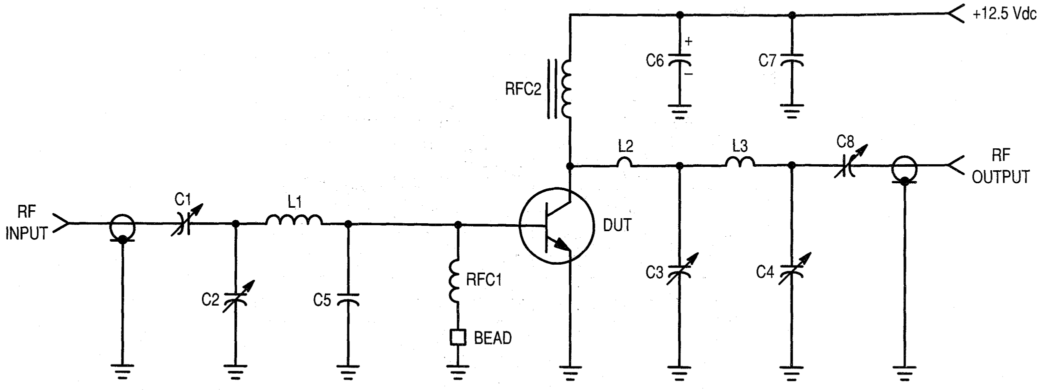
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 13.6 Vdc, V_{BE} = 0)	I_{CES}	—	—	20	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	275	450	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 70 W, f = 50 MHz)	G_{PE}	11	13	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 70 W, f = 50 MHz)	η	50	—	—	%

NOTES:
1. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



C1, C8 — 9.0–180 pF, Arco 463
C2, C3, C4 — 80–480 pF, Arco 466
C5 — 1000 pF, 350 V, Unelco
C6 — 10 µF, 25 Vdc
C7 — 0.01 µF, Ceramic
RFC1 — 10 µH Molded Choke
RFC2 — 12 Turns, #16 AWG, Enameled Wire Closewound on a 2.0 W Carbon Resistor
L1 — 2 Turns, #18 AWG Enameled Wire, 0.4″ ID, 0.15″ Long
L2 — Loop, #12 AWG Wire, 0.6″ High, 0.4″ Wide
L3 — 2 Turns, #12 AWG Wire, ID 0.4″, 0.25″ Long
Bead — Ferrite Bead Ferroxcube #56–590–65/3B

Figure 1. 50 MHz Test Circuit

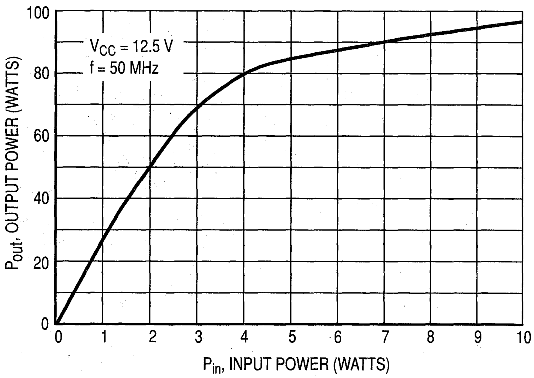


Figure 2. Output Power versus Input Power

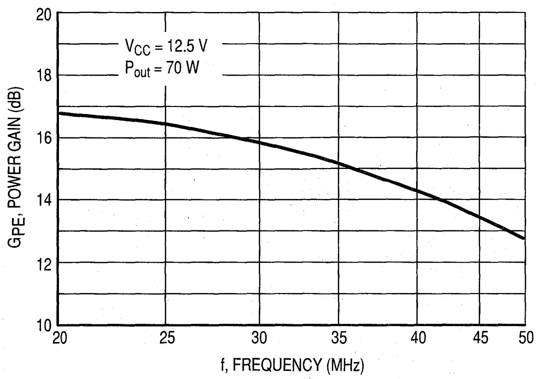


Figure 3. Power Gain versus Frequency

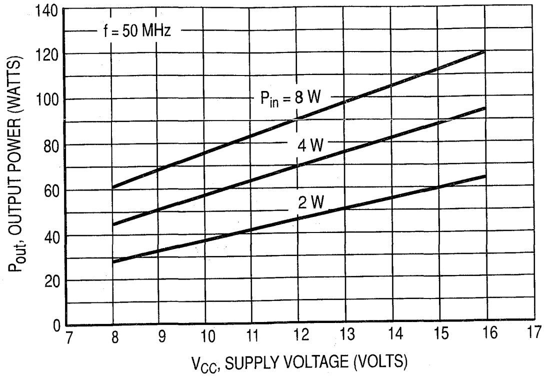
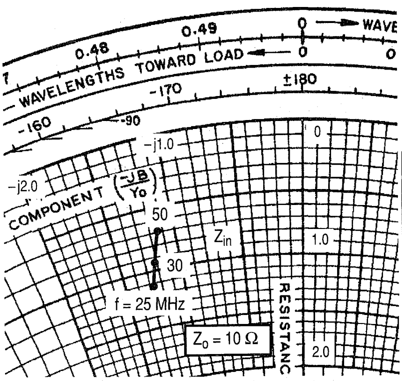


Figure 4. Output Power versus Supply Voltage



V_{CC} = 12.5 V, P_{out} = 70 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
25	1.12 – j1.28	0.85 – j1.46
30	0.93 – j1.24	0.76 – j1.3
50	0.7 – j1.17	0.58 – j1.0

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

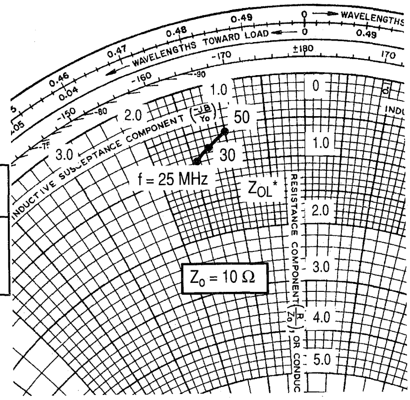


Figure 5. Series Equivalent Input/Output Impedances

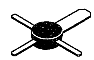
The RF Line
NPN Silicon
RF Low Power Transistor

MRF553

Designed primarily for wideband large signal predriver stages in the VHF frequency range.

- Specified @ 12.5 V, 175 MHz Characteristics
  Output Power = 1.5 W
  Minimum Gain = 11.5 dB
  Efficiency 60% (Typ)
- Cost Effective PowerMacro Package
- Electroless Tin Plated Leads for Improved Solderability
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**1.5 W, 175 MHz
RF LOW POWER
TRANSISTOR
NPN SILICON**



CASE 317D–02, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Device Dissipation @ T_C = 75°C (1, 2) Derate above 75°C	P_D	3.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	—	200	—

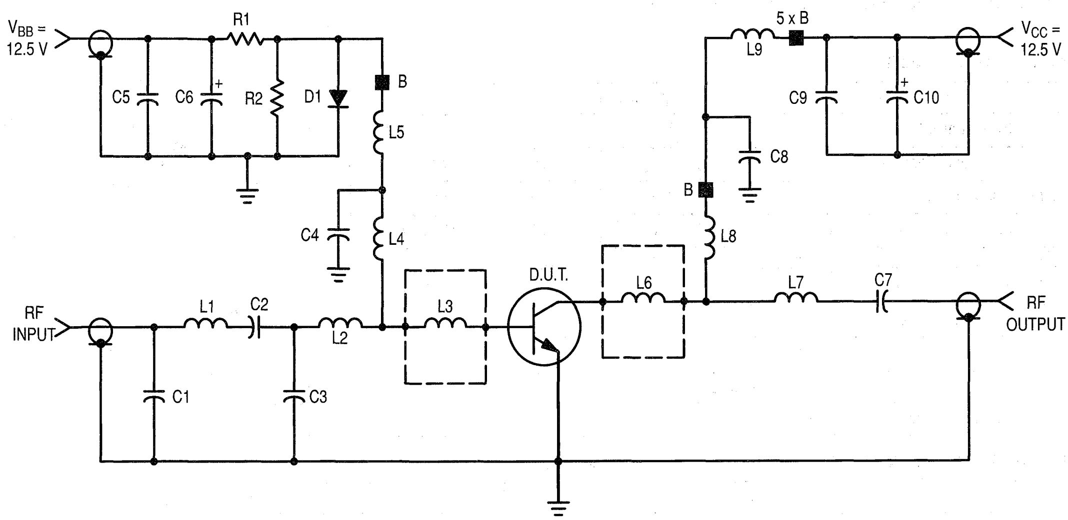
NOTES:
1. T_C, Case temperature measured on collector lead immediately adjacent to body of package.
2. The MRF553 PowerMacro must be properly mounted for reliable operation. AN938, “Mounting Techniques in PowerMacro Transistor,” discusses methods of mounting and heatsinking.

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	12	20	pF
FUNCTIONAL TESTS						
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 175 MHz)	Figures 1, 2	G_{pe}	11.5	13	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 175 MHz)	Figures 1, 2	η	50	60	—	%
Load Mismatch Stress (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 175 MHz, VSWR ≥ 10:1 All Phase Angles)		ψ	No Degradation in Output Power			—



C1 — 36 pF Mini Underwood
C2 — 47 pF Mini Underwood
C3 — 91 pF Mini Underwood
C4 — 68 pF Mini Underwood
C5, C9 — 1.0 μF Erie Red Cap Capacitor
C6, C10 — 0.1 μF, 35 V Tantulum
C7 — 470 pF Chip Capacitor
C8 — 2200 pF Chip Capacitor
R1 — 4.7 kΩ, 1/4 W
R2 — 100 Ω, 1/4 W
D1 — 1N4148 Diode

L1 — 3 Turns, #18 AWG, 0.210″ ID, 3/16″ Length
L2, L4, L7 — 0.62″, #18 AWG Wire Bent into “V”
L3, L6 — 60 x 125 x 250 Mils Copper Pad on 27 Mils Thick Alumina Substrate
L5 — 12 μH Molded Choke
L8 — 7 Turns, #18 AWG, 0.170″ ID, 7/16″ Length
L9 — 1.0″, #18 AWG Wire with 5 Ferrite Beads
B — Ferrite Bead
Board Material — Glass Teflon, ε_r = 2.56, t = 0.0625″

Figure 1. 140–175 MHz Broadband Circuit Schematic

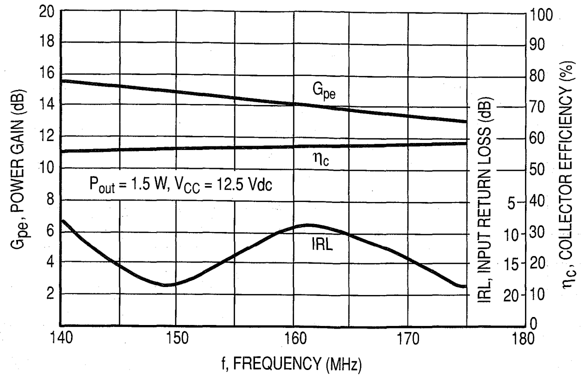


Figure 2. Typical Performance in Broadband Circuit

f Frequency MHz	Z_{in} Ohms						Z_{OL}* Ohms					
	V_{CC} = 7.5 V; P_{in}			V_{CC} = 12.5 V; P_{in}			V_{CC} = 7.5 V; P_{out}			V_{CC} = 12.5 V; P_{out}		
	100 mW	200 mW	300 mW	50 mW	100 mW	150 mW	1.0 W	1.6 W	2.2 W	1.1 W	2.0 W	2.6 W
140	1.65–j3.6	2.0–j2.6	2.3–j1.2	1.7–j4.1	1.8–j3.1	1.9–j2.7	9.9–j11.1	10.6–j5.1	10–j4.9	28.3–j21.5	16–j20.5	16.3–j16.5
175	2.5–j5.6	2.3–j5.9	2.8–j4.0	2.3–j4.6	2.4–j1.2	2.4–j5.7	12.1–j14.9	7.2–j9.8	8.1–j5.4	30.8–j23.3	11.4–j20.9	11.1–j14.3

f Frequency MHz	Z_{in} Ohms						Z_{OL}* Ohms					
	V_{CC} = 7.5 V; P_{in}			V_{CC} = 12.5 V; P_{in}			V_{CC} = 7.5 V; P_{out}			V_{CC} = 12.5 V; P_{out}		
	50 mW	100 mW	200 mW	25 mW	50 mW	100 mW	1.25 W	1.5 W	2.0 W	1.5 W	2.25 W	3.0 W
90	2.5–j9.3	2.5–j6.4	2.5–j4.4	1.6–j10.7	2.5–j7.1	2.2–j1.3	31.8–j9.2	32–j8.9	30.2–j10.7	45.8–j7.2	45.2–j3.9	40–j4.5

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Table 1. Z_{in} and Z_{OL} versus Collector Voltage, Input Power, and Output Power

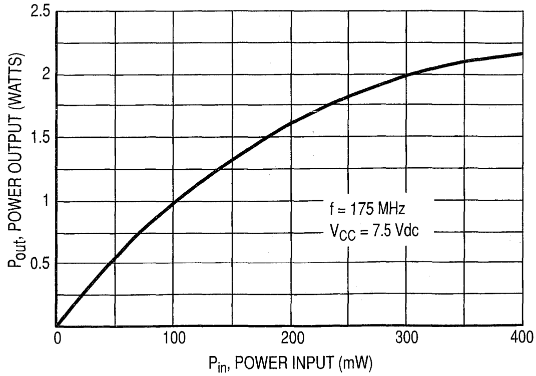


Figure 3. Power Output versus Power Input

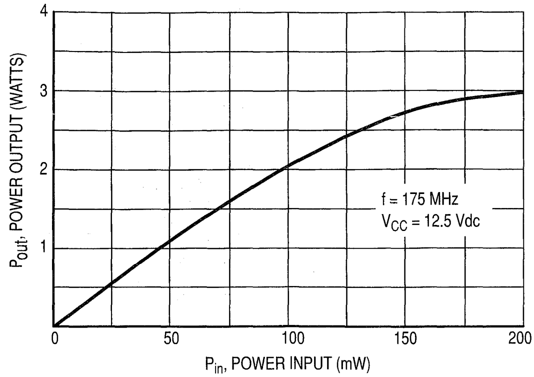


Figure 4. Power Output versus Power Input

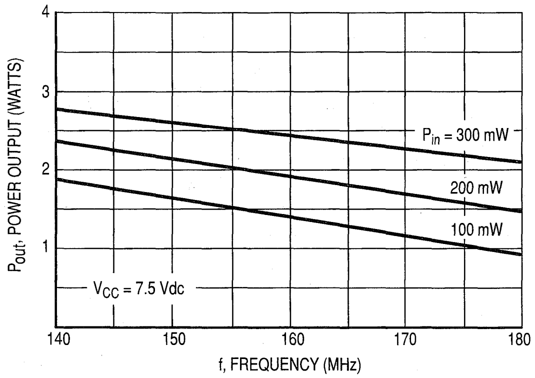


Figure 5. Power Output versus Frequency

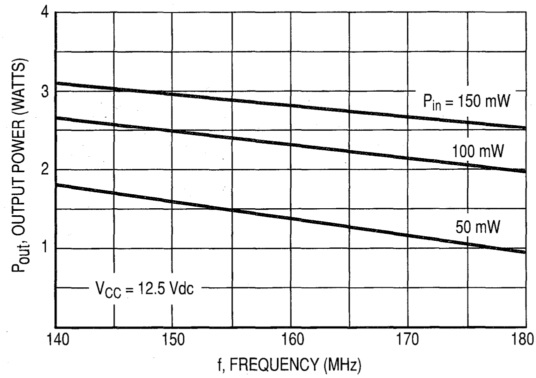


Figure 6. Power Output versus Frequency

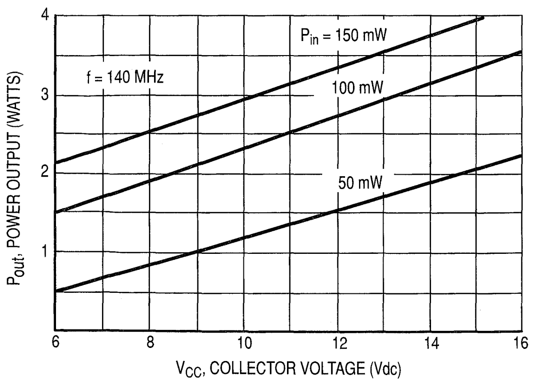


Figure 7. Power Output versus Collector Voltage

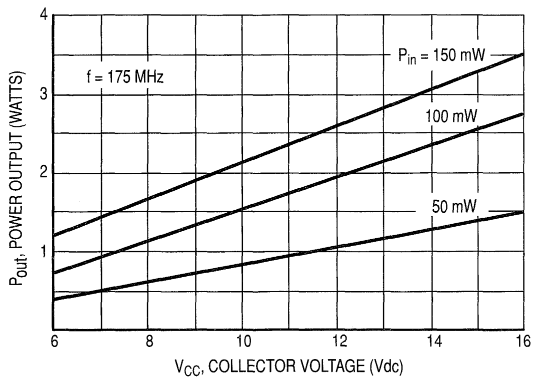


Figure 8. Power Output versus Collector Voltage

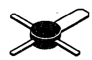
The RF Line
NPN Silicon RF Low Power Transistor

MRF555

Designed primarily for wideband large signal predriver stages in the UHF frequency range.

- Specified @ 12.5 V, 470 MHz Characteristics @ P_{out} = 1.5 W
  Common Emitter Power Gain = 12.5 dB (Typ)
  Efficiency 60% (Typ)
- Cost Effective PowerMacro Package
- Electroless Tin Plated Leads for Improved Solderability
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

1.5 W, 470 MHz
RF LOW POWER
TRANSISTOR
NPN SILICON



CASE 317D–02, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	400	mAdc
Operating Junction Temperature	T_J	150	°C
Total Device Dissipation @ T_C = 75°C (1, 2) Derate above 75°C	P_D	3.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	50	90	200	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.5	5.0	pF

NOTES:

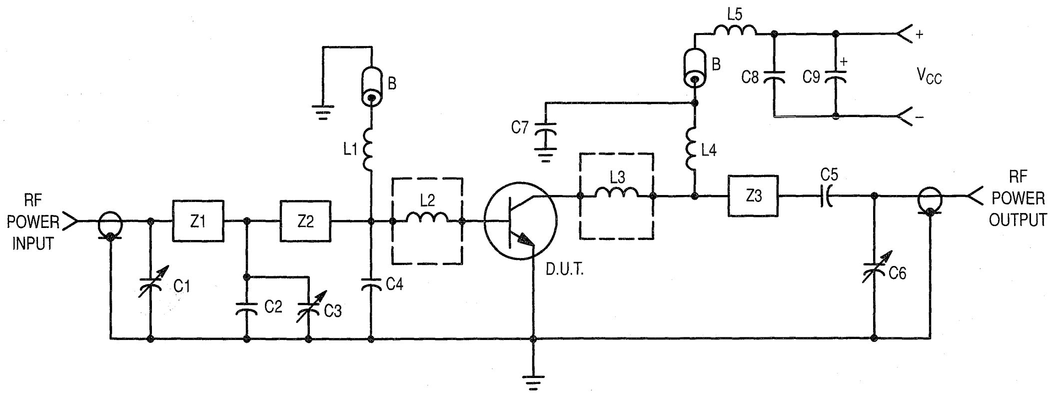
(continued)

1. T_C, Case temperature measured on collector lead immediately adjacent to body of package.
2. The MRF555 PowerMacro must be properly mounted for reliable operation. AN938, "Mounting Techniques in PowerMacro Transistor," discusses methods of mounting and heatsinking.

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (f = 470 MHz)					
Common–Emitter Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W)	G_{pe}	11	12.5	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W)	η_c	50	60	—	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 125 mW, VSWR ≥ 10:1 all phase angles)	ψ	No Degradation in Output Power			



*C1, C3, C6 — 0.8–11 pF Johanson
C2 — 15 pF Clamped Mica, Mini–Underwood
C4 — 36 pF Clamped Mica, Mini–Underwood
C5 — 470 pF Ceramic Chip Capacitor
C7 — 91 pF Clamped Mica, Mini–Underwood
C8 — 68 pF Clamped Mica, Mini–Underwood
C9 — 1.0 µF, 25 V Tantalum
B — Bead, Ferroxcube 56–590–65/3B

*Fixed tuned for broadband response

L1 — 5 Turns #21 AWG, 5/32″ I.D.
L2, L3 — 60 x 125 x 250 Mils Copper Pad on 27 Mil Thick Alumina Substrate
L4, L5 — 7 Turns #21 AWG 5/32″ I.D.
Z1 — 1.29″ x 0.16″ Microstrip
Z2 — 0.70″ x 0.16″ Microstrip
Z3 — 2.18″ x 0.16″ Microstrip

PCB — 1/16″ Glass Teflon, 1 oz. cu. clad, double sided, ε_r = 2.5

Figure 1. 400–512 MHz Broadband Circuit

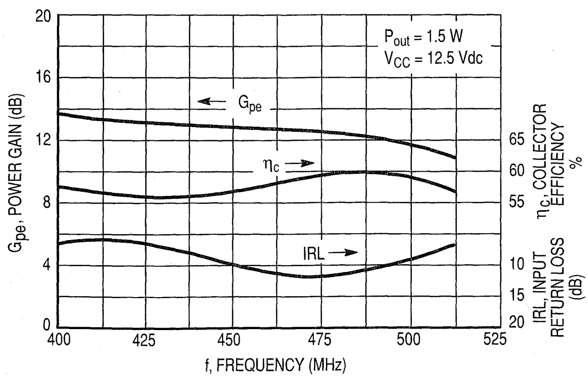


Figure 2. Performance in Broadband Circuit

f Frequency MHz	Z_{in} Ohms		Z_{OL}* Ohms	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 100 mW	P_{in} = 50 mW	P_{out} 400 MHz = 1.5 W P_{out} 450 MHz = 1.35 W P_{out} 512 MHz = 1.05 W	P_{out} 400 MHz = 1.9 W P_{out} 450 MHz = 1.45 W P_{out} 512 MHz = 0.9 W
400	2.9 – j2.7	1.9 – j3.1	18.0 – j13.4	12.2 – j19.7
450	2.2 – j0.8	2.6 – j4.0	21.6 = j9.9	20.2 – j18.6
512	3.5 – j1.2	2.6 – j2.6	20.1 – j1.0	23.4 – j23.0

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Table 1. Z_{in} and Z_{OL} versus Collector Voltage, Input Power and Output Power

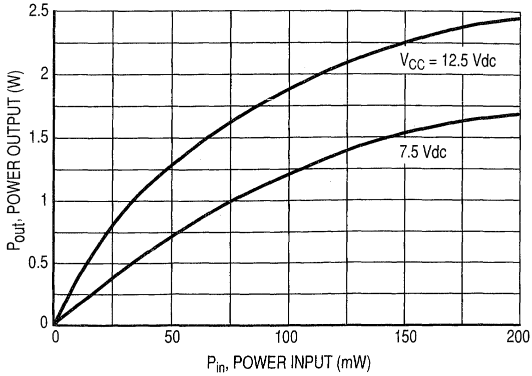


Figure 3. Power Output versus Power Input

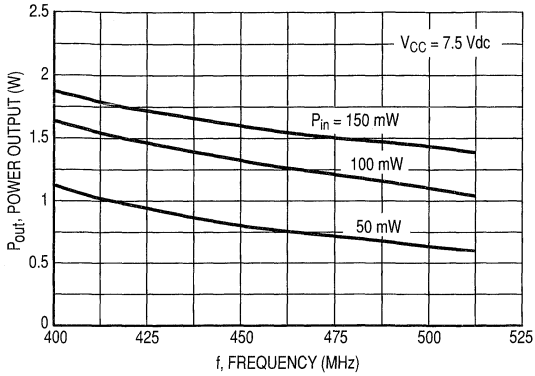


Figure 4. Power Output versus Frequency

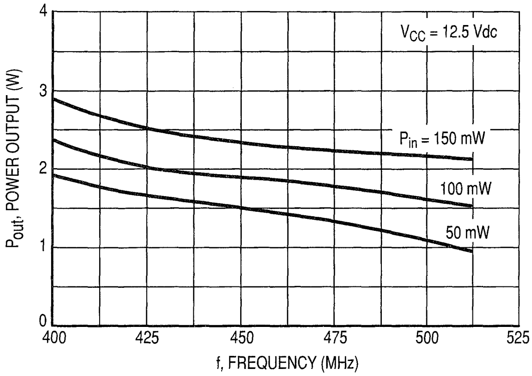


Figure 5. Power Output versus Frequency

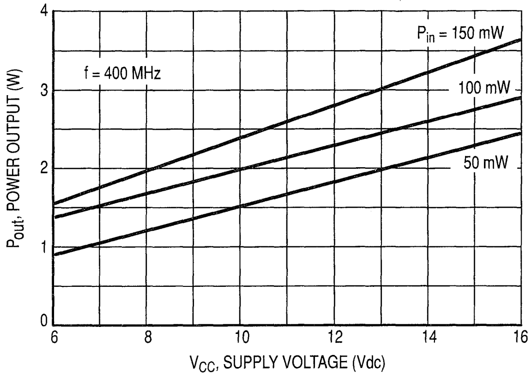


Figure 6. Power Output versus Supply Voltage

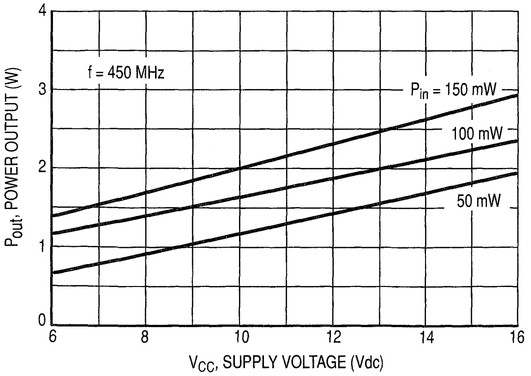


Figure 7. Power Output versus Supply Voltage

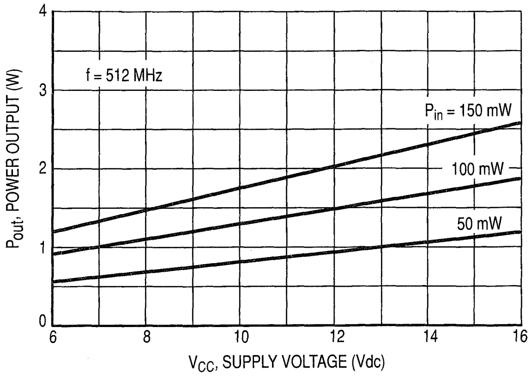


Figure 8. Power Output versus Supply Voltage

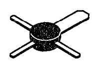
The RF Line
NPN Silicon RF Low Power Transistor

MRF557

1.5 W, 870 MHz
RF LOW POWER TRANSISTOR
NPN SILICON

Designed primarily for wideband large signal predriver stages in the 800 MHz frequency range.

- Specified @ 12.5 V, 870 MHz Characteristics
  Output Power = 1.5 W
  Minimum Gain = 8.0 dB
  Efficiency 60% (Typ)
- Cost Effective PowerMacro Package
- Electroless Tin Plated Leads for Improved Solderability
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 317D–02, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	400	mAdc
Total Device Dissipation @ T_C = 75°C (1, 2) Derate above 75°C	P_D	3.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	50	90	200	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.5	5.0	pF

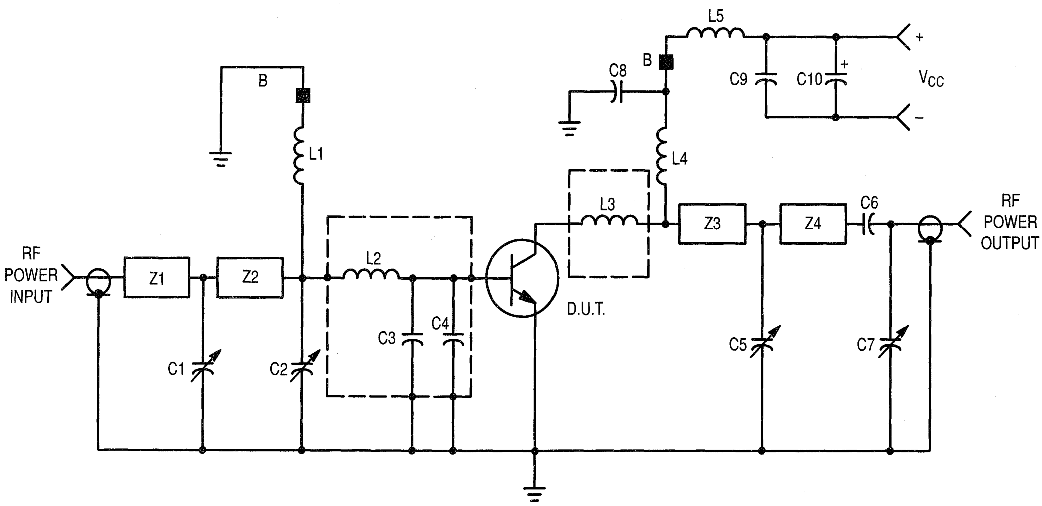
NOTES:
1. T_C, Case temperature measured on collector lead immediately adjacent to body of package.
2. The MRF557 PowerMacro must be properly mounted for reliable operation. AN938, "Mounting Techniques in PowerMacro Transistor," discusses methods of mounting and heatsinking.

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS						
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 870 MHz)	Figures 1, 2	G_{pe}	8.0	9.0	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 870 MHz)	Figures 1, 2	η_c	55	60	—	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 225 mW, f = 870 MHz, VSWR ≥ 10:1 all phase angles)	Figures 1, 2	ψ	No Degradation in Output Power			



C1, C2, C5, C7 — 0.8–8.0 pF Johanson Gigatrim*
C3, C4 — 15 pF Clamped Mica, Mini–Underwood
C6 — 27 pF Clamped Mica, Mini–Underwood
C8 — 91 pF Clamped Mica, Mini–Underwood
C9 — 68 pF Clamped Mica, Mini–Underwood
C10 — 1.0 µF, 25 V Tantalum
B — Bead, Ferroxcube 56–590–65/3B
PCB — 1/16″ Glass Teflon, ε_r = 2.56

*Fixed tuned for broadband response.

L1, L4 — 5 Turns #21 AWG, 5/32″ ID
L2, L3 — 60 x 125 x 250 Mils Copper Tab on 27 Mil Thick Alumina Substrate
L5 — 7 Turns #21 AWG, 5/32″ ID
Z1 — 1.65 x 0.163″ Microstrip, Z_o = 50 Ω
Z2 — 0.85 x 0.163″ Microstrip, Z_o = 50 Ω
Z3 — 0.625 x 0.163″ Microstrip, Z_o = 50 Ω
Z4 — 1.35 x 0.163″ Microstrip, Z_o = 50 Ω

Figure 1. 800–880 MHz Broadband Circuit

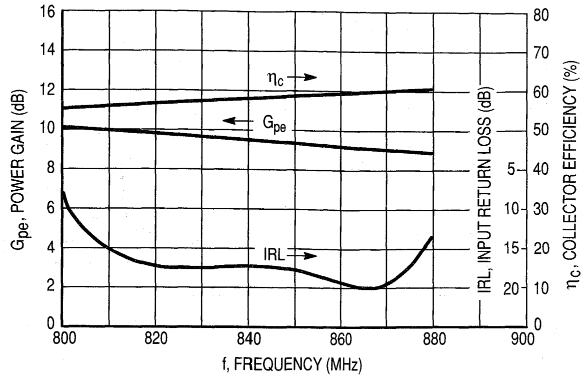


Figure 2. Performance in Broadband Circuit

f Frequency MHz	Z_{in} Ohms		Z_{OL}* Ohms	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 300 mW	P_{in} = 200 mW	P_{out} 806 MHz = 1.7 W P_{out} 870 MHz = 1.4 W P_{out} 960 MHz = 1.0 W	P_{out} 806 MHz = 2.1 W P_{out} 870 MHz = 1.8 W P_{out} 960 MHz = 1.1 W
806	2.4 + j3.9	2.4 + j3.1	14.7 – j4.4	13.6 – j12.8
870	2.5 + j4.6	2.7 + j3.7	17.2 – j8.6	16 – j13.2
960	6.1 + j7.4	6.8 + j8.3	40 – j8.3	38 – j10.5

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Table 1. Z_{in} and Z_{OL} versus Collector Voltage, Input Power and Output Power

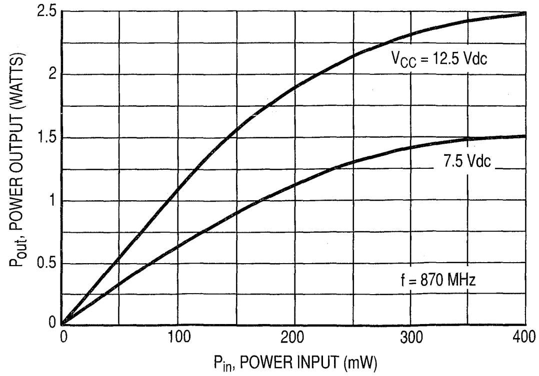


Figure 3. Power Output versus Power Input

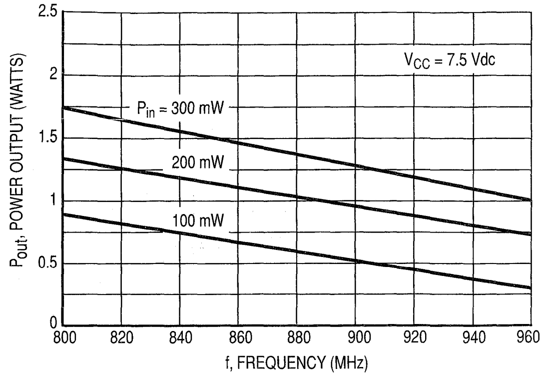


Figure 4. Power Output versus Frequency

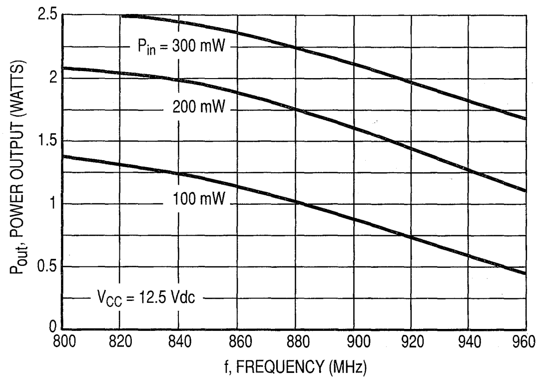


Figure 5. Power Output versus Frequency

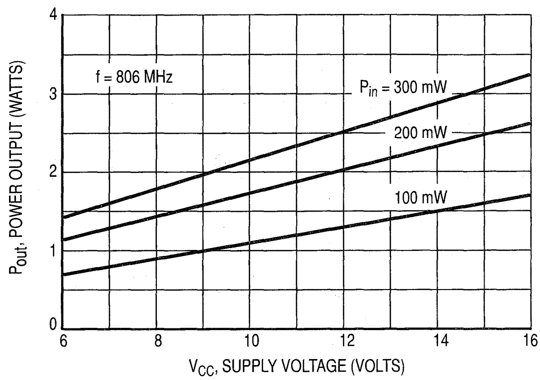


Figure 6. Power Output versus Supply Voltage

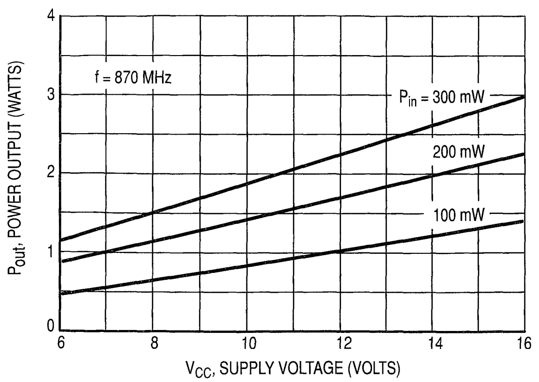


Figure 7. Power Output versus Supply Voltage

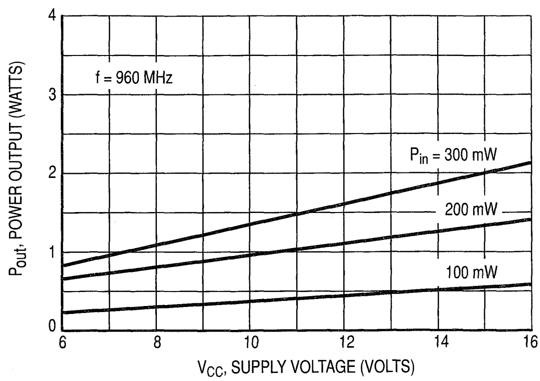


Figure 8. Power Output versus Supply Voltage

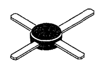
The RF Line
NPN Silicon High-Frequency Transistor

MRF559

. . . designed for UHF linear and large–signal amplifier applications.

- Specified 12.5 Volt, 870 MHz Characteristics —
  Output Power = 0.5 Watts
  Minimum Gain = 8.0 dB
  Efficiency 50%
- S Parameter Data From 250 MHz to 1.5 GHz
- 1.0 dB Compression > +20 dBm Typ
- Ideally Suited for Broadband, Class A, Low–Noise Applications
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

0.5 W, 870 MHz
HIGH–FREQUENCY
TRANSISTOR
NPN SILICON



CASE 317–01, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	150	mAdc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	2.0 20	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0)	I_{CES}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	90	200	—
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 200 MHz)	f_T	—	3000	—	MHz
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	2.0	2.5	pF

(continued)

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS						
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 0.5 W)	f = 870 MHz f = 512 MHz	G_{PE}	8.0 —	9.5 13	— —	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 0.5 W)	f = 870 MHz f = 512 MHz	η	50 —	65 60	— —	%
TYPICAL PERFORMANCE @ V_{CC} = 7.5 V						
Common–Emitter Amplifier Power Gain (V_{CC} = 7.5 Vdc, P_{out} = 0.5 W)	f = 870 MHz f = 512 MHz	G_{PE}	— —	6.5 10	— —	dB
Collector Efficiency (V_{CC} = 7.5 Vdc, P_{out} = 0.5 W)	f = 870 MHz f = 512 MHz	η	— —	70 65	— —	%

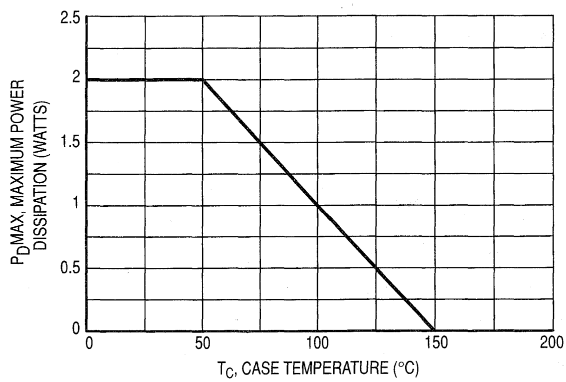
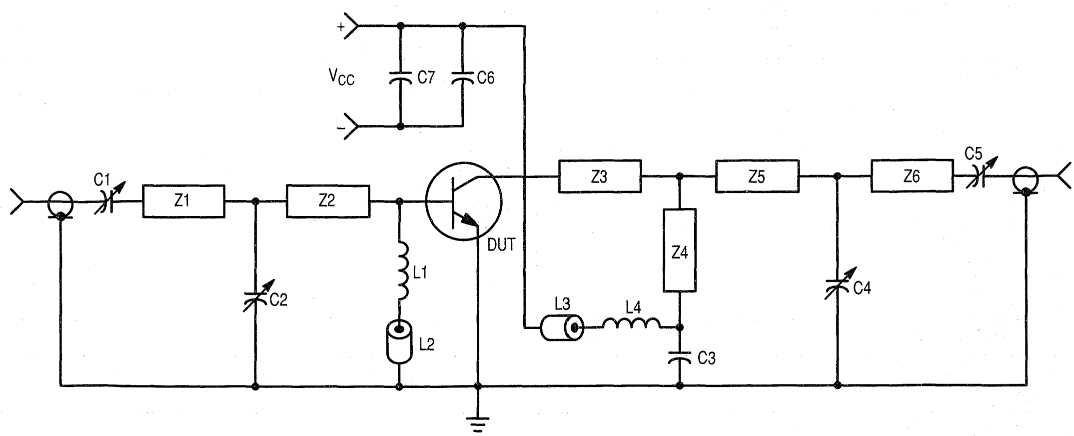


Figure 1. Power Dissipation



C1, C2, C4, C5 — 1.0–10 pF Johanson
C3, C6 — 0.001 μF Chip Capacitor
C7 — 1.0 μF Tantalum
L1, L4 — 4 Turns #26 AWG, 0.3 cm ID, 0.4 cm Long
L2, L3 — Ferrite Bead
Microstrip Elements — ε_r = 2.55

Z1 — 50 Ω 1.5 cm
Z2 — 30 Ω 2.5 cm
Z3 — 50 Ω 2.0 cm
Z4 — 50 Ω 1.2 cm
Z5, Z6 — 50 Ω 1.25 cm

Figure 2. 870 MHz Test Fixture

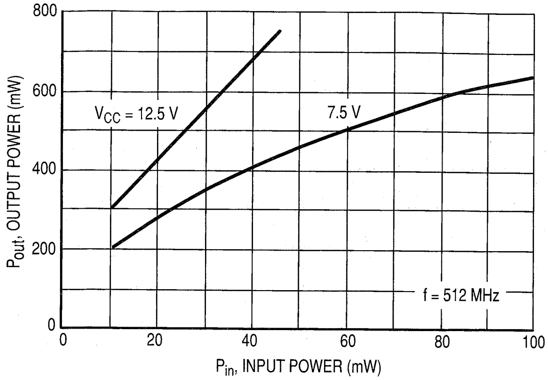


Figure 3. Output Power versus Input Power

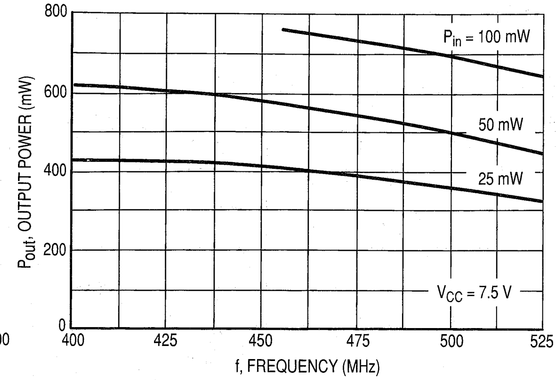


Figure 4. Output Power versus Frequency

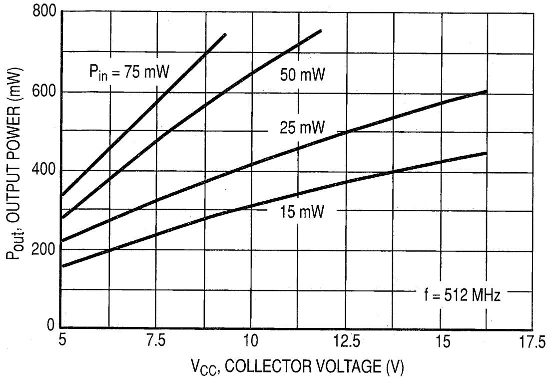


Figure 5. Output Power versus Collector Voltage

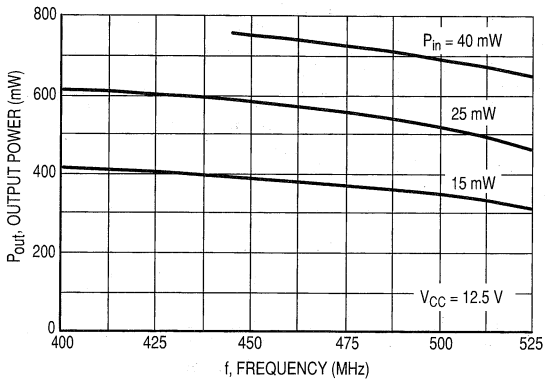


Figure 6. Output Power versus Frequency

f Frequency MHz	Z_{in} Ohms			Z_{OL}* Ohms					
	V_{CC} = 7.5–12.5 V			V_{CC} = 7.5 V			V_{CC} = 12.5 V		
	15 mW	25 mW	50 mW	0.25 W	0.5 W	0.75 W	0.25 W	0.5 W	0.75 W
400	4.3 – j13.3	4.9 – j11.0	5.7 – j8.7	31 – j49	44 – j34	42 – j4.9	20 – j68	42 – j60	52 – j54
440	3.9 – j8.8	4.5 – j8.7	5.4 – j6.9	27 – j42	39 – j30	40 – j6.9	19 – j62	37 – j54	49 – j50
480	3.5 – j4.4	4.1 – j6.5	5.0 – j4.3	24 – j36	36 – j25	39 – j9.0	18 – j56	33 – j48	47 – j46
520	3.2 – j2.2	3.8 – j4.3	4.7 – j1.7	22 – j30	34 – j20	37 – j12	17 – j52	31 – j44	47 – j42

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Table 1. Z_{in} and Z_{OL} versus Collector Voltage, Input Power, and Output Power

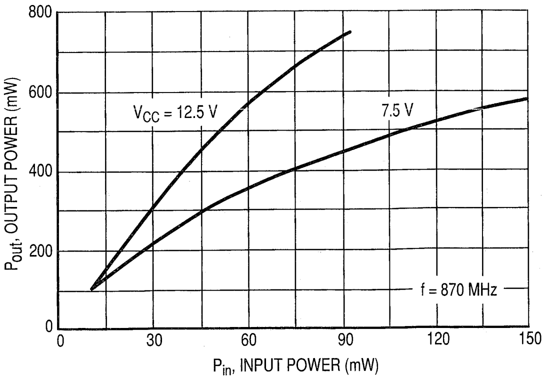


Figure 7. Output Power versus Input Power

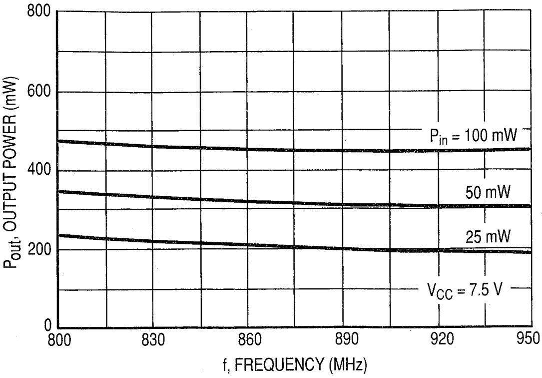


Figure 8. Output Power versus Frequency

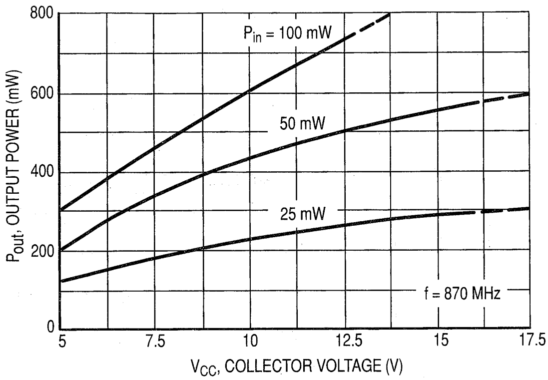


Figure 9. Output Power versus Collector Voltage

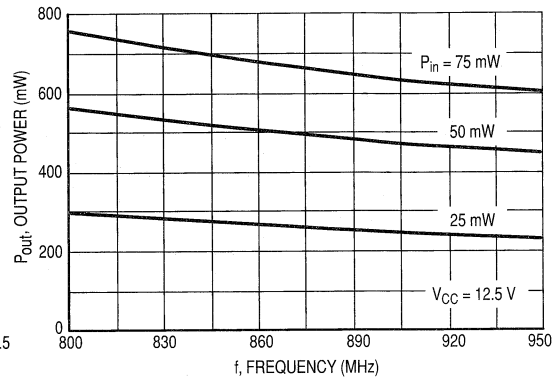


Figure 10. Output Power versus Frequency

f Frequency MHz	Z_{in} Ohms			Z_{OL}* Ohms					
	V_{CC} = 7.5–12.5 V			V_{CC} = 7.5 V			V_{CC} = 12.5 V		
	25 mW	50 mW	100 mW	0.25 W	0.5 W	0.75 W	0.25 W	0.5 W	0.75 W
800	2.9 + j2.2	3.8 + j4.4	4.7 + j6.5	15.0 – j36.8	22.7 – j30.6	27.1 – j22.6	14.6 – j43.6	17.2 – j39.7	23.4 – j37.7
850	3.2 + j3.5	3.8 + j5.2	4.8 + j7.4	15.7 – j35.3	23.9 – j28.7	27.3 – j21.5	16.3 – j40.8	17.8 – j39.5	23.7 – j36.8
900	3.8 + j5.7	4.4 + j7.0	5.4 + j8.7	16.4 – j33.7	25.1 – j27.0	27.5 – j20.5	17.3 – j38.2	18.3 – j39.3	23.9 – j36.0
950	4.1 + j7.4	4.5 + j8.8	5.5 + j10.1	17.0 – j32.2	26.3 – j25.2	27.6 – j19.4	17.2 – j36.1	20.1 – j38.5	24.5 – j35.6

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Table 2. Z_{in} and Z_{OL} versus Collector Voltage, Input Power, and Output Power

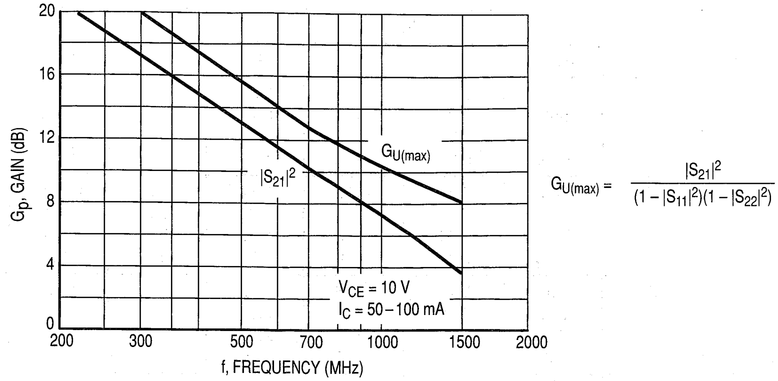


Figure 11. Gain versus Frequency

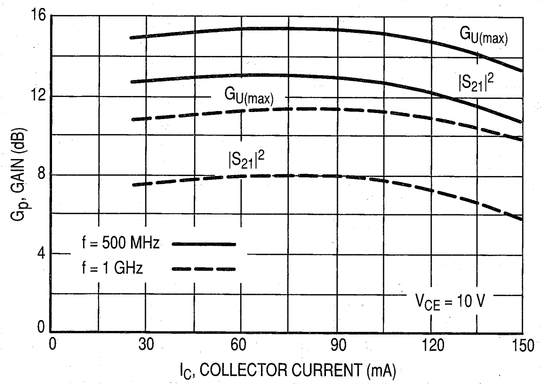


Figure 12. Gain versus Collector Current

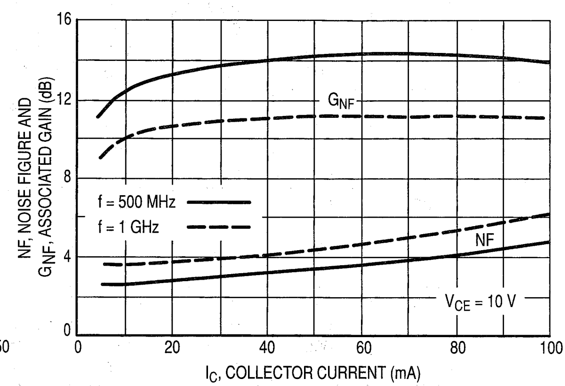


Figure 13. Noise Figure and Associated Gain versus Collector Current

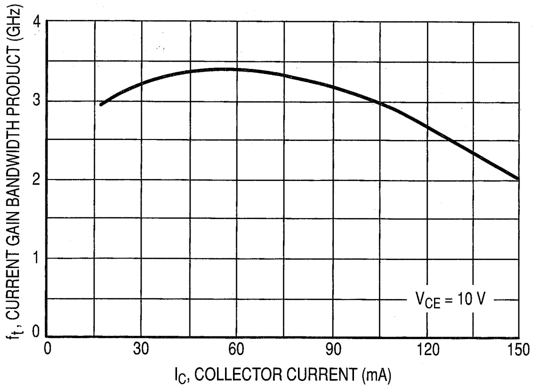


Figure 14. Current Gain Bandwidth Product versus Collector Current

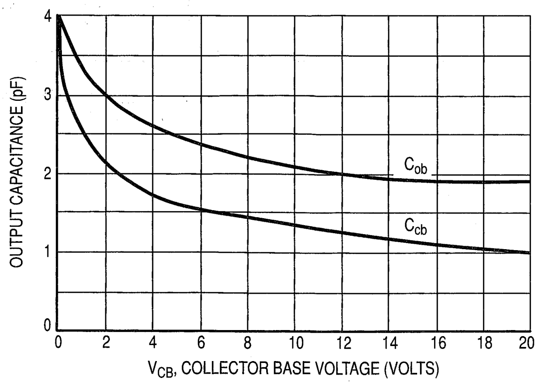


Figure 15. Output Capacitance versus Collector Base Voltage

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
5.0	10	250	0.72	−161	6.20	93	0.057	30	0.30	−91
		500	0.73	179	3.16	76	0.069	43	0.27	−94
		1000	0.76	158	1.62	55	0.105	63	0.27	−119
		1500	0.82	142	1.08	41	0.155	70	0.41	−137
	25	250	0.70	−173	7.17	89	0.045	47	0.26	−123
		500	0.70	172	3.63	75	0.073	60	0.20	−128
		1000	0.74	152	1.90	54	0.134	67	0.21	−157
		1500	0.79	136	1.32	39	0.196	66	0.32	−167
	50	250	0.72	−178	7.63	89	0.038	56	0.27	−139
		500	0.72	170	3.85	77	0.068	67	0.23	−141
		1000	0.75	153	2.01	59	0.129	72	0.23	−162
		1500	0.81	137	1.40	46	0.188	70	0.32	−164
	100	250	0.73	179	7.34	88	0.036	61	0.26	−143
		500	0.74	169	3.70	77	0.067	71	0.22	−144
		1000	0.76	153	1.94	59	0.130	74	0.24	−166
		1500	0.81	138	1.36	46	0.191	71	0.32	−167
	150	250	0.78	176	5.19	92	0.033	64	0.22	−131
		500	0.78	167	2.76	78	0.065	74	0.21	−131
		1000	0.80	151	1.49	58	0.129	77	0.24	−155
		1500	0.85	135	1.05	45	0.191	73	0.35	−161
10	10	250	0.69	−157	7.03	94	0.050	33	0.34	−67
		500	0.70	−178	3.59	77	0.060	46	0.32	−69
		1000	0.74	160	1.84	55	0.094	67	0.29	−94
		1500	0.81	142	1.20	41	0.148	76	0.42	−121
	25	250	0.67	−168	8.30	91	0.039	46	0.24	−93
		500	0.68	176	4.25	77	0.060	60	0.21	−89
		1000	0.72	158	2.19	57	0.109	71	0.19	−114
		1500	0.78	142	1.47	44	0.165	74	0.31	−134
	50	250	0.68	−174	8.88	90	0.035	55	0.21	−110
		500	0.68	172	4.49	77	0.060	67	0.18	−104
		1000	0.72	155	2.31	59	0.113	74	0.17	−128
		1500	0.77	139	1.58	46	0.169	74	0.28	−140
	100	250	0.68	−178	8.49	89	0.030	61	0.19	−104
		500	0.69	170	4.32	76	0.060	71	0.17	−97
		1000	0.72	153	2.25	58	0.120	76	0.17	−123
		1500	0.78	137	1.53	44	0.180	75	0.28	−137
	150	250	0.72	178	6.53	91	0.029	64	0.22	−71
		500	0.73	169	3.37	77	0.056	75	0.24	−75
		1000	0.76	152	1.79	57	0.112	80	0.22	−105
		1500	0.83	137	1.22	43	0.175	79	0.34	−129

Table 3. Common Emitter Scattering Parameters

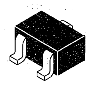
The RF Small Signal Line
NPN Silicon High-Frequency Transistor

MRF577T1

LOW NOISE HIGH FREQUENCY TRANSISTOR

Designed for low noise, wide dynamic range front end amplifiers at frequencies to 1.5 GHz. Specifically aimed at portable communication devices such as pagers and hand–held phones.

- Low Noise Figure
  NF = 1.5 dB (Typ) @ 1.0 GHz
- High Current Gain–Bandwidth Product (f_{τ} = 7.0 GHz Typ @ 6.0 V, 40 mA)
- Small, Surface–Mount Package (SC–70/SOT–323)
- Available in Tape and Reel Packaging.
  T1 Suffix = 3,000 Units per 8 mm, 7 inch Reel.



CASE 419–02, STYLE 3 (SC–70/SOT–323)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	10	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Emitter–Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	80	mAdc
Total Device Dissipation @ T_C = 75°C (1) Derate above 75°C	P_D	232 3.1	mW mW/°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C
Operating Temperature Range	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction–to–Case (1)	$R_{\theta JC}$	323	°C/W

DEVICE MARKING

MRF577T1 = D

(1) Case temperature measured on the collector lead immediately adjacent to body of package.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = 1.0 mA, I_B = 0 mA)		$V_{(BR)CEO}$	10	12	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)		$V_{(BR)CBO}$	20	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 50 μA, I_C = 0)		$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 8.0 Vdc, I_E = 0)		I_{CBO}	—	—	10	μA
ON CHARACTERISTICS						
DC Current Gain (V_{CE} = 10 Vdc, I_C = 30 mA)		h_{FE}	50	—	300	—
DYNAMIC CHARACTERISTICS						
Collector–Base Capacitance (V_{CB} = 6.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	—	0.85	—	pF
Current–Gain Bandwidth Product (V_{CE} = 6.0 Vdc, I_E = 40 mA, f = 1.0 GHz)		f_τ	—	7.0	—	GHz
PERFORMANCE CHARACTERISTICS						
Noise Figure — Minimum (V_{CE} = 6.0 Vdc, I_C = 5.0 mA) Figure 1	500 MHz 1.0 GHz	NF_{min}	— —	1.0 1.5	— —	dB
Associated Gain at Minimum Noise Figure (V_{CE} = 6.0 Vdc, I_C = 5.0 mA) Figure 1	500 MHz 1.0 GHz	G_{NF}	— —	15 10	— —	dB
Maximum Unilateral Gain (V_{CE} = 6.0 Vdc, I_C = 40 mA, f = 1000 MHz)		G_{Umax}	—	12	—	dB
Insertion Gain (V_{CE} = 6.0 Vdc, I_C = 40 mA, f = 1000 MHz)		$\|S_{21}\|^2$	—	11	—	dB
Noise Resistance (V_{CE} = 6.0 Vdc, I_C = 5.0 mA, f = 1000 MHz)		R_N	—	6.0	—	Ohms

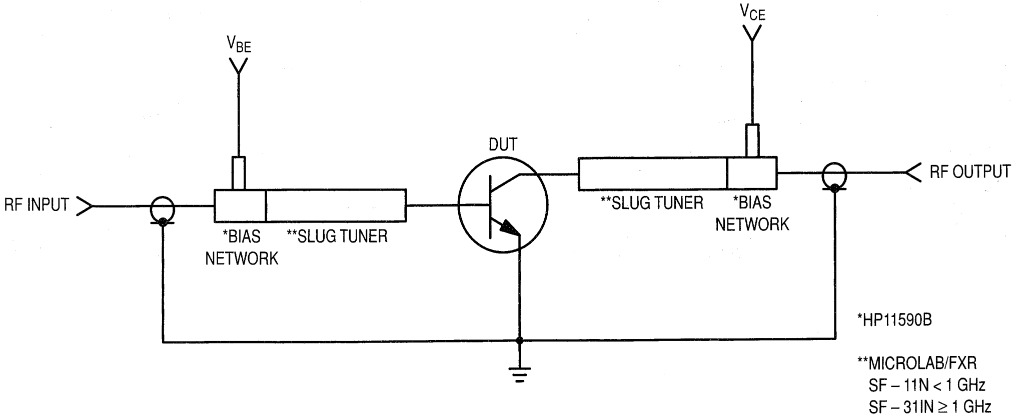


Figure 1. Functional Circuit Schematic

TYPICAL CHARACTERISTICS

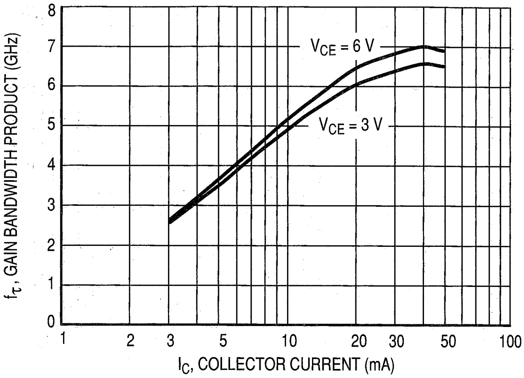


Figure 2. f_τ, Current–Gain Bandwidth Product versus Collector Current

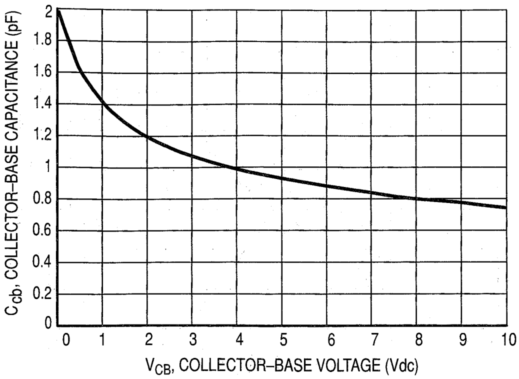


Figure 3. Collector–Base Capacitance versus Voltage

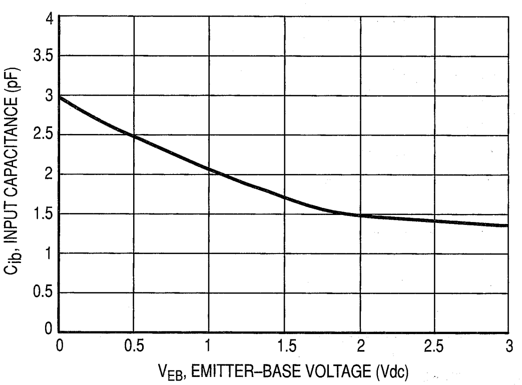


Figure 4. Input Capacitance versus Emitter–Base Voltage

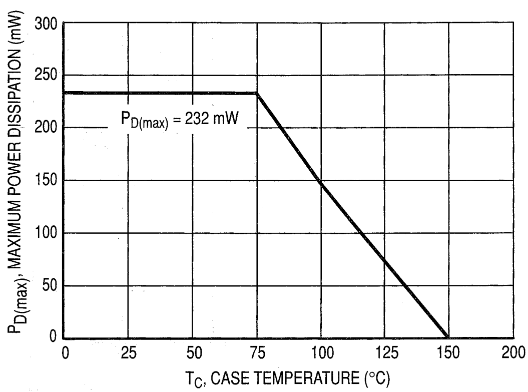


Figure 5. Maximum Power Dissipation versus Collector Lead Temperature (T_C)

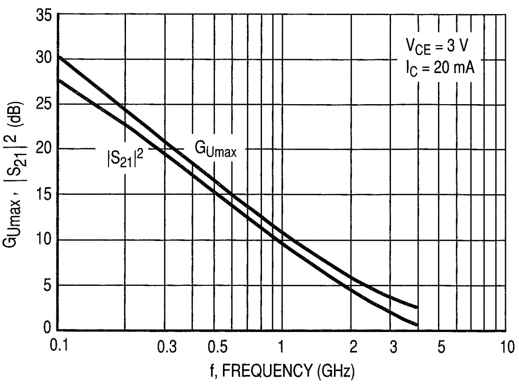


Figure 6. Forward Insertion Gain and Maximum Unilateral Gain versus Frequency

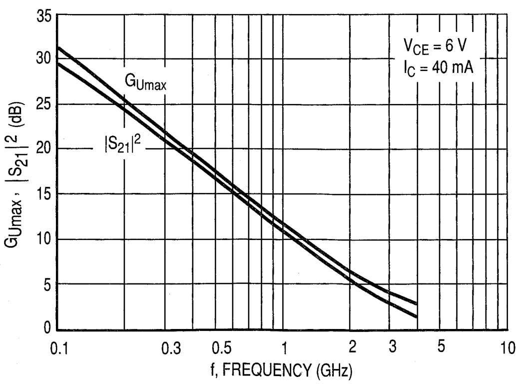


Figure 7. Forward Insertion Gain and Maximum Unilateral Gain versus Frequency

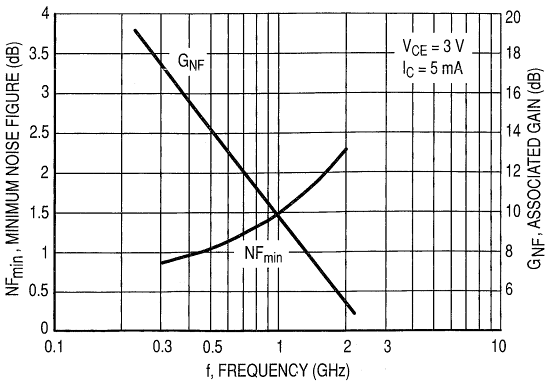


Figure 8. Minimum Noise Figure and Associated Gain versus Frequency

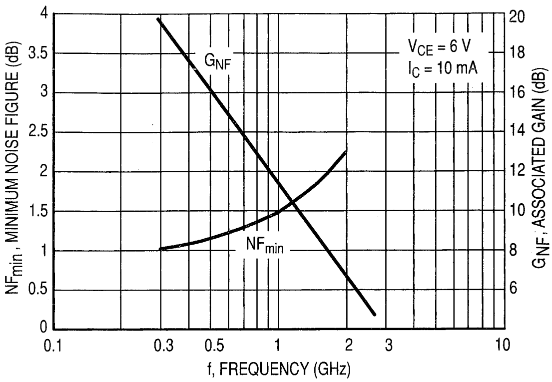


Figure 9. Minimum Noise Figure and Associated Gain versus Frequency

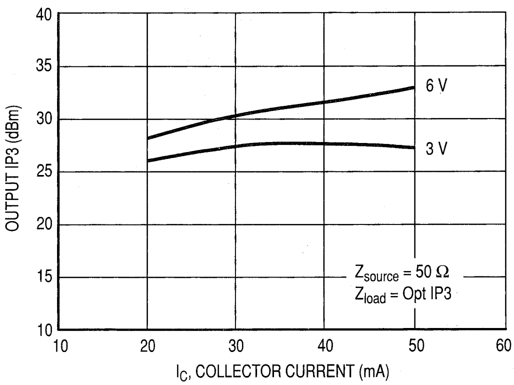


Figure 10. Output Third Order Intercept Point versus Collector Current

V_{CE} (Volts)	I_C (mA)	f (MHz)	NF_{min} (dB)	$\|\Gamma_o\|$	$\angle \Gamma_o$	R_N
3.0	3.0	300	0.81	0.44	57	10
		500	1.05	0.43	88	9
		900	1.51	0.46	138	6
		1000	1.62	0.47	149	6
		1500	2.11	0.56	−173	4
		2000	2.55	0.69	−157	6
	5.0	300	0.86	0.33	58	8
		500	1.03	0.34	88	8
		900	1.40	0.40	139	6
		1000	1.50	0.42	149	5
		1500	1.89	0.52	−173	4
		2000	2.29	0.65	−157	6
6.0	3.0	300	0.81	0.45	50	11
		500	1.07	0.44	81	11
		900	1.56	0.44	132	8
		1000	1.70	0.45	142	7
		1500	2.23	0.53	−177	5
		2000	2.72	0.67	−158	6
	5.0	300	0.85	0.37	50	10
		500	1.04	0.37	80	9
		900	1.42	0.39	130	7
		1000	1.52	0.40	141	6
		1500	2.00	0.50	−179	5
		2000	2.43	0.65	−159	6
	10	300	1.02	0.24	52	9
		500	1.15	0.26	82	9
		900	1.42	0.33	131	7
		1000	1.50	0.35	142	6
		1500	1.85	0.47	−179	5
		2000	2.25	0.61	−159	5

Table 1. MRF577T1 Common Emitter Noise Parameters

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
3.0	3.0	0.10	0.852	−47	9.09	149	0.061	65	0.881	−25
		0.20	0.758	−84	7.13	126	0.095	49	0.708	−41
		0.30	0.687	−108	5.60	112	0.112	41	0.575	−50
		0.40	0.649	−125	4.52	101	0.121	37	0.490	−56
		0.50	0.622	−138	3.79	93	0.127	35	0.434	−60
		0.60	0.588	−148	3.20	87	0.131	35	0.384	−60
		0.70	0.581	−157	2.81	82	0.135	3	0.357	−63
		0.80	0.580	−164	2.48	77	0.140	35	0.342	−65
		0.90	0.574	−170	2.25	72	0.144	37	0.325	−68
		1.00	0.572	−175	2.05	68	0.149	38	0.315	−70
		1.50	0.578	163	1.46	50	0.183	45	0.297	−86
		2.00	0.591	146	1.16	36	0.233	49	0.308	−103
		2.50	0.609	131	0.99	25	0.298	49	0.330	−122
		3.00	0.617	118	0.87	17	0.374	45	0.351	−140
		4.00	0.643	94	0.75	5	0.519	32	0.406	−176
	5.0	0.10	0.770	−60	13.16	141	0.055	61	0.807	−35
		0.20	0.666	−99	9.41	119	0.080	47	0.587	−54
		0.30	0.607	−123	7.02	106	0.092	43	0.450	−64
		0.40	0.580	−138	5.52	97	0.101	42	0.371	−70
		0.50	0.562	−149	4.54	90	0.109	42	0.322	−75
		0.60	0.536	−159	3.83	85	0.117	44	0.273	−75
		0.70	0.533	−166	3.33	80	0.124	45	0.249	−78
		0.80	0.534	−172	2.94	76	0.133	46	0.235	−81
		0.90	0.531	−177	2.65	71	0.142	47	0.222	−84
		1.00	0.530	178	2.41	68	0.152	48	0.213	−87
		1.50	0.539	159	1.71	52	0.204	50	0.199	−102
		2.00	0.551	144	1.36	38	0.262	49	0.212	−119
		2.50	0.568	130	1.15	27	0.324	46	0.237	−136
		3.00	0.578	118	1.02	18	0.390	42	0.260	−152
		4.00	0.614	96	0.86	3	0.513	29	0.326	177
	10	0.10	0.629	−83	19.46	130	0.044	56	0.663	−53
		0.20	0.551	−123	12.13	109	0.060	49	0.426	−75
		0.30	0.522	−143	8.57	98	0.072	50	0.315	−88
		0.40	0.513	−155	6.58	91	0.083	52	0.259	−97
		0.50	0.505	−163	5.35	86	0.096	54	0.227	−103
		0.60	0.489	−171	4.50	82	0.108	56	0.183	−108
		0.70	0.490	−177	3.89	78	0.121	57	0.168	−113
		0.80	0.492	178	3.43	74	0.134	57	0.159	−118
		0.90	0.491	174	3.08	71	0.148	58	0.152	−122
		1.00	0.491	170	2.80	68	0.161	58	0.148	−127
		1.50	0.501	154	1.96	53	0.228	55	0.147	−144
		2.00	0.513	140	1.56	40	0.293	50	0.163	−156
		2.50	0.528	127	1.32	30	0.354	44	0.190	−168
		3.00	0.536	116	1.17	20	0.414	38	0.209	−179
		4.00	0.578	96	0.99	4	0.516	25	0.270	159
	20	0.10	0.509	−111	24.53	119	0.034	56	0.513	−72
		0.20	0.485	−144	13.84	102	0.048	58	0.319	−99
		0.30	0.478	−159	9.51	93	0.062	61	0.249	−115
		0.40	0.478	−167	7.22	88	0.077	63	0.220	−125
		0.50	0.476	−173	5.84	83	0.093	64	0.203	−133
		0.60	0.466	179	4.90	80	0.108	65	0.173	−142
		0.70	0.469	175	4.23	76	0.124	65	0.168	−147
		0.80	0.471	171	3.73	73	0.139	64	0.166	−152
		0.90	0.472	168	3.34	70	0.155	64	0.164	−157
		1.00	0.472	165	3.03	67	0.170	63	0.164	−160
		1.50	0.482	150	2.12	54	0.244	57	0.171	−174
		2.00	0.493	138	1.68	42	0.313	50	0.188	177
		2.50	0.507	125	1.42	32	0.375	44	0.211	168
		3.00	0.514	115	1.26	22	0.432	36	0.226	159
		4.00	0.555	96	1.06	6	0.525	23	0.274	143

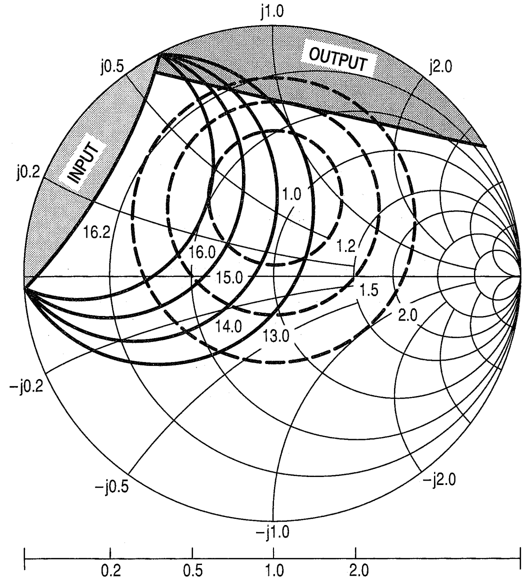
Table 2. Common Emitter S–Parameters

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
3.0	40	0.10	0.457	−136	27.07	111	0.027	61	0.401	−90
		0.20	0.465	−159	14.51	97	0.042	66	0.268	−119
		0.30	0.467	−169	9.85	90	0.059	69	0.230	−135
		0.40	0.471	−175	7.44	85	0.076	70	0.217	−144
		0.50	0.470	−180	6.00	82	0.093	70	0.209	−151
		0.60	0.464	174	5.04	79	0.110	70	0.189	−160
		0.70	0.467	170	4.34	75	0.127	69	0.188	−164
		0.80	0.469	167	3.83	72	0.143	68	0.189	−168
		0.90	0.469	164	3.42	70	0.159	67	0.189	−171
		1.00	0.470	161	3.11	67	0.176	65	0.191	−174
		1.50	0.480	148	2.17	54	0.253	58	0.200	174
		2.00	0.490	136	1.71	42	0.323	51	0.215	166
		2.50	0.504	124	1.45	32	0.386	43	0.237	159
		3.00	0.510	114	1.29	23	0.443	36	0.249	150
		4.00	0.549	95	1.09	6	0.532	22	0.291	136
6.0	3.0	0.10	0.872	−42	9.23	151	0.049	68	0.903	−20
		0.20	0.776	−76	7.48	130	0.079	53	0.757	−33
		0.30	0.695	−100	6.01	115	0.095	45	0.635	−40
		0.40	0.647	−117	4.91	105	0.104	40	0.555	−45
		0.50	0.612	−131	4.14	97	0.110	38	0.500	−47
		0.60	0.572	−141	3.51	90	0.114	38	0.454	−47
		0.70	0.56	−151	3.09	85	0.118	38	0.427	−49
		0.80	0.558	−158	2.72	80	0.123	38	0.412	−50
		0.90	0.549	−165	2.48	75	0.127	40	0.395	−52
		1.00	0.544	−171	2.26	71	0.132	42	0.384	−54
		1.50	0.548	167	1.60	53	0.163	49	0.360	−66
		2.00	0.562	149	1.27	39	0.209	54	0.360	−82
		2.50	0.581	133	1.06	27	0.271	54	0.366	−99
		3.00	0.593	120	0.93	18	0.346	51	0.375	−117
		4.00	0.628	96	0.77	6	0.498	38	0.405	−155
	5.0	0.10	0.797	−52	13.58	145	0.045	64	0.840	−28
		0.20	0.678	−89	10.10	122	0.068	51	0.642	−43
		0.30	0.601	−113	7.68	109	0.080	46	0.509	−50
		0.40	0.562	−130	6.10	100	0.089	45	0.430	−54
		0.50	0.537	−141	5.05	93	0.096	45	0.380	−56
		0.60	0.505	−152	4.25	87	0.103	46	0.335	−55
		0.70	0.499	−160	3.71	82	0.110	47	0.311	−56
		0.80	0.498	−166	3.27	78	0.118	48	0.296	−58
		0.90	0.492	−172	2.95	74	0.127	50	0.282	−59
		1.00	0.49	−177	2.68	70	0.135	51	0.272	−61
		1.50	0.498	163	1.89	54	0.183	53	0.249	−72
		2.00	0.512	147	1.49	40	0.237	53	0.249	−87
		2.50	0.533	132	1.25	29	0.295	51	0.256	−105
		3.00	0.547	120	1.10	19	0.359	46	0.266	−121
		4.00	0.594	98	0.90	4	0.488	34	0.309	−158
	10	0.100	0.658	−71	20.57	134	0.038	60	0.710	−42
		0.200	0.542	−111	13.36	112	0.053	52	0.473	−58
		0.300	0.492	−132	9.57	101	0.065	52	0.353	−65
		0.400	0.472	−146	7.39	94	0.075	54	0.288	−70
		0.500	0.46	−155	6.02	88	0.086	56	0.250	−72
		0.600	0.438	−164	5.06	84	0.097	58	0.207	−70
		0.700	0.437	−171	4.38	80	0.109	59	0.189	−72
		0.800	0.438	−176	3.86	76	0.120	59	0.176	−74
		0.900	0.437	179	3.46	73	0.132	59	0.166	−76
		1.000	0.437	175	3.14	69	0.144	59	0.158	−78
		1.500	0.448	158	2.19	55	0.205	57	0.140	-91
		2.000	0.463	144	1.73	42	0.265	53	0.143	−107
		2.500	0.482	130	1.45	31	0.323	48	0.155	−126
		3.000	0.496	119	1.28	21	0.381	42	0.165	−141
		4.000	0.549	99	1.05	5	0.488	30	0.216	−173

Table 2. Common Emitter S–Parameters (continued)

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle \phi$	$\|S_{21}\|$	$\angle \phi$	$\|S_{12}\|$	$\angle \phi$	$\|S_{22}\|$	$\angle \phi$
6.0	20	0.10	0.521	−94	26.70	123	0.030	59	0.555	−56
		0.20	0.448	−131	15.53	104	0.043	58	0.335	−74
		0.30	0.426	−149	10.76	96	0.056	62	0.243	−82
		0.40	0.42	−159	8.19	90	0.070	64	0.199	−88
		0.50	0.415	−166	6.63	85	0.083	65	0.172	−92
		0.60	0.401	−175	5.56	82	0.097	66	0.132	−93
		0.70	0.403	−180	4.80	78	0.111	66	0.121	−96
		0.80	0.405	176	4.23	75	0.125	65	0.112	−100
		0.90	0.405	173	3.78	72	0.139	65	0.106	−104
		1.00	0.406	169	3.43	69	0.153	64	0.101	−107
		1.50	0.42	154	2.38	56	0.220	59	0.094	−125
		2.00	0.434	141	1.87	44	0.284	53	0.105	−141
		2.50	0.454	128	1.57	33	0.343	47	0.125	−157
		3.00	0.466	118	1.39	23	0.399	40	0.137	−169
		4.00	0.52	99	1.15	6	0.495	28	0.189	167
	40	0.10	0.438	−116	30.08	114	0.025	61	0.423	−68
		0.20	0.407	−147	16.43	99	0.039	65	0.245	−86
		0.30	0.400	−160	11.20	92	0.053	68	0.179	−96
		0.40	0.400	−168	8.48	87	0.068	70	0.152	−103
		0.50	0.398	−173	6.84	83	0.083	70	0.135	−108
		0.60	0.389	179	5.74	80	0.098	70	0.100	−113
		0.70	0.392	175	4.95	77	0.113	69	0.094	−117
		0.80	0.395	172	4.35	74	0.128	69	0.090	−123
		0.90	0.396	169	3.89	71	0.143	68	0.087	−127
		1.00	0.397	165	3.53	68	0.157	67	0.085	−131
		1.50	0.411	152	2.44	55	0.227	60	0.088	−149
		2.00	0.426	139	1.92	44	0.293	53	0.103	−161
		2.50	0.446	127	1.61	33	0.352	47	0.126	−173
		3.00	0.459	117	1.42	24	0.408	40	0.139	176
		4.00	0.512	99	1.17	7	0.500	27	0.190	156

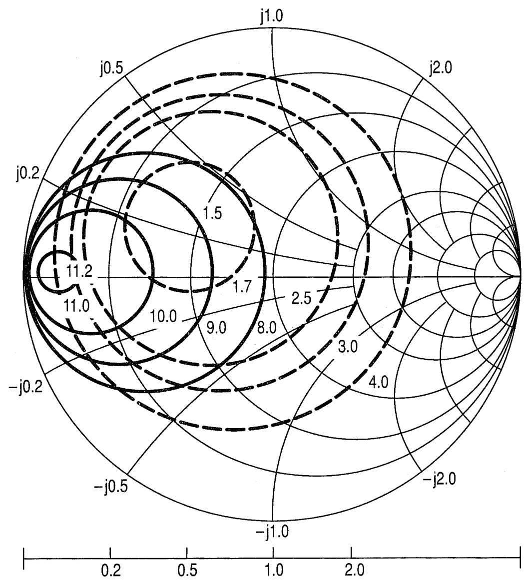
Table 2. Common Emitter S–Parameters (continued)



$V_{CE} = 3.0$ V
$I_C = 5.0$ mA
— Potentially Unstable

f (MHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
500	1.03	0.34 ∠ 88°	8	0.69

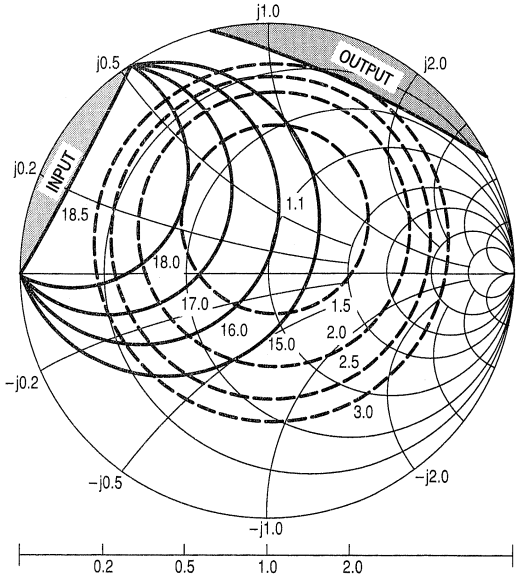
Figure 11. MRF577T1 Constant Gain and Noise Figure Contours



$V_{CE} = 3.0$ V
$I_C = 5.0$ mA

f (MHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
1000	1.47	0.42 ∠ 149°	5	1.02

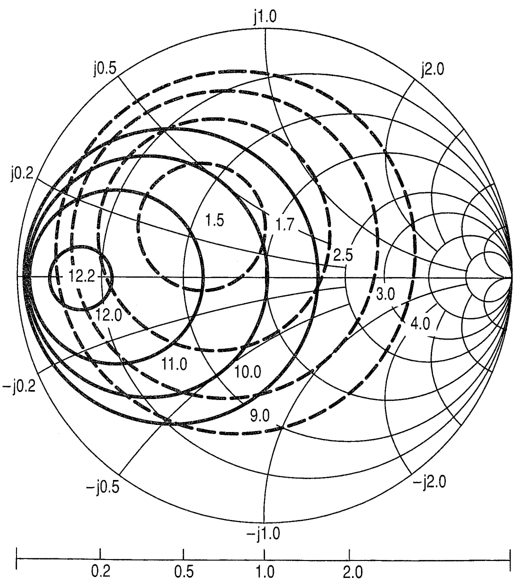
Figure 12. MRF577T1 Constant Gain and Noise Figure Contours



V_{CE} = 6.0 V
I_C = 10 mA
▩ — Potentially Unstable

f (MHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
500	1.15	0.26 ∠ 82°	9	0.86

Figure 13. MRF577T1 Constant Gain and Noise Figure Contours



V_{CE} = 6.0 V
I_C = 10 mA

f (MHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
1000	1.49	0.35 ∠ 142°	6	1.04

Figure 14. MRF577T1 Constant Gain and Noise Figure Contours

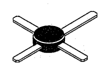
The RF Line
NPN Silicon High-Frequency Transistors

MRF581
MRF5812R1, R2

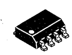
I_C = 200 mA
LOW NOISE
HIGH–FREQUENCY
TRANSISTORS
NPN SILICON

Designed for high current low power amplifiers up to 1.0 GHz.

- Low Noise (2.0 dB @ 500 MHz)
- Low Intermodulation Distortion
- High Gain
- State–of–the–Art Technology
  Fine Line Geometry
  Arsenic Emitters
  Gold Top Metallization
  Nichrome Thin–Film Ballasting Resistors
- Excellent Dynamic Range
- Fully Characterized
- High Current–Gain Bandwidth Product
- MRF5812 available in tape and reel packaging by adding suffix:
  R1 suffix = 500 units per reel
  R2 suffix = 2,500 units per reel



CASE 317–01, STYLE 2
MRF581



CASE 751–05, STYLE 1
SORF (SO–8)
MRF5812

MAXIMUM RATINGS

Rating		Symbol	MRF581	MRF5812	Unit
Collector–Emitter Voltage		V_{CEO}	18	15	Vdc
Collector–Base Voltage		V_{CBO}	36	30	Vdc
Emitter–Base Voltage		V_{EBO}	2.5		Vdc
Collector Current — Continuous		I_C	200		mAdc
Thermal Resistance θJC (1)	MRF581	$R_{\theta JC}$	40		°C/W
Thermal Resistance θJC (1)	MRF5812	$R_{\theta JC}$	45		°C/W
Total Device Dissipation @ T_C = 75°C (1) Derate above T_C = 75°C	MRF581	P_D	1.88 25		Watts mW/°C
Total Device Dissipation @ T_C = 75°C (1) Derate above T_C = 75°C	MRF5812	P_D	1.67 22.2		Watts mW/°C
Storage Junction Temperature Range		T_{stg}	– 55 to +150		°C
Maximum Junction Temperature		T_{Jmax}	150		°C

DEVICE MARKING

MRF5812 = 5812

NOTES:
1. Case temperature measured on collector lead immediately adjacent to body of package.

REV 8

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	MRF581	$V_{(BR)CEO}$	18 15	— —	— —	Vdc
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	MRF5812	$V_{(BR)CEO}$	15	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	MRF5812	$V_{(BR)CES}$	30	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 1.0 mAdc, I_E = 0)	MRF581	$V_{(BR)CBO}$	36 30	— —	— —	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	MRF581 MRF5812	$V_{(BR)EBO}$	2.5	—	—	Vdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, V_{BE} = 0)	MRF581	I_{EBO}	—	—	100	µAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	MRF581	I_{CBO}	—	—	100	µAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	MRF5812	I_{CBO}	—	—	0.1	mAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	MRF581	h_{FE}	50	—	200	—
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	MRF5812	h_{FE}	30	90	200	—
DYNAMIC CHARACTERISTICS						
Collector–Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	MRF581	C_{ob}	—	1.4	2.0	pF
Collector–Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	MRF5812	C_{cb}	—	1.2	2.0	pF
Current–Gain Bandwidth Product (I_C = 75 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	MRF581	f_T	—	5.0	—	GHz
Current–Gain — Bandwidth Product (I_C = 75 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	MRF5812	f_T	—	5.5	—	GHz
FUNCTIONAL TESTS						
Noise Figure (Minimum) (Figure 11) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MRF581	NF_{min}	—	2.0	3.0	dB
Noise Figure (Minimum) (Figure 11) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MRF5812	NF_{min}	—	2.0	—	dB
Noise Figure (50 Ohm Insertion) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MRF5812	$NF_{50\,\Omega}$	—	2.5	3.0	dB
Power Gain at Optimum Noise Figure (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MRF581	G_{NF}	13	15.5	—	dB
Insertion Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MRF5812	$\|S_{21}\|^2$	13	15.5	—	dB
Maximum Unilateral Gain (I_C = 75 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)		G_{Umax}(2)	—	17	—	dB
Intermodulation Distortion (3) (V_{CE} = 10 V, I_C = 75 mA, V_{out} = +50 dBmV)		IMD(d3)	—	−65	—	dB

NOTES:

1. 300 µs pulse on Tektronix 576 or equivalent.
2. $G_{Umax} = \dfrac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$
3. 2 Tones, f1 = 497 MHz, f2 = 503 MHz, 3rd Order Single Tone reference.

TYPICAL CHARACTERISTICS
MRF581

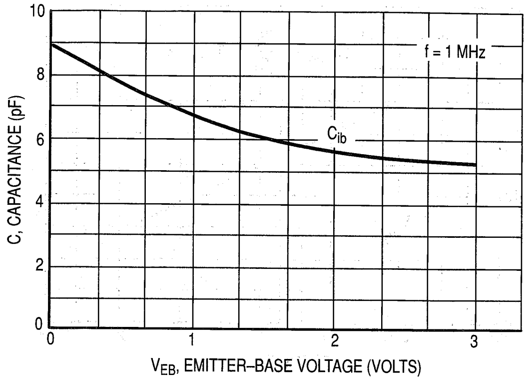


Figure 1. C_{ib} Input Capacitance versus Voltage

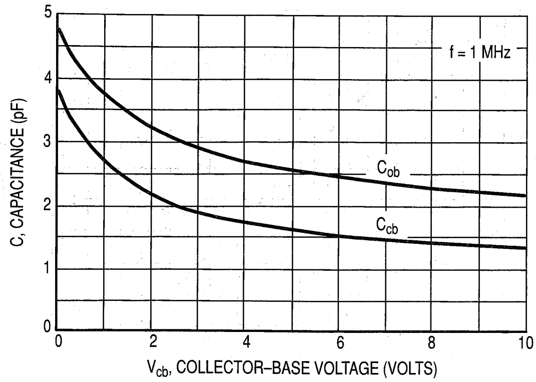


Figure 2. C_{cb}, C_{ob} Collector–Base Capacitance versus Voltage

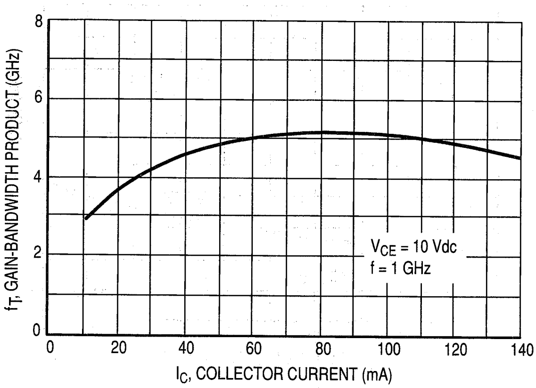


Figure 3. Gain–Bandwidth Product versus Collector Current

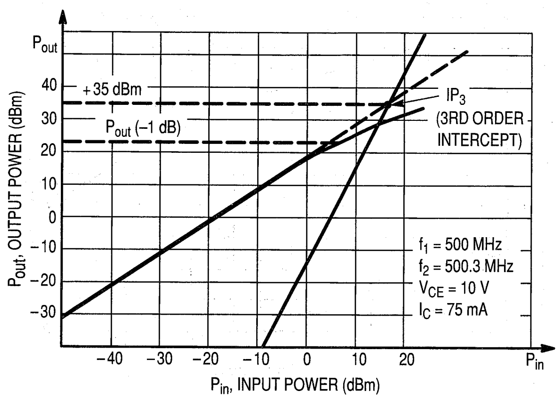


Figure 4. 3rd Order Intercept Point

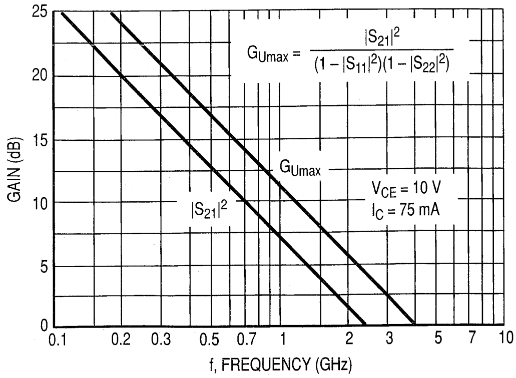


Figure 5. G_{Umax} — Maximum Unilateral Gain, $|S_{21}|^2$ versus Frequency

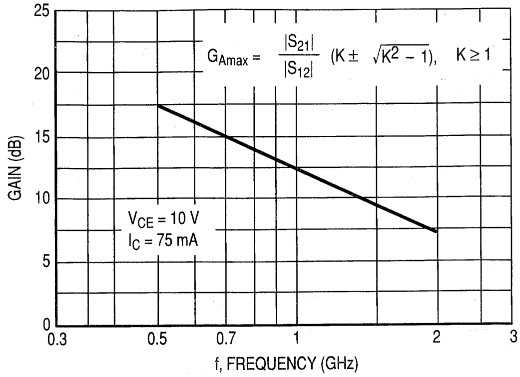


Figure 6. G_{Amax}, Maximum Available Gain versus Frequency

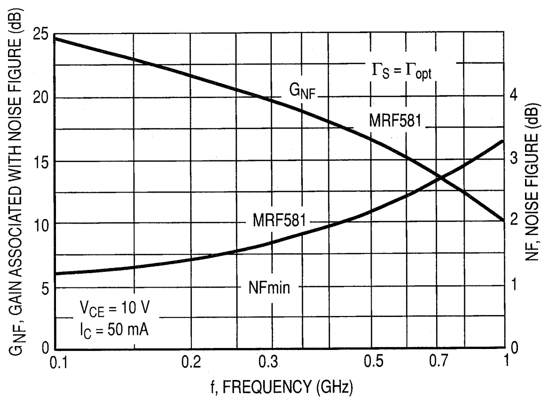


Figure 7. Minimum Noise Figure and Gain Associated with Minimum Noise Figure versus Frequency

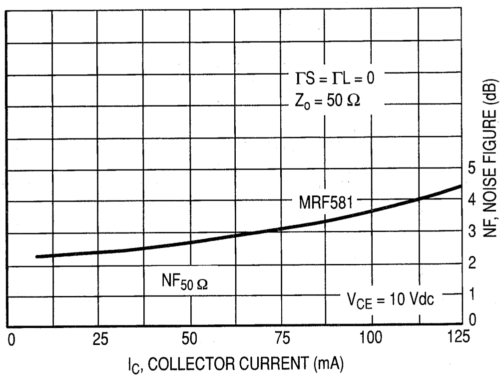


Figure 8. Noise Figure versus Collector Current f = 500 MHz

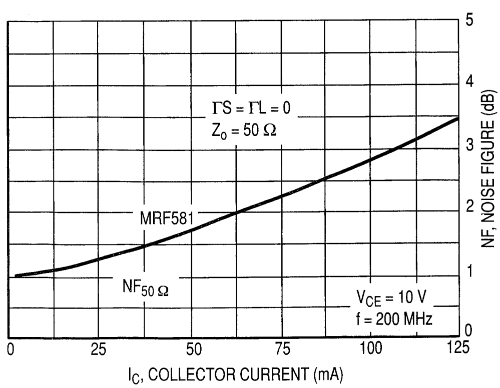


Figure 9. Noise Figure versus Collector Current

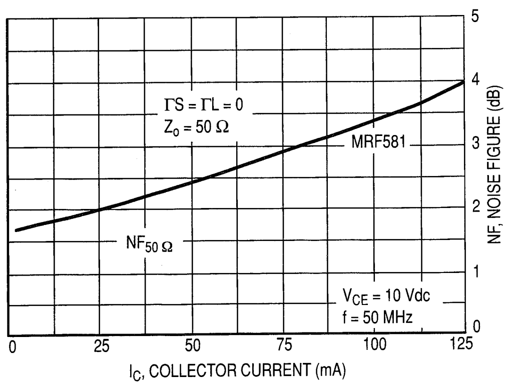


Figure 10. Noise Figure and Gain Associated with Noise Figure versus Collector Current

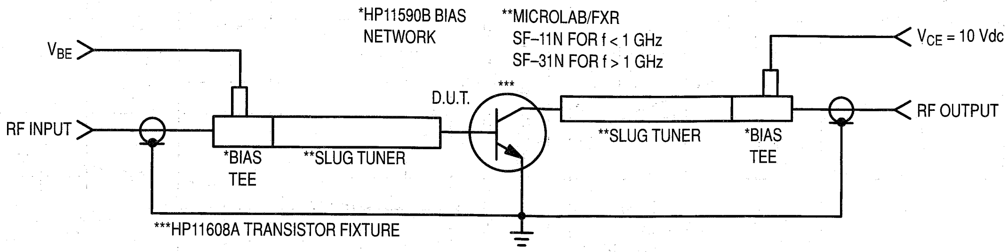


Figure 11. MRF581, MRF5812 Functional Circuit Schematic

TYPICAL CHARACTERISTICS
MRF5812

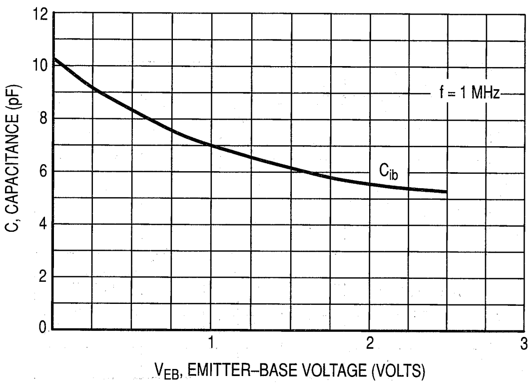


Figure 12. C_{ib} Input Capacitance versus Voltage

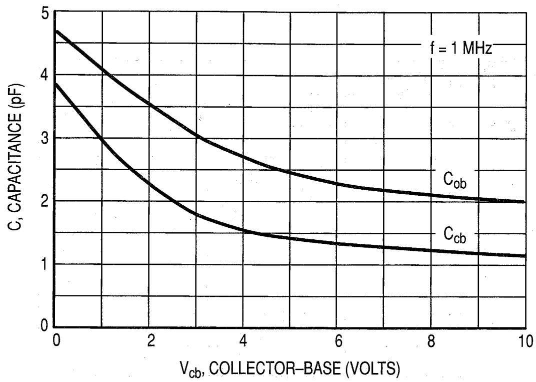


Figure 13. C_{cb}, C_{ob} Collector–Base Capacitance versus Voltage

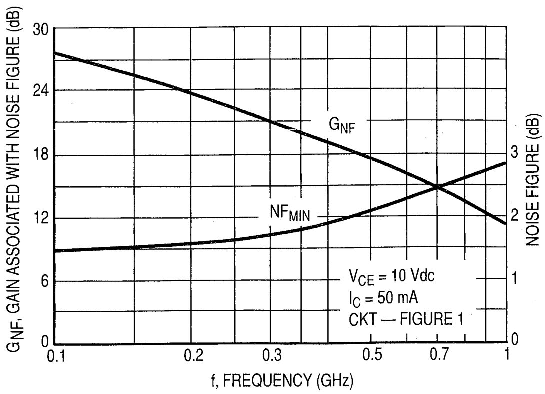


Figure 14. Minimum Noise Figure and Gain Associated with Noise Figure versus Frequency

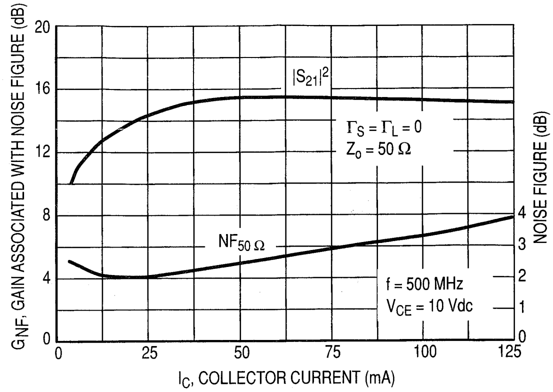


Figure 15. Noise Figure and Insertion Gain versus Collector Current

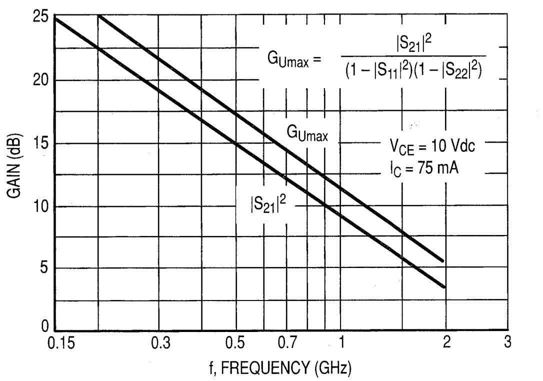


Figure 16. G_{Umax} — Maximum Unilateral Gain, $|S_{21}|^2$ versus Frequency

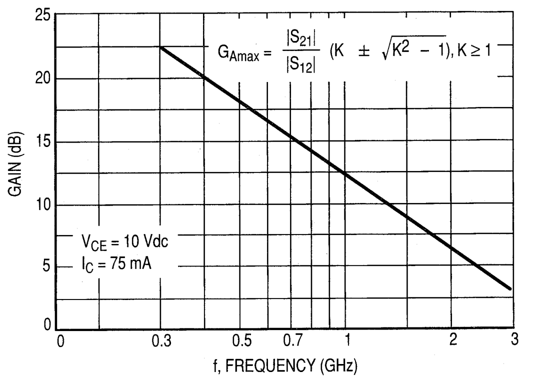


Figure 17. G_{Amax}, Maximum Available Gain versus Frequency

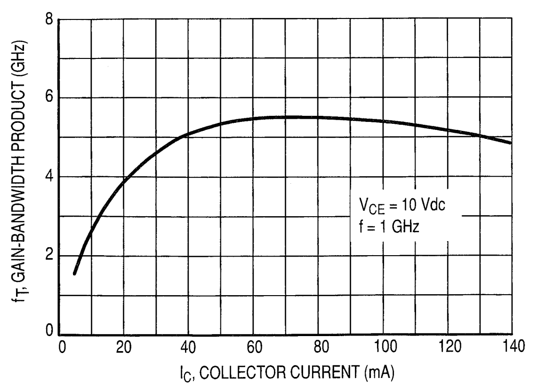


Figure 18. Gain–Bandwidth Product versus Collector Current

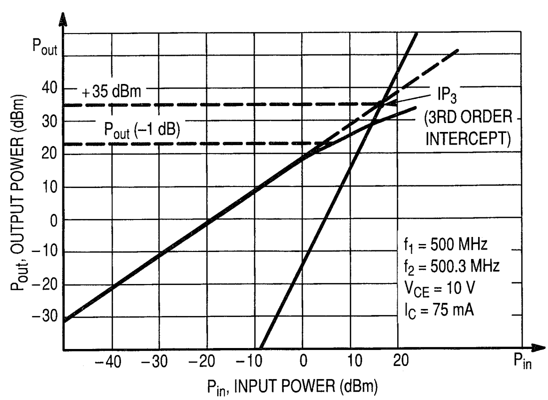


Figure 19. 3rd Order Intercept Point and 1.0 dB Compression Point

V_{CE} = 10 V I_C = 50 mA

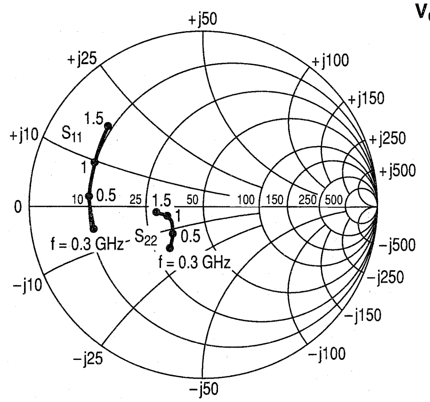


Figure 20. MRF581 Input/Output Reflection Coefficient versus Frequency

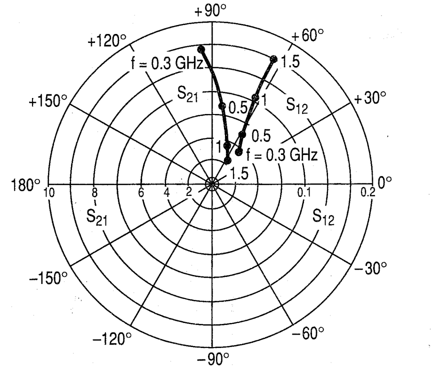


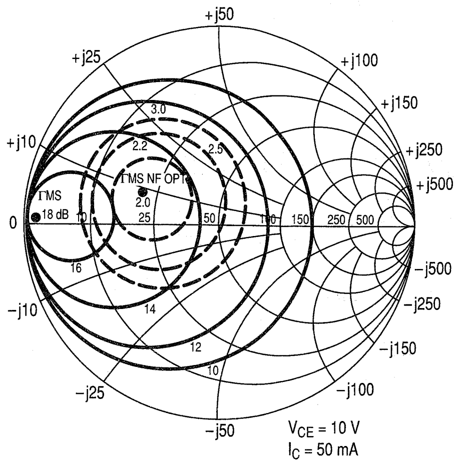
Figure 21. MRF581 Forward/Reverse Transmission Coefficients versus Frequency

V_{CE} (Volts)	I_C (mA)	f (MHz)	S11 $\|S_{11}\|$	S11 ∠ φ	S21 $\|S_{21}\|$	S21 ∠ φ	S12 $\|S_{12}\|$	S12 ∠ φ	S22 $\|S_{22}\|$	S22 ∠ φ
5.0	25	300	0.69	–169	6.57	93	0.06	39	0.34	–129
		500	0.72	176	3.95	82	0.07	47	0.29	–142
		1000	0.73	157	2.10	62	0.12	60	0.27	–165
		1500	0.76	139	1.47	50	0.17	61	0.33	–172
	50	300	0.70	–173	7.14	93	0.05	45	0.38	–144
		500	0.72	173	4.27	82	0.07	53	0.34	–157
		1000	0.72	157	2.24	65	0.13	62	0.33	179
		1500	0.76	138	1.61	53	0.18	61	0.37	173
	75	300	0.70	–175	7.26	92	0.05	48	0.40	–148
		500	0.72	172	4.33	82	0.07	55	0.37	–161
		1000	0.72	155	2.28	65	0.13	63	0.30	176
		1500	0.76	138	1.64	53	0.19	61	0.39	170
	100	300	0.70	–176	7.30	92	0.05	48	0.40	–151
		500	0.72	172	4.34	82	0.07	56	0.37	–163
		1000	0.72	155	2.28	65	0.13	63	0.36	175
		1500	0.75	137	1.64	53	0.19	61	0.39	168
10	25	300	0.66	–165	7.58	95	0.05	40	0.29	–106
		500	0.69	178	4.56	82	0.07	48	0.23	–116
		1000	0.70	159	2.39	64	0.11	61	0.19	–141
		1500	0.74	141	1.65	50	0.16	64	0.26	–153
	50	300	0.65	–169	8.25	94	0.05	46	0.30	–126
		500	0.68	175	4.96	82	0.07	54	0.24	–138
		1000	0.69	157	2.60	65	0.12	63	0.22	–164
		1500	0.72	139	1.82	52	0.17	63	0.27	–171
	75	300	0.66	–171	8.49	93	0.05	48	0.30	–132
		500	0.68	175	5.06	82	0.07	55	0.25	–145
		1000	0.69	157	2.64	65	0.12	64	0.23	–170
		1500	0.72	139	1.86	53	0.17	63	0.27	–176
	100	300	0.66	–172	8.46	93	0.05	49	0.30	–134
		500	0.68	174	5.06	82	0.07	56	0.25	–147
		1000	0.68	157	2.64	65	0.12	64	0.23	–172
		1500	0.72	139	1.86	52	0.17	63	0.27	–177
15	25	300	0.65	–163	7.96	95	0.05	40	0.28	–92
		500	0.67	179	4.82	82	0.06	48	0.21	–98
		1000	0.68	160	2.51	63	0.11	62	0.17	–119
		1500	0.72	141	1.73	49	0.16	65	0.24	–137
	50	300	0.64	–167	8.76	94	0.0	46	0.26	–112
		500	0.66	177	5.37	82	0.06	54	0.20	–122
		1000	0.67	159	2.75	65	0.11	64	0.16	–148
		1500	0.71	141	1.91	51	0.16	64	0.22	–157
	75	300	0.64	–168	8.93	93	0.05	47	0.25	–117
		500	0.66	176	5.34	82	0.06	55	0.20	–128
		1000	0.69	158	2.78	65	0.11	65	0.16	–154
		1500	0.70	140	1.93	51	0.16	64	0.22	–162
	100	300	0.64	–169	8.91	93	0.05	48	0.25	–117
		500	0.66	176	5.33	82	0.06	56	0.19	–129
		1000	0.67	158	2.78	64	0.11	65	0.16	–154
		1500	0.70	140	1.93	51	0.16	64	0.21	–160

Table 1. MRF581 Common Emitter S–Parameters

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
5.0	25	100	0.66	−123	18.3	118	0.04	43	0.53	−79
		300	0.66	−167	7.0	92	0.06	44	0.31	−120
		500	0.65	178	4.3	81	0.08	52	0.28	−133
		1000	0.62	154	2.2	63	0.13	61	0.28	−141
		2000	0.57	109	1.3	39	0.28	57	0.31	−148
		3000	0.55	68	1.0	23	0.41	41	0.34	−164
	50	100	0.64	−133	20.2	114	0.04	44	0.51	−93
		300	0.65	−171	7.6	91	0.06	50	0.34	−137
		500	0.65	175	4.6	81	0.08	56	0.31	−148
		1000	0.61	152	2.3	63	0.13	63	0.28	−149
		2000	0.56	109	1.3	39	0.28	57	0.30	−150
		3000	0.52	70	1.0	23	0.41	39	0.29	−169
	75	100	0.64	−137	20.8	113	0.04	44	0.50	−99
		300	0.66	−173	7.7	91	0.06	52	0.35	−142
		500	0.64	174	4.7	82	0.08	59	0.32	−154
		1000	0.61	151	2.4	65	0.14	64	0.30	−164
		2000	0.54	107	1.4	42	0.30	55	0.27	−167
		3000	0.52	69	1.1	24	0.42	37	0.25	−172
	100	100	0.64	−140	20.8	112	0.03	44	0.50	−103
		300	0.65	−174	7.6	90	0.06	53	0.36	−145
		500	0.64	173	4.7	81	0.08	60	0.33	−156
		1000	0.61	151	2.4	65	0.15	64	0.31	−166
		2000	0.54	107	1.4	42	0.30	54	0.27	−169
		3000	0.52	65	1.1	24	0.42	37	0.25	−174
10	25	100	0.65	−112	20.2	121	0.04	46	0.56	−62
		300	0.63	−162	8.0	93	0.05	46	0.29	−93
		500	0.62	−178	5.0	82	0.07	52	0.25	−102
		1000	0.60	157	2.5	63	0.11	63	0.26	−112
		2000	0.55	112	1.4	39	0.25	61	0.35	−125
		3000	0.55	69	1.0	23	0.39	47	0.40	−145
	50	100	0.63	−122	22.9	117	0.03	46	0.50	−74
		300	0.62	−167	8.8	92	0.05	51	0.28	−112
		500	0.60	178	5.3	82	0.07	58	0.24	−122
		1000	0.58	154	2.7	64	0.12	65	0.23	−129
		2000	0.51	111	1.5	40	0.26	59	0.28	−132
		3000	0.50	70	1.2	24	0.39	44	0.34	−144
	75	100	0.63	−126	23.8	116	0.03	45	0.49	−80
		300	0.63	−168	9.0	92	0.05	51	0.28	−120
		500	0.62	177	5.5	82	0.07	58	0.24	−130
		1000	0.58	154	2.8	65	0.12	65	0.23	−137
		2000	0.52	111	1.5	41	0.26	58	0.27	−135
		3000	0.50	70	1.2	24	0.39	42	0.32	−145
	100	100	0.62	−128	23.8	114	0.03	46	0.46	−82
		300	0.62	−169	8.9	91	0.05	54	0.26	−120
		500	0.60	176	5.4	81	0.07	61	0.23	−130
		1000	0.57	152	2.8	64	0.12	66	0.21	−136
		2000	0.51	109	1.5	40	0.27	59	0.26	−134
		3000	0.50	68	1.2	24	0.39	43	0.32	−145
15	25	100	0.66	−106	21	123	0.03	47	0.57	−54
		300	0.63	−159	8.5	94	0.05	46	0.30	−77
		500	0.61	−177	5.2	82	0.06	52	0.26	−84
		1000	0.58	156	2.6	62	0.11	64	0.28	−96
		2000	0.54	110	1.4	36	0.23	63	0.39	−115
		3000	0.56	68	1.0	22	0.37	49	0.46	−137
	50	100	0.62	−114	24	119	0.03	46	0.51	−64
		300	0.60	−163	9.2	93	0.05	51	0.26	−92
		500	0.58	−179	5.7	81	0.07	58	0.22	−100
		1000	0.56	154	2.9	63	0.12	66	0.23	−109
		2000	0.52	109	1.5	39	0.25	60	0.32	−118
		3000	0.52	67	1.1	22	0.37	46	0.39	−137
	75	100	0.62	−118	24.6	117	0.03	46	0.48	−67
		300	0.59	−165	9.4	92	0.05	53	0.24	−96
		500	0.58	179	5.7	81	0.07	60	0.21	−104
		1000	0.56	154	2.9	63	0.12	66	0.22	−111
		2000	0.50	109	1.5	38	0.25	60	0.31	−118
		3000	0.52	67	1.1	22	0.37	46	0.38	−136
	100	100	0.62	−121	24.8	116	0.03	46	0.46	−68
		300	0.60	−165	9.3	91	0.05	53	0.23	−96
		500	0.58	179	5.7	81	0.07	61	0.20	−102
		1000	0.56	155	2.9	63	0.12	65	0.22	−109
		2000	0.50	111	1.5	39	0.25	62	0.32	−117
		3000	0.50	68	1.1	23	0.37	47	0.39	−136

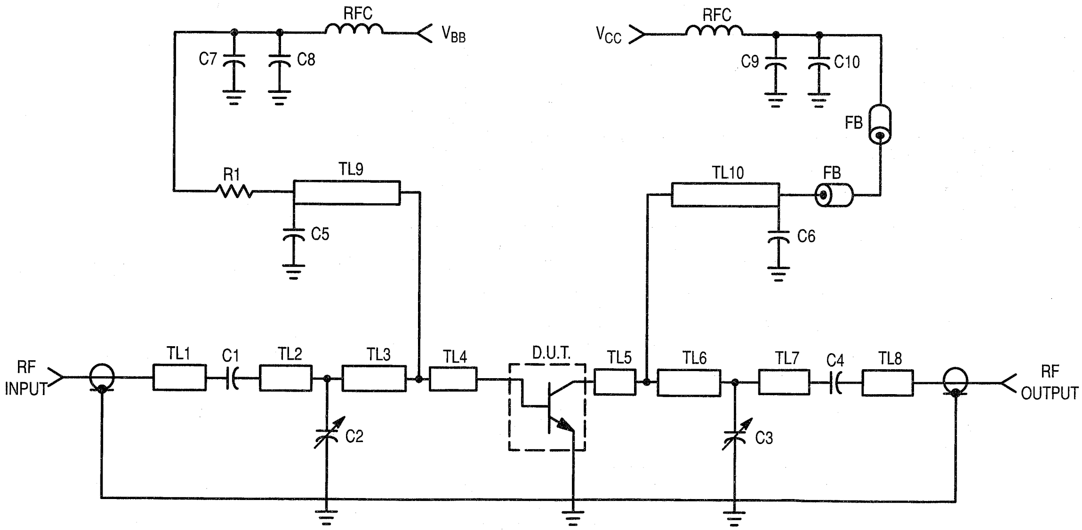
Table 2. MRF5812 Common Emitter S–Parameters



f (MHz)	ΓMS	ΓML	ΓMS NF OPT	G_AMAX (dB)	Rn (Ω)	NF OPT	NF (50 Ω)
500	0.91 ∠ 176°	0.78 ∠ 77°	0.39 ∠ 159°	18	10.5	2.0	2.5

Circuit Per Figure 14

Figure 22. MRF581 Constant Gain Contours Noise Figure Contours



C1, C4, C5, C6, C8, C9 — 1000 pF, Chip Capacitor
C2, C3 — 1.0−10 pF, Johanson Capacitor
C7, C10 — 10 μF, Tantalum Capacitor
R1 — 1.0 kΩ Res.
RFC — VK–200, Ferroxcube
FB — Ferrite Bead, Ferroxcube, 56–590–65/3B
Board Material — 0.0625″ Thick Glass Teflon ε_r = 2.55

TL1, TL7, TL8 — Microstrip 0.162″ x 0.600″
TL2 — Microstrip 0.162″ x 1.000″
TL3 — Microstrip 0.162″ x 0.800″
TL4 — Microstrip 0.162″ x 0.440″
TL5 — Microstrip 0.120″ x 0.440″
TL6 — Microstrip 0.120″ x 1.160″
TL9, TL10 — Microstrip 0.025″ x 4.250″

Figure 23. MRF581 Test Fixture Schematic

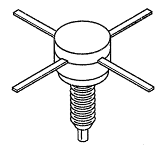
MRF587

The RF Line
NPN Silicon High-Frequency Transistor

. . . designed for use in high–gain, low–noise, ultra–linear, tuned and wideband amplifiers. Ideal for use in CATV, MATV, and instrumentation applications.

- Low Noise Figure —
  NF = 3.0 dB (Typ) @ f = 500 MHz, I_C = 90 mA
- High Power Gain —
  $G_{U(max)}$ = 16.5 dB (Typ) @ f = 500 MHz
- Ion Implanted
- All Gold Metal System
- High f_T — 5.5 GHz
- Low Intermodulation Distortion:
  TB_3 = −70 dB
  DIN = 125 dB µV
- Nichrome Emitter Ballast Resistors

NF = 3.0 dB @ 0.5 GHz
HIGH–FREQUENCY TRANSISTOR
NPN SILICON



CASE 244A–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	17	Vdc
Collector–Base Voltage	V_{CBO}	34	Vdc
Emitter–Base Voltage	V_{EBO}	2.5	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_C = 50°C Derate above T_C = 50°C	P_D	5.0 33	Watts mW/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Junction Temperature	T_J	200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	17	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 1.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	34	—	—	Vdc
Emitter–Base Breakdown Voltage (I_C = 0, I_E = 0.1 mAdc)	$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	—	50	µAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	50	—	200	—

(continued)

NOTE:
1. 300 µs pulse on Tektronix 576 or equivalent.

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 90 mAdc, V_{CE} = 15 Vdc, f = 0.5 GHz)	f_T	—	5.5	—	GHz
Collector–Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	1.7	2.2	pF
FUNCTIONAL TESTS					
Narrowband — Figure 15 (I_C = 90 mA, V_{CC} = 15 V, f = 0.5 GHz)					dB
Noise Figure	NF	—	3.0	4.0	
Power Gain at Optimum Noise Figure	G_{NF}	11	13	—	
Broadband — Figure 16 (I_C = 90 mA, V_{CC} = 15 V, f = 0.3 GHz)					dB
Noise Figure	NF	—	6.3	—	
Power Gain at Optimum Noise Figure	G_{NF}	—	11	—	
Triple Beat Distortion (I_C = 50 mA, V_{CC} = 15 V, P_{Ref} = 50 dBmV) (I_C = 90 mA, V_{CC} = 15 V, P_{Ref} = 50 dBmV)	TB_3	—	−70	—	dB
DIN 45004 (I_C = 90 mA, V_{CC} = 15 V) (I_C = 90 mA, V_{CC} = 15 V)	DIN	—	125	—	dBμV
Maximum Available Power Gain (3) (I_C = 90 mA, V_{CE} = 15 Vdc, f = 0.5 GHz)	G_{Umax}	—	16.5	—	dB

NOTES:

2. Characterized on HP8542 Automatic Network Analyzer
3. $G_{Umax} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

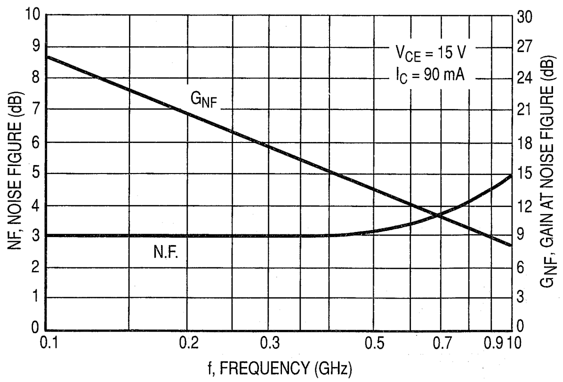


Figure 1. Typical Noise Figure and Associated Gain versus Frequency

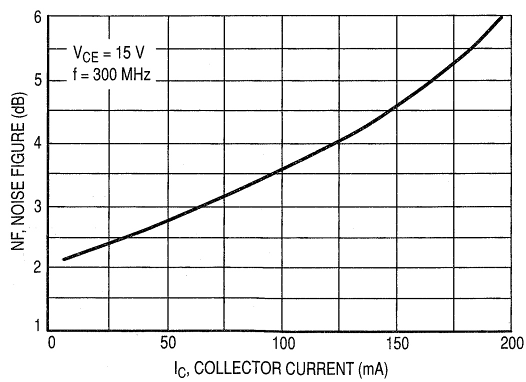


Figure 2. Noise Figure versus Collector Current

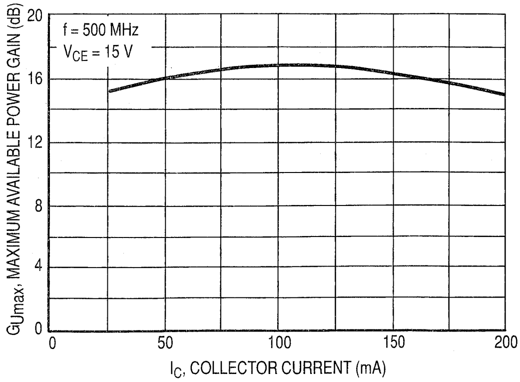


Figure 3. G_{Umax} versus Collector Current

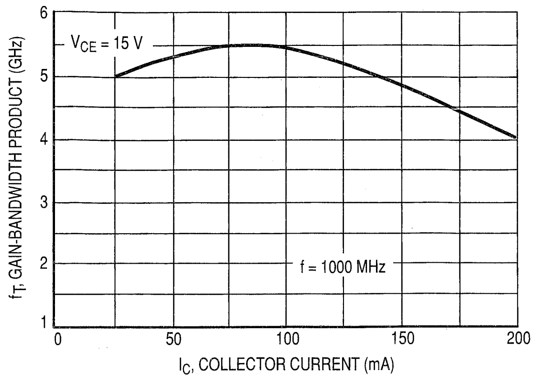


Figure 4. Gain–Bandwidth Product versus Collector Current

TYPICAL PERFORMANCE

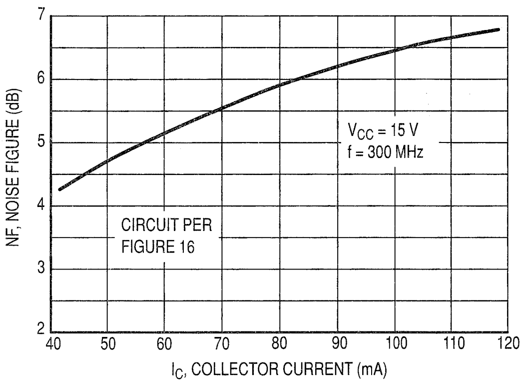


Figure 5. Broadband Noise Figure

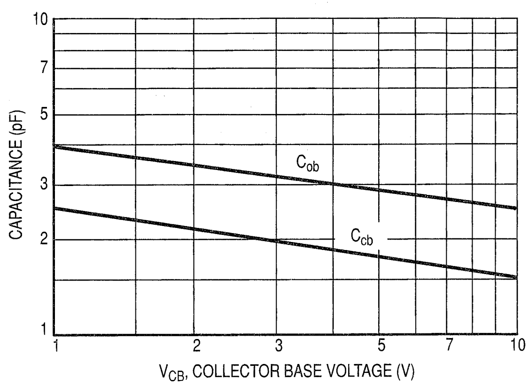


Figure 6. Junction Capacitance versus Voltage

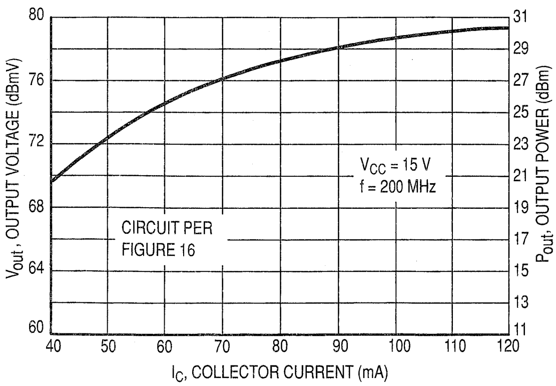


Figure 7. 1.0 dB Compression Point versus Collector Current

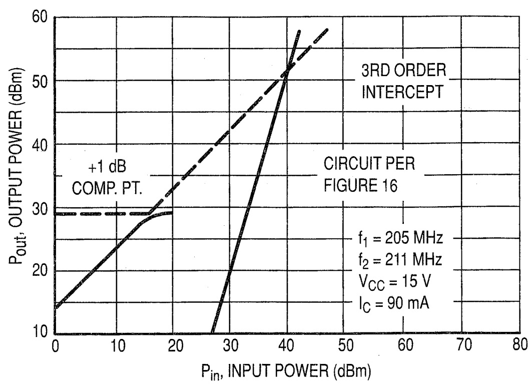


Figure 8. Third Order Intercept Point

TYPICAL PERFORMANCE (continued)

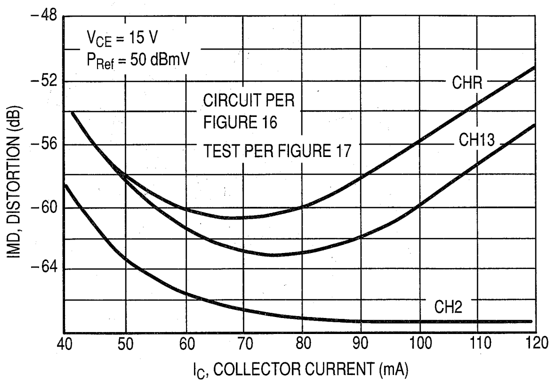


Figure 9. Second Order Distortion versus Collector Current

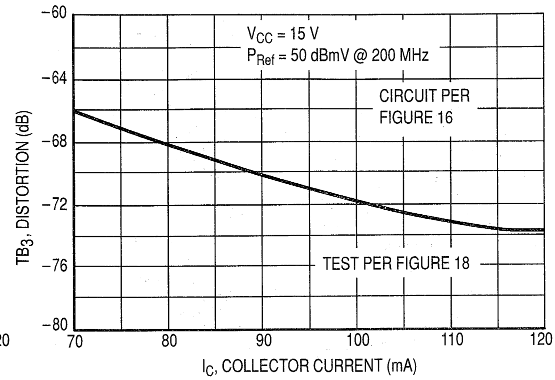


Figure 10. Triple Beat Distortion versus Collector Current

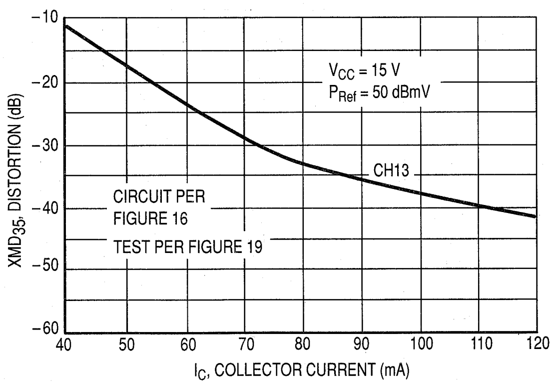


Figure 11. 35–Channel X–Modulation Distortion versus Collector Current

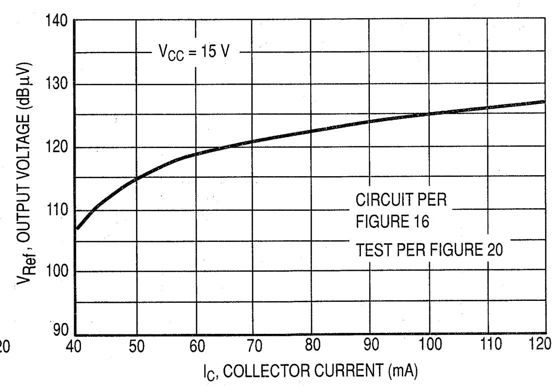


Figure 12. DIN 45004B versus Collector Current

V_{CE} = 15 V I_C = 90 mA

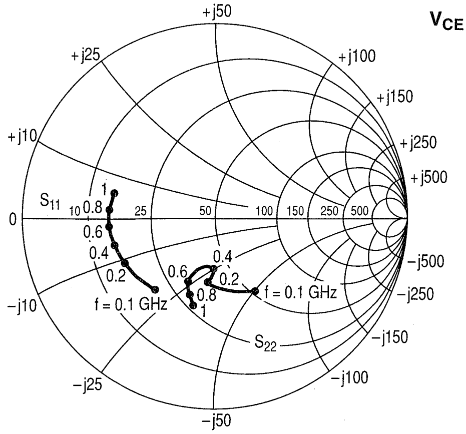


Figure 13. Input/Output Reflection Coefficient versus Frequency (GHz)

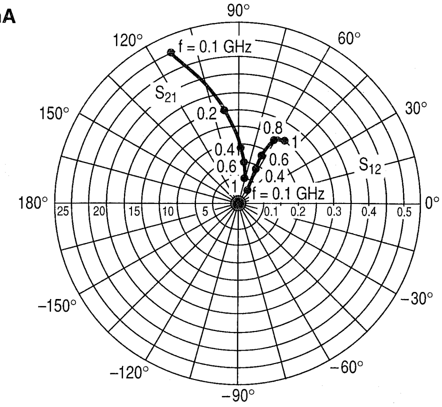


Figure 14. Forward/Reverse Transmission Coefficients versus Frequency (GHz)

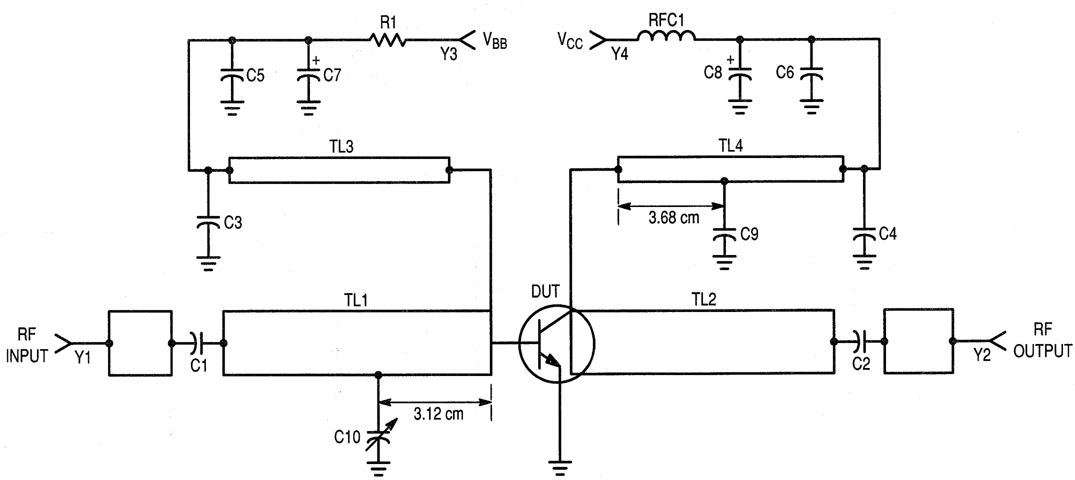
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
5.0	30	100	0.56	−131	16.45	113	0.04	45	0.49	−91
		200	0.58	−159	9.42	98	0.06	49	0.38	−116
		400	0.60	−178	5.00	86	0.08	55	0.35	−132
		600	0.64	170	3.61	76	0.11	56	0.38	−138
		800	0.67	162	2.92	67	0.14	55	0.41	−144
		1000	0.70	155	2.55	58	0.17	54	0.44	−152
	60	100	0.53	−141	17.89	110	0.04	50	0.47	−102
		200	0.56	−164	10.05	97	0.05	55	0.39	−126
		400	0.59	178	5.31	85	0.09	60	0.38	−141
		600	0.63	169	3.82	76	0.12	59	0.40	−146
		800	0.66	161	3.09	67	0.15	57	0.44	−153
		1000	0.69	155	2.67	58	0.18	55	0.47	−160
	90	100	0.52	−145	18.26	109	0.04	52	0.47	−106
		200	0.56	−166	10.20	96	0.05	57	0.39	−130
		400	0.59	177	5.38	85	0.09	62	0.39	−144
		600	0.63	168	3.86	76	0.12	60	0.41	−149
		800	0.66	161	3.12	67	0.15	58	0.45	−155
		1000	0.69	155	2.70	58	0.19	55	0.48	−162
10	30	100	0.53	−122	18.36	115	0.04	48	0.50	−75
		200	0.53	−153	10.63	100	0.05	51	0.36	−96
		400	0.55	175	5.71	87	0.08	57	0.33	−112
		600	0.59	173	4.16	78	0.10	58	0.35	−119
		800	0.62	165	3.37	68	0.13	57	0.39	−127
		1000	0.65	158	2.95	59	0.15	55	0.42	−136
	60	100	0.49	−132	20.19	112	0.03	51	0.46	−85
		200	0.51	−158	11.54	99	0.05	57	0.35	−107
		400	0.53	−178	6.12	87	0.08	61	0.33	−123
		600	0.58	171	4.43	78	0.11	60	0.36	−129
		800	0.60	164	3.58	68	0.14	59	0.40	−136
		1000	0.63	157	3.12	60	0.16	57	0.44	−144
	90	100	0.48	−135	20.82	111	0.03	53	0.45	−88
		200	0.50	−160	11.77	98	0.05	59	0.34	−111
		400	0.53	−179	6.22	86	0.08	63	0.33	−126
		600	0.57	171	4.50	78	0.11	62	0.36	−131
		800	0.60	164	3.64	68	0.14	59	0.41	−139
		1000	0.63	157	3.18	60	0.17	57	0.44	−147

(continued)

Table 1. Common–Emitter S–Parameters

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
15	30	100	0.49	−112	20.34	118	0.04	54	0.51	−52
		200	0.52	−145	11.51	101	0.05	56	0.36	−77
		400	0.48	−164	6.12	87	0.09	63	0.32	−74
		600	0.52	−174	4.19	75	0.12	62	0.32	−90
		800	0.53	177	3.29	68	0.16	61	0.38	−90
		1000	0.53	168	2.76	61	0.20	56	0.47	−90
	60	100	0.45	−122	22.14	115	0.03	56	0.45	−60
		200	0.49	−150	12.24	99	0.05	60	0.33	−86
		400	0.45	−166	6.45	86	0.09	65	0.30	−83
		600	0.50	−175	4.42	75	0.13	63	0.32	−99
		800	0.51	177	3.47	68	0.16	61	0.38	−98
		1000	0.51	168	2.91	62	0.20	55	0.46	−96
	90	100	0.44	−127	22.76	114	0.03	58	0.43	−62
		200	0.48	−152	12.44	98	0.05	62	0.32	−89
		400	0.44	−167	6.55	85	0.09	66	0.29	−85
		600	0.50	−176	4.47	75	0.13	64	0.32	−102
		800	0.51	176	3.51	69	0.17	61	0.38	−100
		1000	0.51	168	2.95	62	0.20	55	0.46	−98

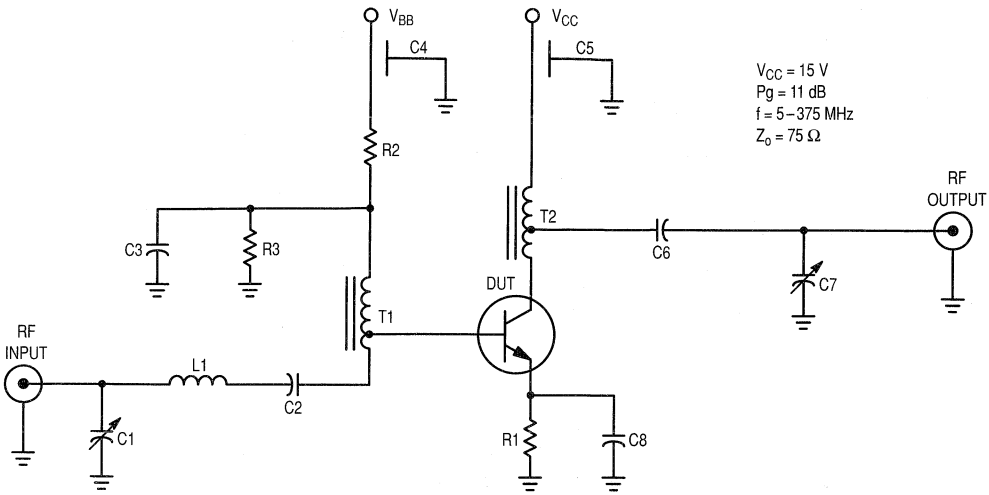
Table 1. Common–Emitter S–Parameters (continued)



C1, C2 — 470 pF Chip (Ceramic)
C3, C4 — 0.018 μF Chip Capacitor
C5, C6 — 0.1 μF Mylar
C7, C8 — 1.0 μF, 25 Vdc Electrolytic
C9 — 91 pF Mini–Unelco (C9 Taped 3.68 cm from Collector Connection on TL4 as shown)
C10 — 35–45 pF Johanson Ceramic Capacitor, JMC 5801 or Equivalent (C10 Taped 3.12 cm from Base Connection on TL1)

R1 — 2.7 kΩ, 1–1/2 W
RFC1 — 0.15 μH Molded Choke
TL1, TL2 — Z_o = 26 Ω, 0.0625 TFG as shown in Photomaster
TL3, TL4 — λ/4 Microstrip, Z_o = 100 Ω
Y1, Y2 — N–Type Connection (Female)
Y3, Y4 — BNC–Type Connector (Female)
Board Material — 0.0625″ Thick Glass Teflon ε_r = 2.5

Figure 15. Narrowband Test Fixture Schematic 500 MHz



C1, C7 — 0.5−10 pF
C2, C6 — 0.001 μF
C3 — 0.01 μF
C4, C5 — 0.01 μF Feedthru
C8 — 12 pF

R1 — 12 Ω 1.0 W (2.0−24 Ω on each emitter port)
R2 — 1.8 k 1/8 W
R3 — 2.2 k 1/8 W
L1 — 1 Turn 0.012 dia #22 AWG
T1(1) — 5 Turns Tapped at 2 Turns, #30 AWG
T2(1) — 8 Turns Tapped at 3 Turns, #30 AWG

(1) Ferroxcube 135 CT050 3D3 Material

Figure 16. Broadband Test Circuit Schematic

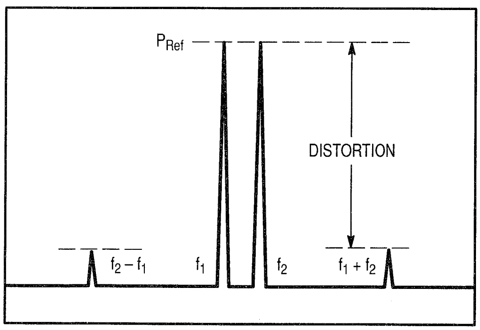


Figure 17. Second Order Distortion Test

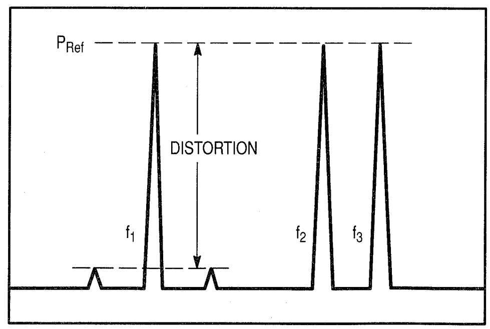


Figure 18. Triple Beat Distortion Test

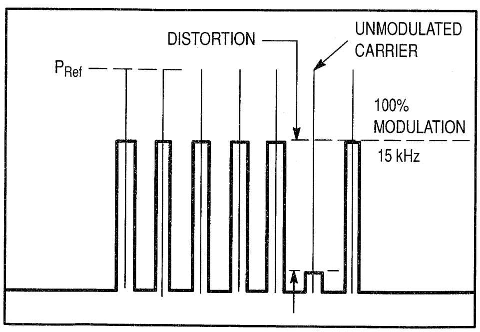


Figure 19. Cross Modulation Distortion Test

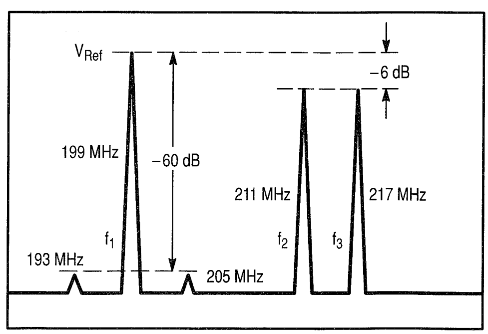


Figure 20. DIN 45004B Intermodulation Test

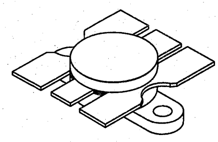
The RF Line
NPN Silicon RF Power Transistor

MRF641

. . . designed for 12.5 Volt UHF large–signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics —
  Output Power = 15 Watts
  Minimum Gain = 7.8 dB
  Efficiency = 55%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Built–In Matching Network for Broadband Operation
- Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 16–Volt High Line and Overdrive

15 W, 470 MHz
CONTROLLED Q
RF POWER
TRANSISTOR
NPN SILICON



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	43.7 0.25	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

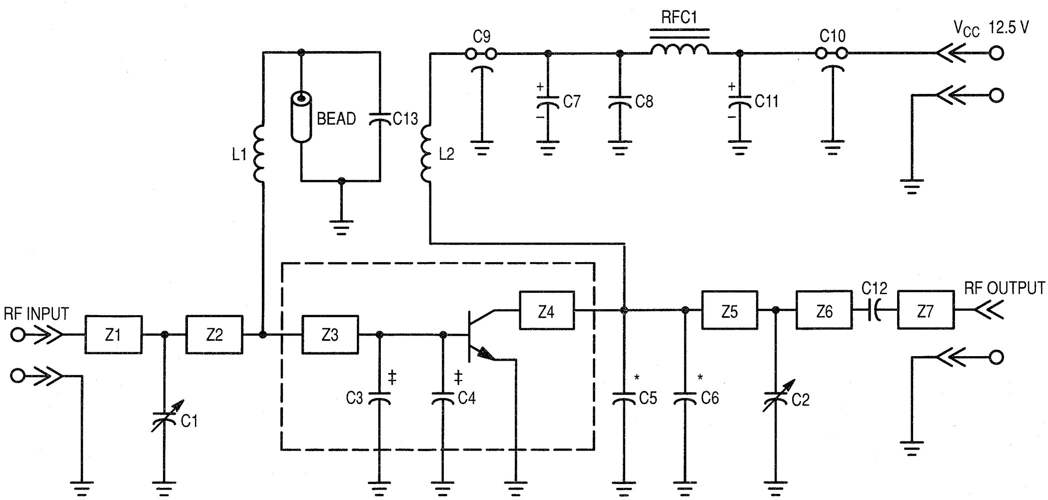
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5.0	mAdc

(continued)

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	30	70	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	40	60	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 470 MHz)	G_{pe}	7.8	8.5	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 470 MHz)	η	55	60	—	%
Output Mismatch Stress (V_{CC} = 16 Vdc, P_{in} = 3.0 W, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ	No Degradation in Output Power			



PARTS

Z1 — 1.225″ x 0.187″ Microstrip
Z2 — 0.884″ x 0.187″ Microstrip
Z3 — Capacitor Block (Base)
Z4 — Collector Block
Z5 — 1.1″ x 0.187″ Microstrip
Z6 — 0.433″ x 0.187″ Microstrip
Z7 — 0.4″ x 0.187″ Microstrip

Dotted Area — Capacitor Assembly

C1, C2 — 0.8–10 pF Johanson
C3, C4 — 24 pF Chip Caps 100 mils ATC
C5, C6 — 22 pF Chip Caps 100 mils ATC
C12 — 220 pF Chip Cap 100 mils ATC
C7, C11 — 1.0 µF Tantalum 35 Vdc
C9, C10 — 680 pF Feedthrough Allen–Bradley
C13 — 200 pF UNELCO
C8 — 0.1 µF, 50 V Erie Red Cap
RFC1 — VK 200 — 104B Ferrite Choke
L1 — 4 Turns 0.2″ Dia. #16 AWG
L2 — 9 Turns 0.15″ Dia. #16 AWG

Bead — Ferroxcube 56–590–65–35EB

NOTES

*C5, C6, are mounted as close to the capacitor assembly as possible.
‡‡C3, C4 are mounted in the capacitor assembly.
Board — 62.5 mil Glass Teflon, ε_r = 2.55.

Figure 1. Test Circuit Schematic

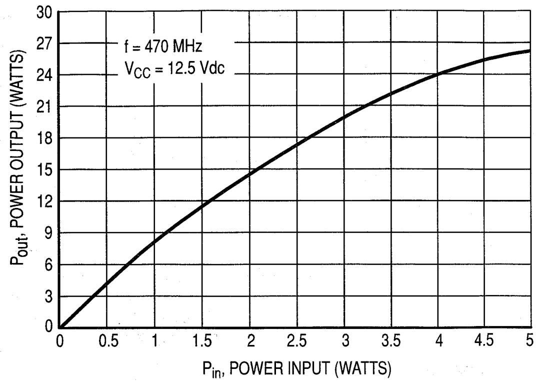


Figure 2. Power Output versus Power Input

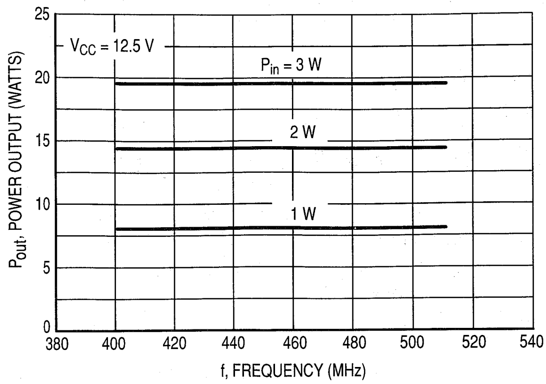


Figure 3. Power Output versus Frequency

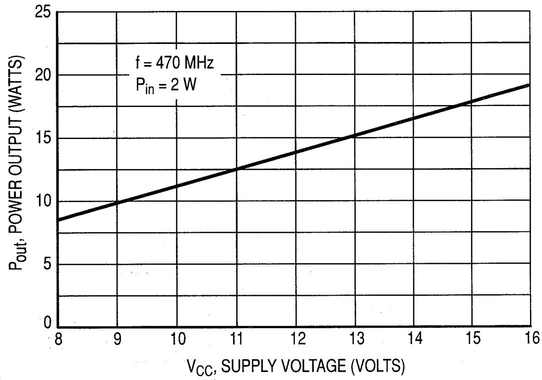


Figure 4. Power Output versus Supply Voltage

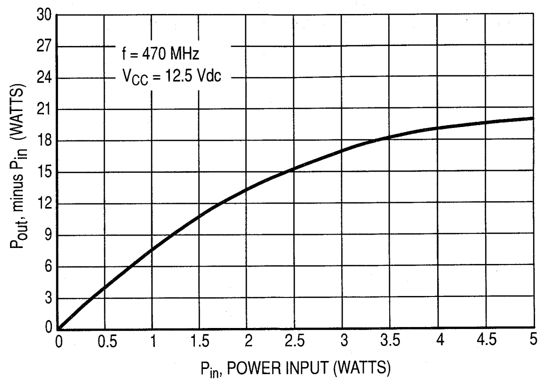
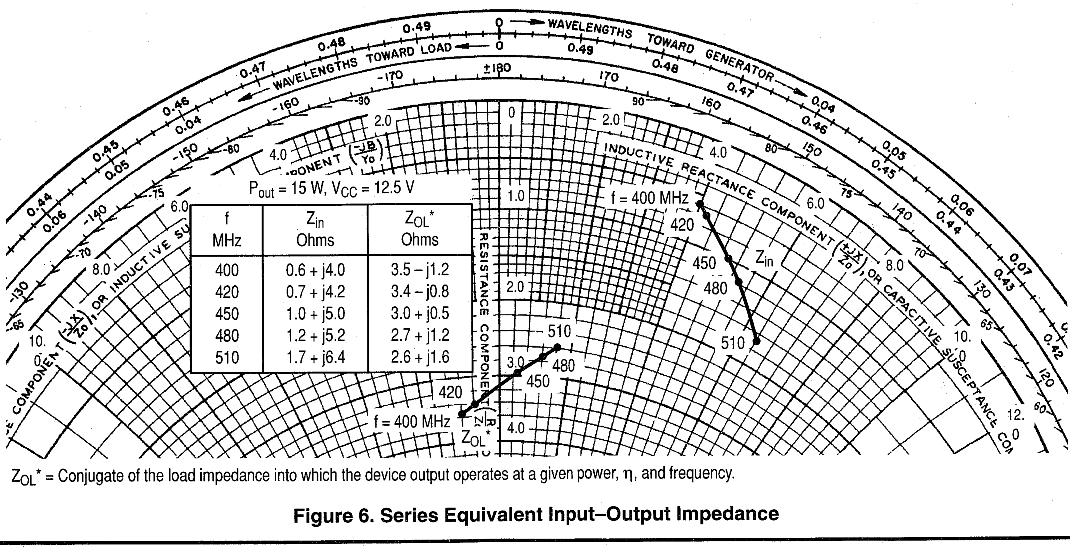


Figure 5. Power Saturation Profile



f MHz	Zin Ohms	ZOL* Ohms
400	0.6 + j4.0	3.5 – j1.2
420	0.7 + j4.2	3.4 – j0.8
450	1.0 + j5.0	3.0 + j0.5
480	1.2 + j5.2	2.7 + j1.2
510	1.7 + j6.4	2.6 + j1.6

Z_{OL}* = Conjugate of the load impedance into which the device output operates at a given power, η, and frequency.

Figure 6. Series Equivalent Input–Output Impedance

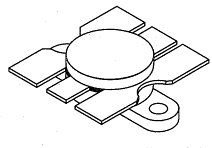
The RF Line
NPN Silicon RF Power Transistor

MRF644

. . . designed for 12.5 Volt UHF large–signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics —
  Output Power = 25 Watts
  Minimum Gain = 6.2 dB
  Efficiency = 60%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Built–In Matching Network for Broadband Operation
- Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 16–Volt High Line and 50% Overdrive
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**25 W, 470 MHz
CONTROLLED Q
RF POWER
TRANSISTOR
NPN SILICON**



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	103 0.59	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5.0	mAdc

(continued)

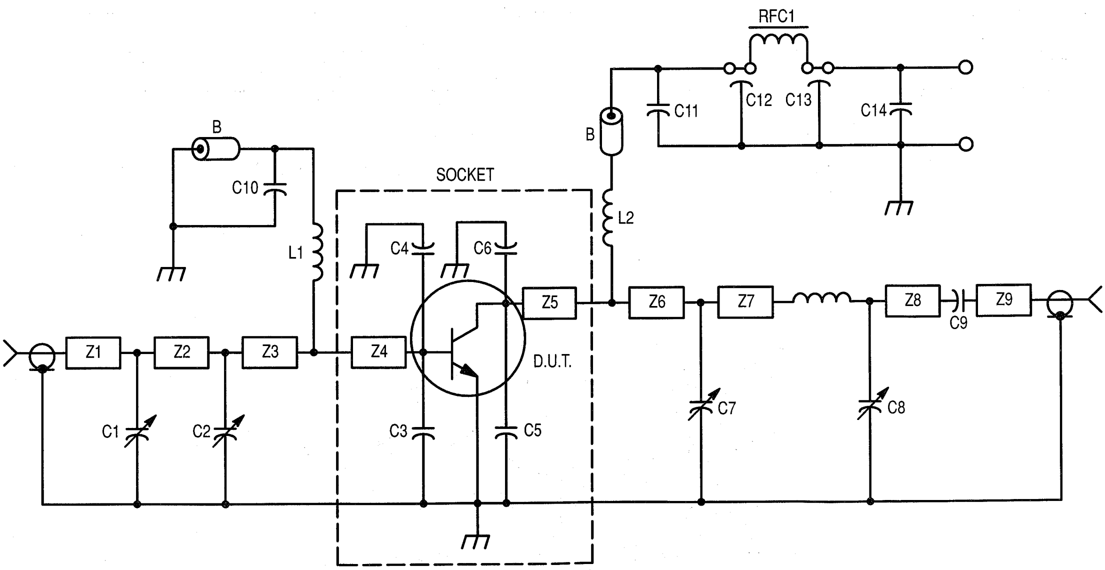
REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	70	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	60	85	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 25 W, I_C (MAX) = 3.6 Adc, f = 470 MHz)	G_{pe}	6.2	7.0	—	dB
Input Power (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 470 MHz)	P_{in}	—	5.0	6.0	Watts
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 25 W, I_C (MAX) = 3.6 Adc, f = 470 MHz)	η	55	60	—	%
Output Mismatch Stress (V_{CC} = 16 Vdc, P_{in} = Note 1, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ *	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 470 MHz)	Z_{in}	—	1.2 + j3.3	—	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 470 MHz)	Z_{OL}	—	1.9 + j2.1	—	Ohms

NOTE:
1. P_{in} = 150% of Drive Requirement for 25 W Output at 12.5 Vdc.

* ψ = Mismatch stress factor — the electrical criterion established to verify the device resistance to load mismatch failure. The mismatch stress test is accomplished in the standard test fixture (Figure 1) terminated in a 20:1 minimum load mismatch at all phase angles.



C1, C2, C7, C8 — 1.0–20 pF Johanson Variable
C3 — 27 pF 100 mil ATC
C4 — 30 pF 100 mil ATC
C5, C6 — 33 pF 100 mil ATC
C9 — 250 pF 100 mil ATC
C10 — 100 pF UNELCO
C11, C14 — 1.0 µF 35 V TANTALUM
C12, C13 — 680 pF Feedthrough
L1 — 5″ #22 AWG 0.100″ ID
L2 — 5″ #20 AWG 0.187″ ID
RFC1 — Ferroxcube VK200–20–4B
B — Ferroxcube Bead 56–590–65–3B
Z1 — 0.25″ x 0.20″ Microstrip
Z2 — 1.63″ x 0.20″ Microstrip
Z3 — 0.20″ x 0.20″ Microstrip
Z4, Z5 — 1/2″ #18 AWG bent in a "V" shape 1/8″ Wide
Z6 — 0.20″ x 0.20″ Microstrip
Z7 — 0.70″ x 0.20″ Microstrip
Z8 — 0.33″ x 0.20″ Microstrip
Z9 — 0.50″ x 0.20″ Microstrip
Board — 62.5 mil Glass Teflon, ε_r = 2.55

Figure 1. Test Circuit Schematic

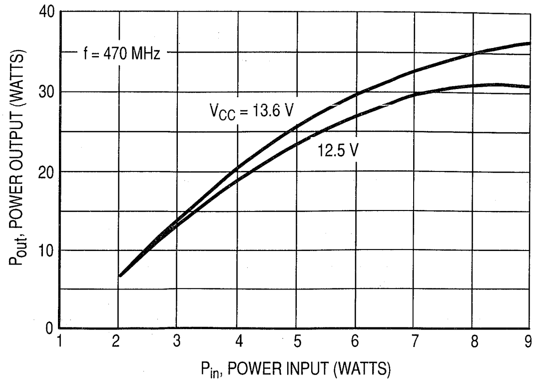


Figure 2. Power Output versus Power Input

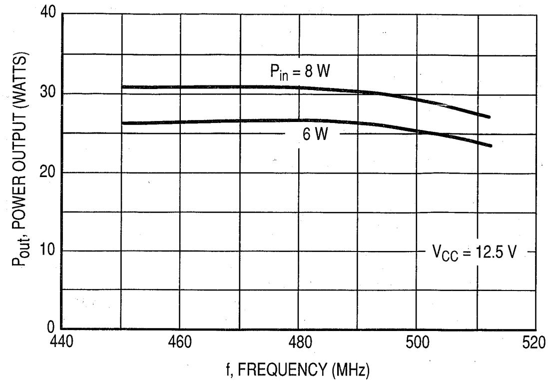


Figure 3. Power Output versus Frequency

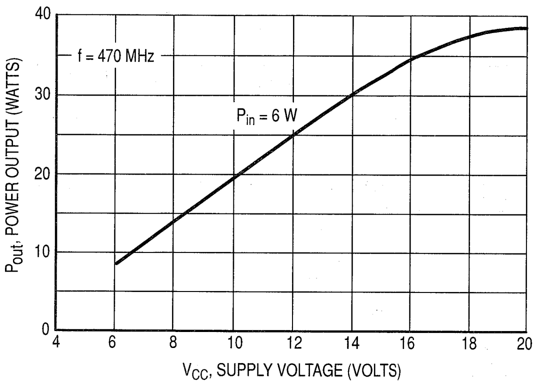


Figure 4. Power Output versus Supply Voltage

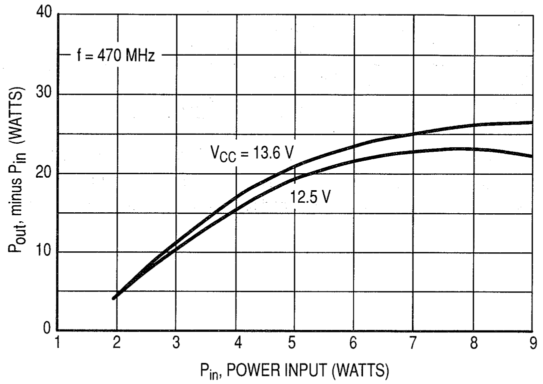
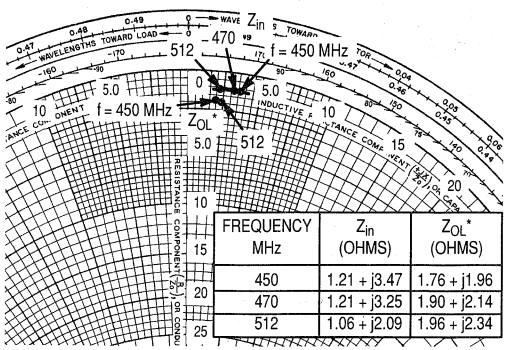


Figure 5. Power Saturation Profile



FREQUENCY MHz	Z_{in} (OHMS)	Z_{OL}* (OHMS)
450	1.21 + j3.47	1.76 + j1.96
470	1.21 + j3.25	1.90 + j2.14
512	1.06 + j2.09	1.96 + j2.34

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Input–Output Impedance

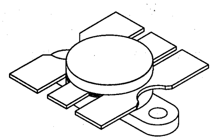
The RF Line
NPN Silicon RF Power Transistor

MRF650

**50 W, 512 MHz
RF POWER
TRANSISTOR
NPN SILICON**

Designed for 12.5 Volt UHF large–signal amplifier applications in industrial and commercial FM equipment operating to 520 MHz.

- Guaranteed 440, 470, 512 MHz 12.5 Volt Characteristics
  Output Power = 50 Watts
  Minimum Gain = 5.2 dB @ 440, 470 MHz
  Efficiency = 55% @ 440, 470 MHz
  IRL = 10 dB
- Characterized with Series Equivalent Large–Signal Impedance Parameters from 400 to 520 MHz
- Built–In Matching Network for Broadband Operation
- Triple Ion Implanted for More Consistent Characteristics
- Implanted Emitter Ballast Resistors
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 15.5 Vdc, 2.0 dB Overdrive
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16.5	Vdc
Collector–Emitter Voltage	V_{CES}	38	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	12	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	135 0.77	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16.5	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	38	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	70	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	135	170	pF

(continued)

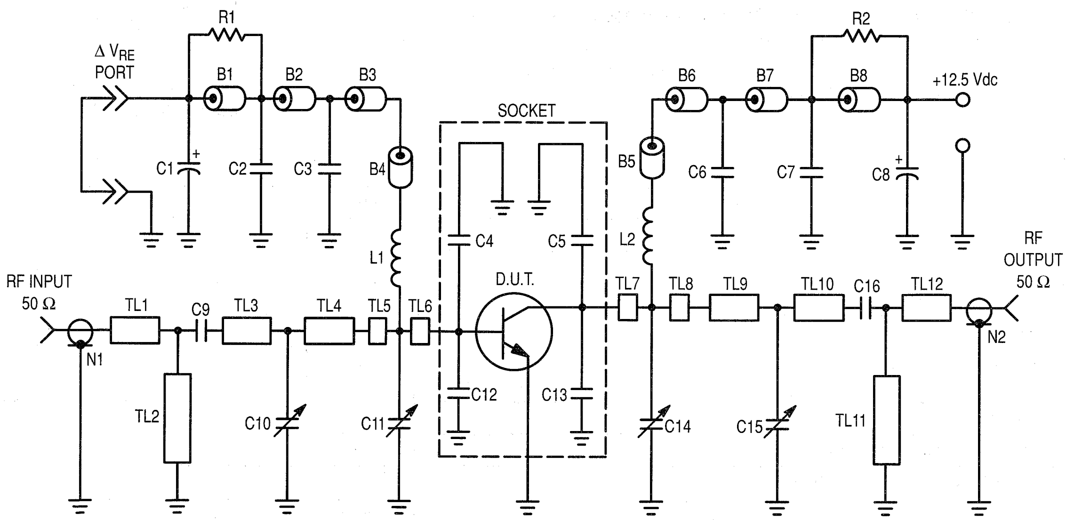
REV 8

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture. See Figure 1.)					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 50 W, f = 440, 470 MHz)	G_{pe}	5.2	6.1	—	dB
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 50 W, f = 512 MHz)	G_{pe}	5.0	5.9	—	dB
Input Return Loss (V_{CC} = 12.5 Vdc, P_{out} = 50 W, f = 440, 470, 512 MHz)	IRL	10	15	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 50 W, f = 440, 470 MHz)	η	55	65	—	%
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 50 W, f = 512 MHz)	—	50	60	—	%
Output Mismatch Stress (V_{CC} = 15.5 V, 2.0 dB Overdrive, f = 470 MHz, VSWR = 20:1, All Phase Angles) (1)	ψ (2)	No Degradation in Output Power			

NOTES:

1. P_{in} = 2.0 dB above drive requirement for 50 W output at 12.5 Vdc.
2. ψ = Mismatch stress factor — the electrical criterion established to verify the device resistance to load mismatch failure. The mismatch stress test is accomplished in the standard test fixture (Figure 1) terminated in a 20:1 minimum load mismatch at all phase angles.



B1, B8 — Ferrite Bead Ferroxcube VK200 20–4B
B2, B3, B4, B5, B6, B7 — Ferrite Bead Ferroxcube #56–590–3B
C1, C8 — 10 µF, 25 V, 25%, Electrolytic, ECS TE–1204
C2, C7 — 1000 pF, Chip Cap, 5%, ATC 100B102JC50
C3, C6 — 91 pF, 5%, Mica, SAHA 3HS0006–91
C4, C5, C12, C13 — 36 pF, 5%, SAHA 3HS0006–36
C9, C16 — 220 pF, Chip Cap, 5%, ATC 100B221JC200
C10, C11, C15 — 0.8–10 pF, Variable, Johanson JMC501 PG26J200
C14 — 1.0–20 pF, Variable, Johanson JMC5501 PG26J200
L1, L2 — 3 Turns, 18 AWG, 0.19″ ID — Total Length 3.5″
N1, N2 — N Coaxial Conn., Omni–Spectra 3052–1648–10
R1, R2 — 10 Ohm, 10%, 1.0 W, Carbon, RCA 831010

TL1, TL12 — Z_o = 50 Ohm
TL2 — See Photomaster
TL3 — See Photomaster
TL4 — See Photomaster
TL5 — See Photomaster
TL6 — See Photomaster
TL7 — See Photomaster
TL8 — See Photomaster
TL9 — See Photomaster
TL10 — See Photomaster
TL11 — See Photomaster

Transmission Line Boards: 1/16″ Glass–Teflon
Keene GX–0600–55–22
2 oz. Cu Clad Both Sides
ε_r = 2.55

Bias Boards: 1/16″ G10 or Equivalent
2 oz. Cu Clad Double Sided

Figure 1. 440 to 512 MHz Broadband Test Circuit Schematic

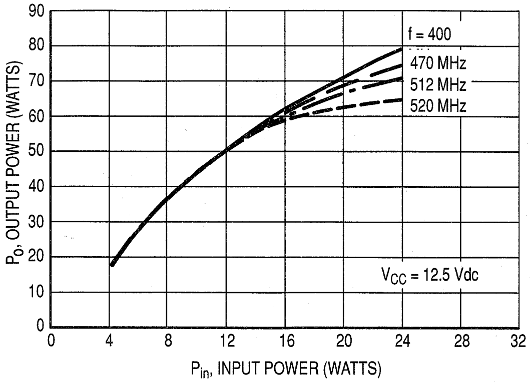


Figure 2. Output Power versus Input Power

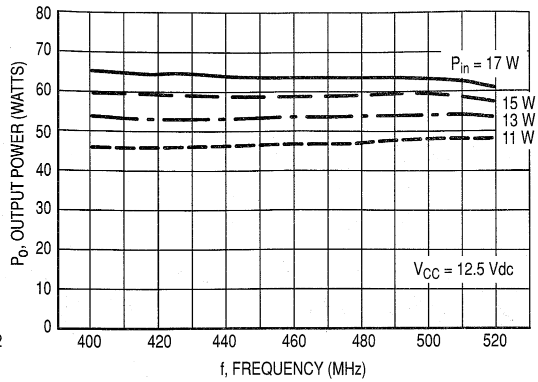


Figure 3. Output Power versus Frequency

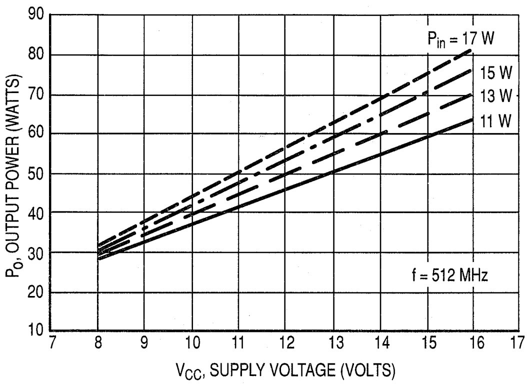


Figure 4. Output Power versus Supply Voltage

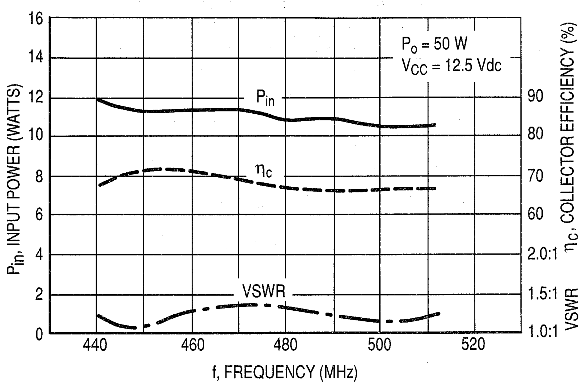
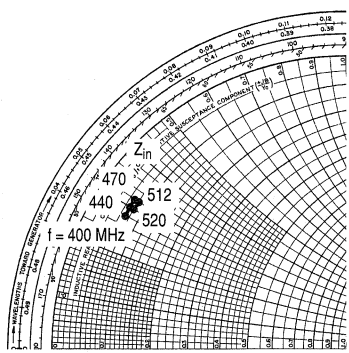


Figure 5. Broadband Performance for P_o = 50 W

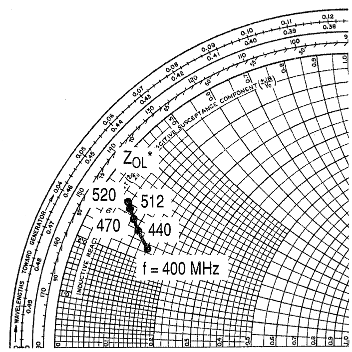


P_{out} = 50 W, V_{CC} = 12.5 Vdc

TUNED FOR MAXIMUM GAIN AT P_o = 50 W

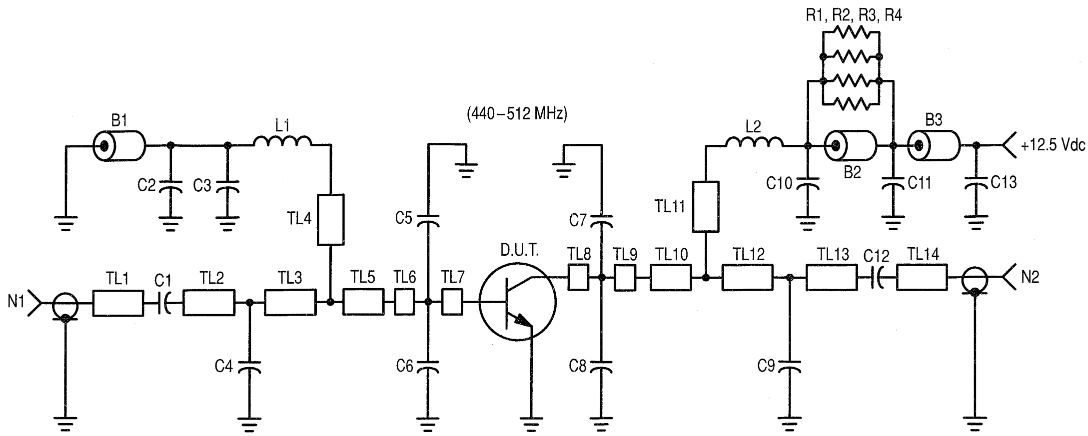
f (MHz)	Z_{in} Ω	Z_{OL}* Ω
400	0.7 + j2.8	1.4 + j2.3
440	0.7 + j3.2	1.1 + j2.6
470	0.8 + j3.3	0.8 + j2.7
512	0.8 + j3.2	0.7 + j2.9
520	0.7 + j3.0	0.6 + j3.0

NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively.



Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 6. Input and Output Impedance Normalized to 10 Ohms Circuit Tuned for Maximum Gain @ P_o = 50 W



B1, B2 — Ferrite Bead Fair Rite Products Corp.
B3 — Ferrite Bead Fair Rite Products Corp.

C2, C11 — 820 pF, 5%
C3, C10 — 91 pF, 5%, Mica, SAHA 3HS0006–91
C1, C12 — 220 pF, 5%, Murata Erie
C4 — 9.1 pF, 5%, Murata Erie
C5, C6, C7, C8 — 43 pF, 5%, Mica SAHA 3HS0006–43
C9 — 10 pF, 5%, Murata Erie
C13 — 10 μF, Electrolytic, 50 V, Panasonic

L1 — 7 Turns, 24 AWG, ID Dia. 0.116″
L2 — 5 Turns, 18 AWG, ID Dia. 0.165″

N1, N2 — SMA Flange Mount, Omni–Spectra 2052–1618–02

R1, R2, R3, R4 — 39 Ohm 1/8 W 5% Rohm

TL1 — Z_o = 50 Ohm
TL2 — Z_o = 50 Ohm
TL3 — Z_o = 50 Ohm
TL4 — See Photomaster
TL5 — Z_o = 50 Ohm
TL6 — See Photomaster
TL7 — See Photomaster
TL8 — See Photomaster
TL9 — See Photomaster
TL10 — Z_o = 50 Ohm
TL11 — See Photomaster
TL12 — Z_o = 50 Ohm
TL13 — Z_o = 50 Ohm
TL14 — Z_o = 50 Ohm

Board Material: 1/16″ G10, ε_r = 4.5
2 oz. Cu Clad Both Sides

Figure 7. Schematic of Broadband Demonstration Amplifier (3)

PERFORMANCE CHARACTERISTICS OF BROADBAND DEMONSTRATION AMPLIFIER

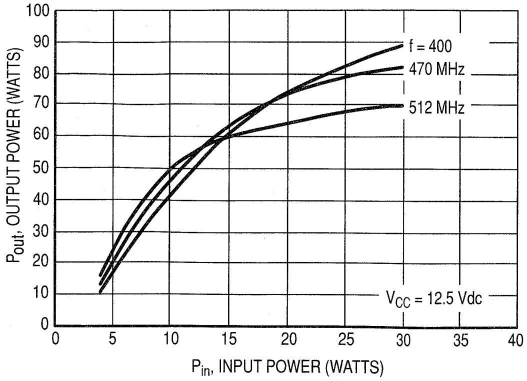


Figure 8. Output Power versus Input Power

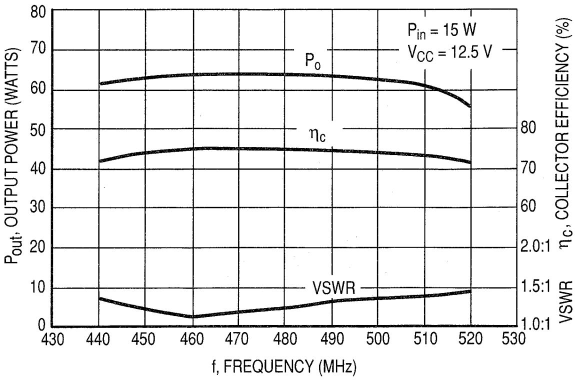


Figure 9. P_o, η_c and VSWR versus Frequency

(3) Detailed design and performance information available from Motorola upon request.

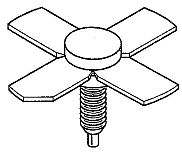
The RF Line
NPN Silicon RF Power Transistors

MRF652
MRF652S

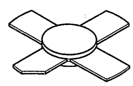
Designed for 12.5 Vdc UHF large–signal, amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Guaranteed 12.5 Volt, 512 MHz Characteristics
  Output Power = 5.0 Watts
  Minimum Gain = 10 dB
  Efficiency = 65% (Typ)
- Typical Performance at 512 MHz, 12.5 V, 5.0 W Output = 6.0 dB
- Series Equivalent Large–Signal Characterization
- Gold Metallized, Emitter Ballasted for Long Life and Reliability
- Capable of 30:1 VSWR Load Mismatch at 15.5 V Supply Voltage
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

5.0 W, 512 MHz
RF POWER
TRANSISTORS
NPN SILICON



CASE 244–04, STYLE 1
MRF652



CASE 249–06, STYLE 1
MRF652S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 143	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

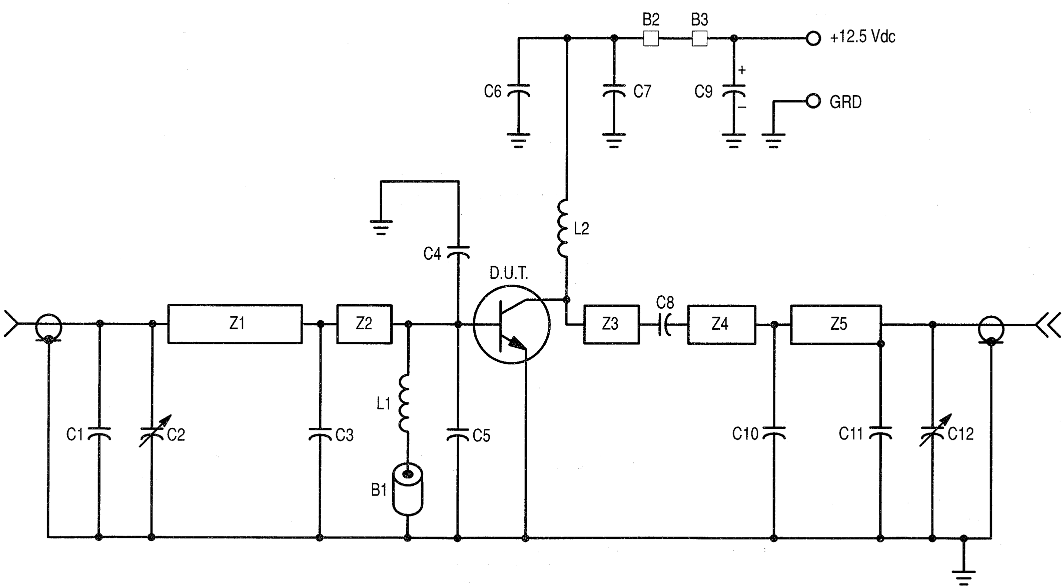
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mAdc, I_E = 0)	$V_{(BR)CBO}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0)	I_{CES}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	150	—

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	9.5	15	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 5.0 W) f = 512 MHz f = 870 MHz	G_{pe}	10 —	11 6.0	— —	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 5.0 W, f = 512 MHz)	η	60	65	—	%
Load Mismatch (V_{CC} = 15.5 Vdc, P_{in} = 500 mW, f = 512 MHz, VSWR = 30:1, At All Phase Angles)	ψ	No Degradation in Output Power			



B1, B2, B3 — Ferrite Bead
C1 — 7.0 pF Unelco Mica
C2 — 1.0–6.0 pF Johanson Variable 5201
C3 — 15 pF Unelco Mica
C4 — 43 pF Mini–Underwood Mica
C5 — 56 pF Mini–Underwood Mica
C6 — 1000 pF Unelco Mica
C7 — 0.1 µF Ceramic
C8 — 68 pF Mini–Underwood Mica
C9 — 1.0 µF Electrolytic 25 V
C10, C11 — 5.0 pF Unelco Mica
C12 — 1.0–10 pF Johanson Variable 5501
L1, L2 — 6 Turns, 20 AWG Wire 0.125″ ID
Z1, Z2 — 25 Ohm µStripline
Z3, Z4, Z5 — 50 Ohm µStripline
Board — 0.032″ Glass–Teflon

Figure 1. 440–512 MHz Broadband Test Circuit

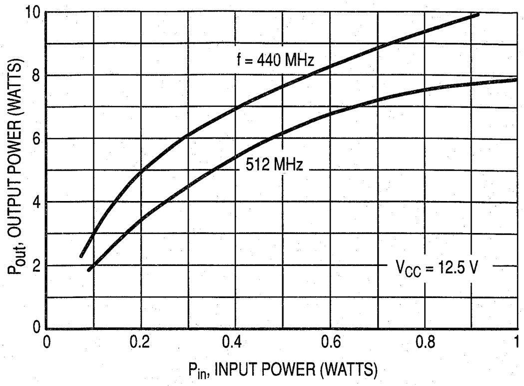


Figure 2. Output Power versus Input Power

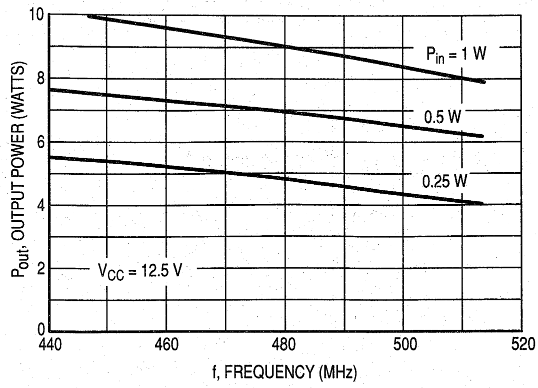


Figure 3. Output Power versus Frequency

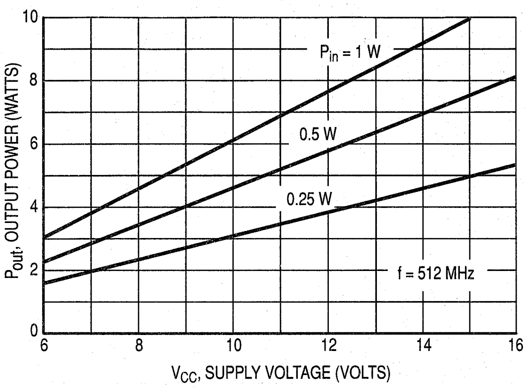


Figure 4. Output Power versus Supply Voltage

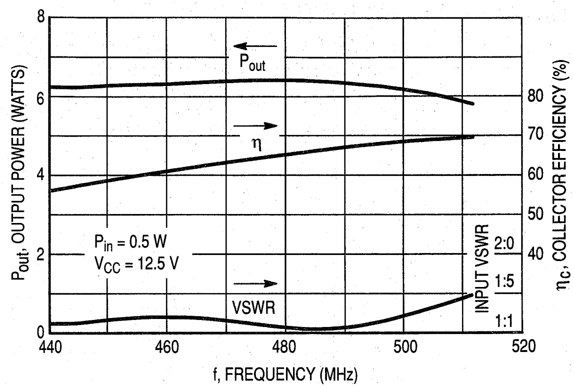
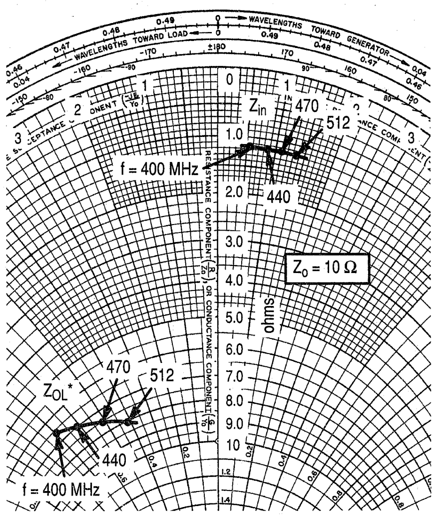


Figure 5. Typical Broadband Circuit Performance



V_{CC} = 12.5 Vdc
P_{out} = 5.0 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	1.18 + j0.54	6.7 – j6.9
440	1.19 + j0.88	7.05 – j6.1
470	1.19 + j1.11	7.6 – j5.1
512	1.19 + j1.35	8.1 – j4.1

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Input/Output Impedance

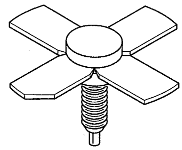
The RF Line
NPN Silicon RF Power Transistor

MRF653

Designed for 12.5 Volt UHF large–signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 512 MHz Characteristics
  Output Power = 10 W
  Gain = 8.0 dB (Typ)
  Efficiency = 65% (Typ)
- Gold Metallized, Emitter Ballasted for Long Life and Reliability
- Capable of 20:1 VSWR Load Mismatch at 16 V Supply Voltage
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

10 W, 512 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 244–04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16.5	Vdc
Collector–Base Voltage	V_{CBO}	38	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	2.75	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	44 0.25	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

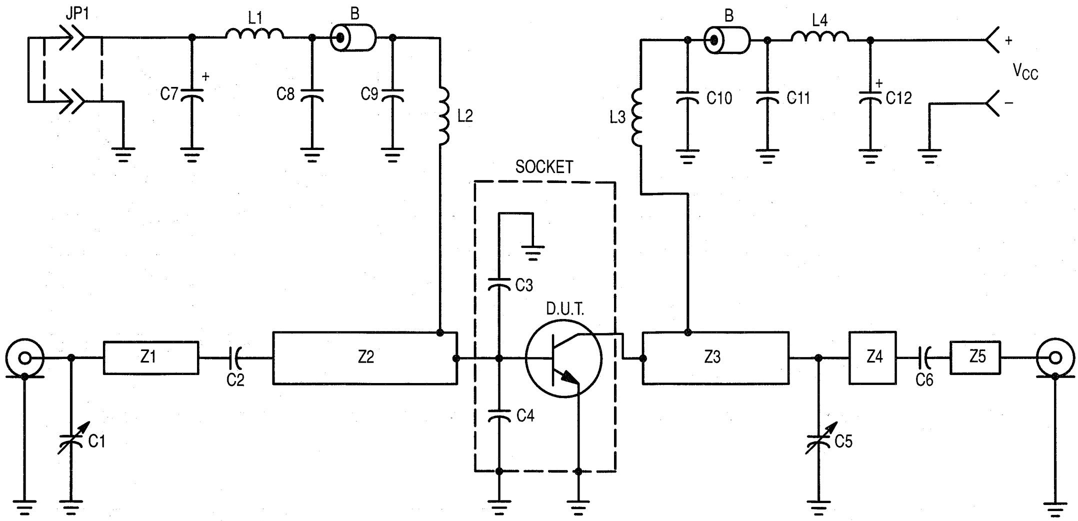
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16.5	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	38	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0)	I_{CES}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	22	28	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 10 W, f = 512 MHz)	G_{pe}	7.0	8.0	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 10 W, f = 512 MHz)	η_c	55	65	—	%
Load Mismatch Stress (V_{CC} = 16 Vdc, f = 512 MHz, P_{in} (1) = 2.6 W, VSWR = 20:1, All Phase Angles)	ψ	No Degradation in Output Power			

NOTE:
1. P_{in} = 2.0 dB over the typical input power required for 10 W output power @ 12.5 Vdc.

REV 8



C1, C5 — 1.0–20 pF, Johanson
C2, C6 — 330 pF, 100 Mil ATC
C3, C4 — 36 pF, Mini–Unelco
C7, C12 — 10 µF, 35 V, Tantalum
C8, C11 — 0.1 µF, Ceramic
C9, C10 — 91 pF, Mini–Unelco

L1, L4 — 4–1/2 Turns, #18 AWG, 0.16″ ID
L2, L3 — 2 Turns, #18 AWG, 0.16″ ID
B — Ferrite Bead, Ferroxcube 56–590–65–3B
Z1 — 51 x 630 mils
Z2 — 162 x 1300 mils
Z3 — 210 x 1350 mils
Z4 — 210 x 280 mils
Z5 — 51 x 300 mils
Board Material — 0.032″ epoxy glass G10, 1 oz., copper clad, double sided, $\varepsilon_r = 5$
JP1 — Jumper, #14 AWG w/Banana Plugs

Figure 1. Broadband Test Circuit Schematic

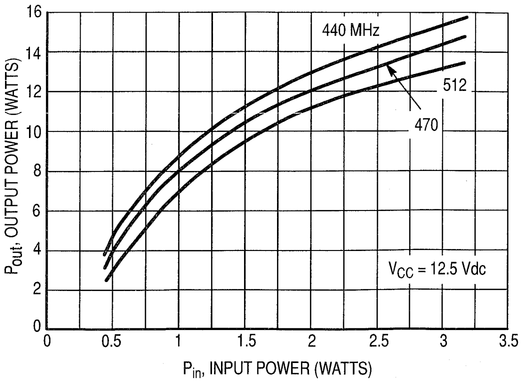


Figure 2. Output Power versus Input Power

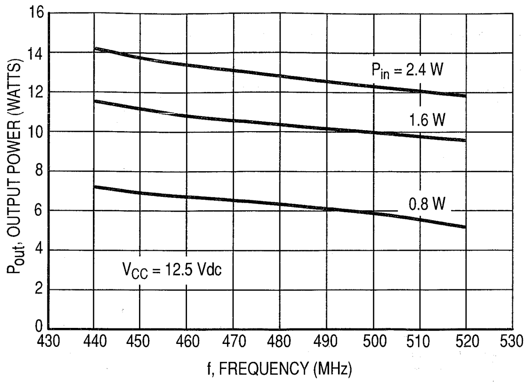


Figure 3. Output Power versus Frequency

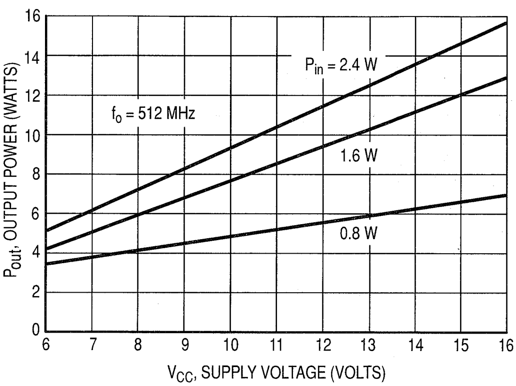


Figure 4. Output Power versus Supply Voltage

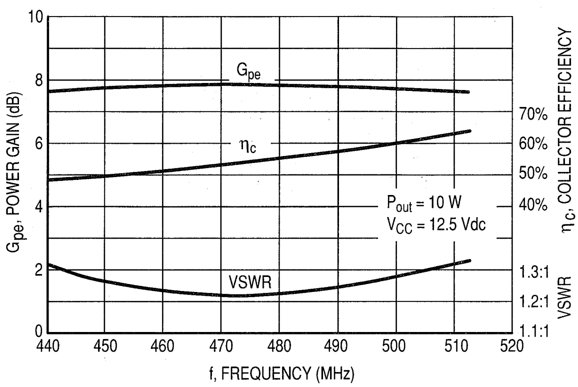
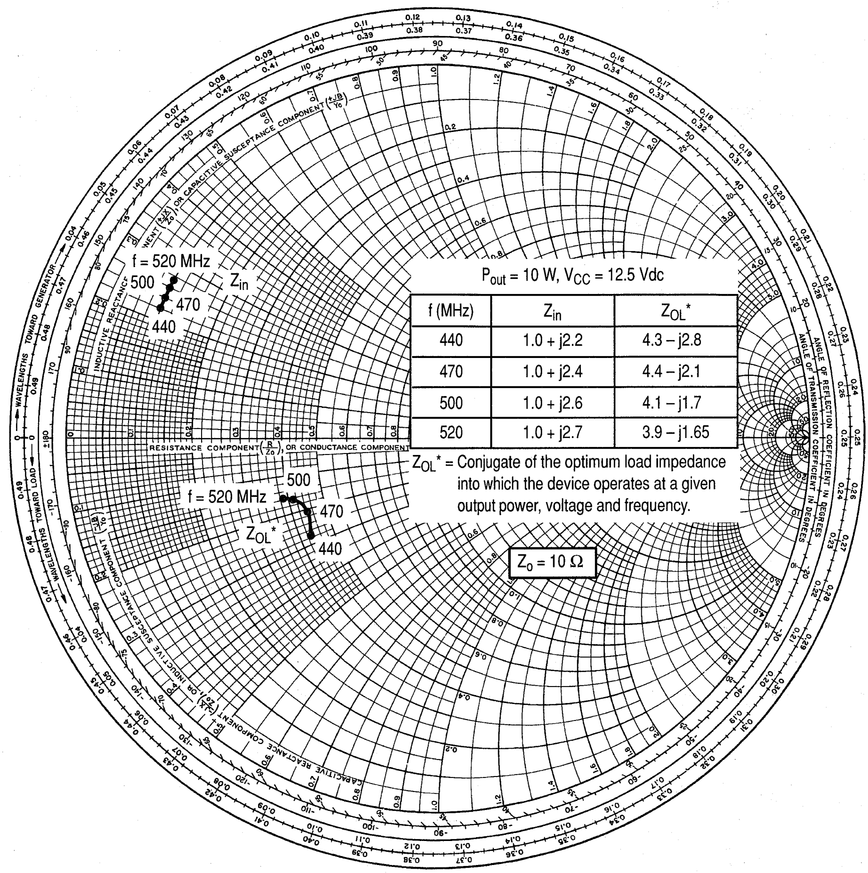


Figure 5. Typical Broadband Circuit Performance



P_{out} = 10 W, V_{CC} = 12.5 Vdc

f (MHz)	Z_{in}	Z_{OL}*
440	1.0 + j2.2	4.3 – j2.8
470	1.0 + j2.4	4.4 – j2.1
500	1.0 + j2.6	4.1 – j1.7
520	1.0 + j2.7	3.9 – j1.65

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Input and Output Impedance

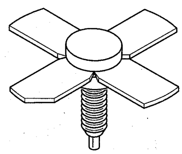
The RF Line
NPN Silicon RF Power Transistor

MRF654

. . . designed for 12.5 Volt UHF large–signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 512 MHz Characteristics
  Output Power = 15 W
  Minimum Gain = 7.8 dB
  Efficiency = 55%
- Built–In Matching Network for Broadband Operation
- Gold Metallized, Emitter Ballasted for Long Life and Reliability
- Capable of 20:1 VSWR Load Mismatch at 15.5 V Supply Voltage
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**15 W, 470 MHz
RF POWER
TRANSISTOR
NPN SILICON**



CASE 244–04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	44 0.25	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.0	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted.)

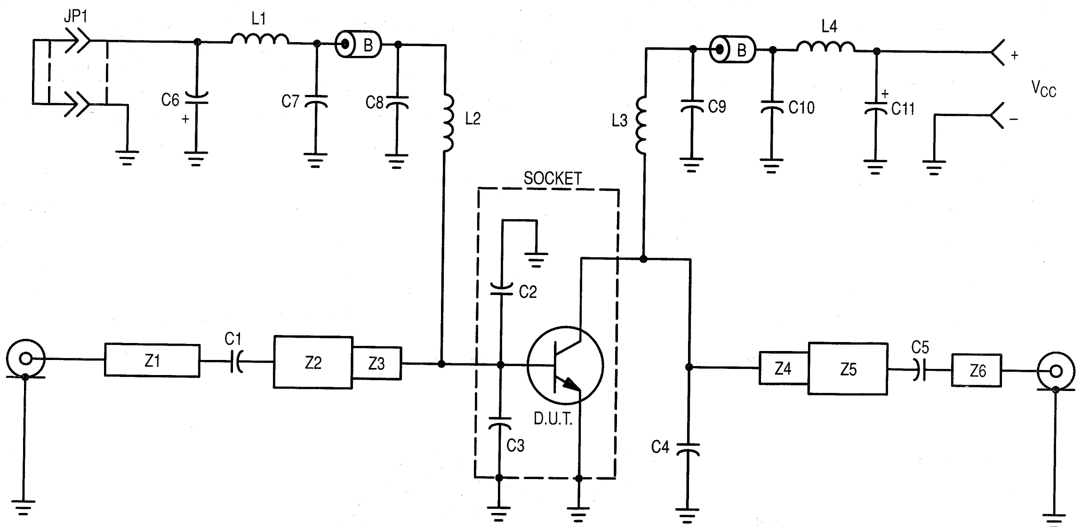
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage ($I_C = 25$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage ($I_C = 25$ mAdc, $V_{BE} = 0$)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage ($I_E = 5.0$ mAdc, $I_C = 0$)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector–Cutoff Current ($V_{CE} = 15$ Vdc, $V_{BE} = 0$)	I_{CES}	—	—	2.0	mAdc

(continued)

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	31	45	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 512 MHz)	G_{pe}	7.8	8.8	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 512 MHz)	η	55	63	—	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, f = 512 MHz, P_{in} = 3.0 W, VSWR = 20:1, All Phase Angles)	ψ	No Degradation in Output Power			



C1, C5 — 68 pF Mini–Unelco
C2, C3 — 33 pF, Mini–Unelco
C4 — 47 pF, Mini–Unelco
C6, C11 — 10 µF, 25 V Tantalum
C7, C10 — 0.1 µF, Ceramic
C8, C9 — 91 pF, Mini–Unelco
L1, L4 — 4–1/2 Turns, #18 AWG, Enamel Covered, 0.16″ ID
L2, L3 — 2 Turns, #18 AWG Enamel Covered, 0.16″ ID
B — Ferrite Bead, Ferroxcube 56–590–65–3B
Z1–Z6 — See PCB Artwork
PCB — 1/32″ G–10, ε_r = 4.5 @ UHF
Socket — See Socket Drawings
JP1 — Jumper, #14 AWG w/Banana Plugs

Figure 1. 440–512 MHz Broadband Test Circuit

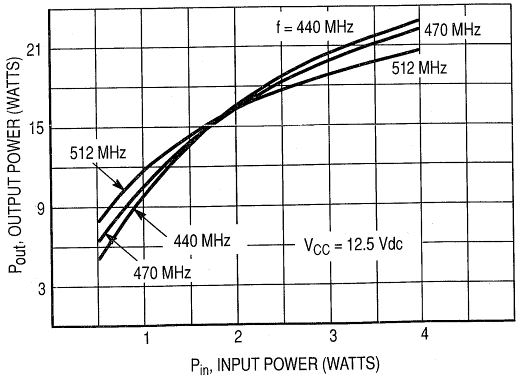


Figure 2. Output Power versus Input Power

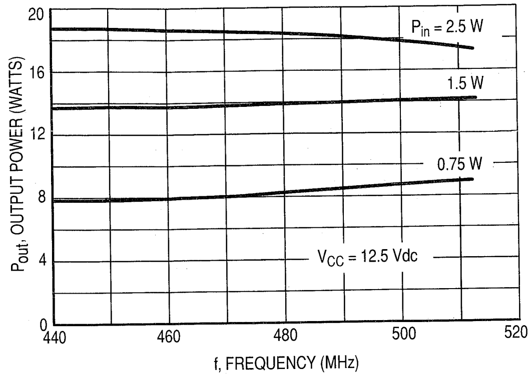


Figure 3. Output Power versus Frequency

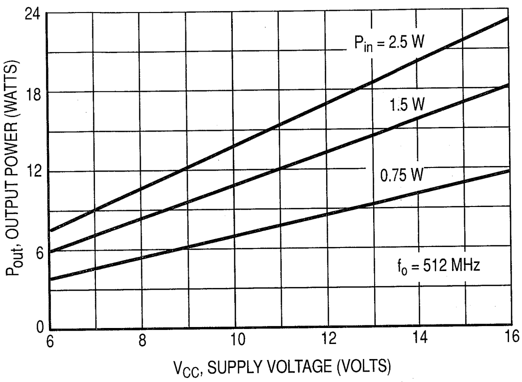


Figure 4. Power Output versus Supply Voltage

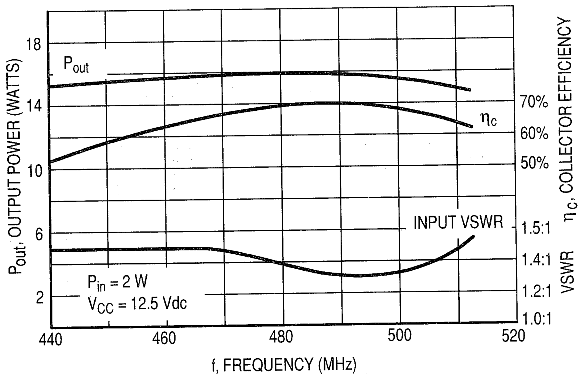
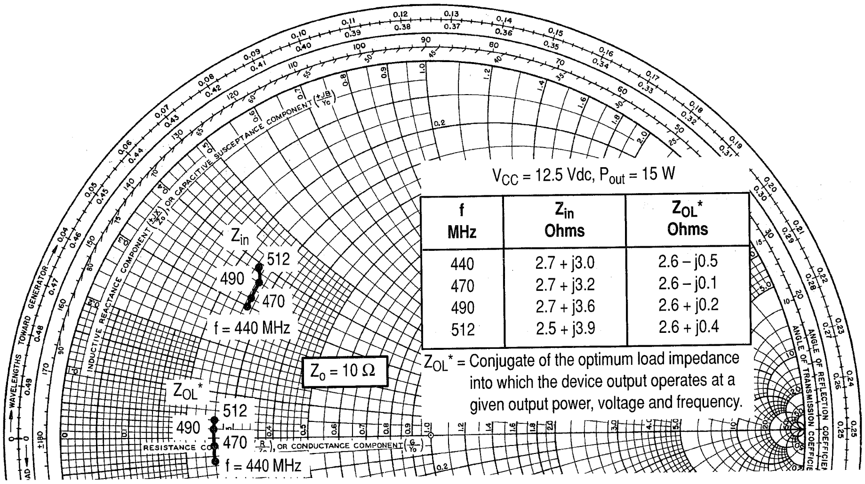


Figure 5. Typical Broadband Circuit Performance



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
440	2.7 + j3.0	2.6 – j0.5
470	2.7 + j3.2	2.6 – j0.1
490	2.7 + j3.6	2.6 + j0.2
512	2.5 + j3.9	2.6 + j0.4

Figure 6. Series Equivalent Input and Output Impedance

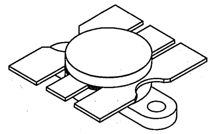
The RF Line
NPN Silicon RF Power Transistor

MRF658

Designed for 12.5 Volt UHF large–signal, common emitter, class–C amplifier applications in industrial and commercial FM equipment operating to 520 MHz.

- Specified 12.5 Volt, 512 MHz Characteristics
  Output Power = 65 Watts
  Minimum Gain = 4.15 dB
  Minimum Efficiency = 50%
- Characterized with Series Equivalent Large–Signal Impedance Parameters from 400 to 520 MHz
- Built–In Matching Network for Broadband Operation
- Triple Ion Implanted for More Consistent Characteristics
- Implanted Emitter Ballast Resistors for Improved Ruggedness
- Silicon Nitride Passivated
- Capable of Surviving Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 15.5 Vdc and 2.0 dB Overdrive

**65 W, 512 MHz
RF POWER TRANSISTOR
NPN SILICON**



CASE 316–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16.5	Vdc
Collector–Emitter Voltage	V_{CES}	38	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	175 1.0	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{θJC}$	1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16.5	29	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	38	45	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	4.6	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	0.1	10	mAdc

(continued)

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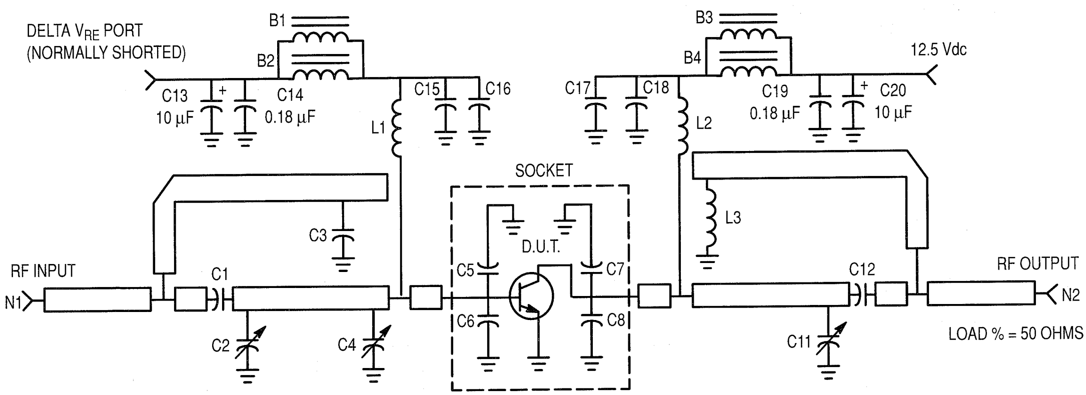
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	85	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	170	220	pF
FUNCTIONAL TESTS (In Motorola Test Fixture. See Figure 1.)					
Output Power (V_{CC} = 12.5 Vdc, P_{in} = 25 W, f = 470 & 512 MHz)	P_{out}	65	—	—	W
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 65 W, f = 470 & 512 MHz)	η	50	60	—	%
Output Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 32 W, f = 512 MHz, VSWR 20:1, All Phase Angles)	ψ	No Degradation in Output Power			



B1–B4 — Long Bead, Fair Rite (2743019446)
C1 — 56 pF, Chip Capacitor, Murata Erie
C2 — 1–20 pF Trimmer, Johanson–JMC 5501 PG26J200
C3 — 39 pF, Chip Capacitor, Murata Erie
C4 — 1–20 pF Trimmer, Johanson–JMC 5501
C5 — 33 pF, Miniature Clamped Mica, SAHA
C6 — 33 pF, Miniature Clamped Mica, SAHA
C7 — 33 pF, Miniature Clamped Mica, SAHA
C8 — 27 pF, Miniature Clamped Mica, SAHA
C11 — 1–20 pF Trimmer, Johanson–JMC 5501 PG26J200
C12 — 110 pF, Chip Capacitor, Murata Erie
C13 — 10 µF, 50 V Electrolytic, Panasonic–ECEV1HV100R
C14 — 0.18 µF Chip Capacitor
C15 — 130 pF, Chip Capacitor, Murata Erie
C16 — 130 pF, Chip Capacitor, Murata Erie
C17 — 130 pF, Chip Capacitor, Murata Erie
C18 — 130 pF, Chip Capacitor, Murata Erie
C19 — 0.18 µF Chip Capacitor
C20 — 10 µF, 50 V Electrolytic, Panasonic–ECEV1HV100R
Board — 1/16″ Glass Teflon, ε_r = 2.55, Keene (GX–0600–55–22)
L1, L2 — 5 Turns, 20 AWG, ID 0.126″
L3 — 2 Turns, 26 AWG, ID 0.073″
N1, N2 — Type N Flange, Omni Spectra (3052–1648–10)

Murata Erie Chip Capacitors — GRH710COGxxxx100VBE
SAHA Mini Clamped Mica Capacitors — 3HS0006–xx

Figure 1. 512 MHz Test Circuit

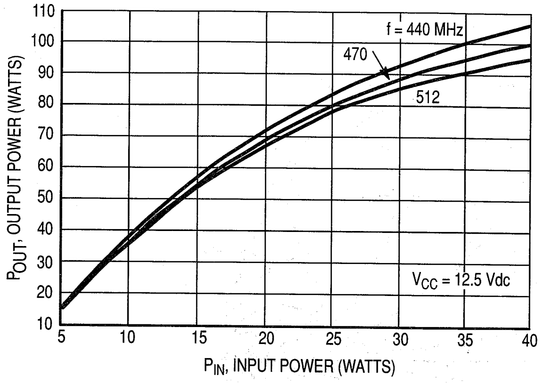


Figure 2. Output Power versus Input Power

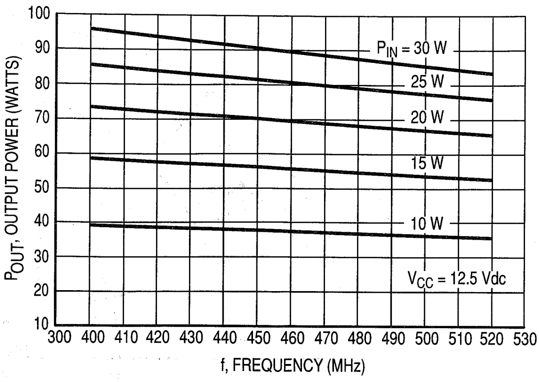


Figure 3. Output Power versus Frequency

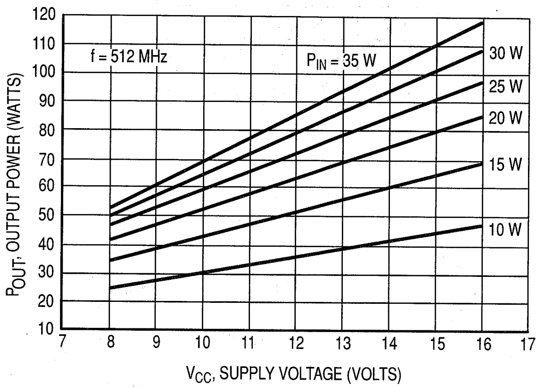
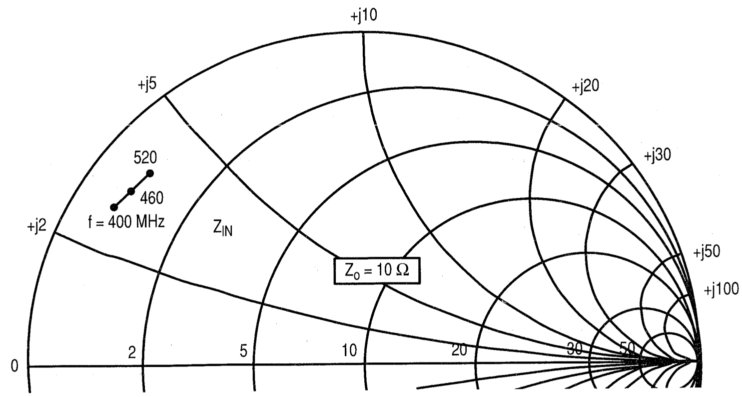
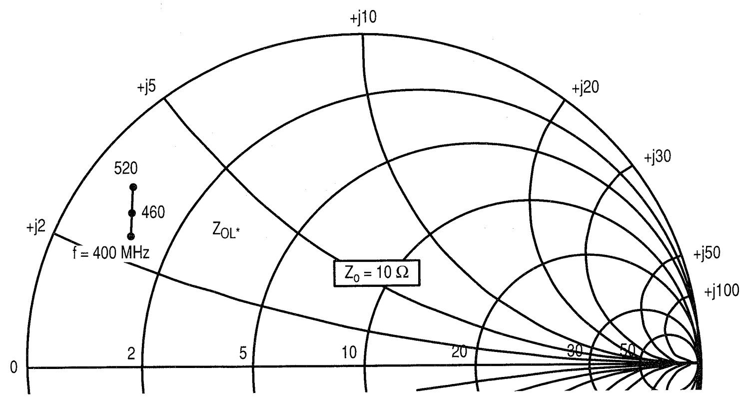


Figure 4. Output Power versus Supply Voltage



$V_{CC} = 12.5\ V \quad P_o = 70\ W$

f MHz	ZIN OHMS	Z_{OL}* OHMS
400	0.62 + j2.8	1.20 + j2.5
440	0.72 + j3.1	1.10 + j2.8
480	0.81 + j3.3	0.94 + j3.1
520	0.90 + j3.6	0.80 + j3.4



Z_{OL}* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 5. Series Equivalent Input and Output Impedances

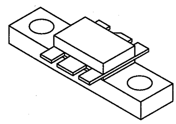
The RF Line
NPN Silicon RF Power Transistor

. . . designed for 12.5 volt UHF large–signal, common–base amplifier applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics
  Output Power = 10 Watts
  Power Gain = 6.0 dB Min
  Efficiency = 50% Min
- Series Equivalent Large–Signal Characterization
- Internally Matched Input for Broadband Operation
- Tested for Load Mismatch Stress at All Phase Angles with 20:1 VSWR @ 15.5 Volt Supply and 50% RF Overdrive
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated

MRF840

10 W, 870 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 319–07, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.8	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	40 0.32	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	3.1	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	2.0	mAdc

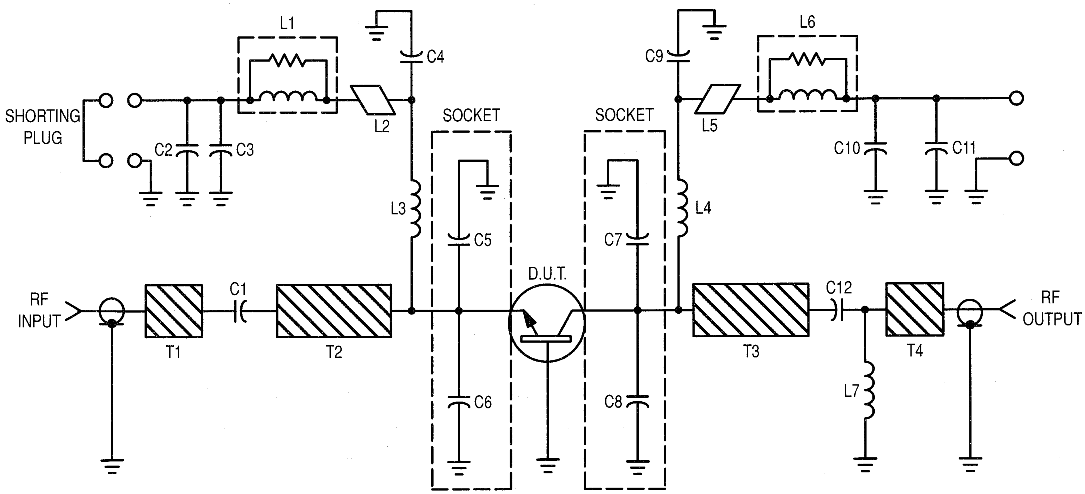
NOTES:
(continued)
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	24	35	pF
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (P_{out} = 10 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	G_{PB}	6.0	7.0	—	dB
Collector Efficiency (P_{out} = 10 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	η	50	55	—	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 3.0 W, (3) f = 870 MHz, VSWR = 20:1, all phase angles)	—	No Degradation in Output Power			

NOTE:
3. P_{in} = 150% of the typical input power requirement for 10 W output power @ 12.5 Vdc.



C1, C12 — 50 pF, 100 Mil Chip Capacitor
C2, C11 — 15 μF, 20 V Tantalum
C3, C10 — 1000 pF, 350 V UNELCO
C4, C9 — 91 pF Mini–Underwood
C5 — 15 pF
C6 — 15 pF
C7 — 15 pF
C8 — 15 pF

L1, L6 — 11 Turns 20 AWG Around 10 Ω 1/2 W Resistor
L2, L5 — Ferrite Bead
L3, L4 — 4 Turn 20 AWG 0.2″ I.D.
T1, T4 — Z_O = 50 Ω
T2 — Z_O = 30 Ω ℓ = λ/4 @ 838 MHz
T3 — Z_O = 13.5 Ω ℓ= λ/4 @ 838 MHz

L7 — 18 AWG Wire Loop

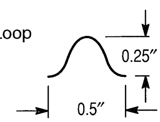


Figure 1. 870 MHz Test Circuit

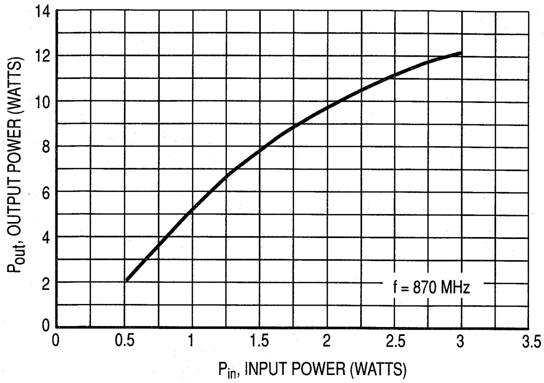


Figure 2. Output Power versus Input Power

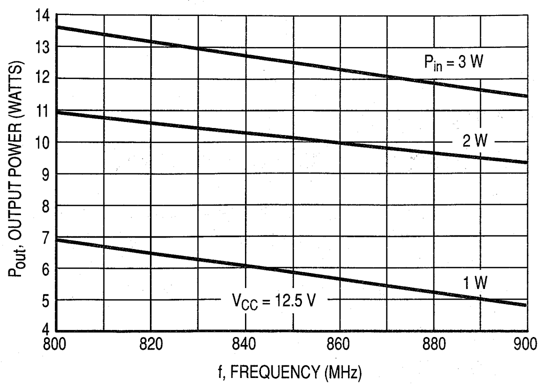


Figure 3. Output Power versus Frequency

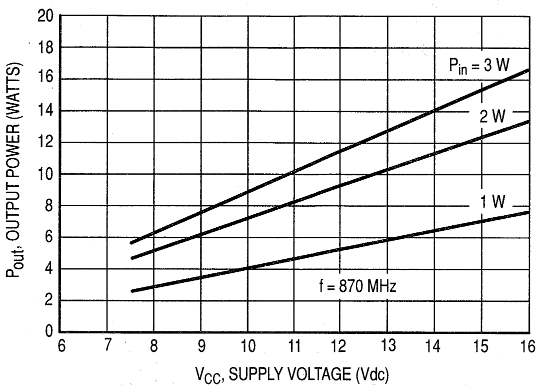
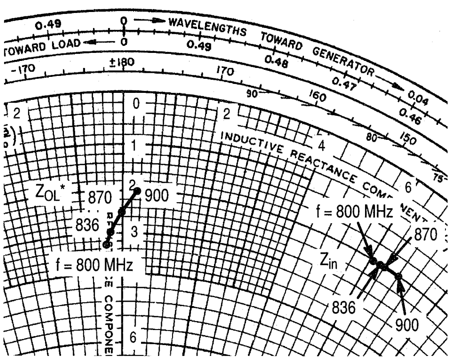


Figure 4. Output Power versus Supply Voltage



P_{out} = 10 W, V_{CC} = 12.5 Vdc

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	2.0 + j6.1	3.3 – j0.4
836	2.0 + j6.2	3.0 – j0.3
870	2.0 + j6.4	2.5 + j0.0
900	2.0 + j6.8	2.0 + j0.3

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 5. Series Equivalent Input/Output Impedance

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

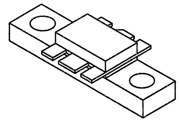
The RF Line
NPN Silicon RF Power Transistor

MRF842

. . . designed for 12.5 volt UHF large–signal, common–base amplifier applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics
  Output Power = 20 Watts
  Power Gain = 6.0 dB Min
  Efficiency = 50% Min
- Series Equivalent Large–Signal Characterization
- Internally Matched Input for Broadband Operation
- 100% Tested for Load Mismatch Stress at All Phase Angles with 20:1 VSWR @ 15.5 Volt Supply and 50% RF Overdrive
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated

20 W, 870 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 319–07, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	7.6	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	80 0.64	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

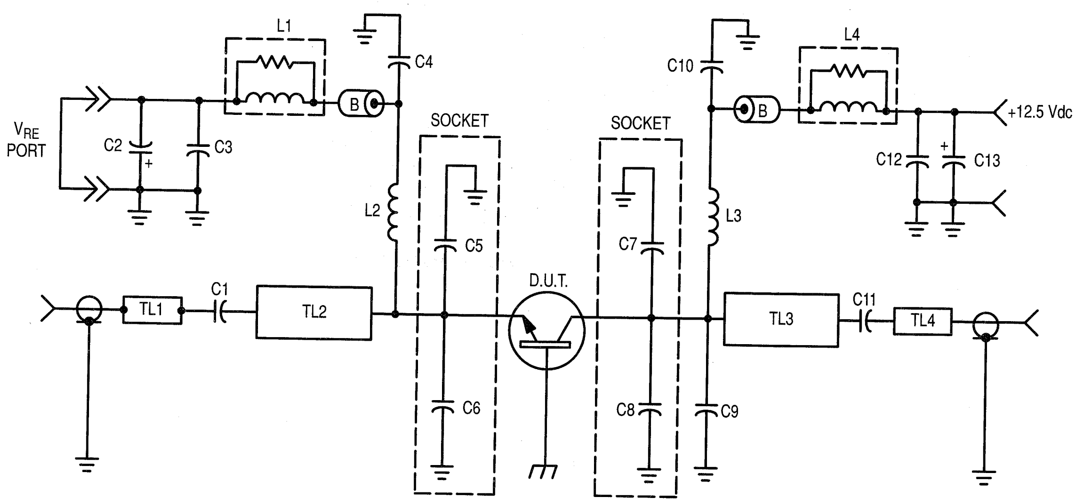
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc

NOTES:
(continued)
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	45	65	pF
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (P_{out} = 20 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	G_{PB}	6.0	7.0	—	dB
Collector Efficiency (P_{out} = 20 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	η	50	55	—	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} (3) = 6.0 W, f = 870 MHz, VSWR = 20:1, all phase angles)	—	No Degradation in Output Power			

NOTE:
3. P_{in} = 150% of the typical input power requirement for 20 W output power @ 12.5 Vdc.



B — Ferrite Bead, Ferroxcube 56–590–65–3B
C1, C11 — 51 pF, 100 Mil Chip Capacitor
C2, C13 — 15 µF, 20 WV Tantalum
C3, C12 — 1000 pF Unelco J101
C4, C10 — 91 pF Mini–Underwood
C5 — 15 pF Mini–Underwood
C6 — 12 pF Mini–Underwood
C7, C8 — 21 pF Mini–Underwood
C9 — 11 pF Mini–Underwood

L1, L4 — 11 Turns #20 AWG Over 10 ohm 1/2 W Carbon
L2, L3 — 4 Turns #20 AWG, 200 Mil ID
TL1, TL4 — Micro Strip, Z_o = 50 Ω
TL2 — Micro Strip, Z_o = 38 Ω, λ/4 @ 838 MHz
TL3 — Micro Strip, Z_o = 24 Ω, λ/4 @ 838 MHz
Board — 0.032″ Glass Teflon
2 oz. Cu CLAD, ε_r = 2.55

Figure 1. 870 MHz Test Circuit Schematic

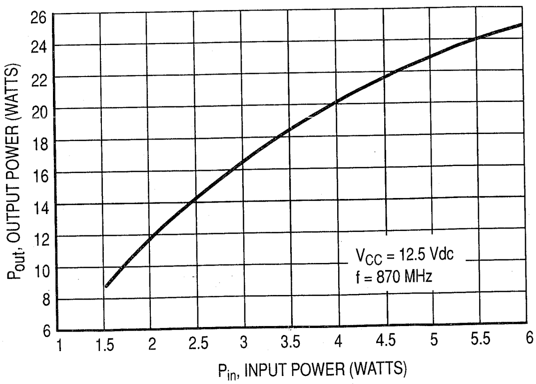


Figure 2. Output Power versus Input Power

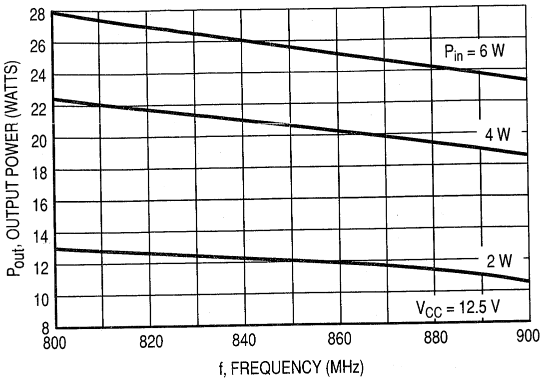


Figure 3. Output Power versus Frequency

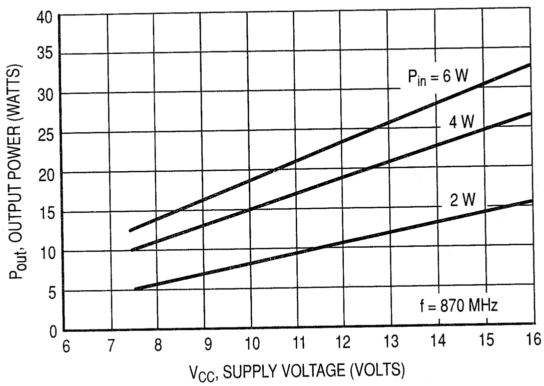
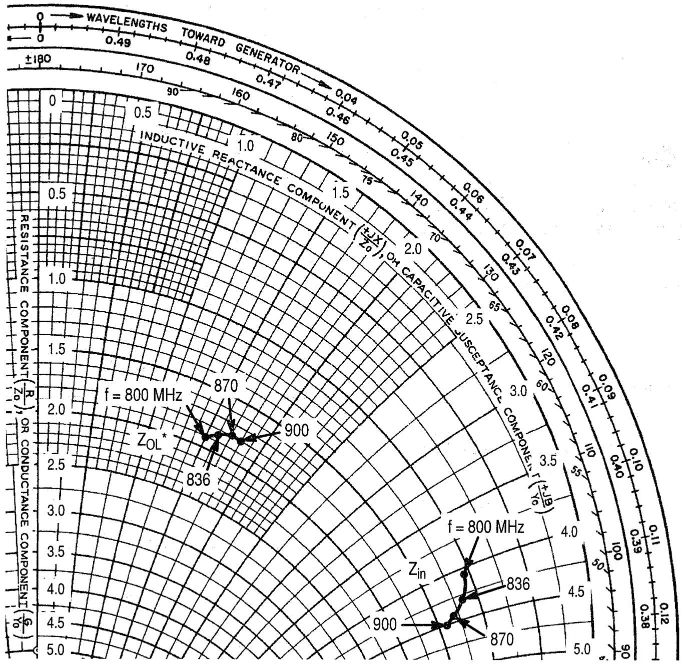


Figure 4. Output Power versus Supply Voltage



P_{out} = 20 W, V_{CC} = 12.5 Vdc

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
800	1.1 + j4.1	1.9 + j1.5
836	1.2 + j4.3	1.85 + j1.6
870	1.4 + j4.4	1.8 + j1.7
900	1.6 + j4.5	1.8 + j1.8

Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 5. Series Equivalent Input/Output Impedance

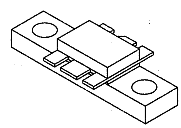
The RF Line
NPN Silicon RF Power Transistor

MRF847

. . . designed for 12.5 volt UHF large–signal, **common–base** amplifier applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics
  Output Power = 45 Watts
  Power Gain = 4.5 dB Min
  Efficiency = 60% Min
- Series Equivalent Large–Signal Characterization
- Internally Matched Input for Broadband Operation
- Tested for Load Mismatch Stress at All Phase Angles with 10:1 VSWR @ High Line and Rated Drive
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated

45 W, 870 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 319–07, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16.5	Vdc
Collector–Base Voltage	V_{CBO}	38	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	12	Adc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	150 0.85	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

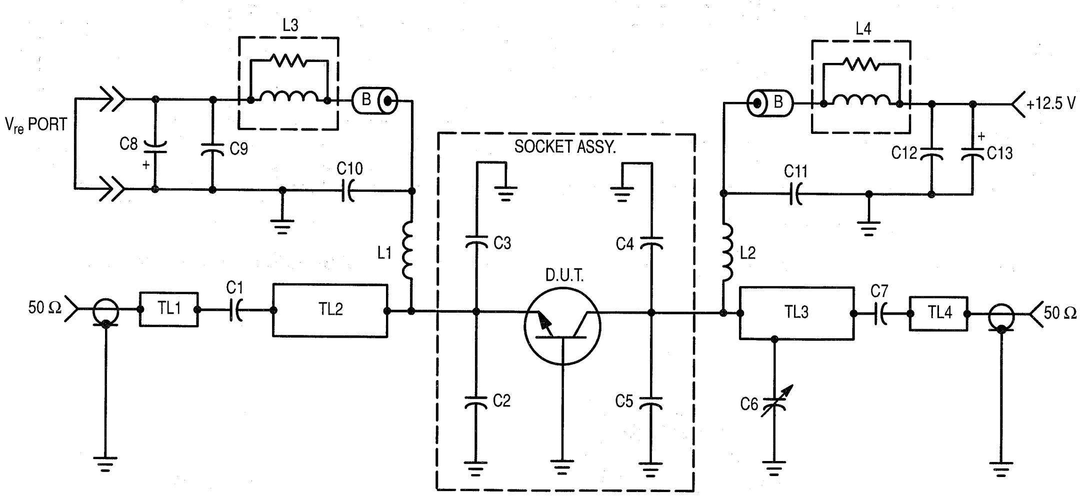
ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Emitter–Base Breakdown Voltage ($I_E = 5.0$ mAdc, $I_C = 0$)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector–Emitter Breakdown Voltage ($I_C = 50$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	16.5	—	—	Vdc
Collector–Emitter Breakdown Voltage ($I_C = 50$ mAdc, $V_{BE} = 0$)	$V_{(BR)CES}$	38	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 15$ Vdc, $V_{BE} = 0$)	I_{CES}	—	—	10	mAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	65	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	75	90	pF
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 870 MHz)	G_{PB}	4.5	5.5	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 870 MHz)	η_c	60	68	—	%
Load Mismatch (V_{CC} = 15.5 Vdc, P_{in} = 16 W, f = 870 MHz, VSWR = 10:1, All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 51 pF, 100 mil Chip Capacitor
C2 — 12 pF, Mini–Underwood
C3 — 11 pF, Mini–Underwood
C4, C5 — 21 pF, Mini–Underwood
C6 — 0.08–8.0 pF Johansen Gigatrim
C7 — 47 pF, 100 mil Chip Capacitor
C8, C13 — 10 μF, 25 WV Electrolytic Capacitor
C9, C12 — 1000 pF Unelco J101
C10, C11 — 91 pF Mini–Underwood
L1, L2 — 4 Turns #18 Enameled, 200 mil ID
L3, L4 — 12 Turns #22 Enameled, Wound Over 10 Ω Resistor
TL1, TL4 — 50 Ω Microstrip Line
TL2 — Microstrip (Z_o = 38 ohms, λ/4 @ 838 MHz)
TL3 — Microstrip (Z_o = 28 ohms, λ/4 @ 838 MHz)
Board Material — 0.032″ Glass–Teflon, 2 oz. cu. clad, ε_r = 2.56
B — Ferrite Bead, Ferroxcube 56–590–65–3B

Figure 1. 806–870 MHz Broadband Test Circuit

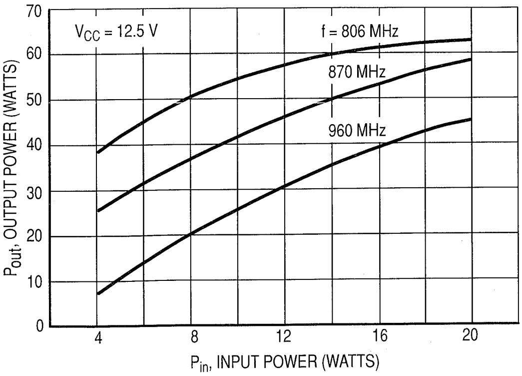


Figure 2. Output Power versus Input Power

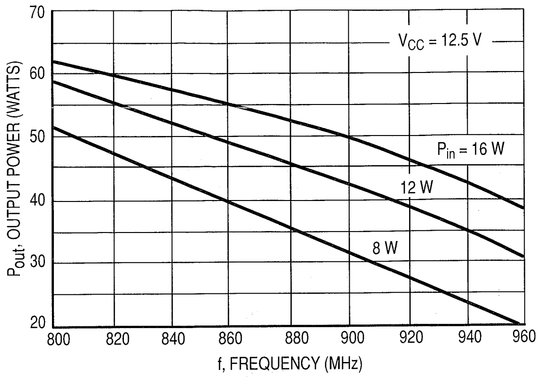


Figure 3. Output Power versus Frequency

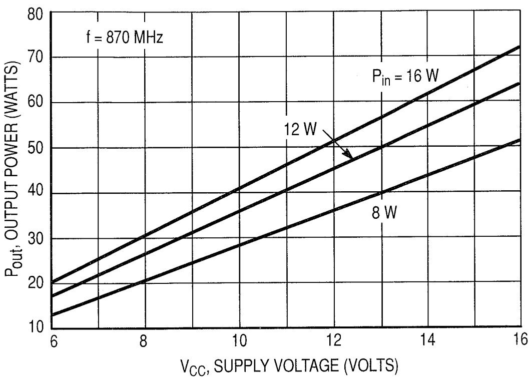


Figure 4. Output Power versus Supply Voltage

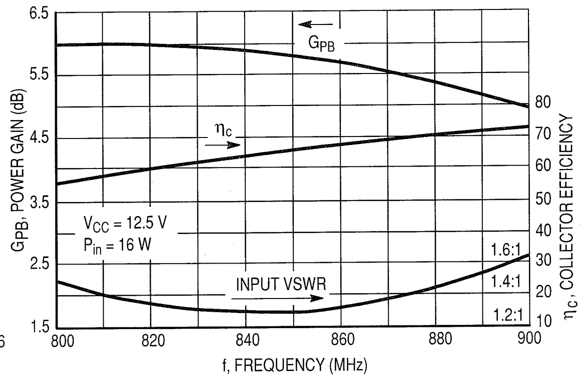
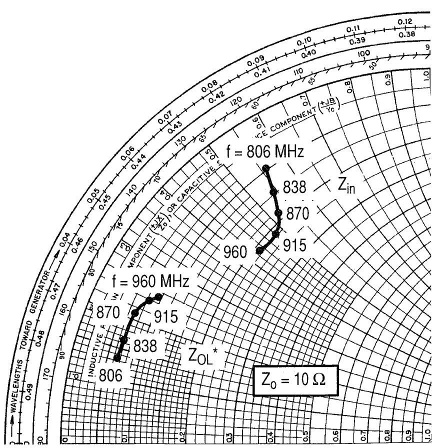


Figure 5. Typical Broadband Circuit Performance



V_{CC} = 12.5 Vdc, P_{in} = 16 W, P_{out} = 45 W

f MHz	Z_{in} (Ohms)		f MHz	Z_{OL}* (Ohms)	
806	0.99	+j5.52	806	0.67	+j1.33
838	1.48	+j5.47	838	0.68	+j1.66
870	1.79	+j5.25	870	0.72	+j2.16
915	2.12	+j4.80	915	0.83	+j2.40
960	2.11	+j4.28	960	0.99	+j2.50

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Input/Output Impedances

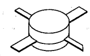
The RF Line
NPN Silicon RF Power Transistor

MRF857S

Designed for 24 Volt UHF large–signal, common emitter, class A linear amplifier applications in industrial and commercial equipment operating in the range of 800–960 MHz.

- Specified for V_{CE} = 24 Vdc, I_C = 0.3 Adc Characteristics
  Output Power = 2.1 Watts CW
  Minimum Power Gain = 12.5 dB
  Minimum ITO = +43 dBm
  Typical Noise Figure = 5.25 dB
- Characterized with Small–Signal S–Parameters and Series Equivalent Large–Signal Parameters from 800–960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at All Phase Angles with 30:1 VSWR @ 24 Vdc, I_C = 0.3 Adc and Rated Output Power
- Will Withstand RF Input Overdrive of 0.4 W CW
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

CLASS A
800–960 MHz
2.1 W (CW), 24 V
NPN SILICON
RF POWER TRANSISTOR



CASE 305D–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	17 0.114	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance (T_J = 150°C, T_C = 50°C)	$R_{\theta JC}$	8.4	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mA, I_B = 0)	$V_{(BR)CEO}$	28	35	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mA, V_{BE} = 0)	$V_{(BR)CES}$	55	85	—	Vdc
Collector–Base Breakdown Voltage (I_C = 20 mA, I_E = 0)	$V_{(BR)CBO}$	55	85	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1 mA, I_C = 0)	$V_{(BR)EBO}$	4	5	—	Vdc
Collector Cutoff Current (V_{CB} = 24 V, I_E = 0)	I_{CES}	—	—	1	mA

(continued)

REV 3

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.1 A, V_{CE} = 5 V)	h_{FE}	30	60	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 V, f = 1 MHz)	C_{ob}	2.4	3.3	4.4	pF
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Power Gain (V_{CE} = 24 V, I_C = 0.3 A, f = 840–900 MHz, Power Output = 2.1 W)	P_g	12.5	13.5	—	dB
Load Mismatch (P_o = 2.1 W) (V_{CE} = 24 V, I_C = 0.3 A, f = 840 MHz, Load VSWR = 30:1, All Phase Angles)	ψ	No Degradation in Output Power			
RF Input Overdrive (V_{CE} = 24 V, I_C = 0.3 A, f = 840 MHz) No degradation	$P_{in(over)}$	—	—	0.4	W
Third Order Intercept Point (V_{CE} = 24 V, I_C = 0.3 A) (f1 = 900 MHz, f2 = 900.1 MHz, Meas. @ IMD 3rd Order = –40 dBc)	ITO	+43	+44.5	—	dBm
Noise Figure (V_{CE} = 24 V, I_C = 0.3 A, f = 900 MHz)	NF	—	5.25	—	dB
Input Return Loss (V_{CE} = 24 V, I_C = 0.3 A, f = 840–900 MHz, Power Output = 2.1 W)	IRL	—	–15	–10	dB

Table 1. MRF857S Common Emitter S–Parameters

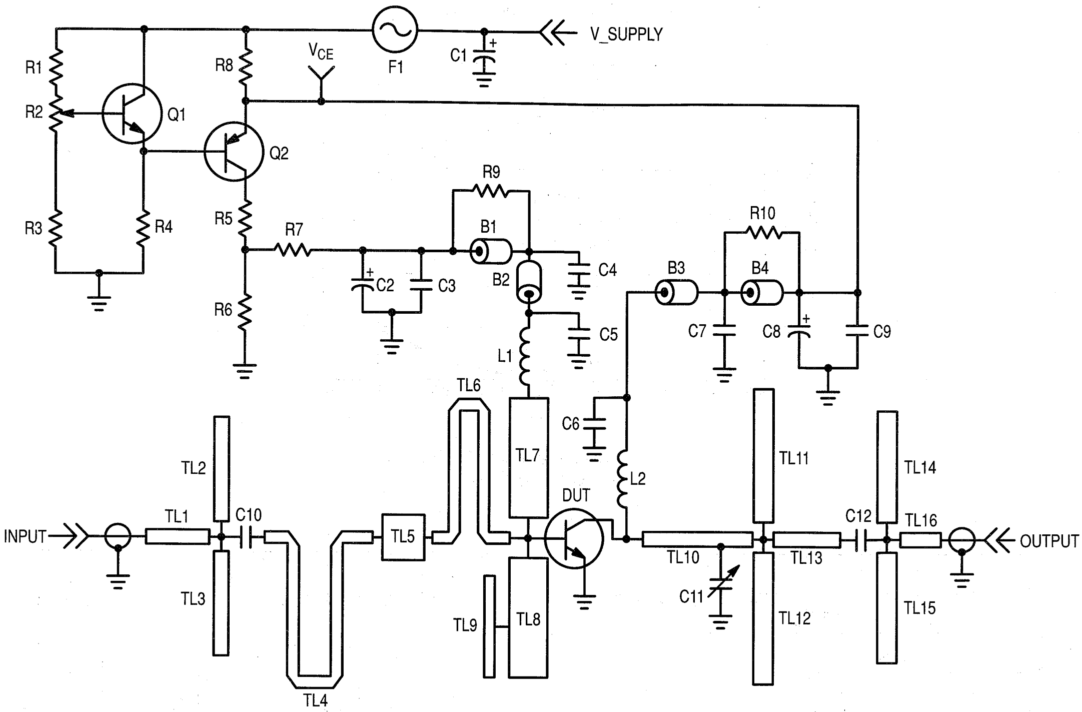
V_{CE} (V)	I_C (A)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
24	0.3	800	0.915	165	2.098	54	0.037	58	0.343	–157
		820	0.915	165	2.049	53	0.038	58	0.345	–157
		840	0.915	165	1.991	52	0.038	58	0.349	–157
		860	0.913	164	1.951	51	0.039	59	0.352	–158
		880	0.914	164	1.912	50	0.040	59	0.355	–158
		900	0.914	163	1.865	49	0.041	59	0.359	–158
		920	0.913	163	1.832	48	0.042	59	0.362	–158
		940	0.915	162	1.783	47	0.043	59	0.366	–159
		960	0.916	162	1.748	46	0.043	59	0.369	–159

Table 2. Z_{in} and Z_{OL}* versus Frequency

f (MHz)	Z_{in} (Ohms)		Z_{OL}* (Ohms)	
840	1.5	4.4	18.4	–26.3
870	1.7	4.7	18.0	–26.1
900	1.5	4.8	14.9	–26.2

V_{CE} = 24 V, I_C = 0.3 A, P_o = 2.1 W

Z_{OL}* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.



B1, B4	Long Ferrite Bead, Fair Rite (2743021447)	R1	330 Ω, 1/4 W
B2, B3	Short Ferrite Bead, Fair Rite (2743019447)	R2	500 Ω Potentiometer, 1/4 W
C1	250 μF, 50 Vdc Electrolytic Capacitor	R3	4.7K Ω, 1/4 W
C2, C8	10 μF, 50 Vdc Electrolytic Capacitor	R4	2 x 4.7K Ω, 1/4 W
C3, C9	0.1 μF, Chip Capacitor	R5	47 Ω, 2 W
C4, C7	1000 pF, Chip Capacitor	R6	75 Ω, 1/4 W
C5, C6	100 pF, Chip Capacitor	R7	4.7 Ω, 1/4 W
C10, C12	43 pF, 100 Mil Chip Capacitor	R8	10 Ω, 3 W
C11	0.8–8 pF, Johansen Gigatrim	R9, R10	4 x 39 Ω, 1/8 W Chip Resistors in Parallel
F1	1 A Micro–Fuse	TL1 – TL16	Microstrip Transmission Line
L1, L2	5 Turns, 20 AWG, 0.126″ ID, 46.2 nH	V_Supply	+27 Vdc ±0.5 V Due to Resistor Tolerance
Q1	MMBT2222ALT1, NPN Transistor	V_{CE}	+24 Vdc @ 0.3 A
Q2	BD136, PNP Transistor	Board	0.030″ Glass–Teflon® 2 oz. Cu, ε_r = 2.55

Figure 1. MRF857S Class A RF Test Fixture Schematic

TYPICAL CHARACTERISTICS

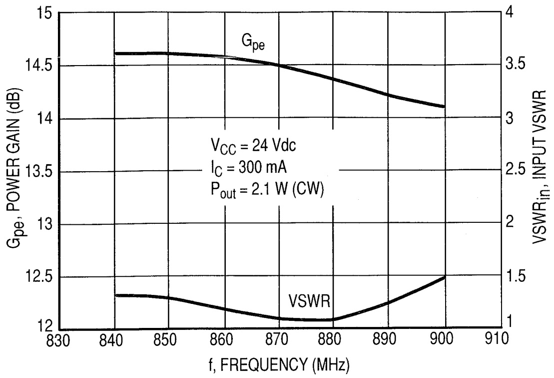


Figure 2. Performance of MRF857S in Broadband Circuit

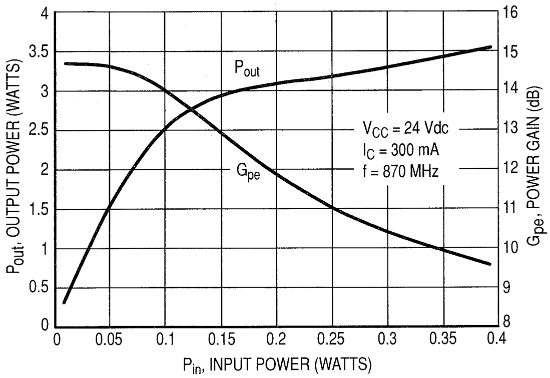


Figure 3. MRF857S Output Power & Power Gain versus Input Power

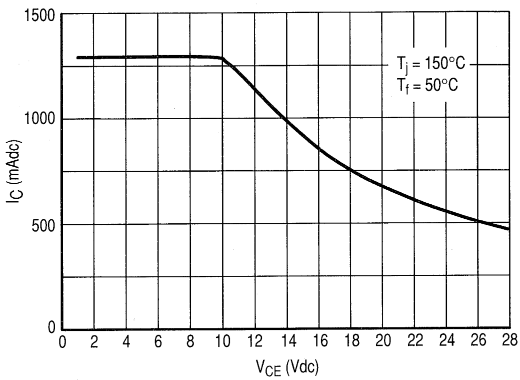


Figure 4. MRF857S DC SOA

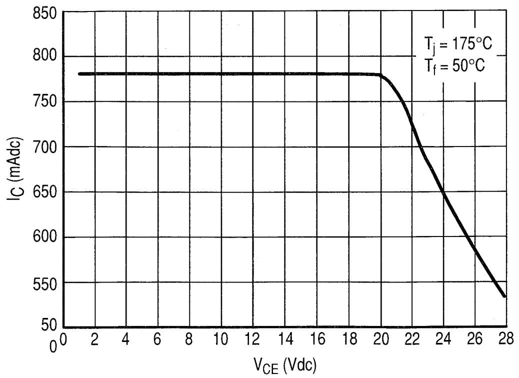


Figure 5. MRF857S DC SOA (This device is MTBF limited for $V_{CE} < 20$ Vdc.)

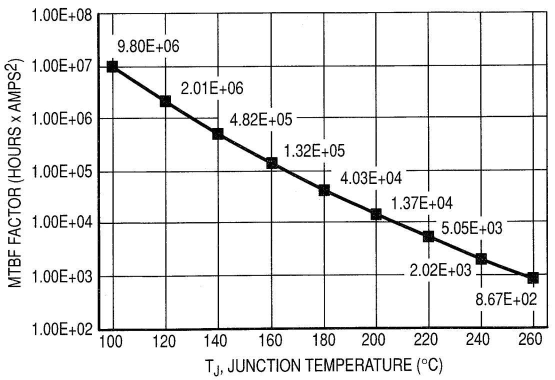


Figure 6. MRF857S MTBF Factor versus Junction Temperature

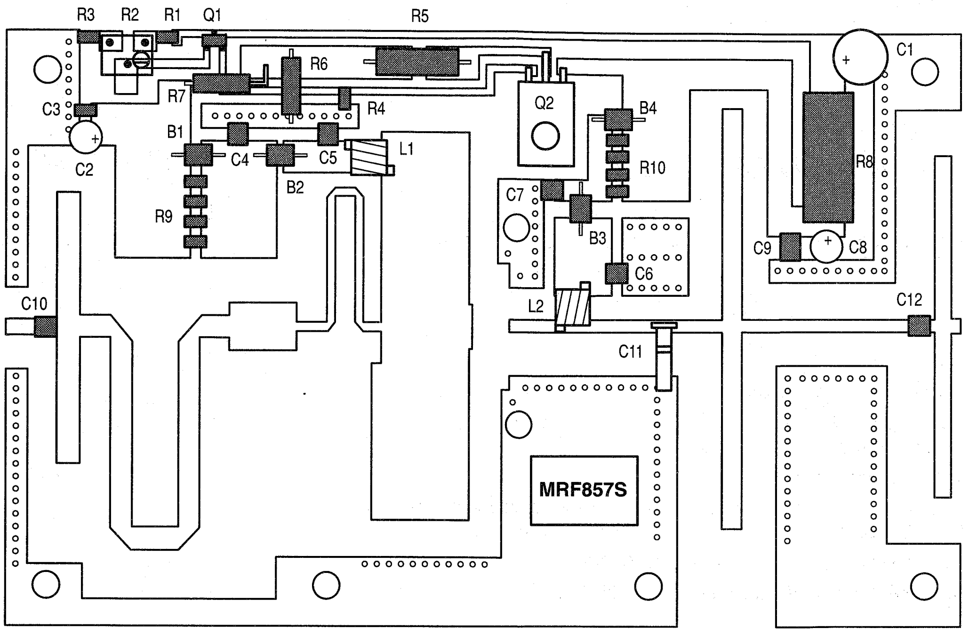
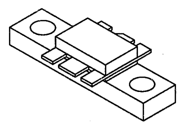


Figure 7. MRF857S Test Fixture Component Layout

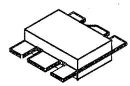
The RF Line
NPN Silicon RF Power Transistor

MRF858
MRF858S

CLASS A
800–960 MHz
3.6 W (CW), 24 V
NPN SILICON
RF POWER TRANSISTOR



CASE 319–07, STYLE 2
MRF858



CASE 319A–02, STYLE 2
MRF858S

Designed for 24 Volt UHF large–signal, common emitter, class A linear amplifier applications in industrial and commercial equipment operating in the range of 800–960 MHz.

- Specified for V_{CE} = 24 Vdc, I_C = 0.5 Adc Characteristics
  Output Power = 3.6 Watts CW
  Minimum Power Gain = 11 dB
  Minimum ITO = +44.5 dBm
  Typical Noise Figure = 6 dB
- Characterized with Small–Signal S–Parameters and Series Equivalent Large–Signal Parameters from 800–960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at All Phase Angles with 30:1 VSWR @ 24 Vdc, I_C = 0.5 Adc and Rated Output Power
- Will Withstand RF Input Overdrive of 0.85 W CW
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	20 0.138	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance (T_J = 150°C, T_C = 50°C)	$R_{\theta JC}$	6.9	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mA, I_B = 0)	$V_{(BR)CEO}$	28	35	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mA, V_{BE} = 0)	$V_{(BR)CES}$	55	85	—	Vdc
Collector–Base Breakdown Voltage (I_C = 20 mA, I_E = 0)	$V_{(BR)CBO}$	55	85	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1 mA, I_C = 0)	$V_{(BR)EBO}$	4	5	—	Vdc
Collector Cutoff Current (V_{CB} = 24 V, I_E = 0)	I_{CES}	—	—	1	mA

(continued)

REV 2

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.1 A, V_{CE} = 5 V)	h_{FE}	30	60	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 V, f = 1 MHz)	C_{ob}	—	6.5	8	pF
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Power Gain (V_{CE} = 24 V, I_C = 0.5 A, f = 840–900 MHz, Power Output = 3.6 W)	P_g	11	12	—	dB
Load Mismatch (P_o = 3.6 W) (V_{CE} = 24 V, I_C = 0.5 A, f = 840 MHz, Load VSWR = 30:1, All Phase Angles)	ψ	No Degradation in Output Power			
RF Input Overdrive (V_{CE} = 24 V, I_C = 0.5 A, f = 840 MHz) No degradation	$P_{in(over)}$	—	—	0.85	W
Third Order Intercept Point (V_{CE} = 24 V, I_C = 0.5 A) (f1 = 900 MHz, f2 = 900.1 MHz, Meas. @ IMD 3rd Order = –40 dBc)	ITO	+44.5	+45.5	—	dBm
Noise Figure (V_{CE} = 24 V, I_C = 0.5 A, f = 900 MHz)	NF	—	6	—	dB
Input Return Loss (V_{CE} = 24 V, I_C = 0.5 A, f = 840–900 MHz, Power Output = 3.6 W)	IRL	—	–12	–9	dB

Table 1. MRF858 Common Emitter S–Parameters

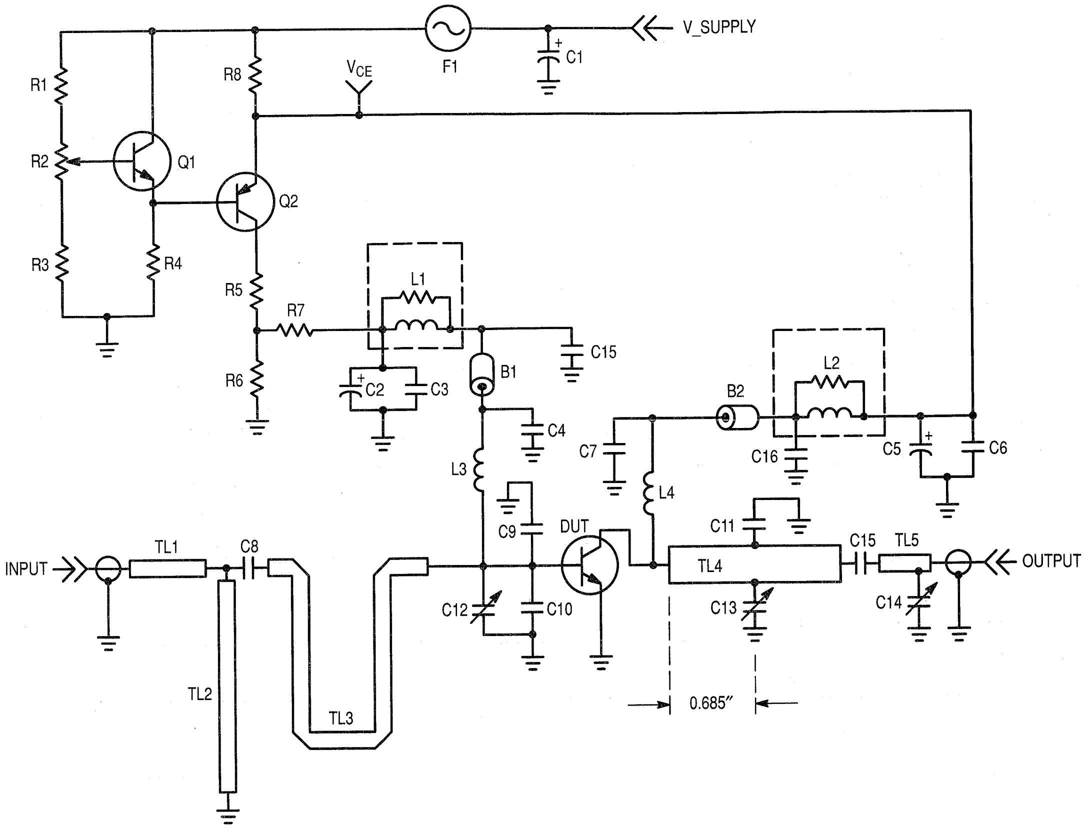
V_{CE} (V)	I_C (A)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
24	0.5	800	0.942	167	1.493	50	0.027	58	0.538	–165
		820	0.942	166	1.453	50	0.027	58	0.541	–164
		840	0.941	166	1.415	49	0.028	59	0.545	–165
		860	0.940	166	1.379	48	0.028	59	0.550	–165
		880	0.941	165	1.351	47	0.029	59	0.553	–165
		900	0.940	165	1.320	46	0.030	59	0.557	–165
		920	0.940	165	1.289	45	0.030	59	0.562	–165
		940	0.940	164	1.252	44	0.031	59	0.566	–165
		960	0.940	164	1.222	43	0.031	59	0.570	–165

Table 2. Z_{in} and Z_{OL}* versus Frequency

f (MHz)	Z_{in} (Ohms)		Z_{OL}* (Ohms)	
840	1.1	2.9	9.9	–14.4
870	1.1	3.5	9.5	–14.6
900	1.2	3.5	9	–14.5

V_{CE} = 24 V, I_C = 0.5 A, P_o = 3.6 W

Z_{OL}* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.



B1, B2	Short Ferrite Bead, Fair Rite (2743021447)
C1	250 µF, 50 Vdc Electrolytic Capacitor
C2, C5	10 µF, 50 Vdc Electrolytic Capacitor
C3, C6	0.1 µF, Chip Capacitor
C4, C7	100 pF, Chip Capacitor
C8, C15	43 pF, 100 Mil Chip Capacitor
C9, C10	10 pF, Mini–Unelco
C11	5 pF, Mini–Unelco
C12, C13, C14	0.8–8.0 pF, Johanson Gigatrim
C15, C16	1000 pF, Chip Capacitor
F1	1 A Micro–Fuse
L1, L2	10 Turns, 20 AWG, 0.150″ ID (10 Ω 1/2 W Resistor)
L3	4 Turns, 16 AWG, 0.101″ ID
L4	0.5″ 18 AWG Wire
Q1	MMBT2222ALT1, NPN Transistor
Q2	BD136, PNP Transistor

R1	390 Ω, 1/4 W
R2	500 Ω Potentiometer, 1/4 W
R3	7.5K Ω, 1/4 W
R4	2 x 4.7K Ω, 1/4 W
R5	56 Ω, 2 W
R6	75 Ω, 1/4 W
R7	4.7 Ω, 1/4 W
R8	4 Ω, 10 W
TL1, TL5	50 Ω, Microstrip Transmission Line
TL2	Microstrip Transmission Line
TL3	Microstrip Transmission Line
TL4	Microstrip Transmission Line
V_Supply	+26 Vdc ±0.5 Vdc Due to Resistor Tolerance
V_{CE}	+24 Vdc @ 0.5 A
Board	0.030″ Glass–Teflon® 2 oz. Cu, ε_r = 2.55

Figure 1. MRF858 Class A RF Test Fixture Schematic

TYPICAL CHARACTERISTICS

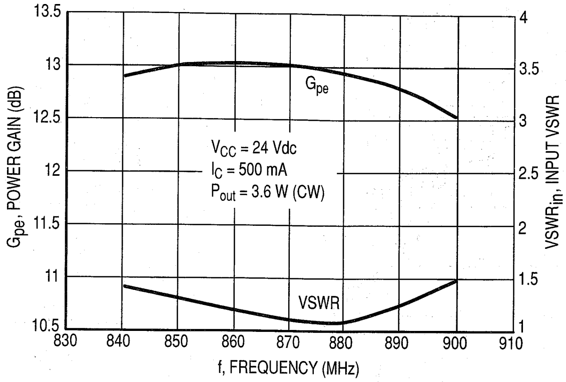


Figure 2. Performance in Broadband Circuit

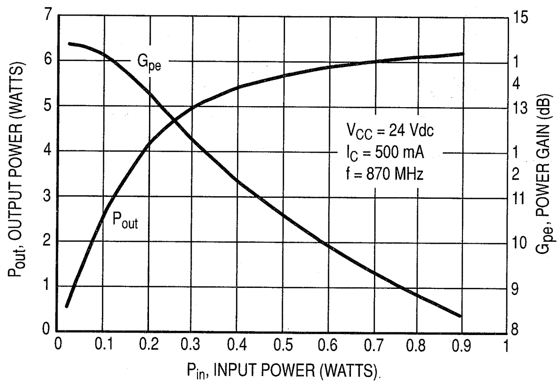


Figure 3. Output Power & Power Gain versus Input Power

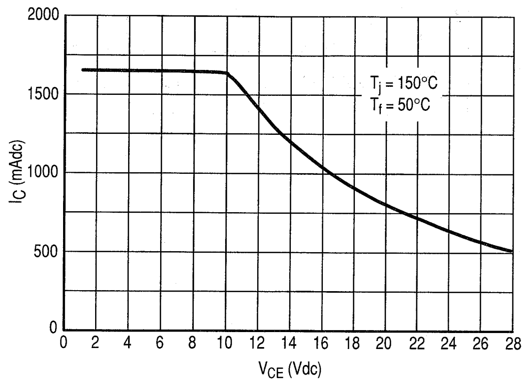


Figure 4. DC SOA

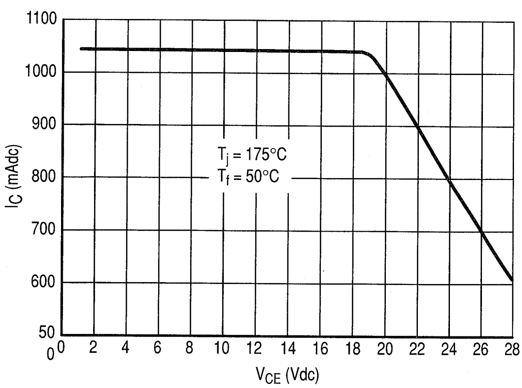


Figure 5. DC SOA (This device is MTBF limited for V_{CE} < 20 Vdc.)

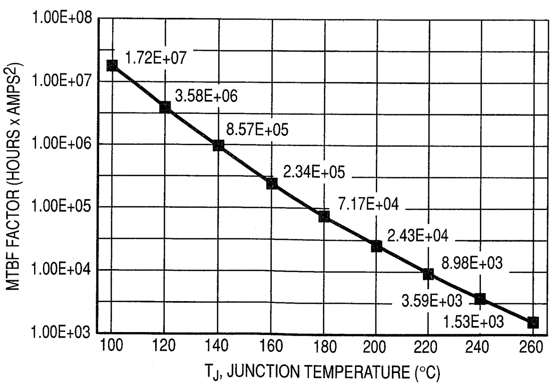


Figure 6. MTBF Factor versus Junction Temperature

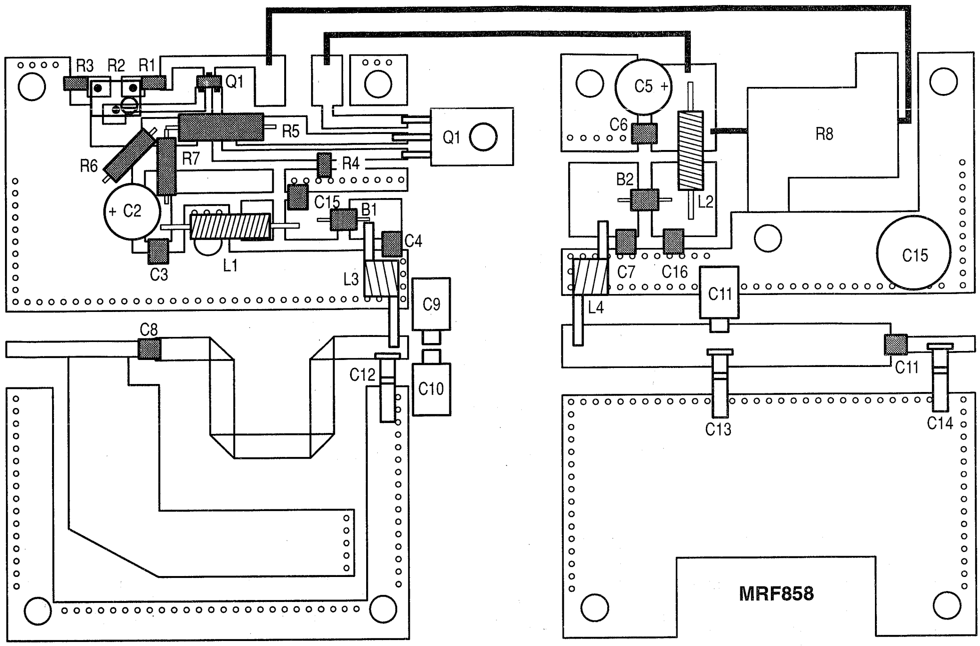


Figure 7. MRF858 Test Fixture Component Layout

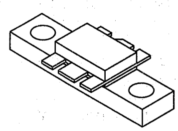
The RF Line
NPN Silicon RF Power Transistor

MRF859
MRF859S

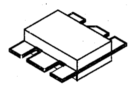
CLASS A
800–960 MHz
6.5 W (CW), 24 V
NPN SILICON
RF POWER TRANSISTOR

Designed for 24 Volt UHF large–signal, common emitter, class A linear amplifier applications in industrial and commercial equipment operating in the range of 800 to 960 MHz.

- Specified for V_{CE} = 24 Vdc, I_C = 0.9 Adc Characteristics
  Output Power = 6.5 Watts CW
  Minimum Power Gain = 11.5 dB
  Minimum ITO = +47 dBm
  Typical Noise Figure = 6 dB
- Characterized with Small–Signal S–Parameters and Series Equivalent Large–Signal Parameters from 800 to 960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at All Phase Angles with 30:1 VSWR @ 24 Vdc, I_C = 0.9 Adc and Rated Output Power
- Will Withstand RF Input Overdrive of 2 W CW
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit Board Photomaster Available by Ordering Document MRF859PHT/D from Motorola Literature Distribution.



CASE 319–07, STYLE 2
MRF859



CASE 319A–02, STYLE 2
MRF859S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Total Device Dissipation @ T_C = 60°C Derate above 60°C	P_D	34 0.24	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance (T_J = 150°C, T_C = 60°C)	$R_{\theta JC}$	3.9	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mA, I_B = 0)	$V_{(BR)CEO}$	28	32	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 25 mA, V_{BE} = 0)	$V_{(BR)CES}$	55	75	—	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mA, I_E = 0)	$V_{(BR)CBO}$	55	75	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5 mA, I_C = 0)	$V_{(BR)EBO}$	4	5	—	Vdc
Collector Cutoff Current (V_{CB} = 15 V, I_E = 0)	I_{CES}	—	—	2	mA

(continued)

REV 2

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 1 A, V_{CE} = 5 V)	h_{FE}	20	60	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 V, f = 1 MHz)	C_{ob}	13	—	26	pF
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Power Gain (V_{CE} = 24 V, I_C = 0.9 A, f = 840–900 MHz, P_{out} = 6.5 W)	P_g	11.5	13	—	dB
Load Mismatch (V_{CE} = 24 V, I_C = 0.9 A, f = 840 MHz, P_{out} = 6.5 W, Load VSWR = 30:1, All Phase Angles)	ψ	No Degradation in Output Power			
RF Input Overdrive (V_{CE} = 24 V, I_C = 0.9 A, f = 840 MHz) No degradation	$P_{in(over)}$	—	—	2	W
Third Order Intercept Point (V_{CE} = 24 V, I_C = 0.9 A, f1 = 900 MHz, f2 = 900.1 MHz, Meas. @ IMD 3rd Order = –40 dBc)	ITO	+47	+48	—	dBm
Noise Figure (V_{CE} = 24 V, I_C = 0.9 A, f = 900 MHz)	NF	—	6	—	dB
Input Return Loss (V_{CE} = 24 V, I_C = 0.9 A, f = 840–900 MHz, P_{out} = 6.5 W)	IRL	—	—	–9	dB

Table 1. Common Emitter S–Parameters

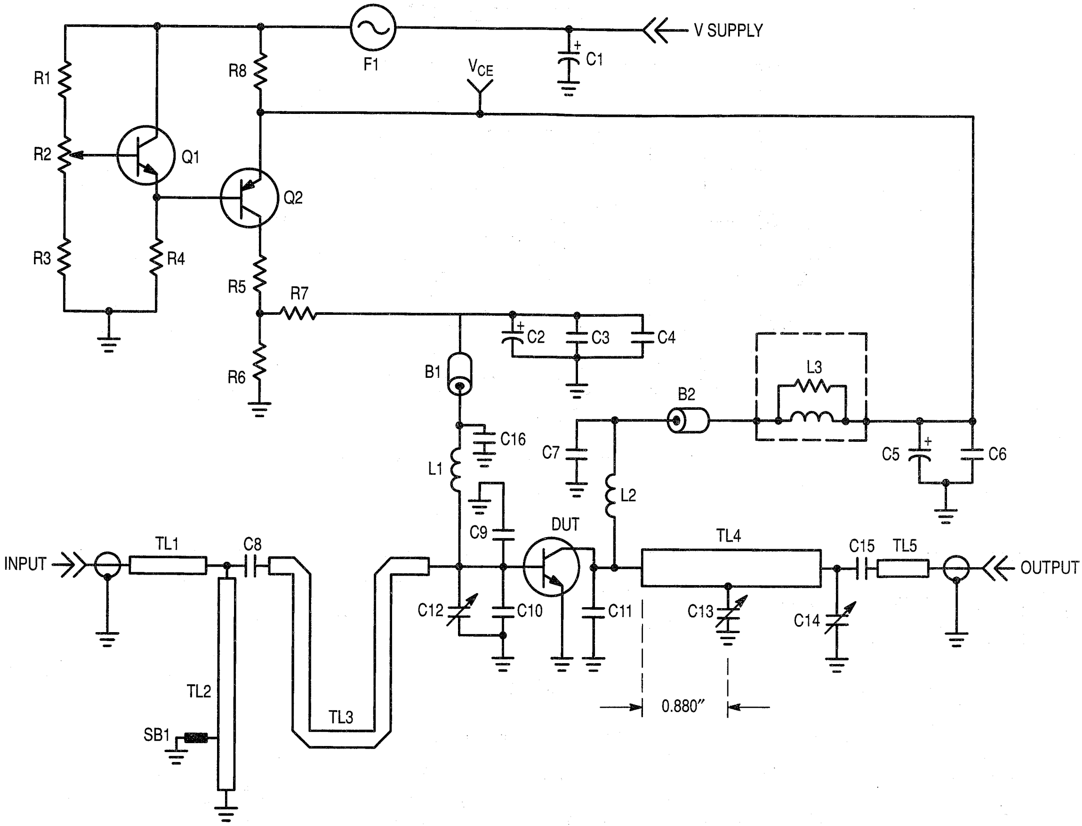
V_{CE} (V)	I_C (A)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
24	0.9	800	0.906	170	1.022	12	0.016	11	0.804	–168
		820	0.902	170	1.022	7	0.015	8	0.823	–167
		840	0.897	171	1.018	3	0.013	6	0.845	–167
		860	0.894	171	1.012	–3	0.011	4	0.870	–167
		880	0.893	171	1.005	–8	0.009	3	0.895	–168
		900	0.893	171	0.988	–14	0.007	5	0.920	–168
		920	0.894	172	0.962	–20	0.005	14	0.946	–169
		940	0.897	172	0.924	–26	0.008	47	0.969	–170
		960	0.903	172	0.884	–32	0.004	102	0.987	–172

Table 2. Z_{in} and Z_{OL}* versus Frequency

f (MHz)	Z_{in} (Ohms)		Z_{OL}* (Ohms)	
840	1.6	3.3	2	–4.1
870	1.5	3.6	1.6	–3.3
900	2.2	3.5	1.7	–2.7

V_{CE} = 24 V, I_C = 0.9 A, P_o = 6.5 W

Z_{OL}* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.



B1, B2	Ferrite Bead, Ferroxcube (56–390–65/3B)	R1	470 Ω, 1/4 W
C1	250 µF, 50 Vdc, Electrolytic Capacitor	R2	500 Ω Potentiometer, 1/4 W
C2, C5	10 µF, 50 Vdc, Electrolytic Capacitor	R3	4.7K Ω, 1/4 W
C3, C6	0.1 µF, Chip Capacitor	R4	2 x 4.7K Ω, 1/4 W
C4	1000 pF, Chip Capacitor	R5	50 Ω, 2 W
C7, C16	100 pF, Chip Capacitor	R6	75 Ω, 1/4 W
C8, C15	43 pF, 100 Mil Chip Capacitor	R7	4.7 Ω, 1/4 W
C9, C10	6.8 pF, Mini–Unelco	R8	4 Ω, 10 W
C11	18 pF, Mini–Unelco	SB1	Copper Block 0.550″ x 0.180″ x 0.050″
C12, C13, C14	0.8–8.0 pF, Johanson Gigatrim	TL1, TL5	50 Ω, Microstrip Transmission Line
F1	3 Amp Micro–Fuse	TL2	Microstrip Transmission Line
L1, L2	3 Turns, 18 AWG, 0.170″ ID	TL3	Microstrip Transmission Line
L3	12 Turns, 22 AWG, 0.150″ ID (10 Ω 1/2 W Resistor)	TL4	Microstrip Transmission Line
Q1	MMBT2222ALT1, NPN Transistor	Board	0.030″ Glass–Teflon® 2 oz. Cu, $\varepsilon_r = 2.55$
Q2	BD136, PNP Transistor	V Supply	+27.6 Vdc ±0.5 Vdc Due to Resistor Tolerance
		V_{CE}	+24 Vdc @ 0.9 A

Figure 1. MRF859 Class A RF Test Fixture Schematic

TYPICAL CHARACTERISTICS

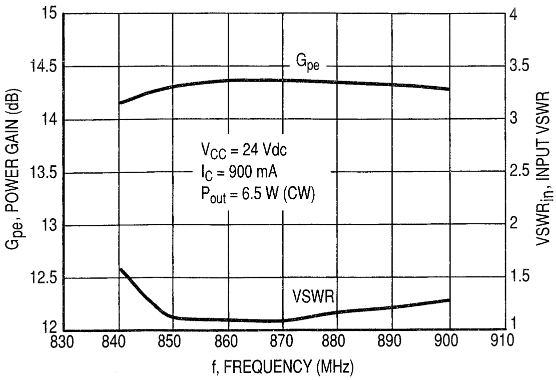


Figure 2. Performance in Broadband Circuit

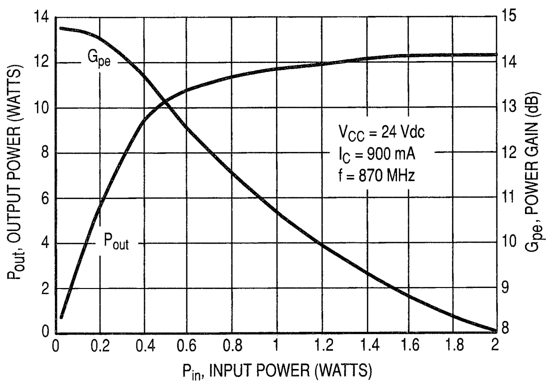


Figure 3. Output Power & Power Gain versus Input Power

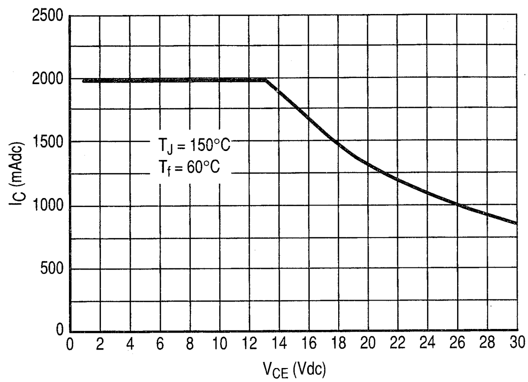


Figure 4. DC SOA

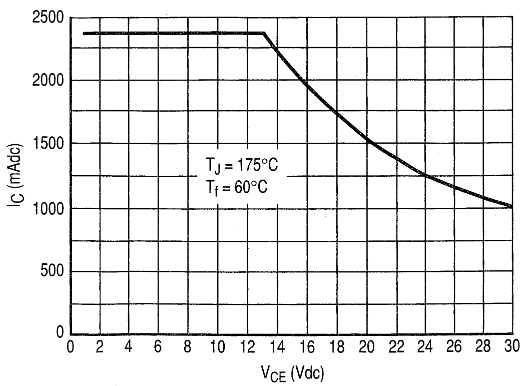


Figure 5. DC SOA

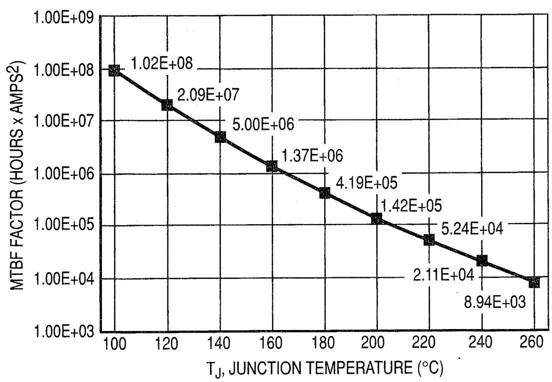


Figure 6. MTBF Factor versus Junction Temperature

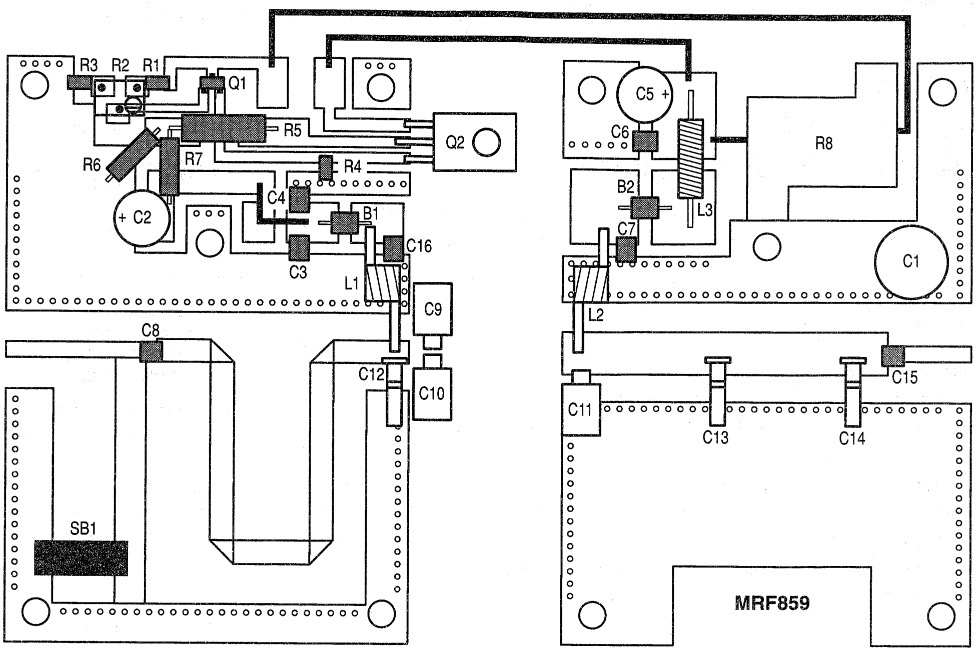


Figure 7. MRF859 Test Fixture Component Layout

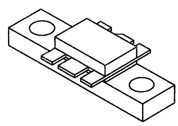
The RF Line
NPN Silicon RF Power Transistors

MRF891
MRF891S

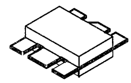
... designed for 24 volt UHF large–signal, common–emitter amplifier applications in industrial and commercial FM equipment operating in the range of 800–960 MHz.

- Specified 24 Volt, 900 MHz Characteristics
  Output Power = 5.0 Watts
  Power Gain = 9.0 dB Min
  Efficiency = 50% Min
- Series Equivalent Large–Signal Characterization
- Capable of Withstanding 20:1 VSWR Load Mismatch at Rated Output Power and Supply Voltage
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

5.0 W, 900 MHz
RF POWER
TRANSISTORS
NPN SILICON



CASE 319–07, STYLE 2
MRF891



CASE 319A–02, STYLE 2
MRF891S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Emitter Voltage	V_{CES}	55	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	0.6	Adc
Total Device Dissipation @ T_A = 50°C (1) Derate above 50°C	P_D	18 0.143	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	7.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	—	150	—

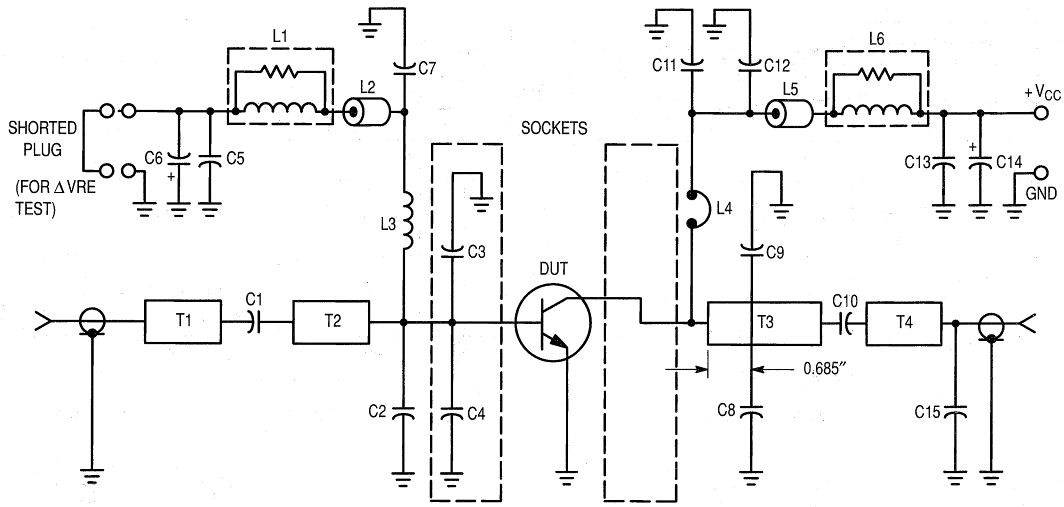
(continued)

NOTES:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	6.5	8.0	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (Broadband) (V_{CC} = 24 Vdc, P_{out} = 5.0 W, f = 900 MHz)	G_{pe}	9.0	10	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 5.0 W, f = 900 MHz)	η	50	57	—	%
Load Mismatch Stress (V_{CC} = 24 Vdc, P_{in} = 0.63 W, f = 900 MHz, VSWR = 20:1, all phase angles)	ψ	No Degradation in Output Power			



C1 — 39 pF, 100 Mil Chip Capacitor
C2, C8, C15 — 0.8–8.0 pF Johansen Gigatrim
C3, C4 — 12 pF, Mini–Unelco
C5, C13 — 1000 pF, 350 V Unelco
C6, C14 — 10 µF, 25 V Tantalum
C7, C11, C12 — 91 pF, Mini–Unelco
C9 — 5.0 pF, MIni–Unelco
C10 — 47 pF, 100 Mil Chip Capacitor

L1, L6 — 10 Turns #20 AWG Around 10 Ohm 1/2 Watt Resistor
L2, L5 — Ferrite Bead
L3 — 4 Turns #16 AWG Choke
L4 — 0.5″, #18 AWG Wire
T1, T4 — 50 Ohm Microstrip Line
T2 — W = 165 Mils, ℓ = 1946 Mils
T3 — W = 166 Mils, ℓ = 1563 Mils
PC Board — 0.031″ Glass Teflon (ε_r = 2.56)

Figure 1. Broadband Test Fixture

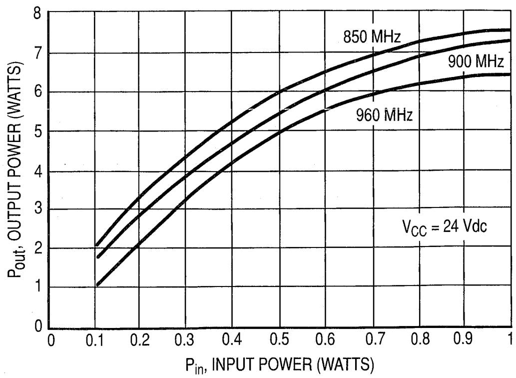


Figure 2. Output Power versus Input Power

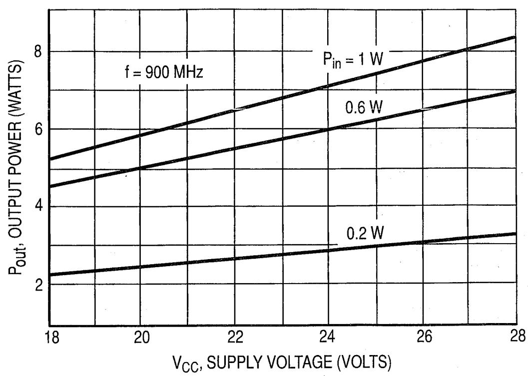


Figure 3. Output Power versus Supply Voltage

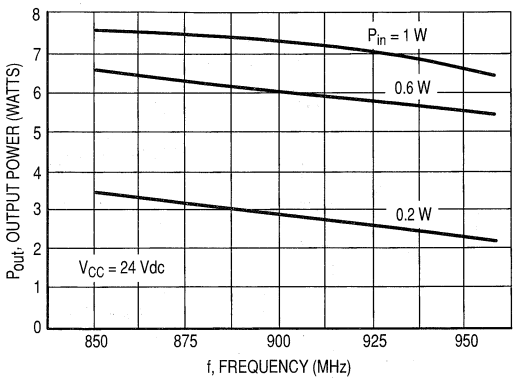


Figure 4. Output Power versus Frequency

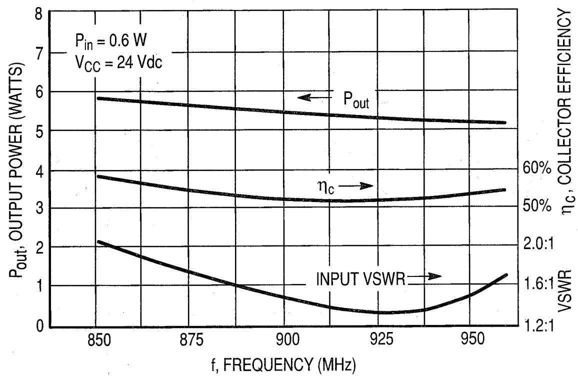


Figure 5. Typical Broadband Circuit Performance

V_{CC} = 24 Vdc, P_{out} = 5.0 W, Eff > 50%

f MHz	Z_{in} Ohms
850	1.1 + j3.0
900	1.0 + j3.25
960	1.18 + j3.5

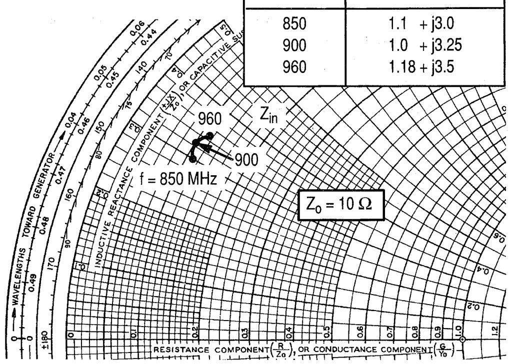


Figure 6. Series Equivalent Input Impedance

V_{CC} = 24 Vdc, P_{out} = 5.0 W, Eff > 50%

f MHz	Z_{OL}* Ohms
850	8.34 – j13.2
900	9.1 – j13.8
960	10.4 – j14.6

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

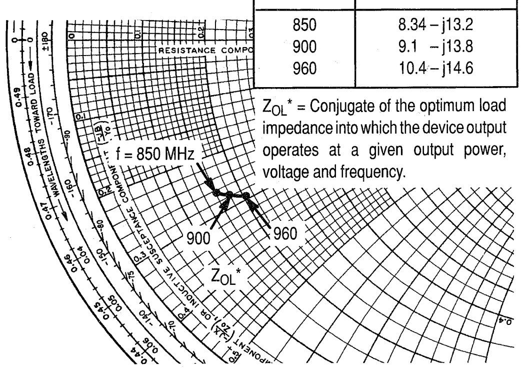


Figure 7. Series Equivalent Output Impedance

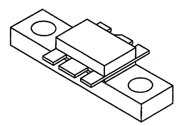
The RF Line
NPN Silicon RF Power Transistor

MRF894

. . . designed for 24 volt UHF large–signal, common–base amplifier applications in industrial and commercial FM equipment operating in the range of 804–960 MHz.

- Specified 24 Volt, 900 MHz Characteristics
  Output Power = 30 Watts
  Power Gain = 7.0 dB Min
  Efficiency = 55% Min
- Series Equivalent Large–Signal Characterization
- Capable of 30:1 VSWR Load Mismatch at Rated Output Power and Supply Voltage
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated

30 W, 900 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 319–07, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	50	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	7.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	10	mAdc

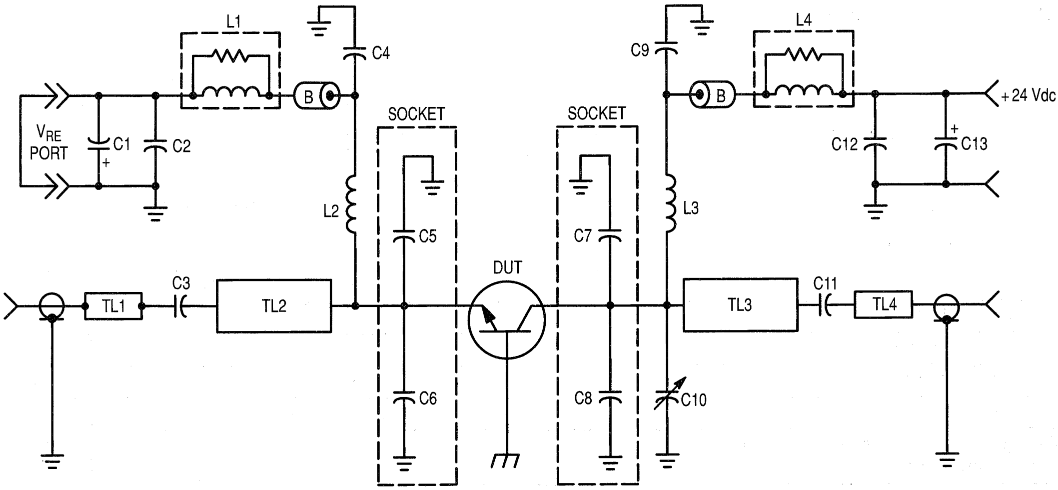
(continued)

NOTES:
1. This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	45	—	pF
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (P_{out} = 30 W, V_{CC} = 24 Vdc, f = 900 MHz)	G_{PE}	7.0	8.5	—	dB
Collector Efficiency (P_{out} = 30 W, V_{CC} = 24 Vdc, f = 900 MHz)	η	55	60	—	%



B — Ferrite Bead, Ferroxcube 56–590–65–3B
C1, C13 — 5.0 µF, 50 Vdc
C2, C12 — 1000 pF Unelco
C3, C11 — 47 pF, 100 Mil Chip Capacitor
C4, C9 — 91 pF, Mini–Underwood
C5, C6 — 12 pF, Mini–Underwood
C7 — 18 pF, Mini–Underwood
C8 — 24 pF, Mini–Underwood
C10 — 0.8–8.0 pF Johanson Gigatrim

L1, L4 — 11 Turns #20 Enameled Over 10 Ω Carbon Resistor
L2, L3 — 4 Turns #20 Enameled, .15″ ID
TL1, TL4 — Micro Strip Line, 50 Ω
TL2 — Micro Strip, Z_o = 30 Ω, λ/4 @ 875 MHz
TL3 — Micro Strip, Z_o = 22 Ω, λ/4 @ 875 MHz
Board — 0.032″ Glass Teflon
2 oz. Cu CLAD, ε_r = 2.55

Figure 1. 850–900 MHz Broadband Circuit Schematic

TYPICAL CHARACTERISTICS

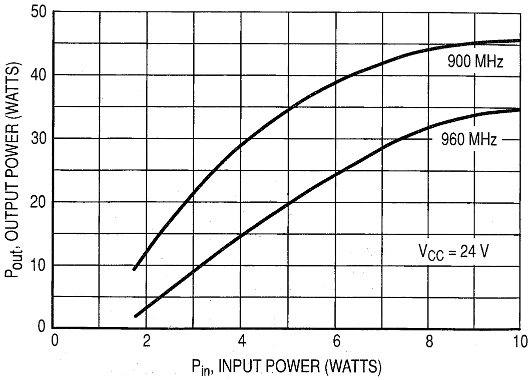


Figure 2. Output Power versus Input Power

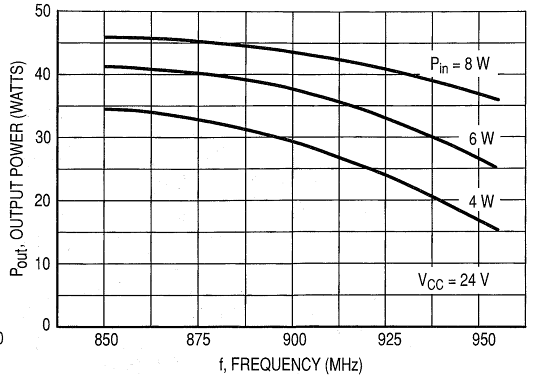


Figure 3. Output Power versus Frequency

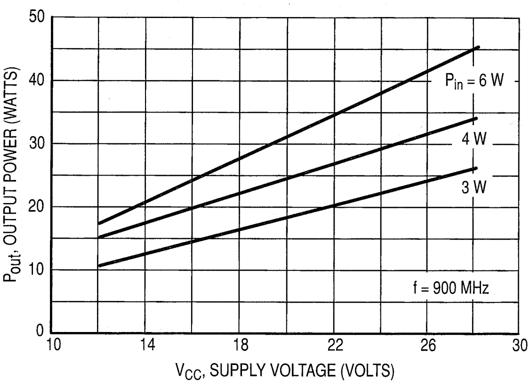


Figure 4. Output Power versus Supply Voltage

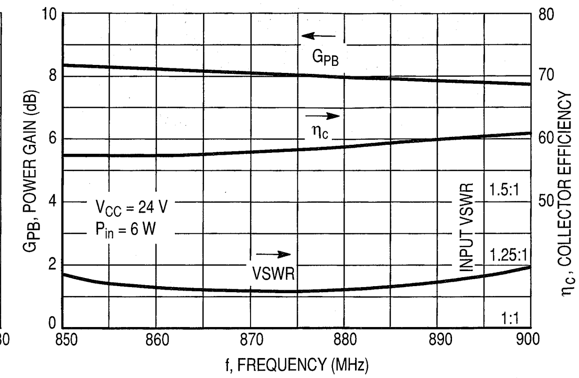
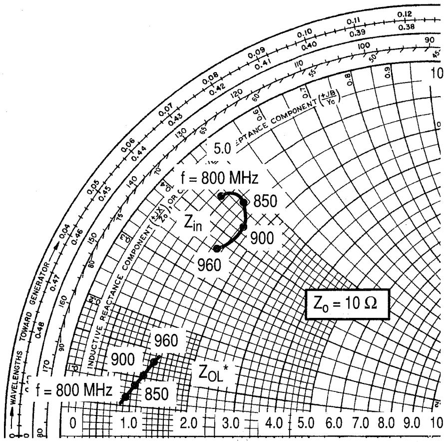


Figure 5. Typical Broadband Circuit Performance



V_{CC} = 24 Vdc, P_{out} = 30 W

f Frequency MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	0.9 + j4.5	1.0 + j0.7
850	1.3 + j4.7	1.1 + j0.9
900	1.6 + j4.4	1.2 + j1.1
960	1.5 + j3.7	1.2 + j1.3

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 6. Series Equivalent Impedance

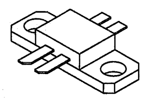
The RF Line
NPN Silicon RF Power Transistor

MRF897

Designed for 24 Volt UHF large–signal, common emitter, class–AB linear amplifier applications in industrial and commercial FM/AM equipment operating in the range 800–970 MHz.

- Specified 24 Volt, 900 MHz Characteristics
  Output Power = 30 Watts
  Minimum Gain = 10 dB @ 900 MHz, class–AB
  Minimum Efficiency = 30% @ 900 MHz, 30 Watts (PEP)
  Maximum Intermodulation Distortion –30 dBc @ 30 Watts (PEP)
- Characterized with Series Equivalent Large–Signal Parameters from 800 to 960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, and Rated Output Power
- Gold Metalized, Emitter Ballasted for Long Life and Resistance to Metal–Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

30 W, 900 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 395B–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	105 0.60	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

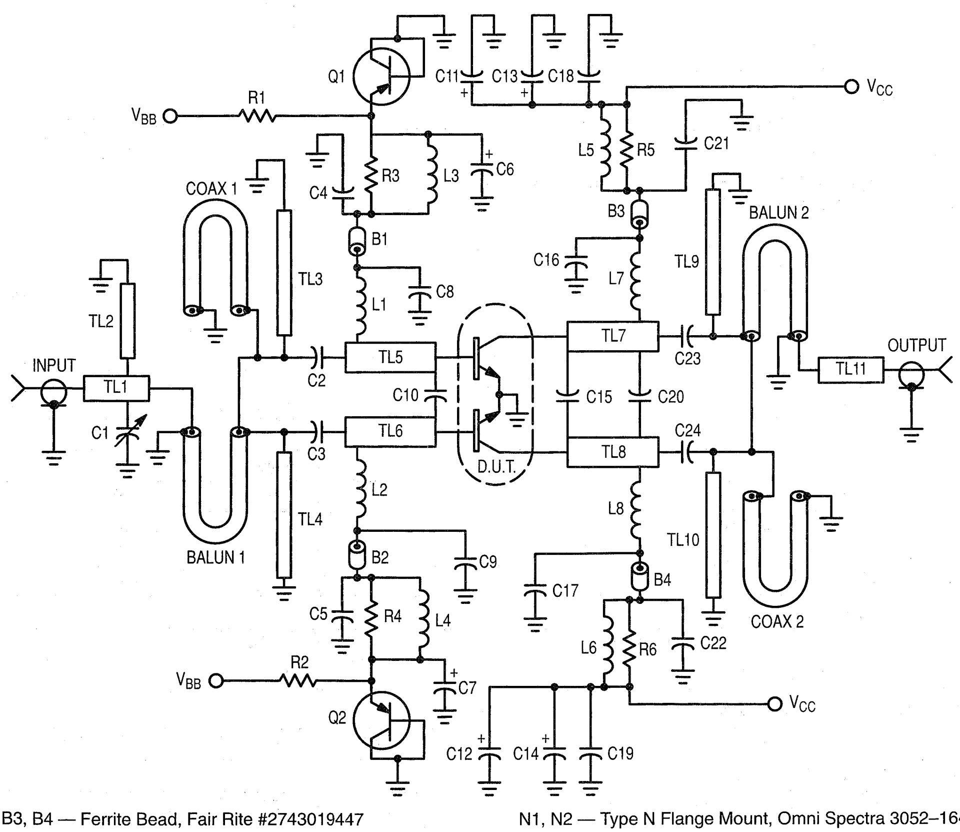
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	33	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	80	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	4.7	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5 Vdc)	h_{FE}	30	80	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	14	21	28	pF

(continued)

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	G_{pe}	10.0	12.0	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	η	35	38	—	%
Intermodulation Distortion (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	IMD	—	–37	–30	dBc
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz, Load VSWR = 5:1 (all phase angles))	ψ	No Degradation in Output Power Before and After Test			



B1, B2, B3, B4 — Ferrite Bead, Fair Rite #2743019447
C1 — 0.8–8.0 pF Trimmer Capacitor, Johanson
C2, C3, C23, C24 — 43 pF, 100 mil, ATC Chip Capacitor
C4, C5, C18, C19, C21, C22 — 820 pF, 100 mil, Chip Capacitor, Kemet
C6, C7, C11, C12 — 10 µF, Lytic Capacitor, Panasonic
C8, C9, C16, C17 — 100 pF, 100 mil, Chip Capacitor, Murata Erie
C10 — 13 pF, 50 mil, ATC Chip Capacitor
C13, C14 — 250 µF Lytic Capacitor, Mallory
C15 — 1.1 pF, 50 mil, ATC Chip Capacitor
C20 — 6.8 pF, 100 mil, ATC Chip Capacitor
L1, L2, L3, L4, L5, L6 — 5 Turns 20 AWG, IDIA 0.126″ choke
N1, N2 — Type N Flange Mount, Omni Spectra 3052–1648–10
Q1 — Bias Transistor BD136 PNP
R1, R12 — 39 Ohm, 2.0 W
R3, R4, R5, R6 — 4.0 x 39 Ohm, 1/8 W, Chips in Parallel, Rohm 390–J
TL1–TL11 — See Photomaster
Balun1, Balun2, Coax 1, Coax 2 — 2.20″ 50 Ohm, 0.088″ o.d. semi–rigid coax, Micro Coax UT–85–M17
Board — 1/32″ Glass Teflon, Arlon GX–0300–55–22, ε_r = 2.55

Figure 1. MRF897 Broadband Test Circuit

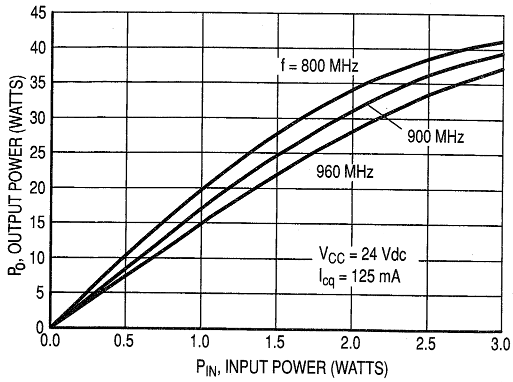


Figure 2. Output Power versus Input Power

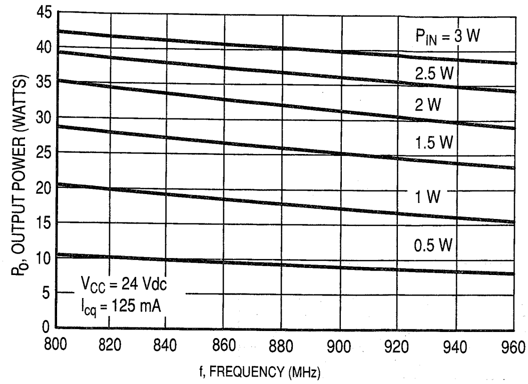


Figure 3. Output Power versus Frequency

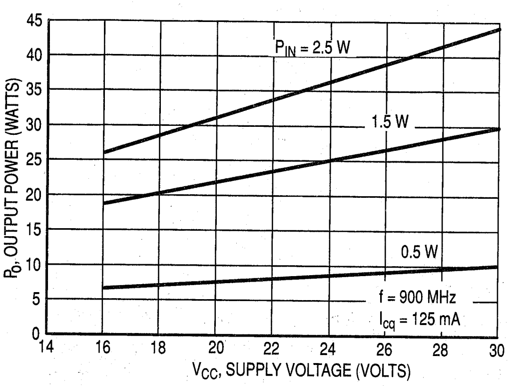


Figure 4. Output Power versus Supply Voltage

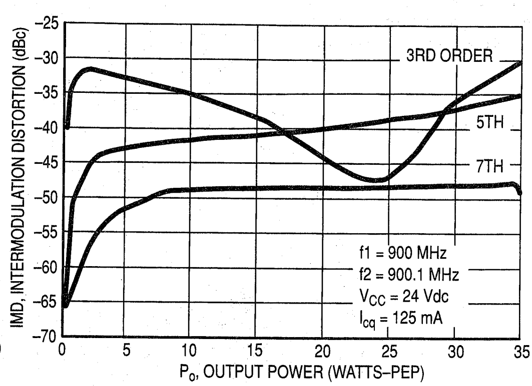


Figure 5. Intermodulation versus Output Power

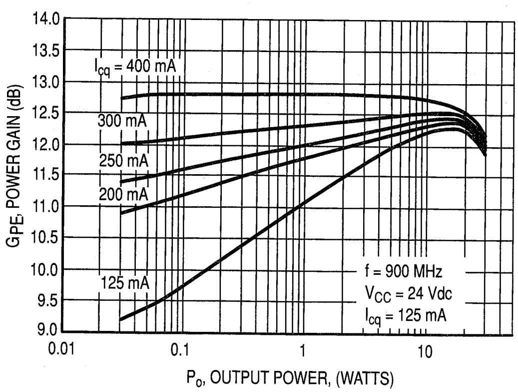


Figure 6. Power Gain versus Output Power

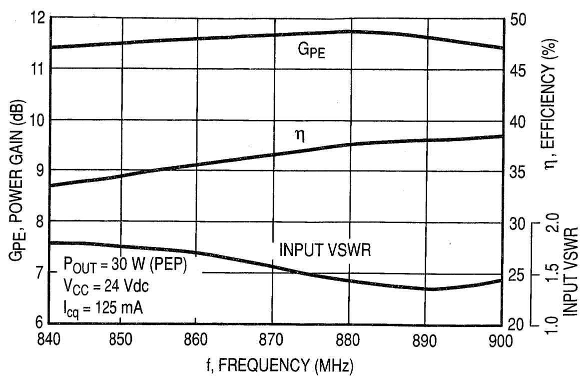
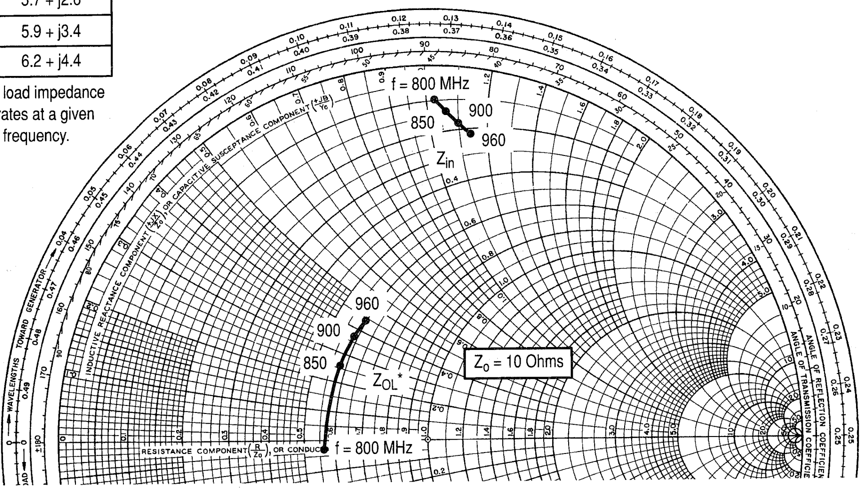


Figure 7. Broadband Test Fixture Performance

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	1.0 + j10.3	5.9 – j0.4
850	1.5 + j10.5	5.7 + j2.6
900	1.8 + j11.0	5.9 + j3.4
960	2.2 + j11.4	6.2 + j4.4

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.



NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively.

P_o = 300 W (PEP), V_{CC} = 24 V

Figure 8. Series Equivalent Input/Output Impedances

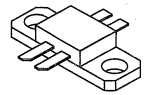
The RF Line
NPN Silicon RF Power Transistor

MRF897R

Designed for 24 Volt UHF large–signal, common emitter, class–AB linear amplifier applications in industrial and commercial FM/AM equipment operating in the range 800–970 MHz.

- Specified 24 Volt, 900 MHz Characteristics
  Output Power = 30 Watts
  Minimum Gain = 10.5 dB @ 900 MHz, class–AB
  Minimum Efficiency = 30% @ 900 MHz, 30 Watts (PEP)
  Maximum Intermodulation Distortion –30 dBc @ 30 Watts (PEP)
- Characterized with Series Equivalent Large–Signal Parameters from 800 to 960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, and Rated Output Power
- Gold Metalized, Emitter Ballasted for Long Life and Resistance to Metal–Migration
- Circuit Board Photomaster Available by Ordering Document MRF897RPHT/D from Motorola Literature Distribution.

30 W, 900 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 395B–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	105 0.60	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W

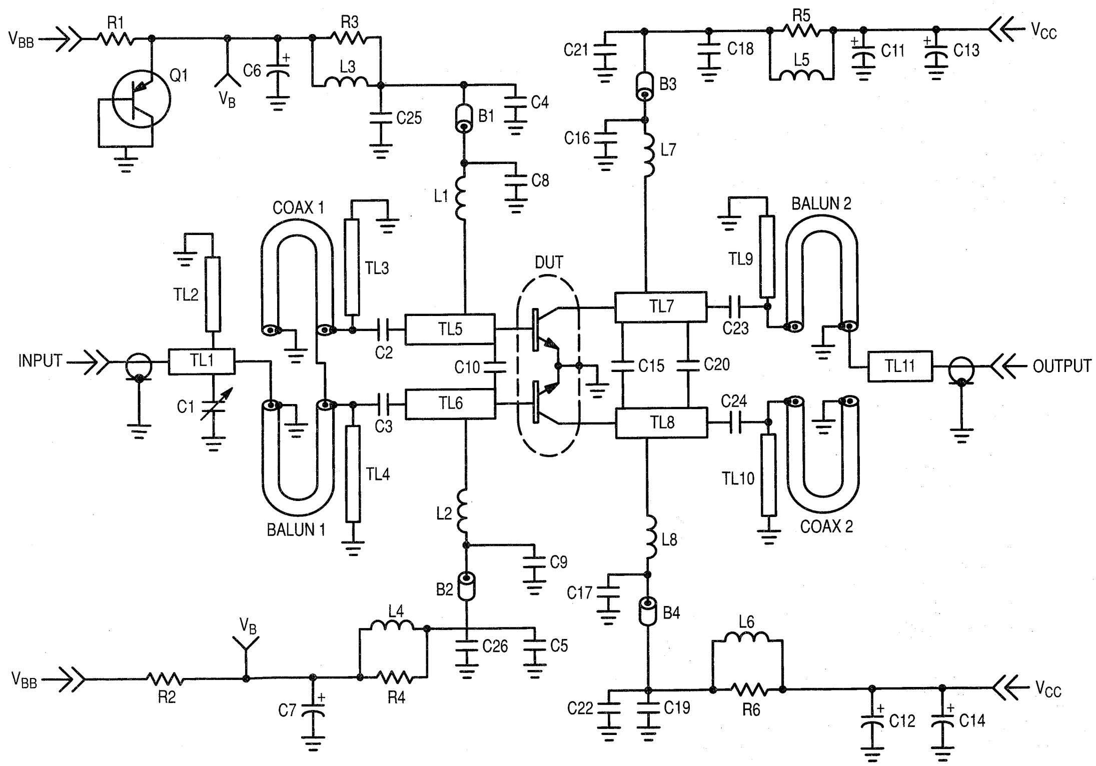
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	33	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	80	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	4.7	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	10.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5 Vdc)	h_{FE}	30	80	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	14	21	28	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	G_{pe}	10.5	12.0	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	η	30	38	—	%
Intermodulation Distortion (V_{CC} = 24 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz)	IMD	—	–37	–30	dBc
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{cq} = 125 mA, f_1 = 900 MHz, f_2 = 900.1 MHz, Load VSWR = 5:1 (all phase angles))	ψ	No Degradation in Output Power			



B1, B2, B3, B4 — Short Ferrite Bead, Fair Rite #2743019447
C1 — 0.8–8.0 pF Var Capacitor, Johansen Gigatrim
C2, C3, C23, C24 — 43 pF, 100 mil, ATC Chip Capacitor
C4, C5, C21, C22 — 1000 pF, 100 mil, ATC Chip Capacitor
C6, C7, C11, C12 — 10 μF, Electrolytic Capacitor, Panasonic
C8, C9, C16, C17 — 100 pF, 100 mil, ATC Chip Capacitor
C10 — 9.1 pF, 50 mil, ATC Chip Capacitor
C13 — 250 μF Electrolytic Capacitor, Mallory
C14, C18, C19, C25 — 0.1 μF, Chip Capacitor, Kemet
C15 — 1.1 pF, 50 mil, ATC Chip Capacitor
C20 — 6.8 pF, 100 mil, ATC Chip Capacitor
L1, L2, L3, L4, L5, L6, L7, L8 — 5 Turns 20 AWG, IDIA 0.126″ Choke, Taylor Spring 46 nH
N1, N2 — Type N Flange Mount, Omni Spectra 3052–1648–10
Q1 — Bias Transistor BD136 PNP
R1, R12 — 27 Ohm, 2.0 W
R3, R4, R5, R6 — 4.0 x 39 Ohm, 1/8 W, Chips Resistors in Parallel, Rohm 390–J
SB1 — 0.15″ x 0.3″ x 0.03″ Cu
TL1–TL11 — Microstrip Line, See Photomaster
Balun1, Balun2, Coax 1, Coax 2 — 2.20″ 50 Ohm, 0.086″ o.d. semi–rigid coax, Micro Coax UT–85–M17
Circuit Board — 1/32″ Glass Teflon, Arlon GX–0300–55–22, ε_r = 2.55

Figure 1. 840–900 MHz Test Circuit Schematic

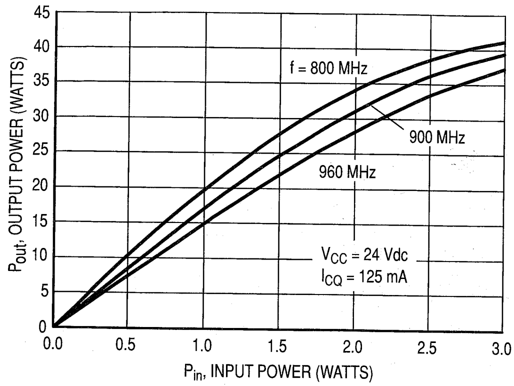


Figure 2. Output Power versus Input Power

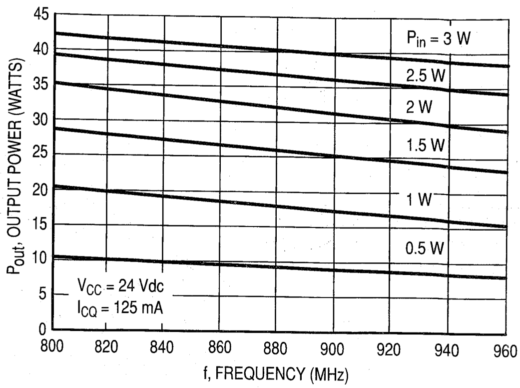


Figure 3. Output Power versus Frequency

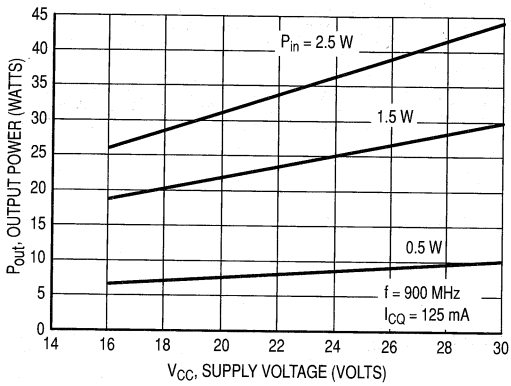


Figure 4. Output Power versus Supply Voltage

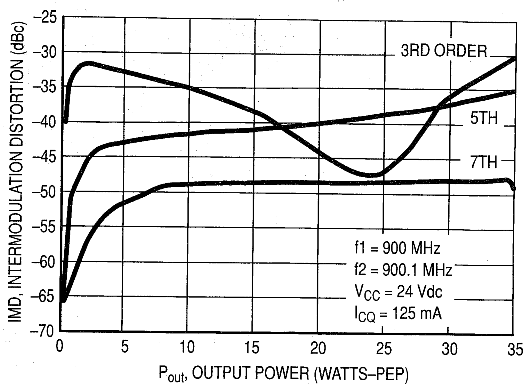


Figure 5. Intermodulation versus Output Power

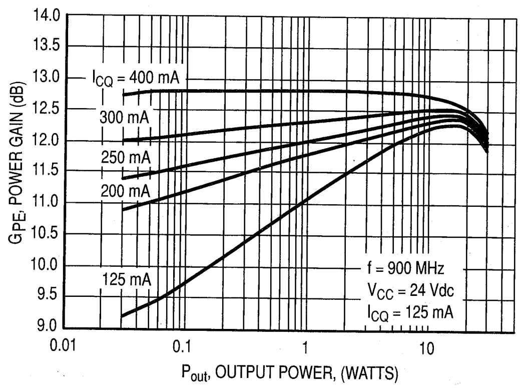


Figure 6. Power Gain versus Output Power

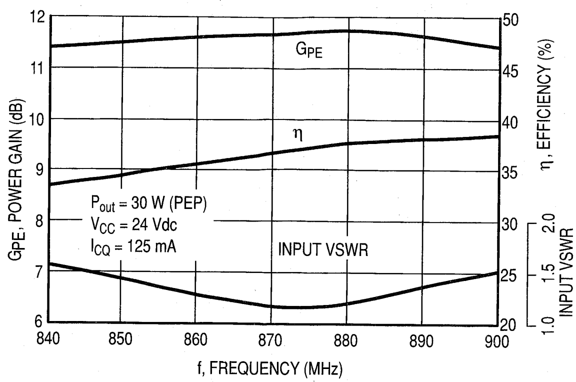
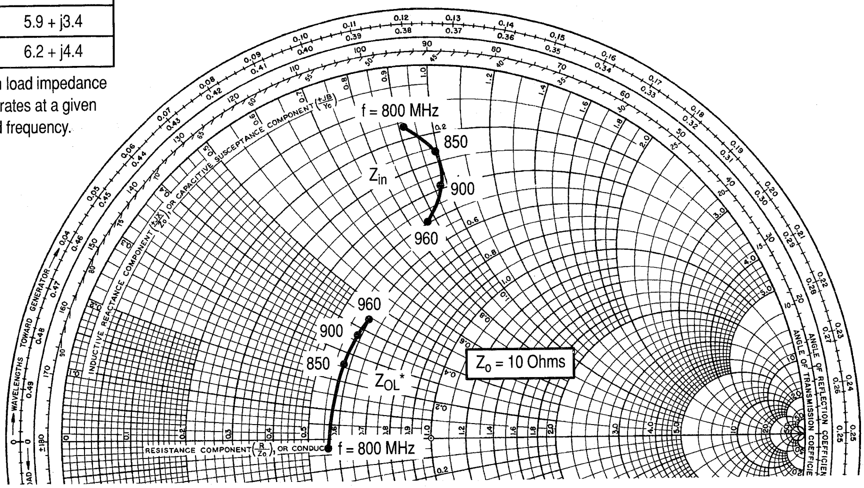


Figure 7. Broadband Test Fixture Performance

P_{out} = 30 W (PEP), V_{CC} = 24 V

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
800	1.7 + j9.2	5.9 – j0.4
850	2.6 + j10	5.7 + j2.6
900	4 + j9.9	5.9 + j3.4
950	5 + j8.8	6.2 + j4.4

Z_{OL}^* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.



NOTE: Z_{in} & Z_{OL}^* are given from base–to–base and collector–to–collector respectively.

Figure 8. Series Equivalent Input/Output Impedances

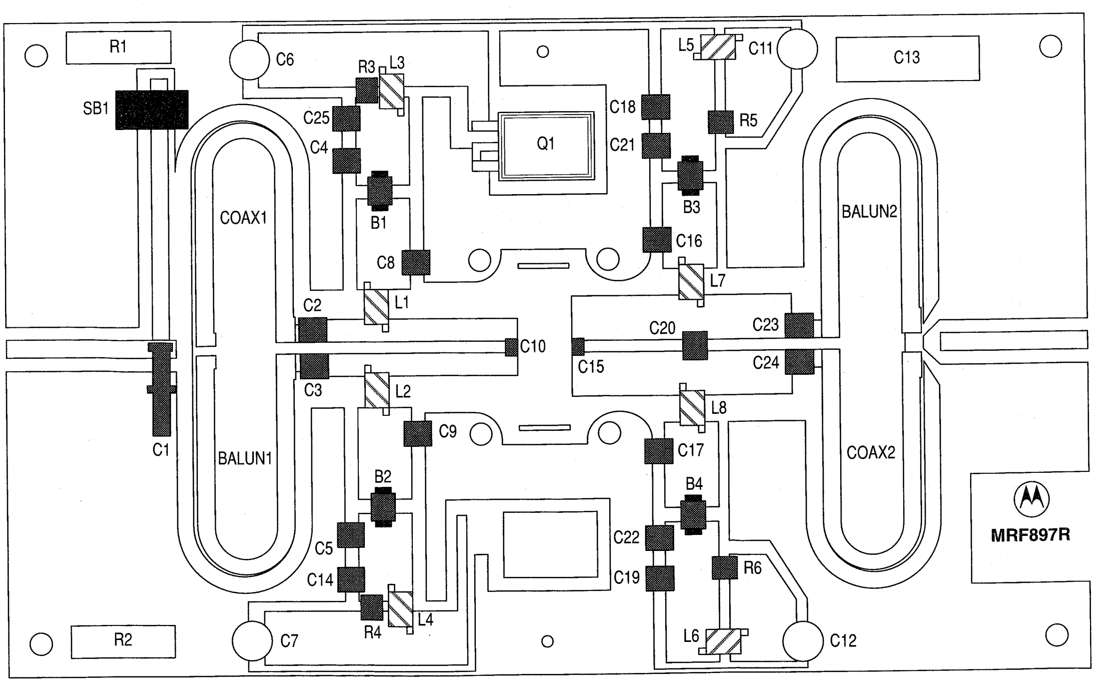


Figure 9. 840–900 MHz Test Circuit Component Layout

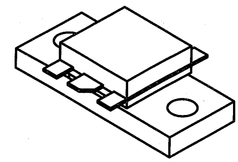
The RF Line
NPN Silicon
RF Power Transistor

MRF898

. . . designed for 24 Volt UHF large–signal, common base amplifier applications in industrial and commercial FM equipment operating in the range of 850–960 MHz.

- Motorola Advanced Amplifier Concept Package
- Specified 24 Volt, 900 MHz Characteristics
  Output Power = 60 Watts
  Power Gain = 7.0 dB Min
  Efficiency = 60% Min
- Double Input/Output Matched for Wideband Performance and Simplified External Matching
- Series Equivalent Large–Signal Characterization
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

60 W, 850–960 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 333A–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	10	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	175 1.0	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	10	mAdc

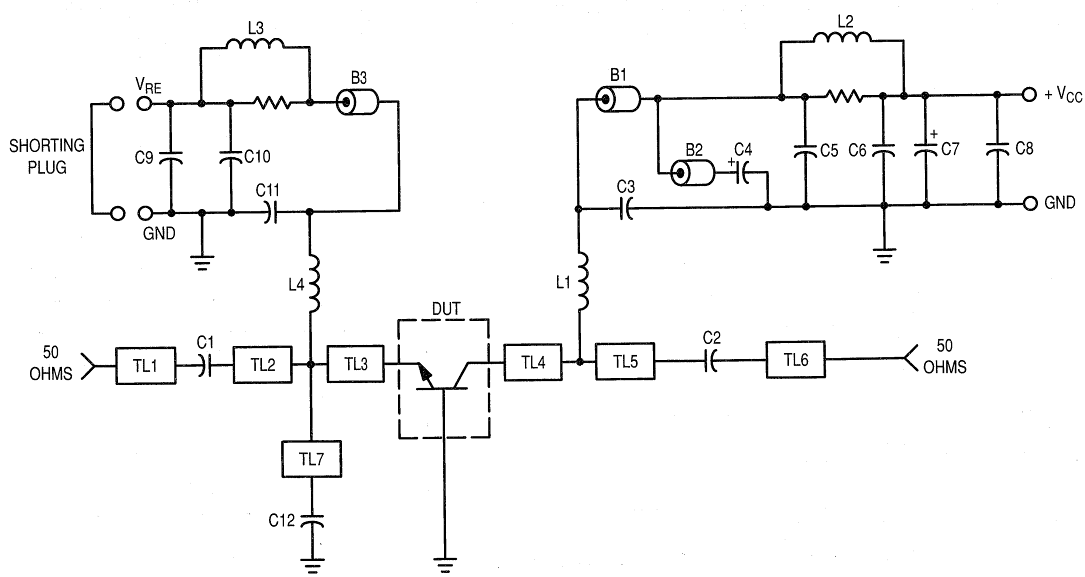
(continued)

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	50	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (1) (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	60	—	pF
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 60 W, f = 900 MHz)	G_{pb}	7.0	7.9	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 60 W, f = 900 MHz)	η	60	65	—	%
Output Mismatch Stress (V_{CC} = 24 Vdc, P_{out} = 60 W, f = 900 MHz, VSWR = 5:1, all phase angles)	ψ	No Degradation in Output Power			

NOTE:
1. Value of "C_{ob}" is that of die only. It is not measurable in MRF898 because of internal matching network.



B1, B2, B3 — Bead, Ferroxcube 56–390–65/3B
C1, C2, C12 — 39 pF, 100 Mil Chip Capacitor
C3, C11 — 91 pF, Mini Underwood or Equivalent
C4, C7, C9 — 10 µF, 35 V Electrolytic
C5 — 4000 pF, 1.0 kV Ceramic
C6, C10 — 1000 pF, 350 V Unelco or Equivalent
C8 — 47 pF, 100 Mil Chip Capacitor
L1, L4 — 4 Turns #18 AWG Choke
L2 — 11 Turns #20 AWG Choke on 10 Ohm, 1.0 Watt Resistor
L3 — 3 Turns #18 AWG Choke on 10 Ohm, 1.0 Watt Resistor

TL1, TL6 — 50 Ohm Microstrip
TL2 — 400 x 950 Mils
TL3, TL4 — 140 x 200 Mils
TL5 — 320 x 690 Mils
TL7 — 260 x 230 Mils
Board — 3M Epsilam–10, 50 Mil
Bias Boards — 1/32″ G10 or Equivalent

Figure 1. 850–960 MHz Broadband Test Circuit

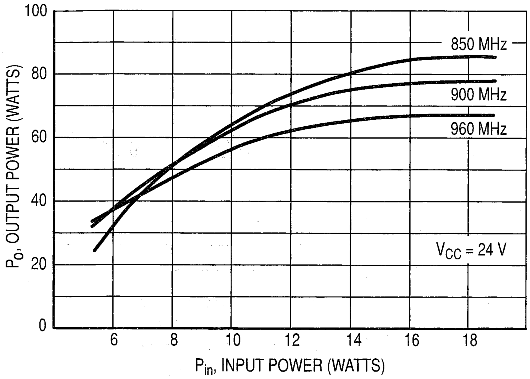


Figure 2. Output Power versus Input Power

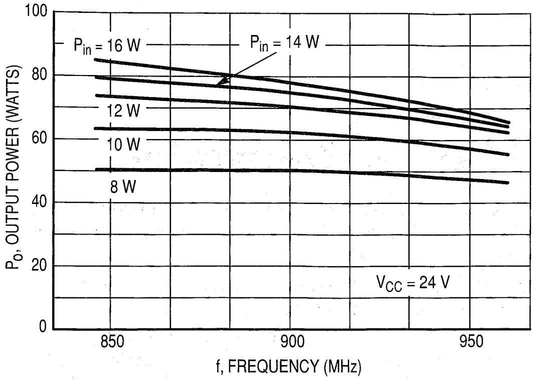


Figure 3. Output Power versus Frequency

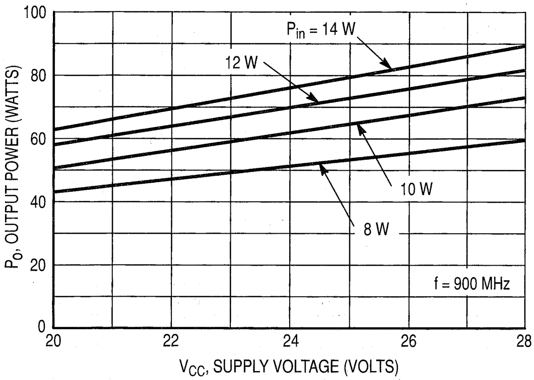


Figure 4. Output Power versus Supply Voltage

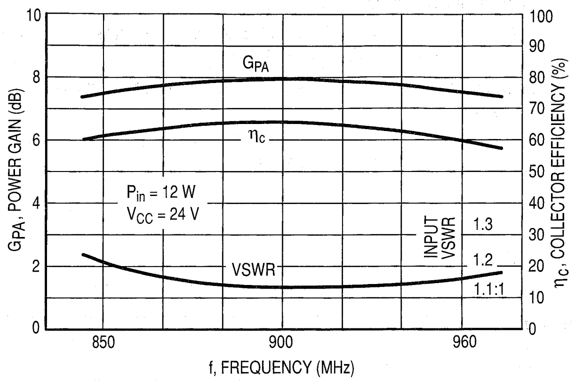
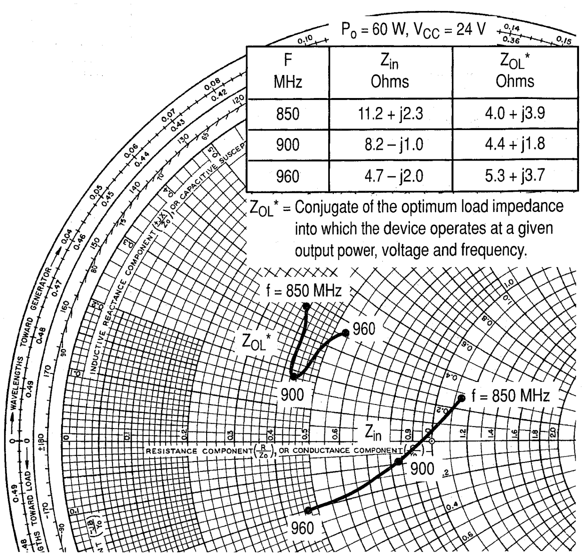


Figure 5. Typical Broadband Circuit Performance



F MHz	Z_{in} Ohms	Z_{OL}* Ohms
850	11.2 + j2.3	4.0 + j3.9
900	8.2 – j1.0	4.4 + j1.8
960	4.7 – j2.0	5.3 + j3.7

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 6. Input/Output Impedance versus Frequency

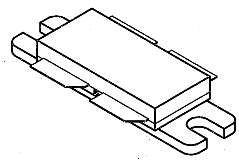
The RF Line
NPN Silicon RF Power Transistor

MRF899

Designed for 26 Volt UHF large–signal, common emitter, Class AB linear amplifier applications in industrial and commercial FM/AM equipment operating in the range 800–960 MHz.

- Specified 26 Volt, 900 MHz Characteristics
  Output Power = 150 Watts (PEP)
  Minimum Gain = 8.0 dB @ 900 MHz, Class AB
  Minimum Efficiency = 35% @ 900 MHz, 150 Watts (PEP)
  Maximum Intermodulation Distortion –28 dBc @ 150 Watts (PEP)
- Characterized with Series Equivalent Large–Signal Parameters from 800 to 960 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 5:1 VSWR @ 26 Vdc, and Rated Output Power
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

150 W, 900 MHz
RF POWER
TRANSISTOR
NPN SILICON



CASE 375A–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	28	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current — Continuous	I_C	25	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	230 1.33	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	28	37	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	85	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	4.9	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	30	75	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1.0 MHz) (1)	C_{ob}	—	75	—	pF

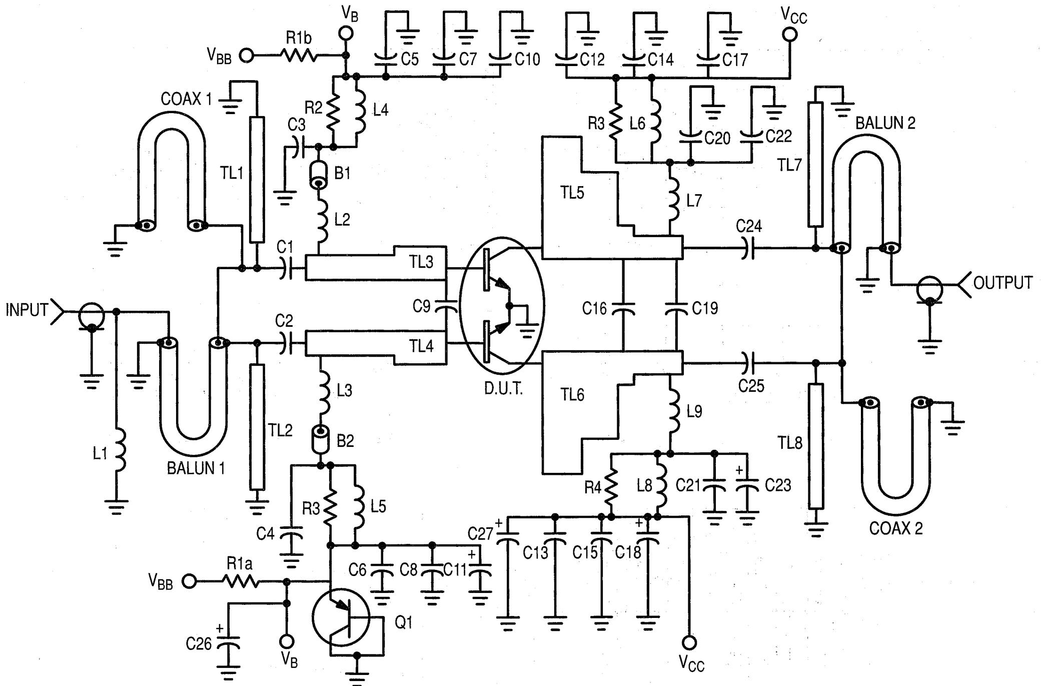
(1) For information only. This part is collector matched.

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS					
Common–Emitter Amplifier Power Gain V_{CC} = 26 Vdc, P_{out} = 150 Watts (PEP), I_{cq} = 300 mA, f_1 = 900 MHz, f_2 = 900.1 MHz	G_{pe}	8.0	9.0	—	dB
Collector Efficiency V_{CC} = 26 Vdc, P_{out} = 150 Watts (PEP), I_{cq} = 300 mA, f_1 = 900 MHz, f_2 = 900.1 MHz	η	30	40	—	%
3rd Order Intermodulation Distortion V_{CC} = 26 Vdc, P_{out} = 150 Watts (PEP), I_{cq} = 300 mA, f_1 = 900 MHz, f_2 = 900.1 MHz	IMD	—	−32	−28	dBc
Output Mismatch Stress V_{CC} = 26 Vdc, P_{out} = 150 Watts (PEP), I_{cq} = 300 mA, f_1 = 900 MHz, f_2 = 900.1 MHz, VSWR = 5:1 (all phase angles)	ψ	No Degradation in Output Power Before and After Test			



B1, B2 — Ferrite Bead, Ferroxcube #56–590–65–3B
C1, C2, C24, C25 — 43 pF, B Case, ATC Chip Capacitor
C3, C4, C20, C21 — 100 pF, B Case, ATC Chip Capacitor
C5, C6, C12, C13 — 1000 pF, B Case, ATC Chip Capacitor
C7, C8, C14, C15 — 1800 pF, AVX Chip Capacitor
C9 — 9.1 pF, A Case, ATC Chip Capacitor
C10, C11, C17, C18, C22, C23 — 10 µF, Electrolytic Capacitor Panasonic
C16 — 3.9 pF, B Case, ATC Chip Capacitor
C19 — 0.8 pF, B Case, ATC Chip Capacitor
C26 — 200 µF, Electrolytic Capacitor Mallory Sprague
C27 — 500 µF Electrolytic Capacitor

L1 — 5 Turns 24 AWG IDIA 0.059″ Choke, 19.8 nH
L2, L3, L7, L9 — 4 Turns 20 AWG IDIA 0.163″ Choke
L4, L5, L6, L8 — 12 Turns 22 AWG IDIA 0.140″ Choke
N1, N2 — Type N Flange Mount, Omni Spectra
Q1 — Bias Transistor BD136 PNP
R2, R3, R4, R5 — 4.0 x 39 Ohm 1/8 W Chips in Parallel
R1a, R1b — 56 Ohm 1.0 W
TL1–TL8 — See Photomaster
Balun1, Balun2, Coax 1, Coax 2 — 2.20″ 50 Ohm 0.088″ o.d. Semi–rigid Coax, Micro Coax
Board — 1/32″ Glass Teflon, ε_r = 2.55″ Arlon (GX–0300–55–22)

Figure 1. 900 MHz Power Gain Test Circuit

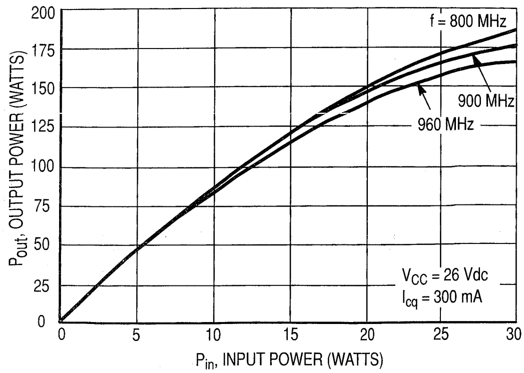


Figure 2. Output Power versus Input Power

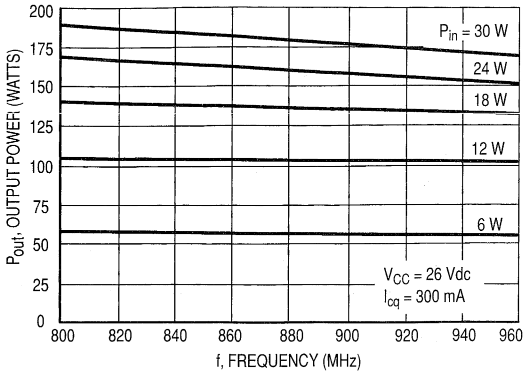


Figure 3. Output Power versus Frequency

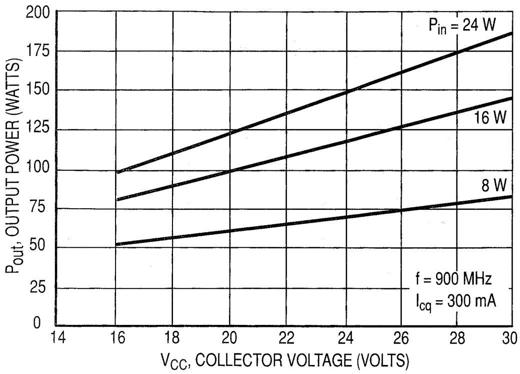


Figure 4. Output Power versus Supply Voltage

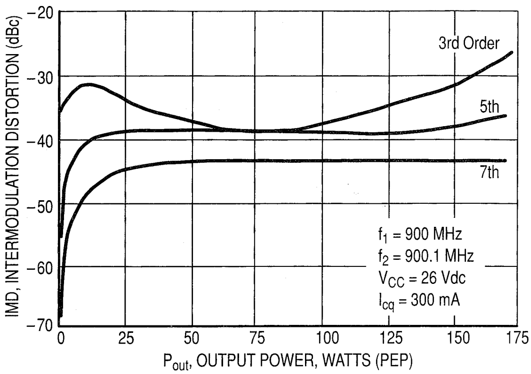


Figure 5. Intermodulation versus Output Power

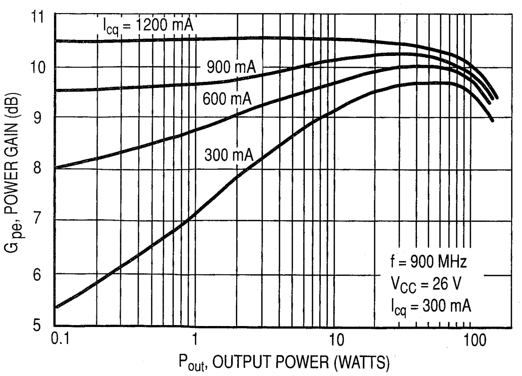


Figure 6. Power Gain versus Output Power

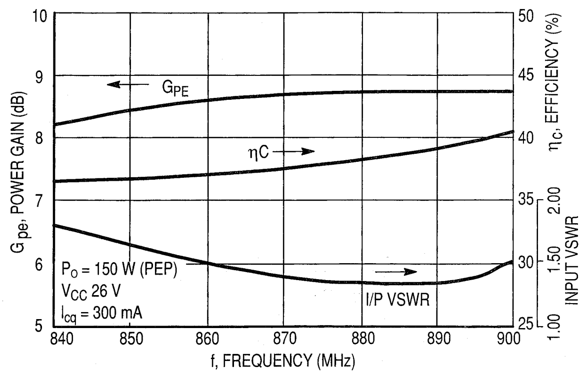
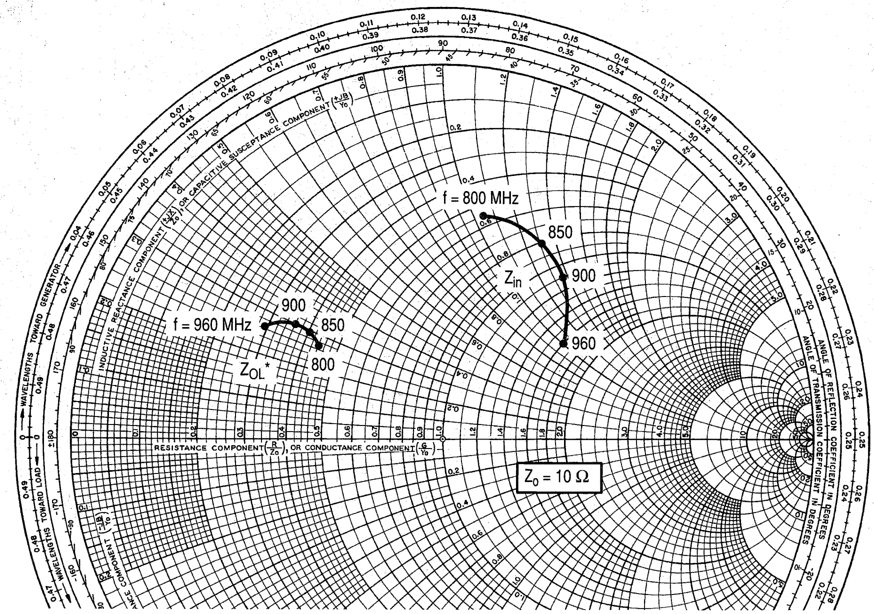


Figure 7. Broadband Test Fixture Performance



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	5.51 + j10.6	4.52 + j2.64
850	8.17 + j13.2	4.21 + j2.98
900	11.2 + j13.8	3.68 + j2.97
960	16.8 + j10.1	2.98 + j2.71

Z_{OL}* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.

NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively

Figure 8. Input and Output Impedances with Circuit Tuned for Maximum Gain @ P_o = 150 W (PEP), V_{CC} = 26 V

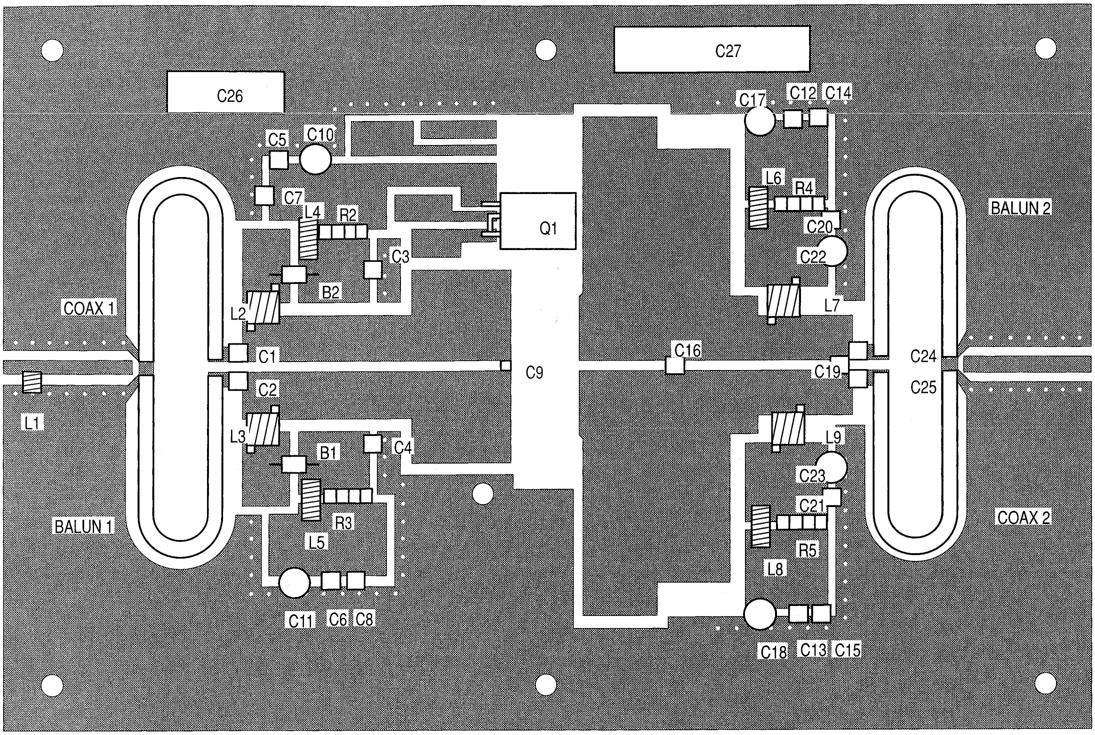


Figure 9. MRF899 Test Fixture Component Layout

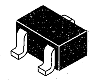
The RF Small Signal Line
NPN Silicon High-Frequency Transistors

MRF917T1

LOW NOISE HIGH FREQUENCY TRANSISTOR

Designed for low noise, wide dynamic range front end amplifiers, at frequencies to 1.5 GHz. Specifically aimed at portable communication devices such as pagers and hand–held phones.

- Small, Surface–Mount Package (SC–70)
- High Current Gain–Bandwidth Product (f_τ = 6.0 GHz Typ @ 6.0 V, 20 mA)
- Low Noise Figure
  NF = 1.7 dB (Typ) @ 500 MHz
- Available in Tape and Reel Packaging.
  T1 Suffix = 3,000 Units per 8 mm, 7 inch Reel



CASE 419–02, STYLE 3 (SC–70/SOT–323)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	12	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Emitter–Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Continuous	I_C	60	mAdc
Total Device Dissipation @ T_C = 75°C (1) Derate above 75°C	P_D	222 3.0	mW mW/°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C
Operating Temperature Range	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction–to–Case (1)	$R_{\theta JC}$	338	°C/W

DEVICE MARKING

MRF917T1 = K

(1) Case temperature measured on the collector lead immediately adjacent to body of package.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = 0.1 mA, I_B = 0 mA)		$V_{(BR)CEO}$	12	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)		$V_{(BR)CBO}$	20	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)		$V_{(BR)EBO}$	2.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)		I_{CBO}	—	—	50	nA
ON CHARACTERISTICS						
DC Current Gain (V_{CE} = 10 Vdc, I_C = 30 mA)		h_{FE}	40	—	200	—
DYNAMIC CHARACTERISTICS						
Collector–Base Capacitance (V_{CB} = 1.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	—	0.54	—	pF
Current–Gain Bandwidth Product (V_{CE} = 6.0 Vdc, I_C = 20 mA, f = 1.0 GHz)		f_τ	—	6.0	—	GHz
PERFORMANCE CHARACTERISTICS						
Noise Figure — Minimum (V_{CE} = 6.0 Vdc, I_C = 5.0 mA) Figure 1	500 MHz 1.0 GHz	NF_{min}	— —	1.7 2.3	— —	dB
Associated Gain at Minimum Noise Figure (V_{CE} = 6.0 Vdc, I_C = 5.0 mA) Figure 1	500 MHz 1.0 GHz	G_{NF}	— —	15.4 10	— —	dB
Maximum Unilateral Gain (V_{CE} = 6.0 Vdc, I_C = 20 mA, f = 1000 MHz)		G_{Umax}	—	12	—	dB
Insertion Gain (V_{CE} = 6.0 Vdc, I_C = 20 mA, f = 1000 MHz)		$\|S_{21}\|^2$	—	11.2	—	dB
Noise Resistance (V_{CE} = 6.0 Vdc, I_C = 5.0 mA, f = 1000 MHz)		R_N	—	15	—	Ohms

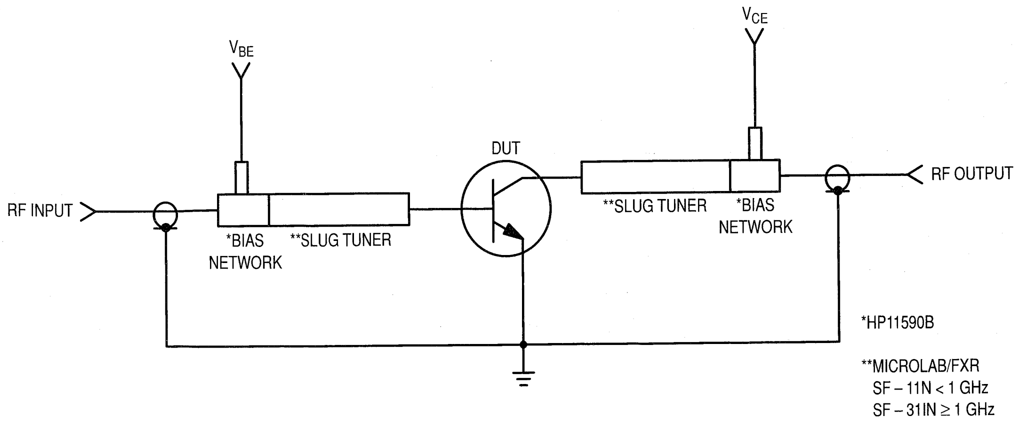


Figure 1. Functional Circuit Schematic

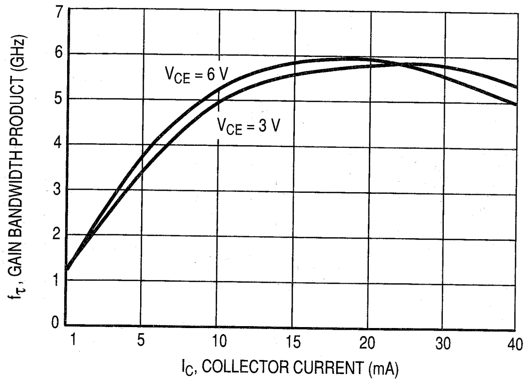


Figure 2. f_τ, Current–Gain Bandwidth Product versus Collector Current

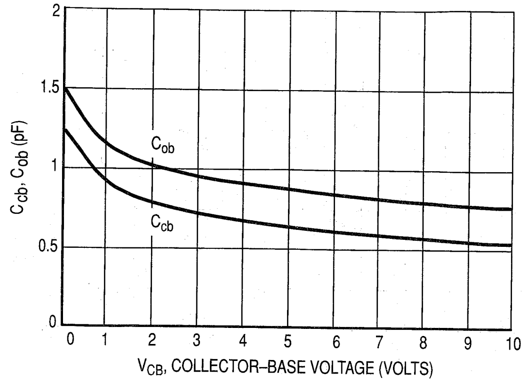


Figure 3. Output Capacitance versus Collector–Base Voltage

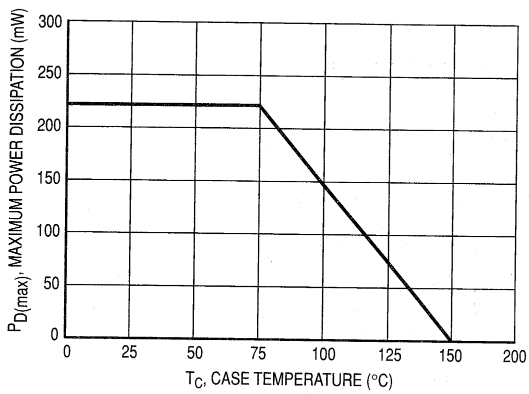


Figure 4. Maximum Power Dissipation versus Collector Lead Temperature (T_C)

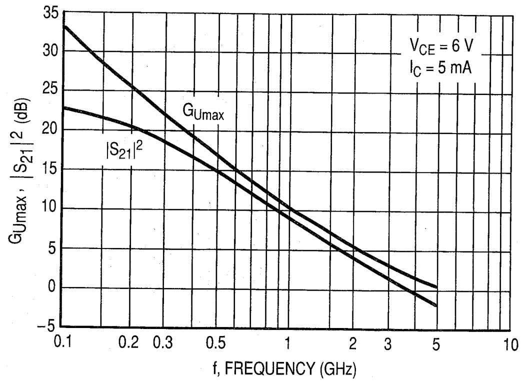


Figure 5. Forward Insertion Gain and Maximum Unilateral Gain versus Frequency

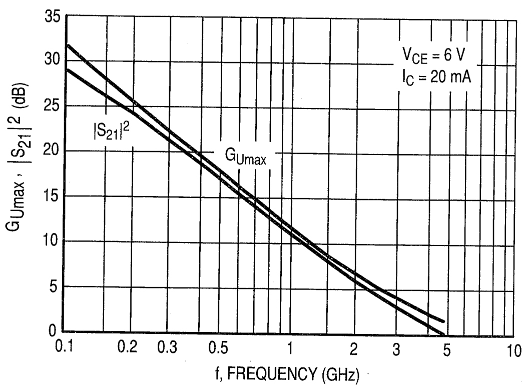


Figure 6. Forward Insertion Gain and Maximum Unilateral Gain versus Frequency

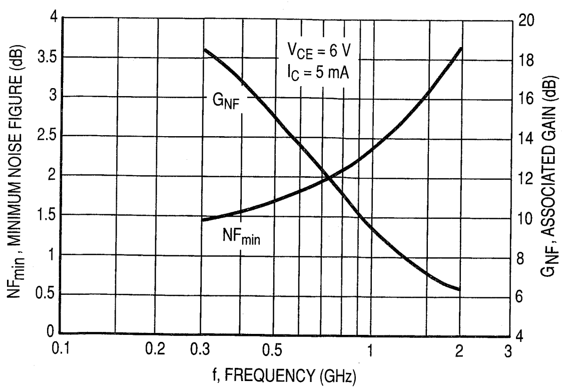


Figure 7. Minimum Noise Figure and Associated Gain versus Frequency

TYPICAL CHARACTERISTICS

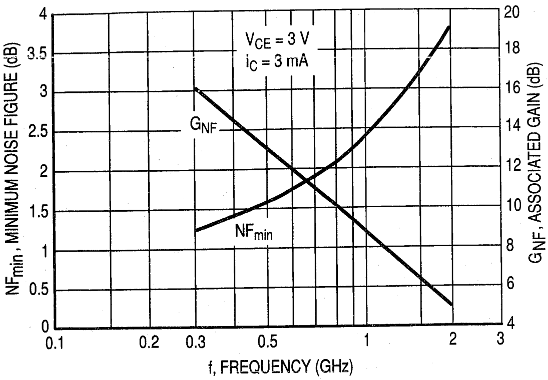


Figure 8. Minimum Noise Figure and Associated Gain versus Frequency

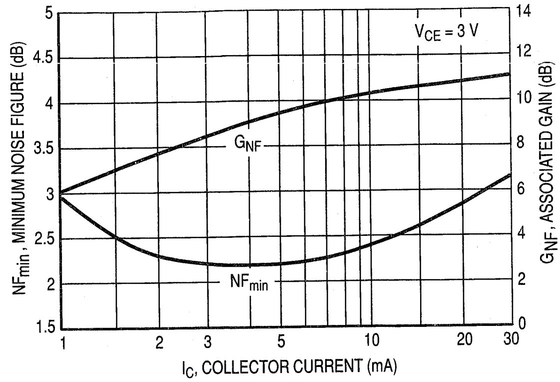


Figure 9. Minimum Noise Figure and Associated Gain versus Collector Current

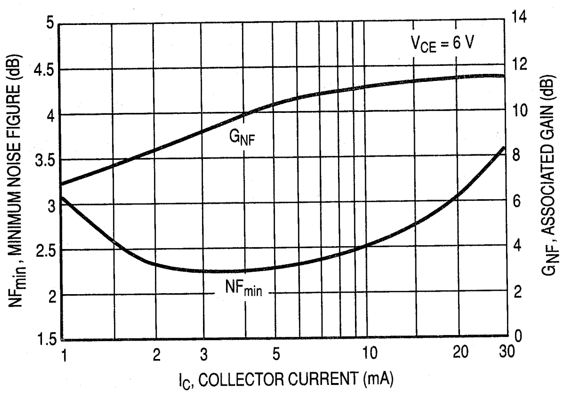
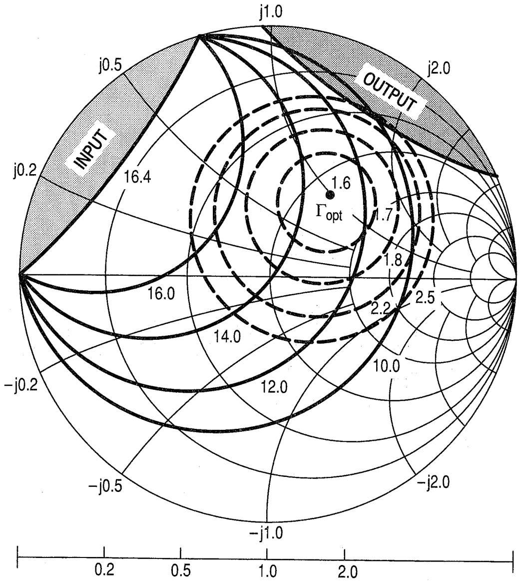


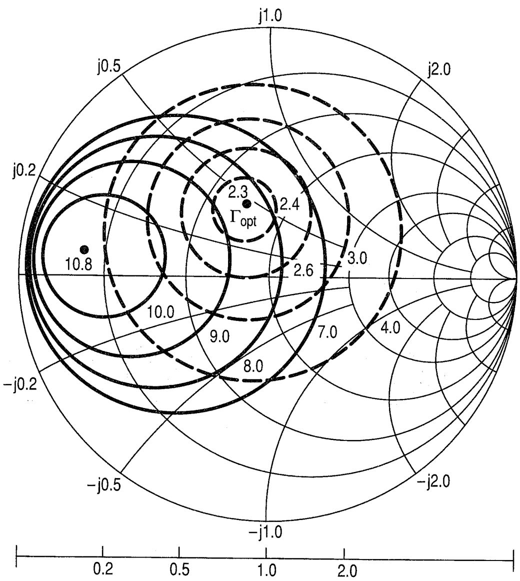
Figure 10. Minimum Noise Figure and Associated Gain versus Collector Current



V_{CE} = 3.0 V
I_C = 3.0 mA
▨ — Potentially Unstable

f (MHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
500	1.60	0.39 ∠ 52°	19	0.67

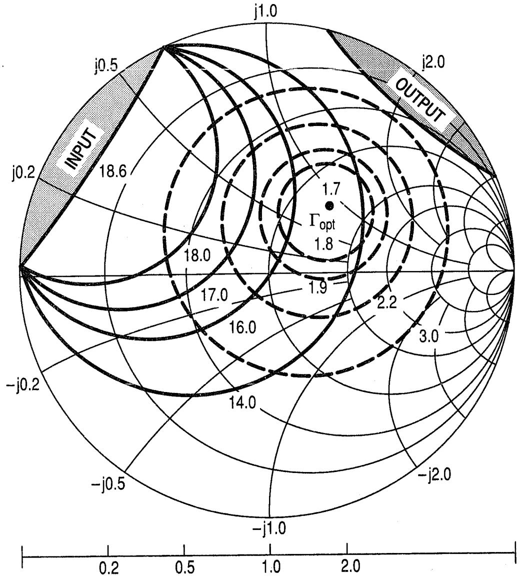
Figure 11. Constant Gain and Noise Figure Contours



V_{CE} = 3.0 V
I_C = 3.0 mA

f (MHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
1000	2.30	0.29 ∠ 110°	15	1.09

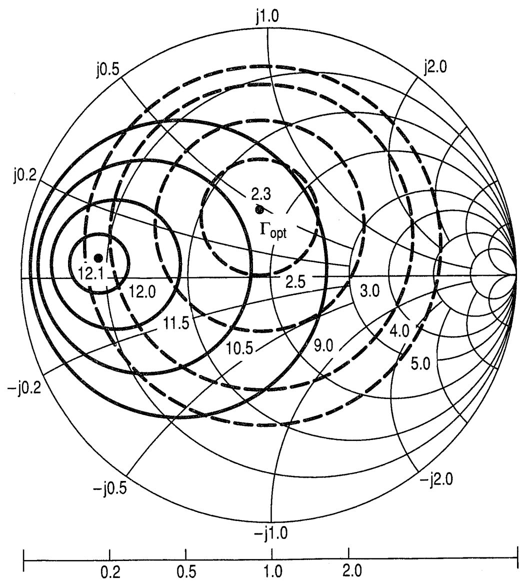
Figure 12. Constant Gain and Noise Figure Contours



V_{CE} = 6.0 V
I_C = 5.0 mA
▨ — Potentially Unstable

f (MHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
500	1.70	0.35 ∠ 45°	19	0.80

Figure 13. Constant Gain and Noise Figure Contours



V_{CE} = 6.0 V
I_C = 5.0 mA

f (MHz)	NF OPT (dB)	ΓMS NF OPT	R_N	K
1000	2.3	0.25 ∠ 99°	16	1.09

Figure 14. Constant Gain and Noise Figure Contours

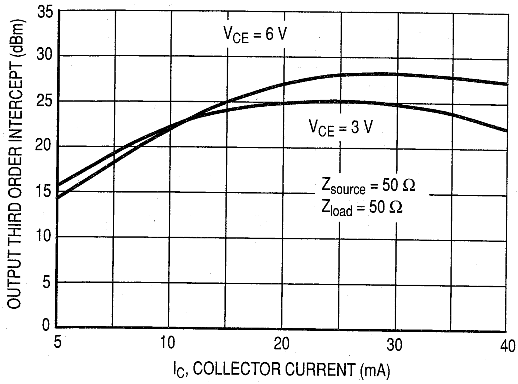


Figure 15. Output Third Order Intercept versus Collector Current

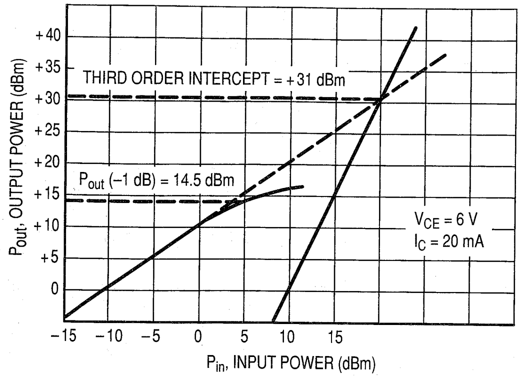


Figure 16. Third Order Intercept and 1 dB Compression Point

V_{CE}	I_C	f (MHz)	NF_{min} (dB)	|Gam Opt|	∠ Gam Opt	R_N
3.0 V	1 mA	300	1.22	0.58	33	27
		500	1.74	0.50	61	25
		900	2.70	0.41	111	19
		1000	2.93	0.40	121	18
		1500	3.96	0.41	166	13
		2000	4.83	0.54	–165	13
	3 mA	300	1.25	0.46	26	20
		500	1.57	0.39	52	19
		900	2.19	0.30	100	16
		1000	2.34	0.29	110	15
		1500	3.08	0.31	158	13
		2000	3.81	0.45	–165	11
6.0 V	3 mA	300	1.28	0.49	23	22
		500	1.60	0.41	48	20
		900	2.24	0.30	94	17
		1000	2.39	0.29	104	16
		1500	3.18	0.30	153	14
		2000	3.97	0.43	–167	12
	5 mA	300	1.45	0.41	21	20
		500	1.68	0.35	45	19
		900	2.17	0.26	89	16
		1000	2.30	0.25	100	16
		1500	2.96	0.26	149	13
		2000	3.66	0.39	–167	12
	10 mA	300	1.96	0.27	21	20
		500	2.09	0.23	46	19
		900	2.40	0.20	93	16
		1000	2.49	0.19	104	16
		1500	3.00	0.24	154	14
		2000	3.60	0.36	–164	12

Table 1. MRF917T1 Common Emitter Noise Parameters

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle \phi$	$\|S_{21}\|$	$\angle \phi$	$\|S_{12}\|$	$\angle \phi$	$\|S_{22}\|$	$\angle \phi$
3.0	3.0	0.10	0.814	−38	9.28	152	0.040	70	0.921	−18
		0.20	0.704	−69	7.56	132	0.066	56	0.784	−28
		0.30	0.615	−91	6.11	117	0.081	49	0.677	−34
		0.40	0.553	−109	5.01	106	0.091	46	0.602	−37
		0.50	0.512	−122	4.24	98	0.098	45	0.552	−39
		0.60	0.465	−134	3.59	92	0.104	44	0.510	−39
		0.70	0.447	−144	3.16	86	0.110	45	0.487	−40
		0.80	0.441	−151	2.79	81	0.117	45	0.472	−41
		0.90	0.428	−159	2.54	77	0.123	46	0.457	−43
		1.00	0.424	−165	2.32	72	0.129	47	0.447	−44
		1.50	0.423	170	1.64	55	0.167	51	0.420	−55
		2.00	0.439	152	1.30	40	0.211	52	0.413	−68
		2.50	0.462	135	1.09	28	0.263	51	0.407	−83
		3.00	0.485	122	0.95	19	0.321	48	0.406	−98
		4.00	0.543	98	0.77	5	0.446	38	0.410	−133
	5.0	0.10	0.717	−48	13.51	146	0.036	67	0.864	−24
		0.20	0.589	−83	10.13	124	0.057	55	0.678	−36
		0.30	0.511	−106	7.75	110	0.068	51	0.559	−41
		0.40	0.463	−123	6.17	101	0.078	50	0.485	−43
		0.50	0.436	−135	5.12	94	0.086	51	0.440	−44
		0.60	0.400	−146	4.31	88	0.094	52	0.402	−42
		0.70	0.390	−154	3.76	84	0.103	53	0.381	−43
		0.80	0.389	−162	3.32	79	0.112	53	0.367	−44
		0.90	0.381	−168	2.99	75	0.121	54	0.356	−45
		1.00	0.380	−173	2.73	71	0.130	55	0.347	−46
		1.50	0.388	165	1.91	55	0.179	55	0.323	−56
		2.00	0.406	148	1.51	42	0.229	53	0.316	−68
		2.50	0.431	133	1.27	30	0.281	50	0.310	−83
		3.00	0.456	121	1.11	20	0.335	46	0.309	−98
		4.00	0.519	99	0.90	4	0.446	36	0.322	−133
	10	0.10	0.552	−67	19.98	136	0.031	63	0.752	−34
		0.20	0.442	−105	13.19	114	0.045	57	0.523	−45
		0.30	0.398	−127	9.51	103	0.056	58	0.413	−49
		0.40	0.377	−142	7.37	95	0.067	59	0.351	−49
		0.50	0.365	−151	6.02	89	0.078	61	0.317	−50
		0.60	0.345	−162	5.05	85	0.089	62	0.284	−46
		0.70	0.343	−168	4.37	81	0.100	62	0.269	−46
		0.80	0.345	−174	3.86	77	0.112	62	0.258	−47
		0.90	0.341	−179	3.46	74	0.123	62	0.250	−48
		1.00	0.344	177	3.14	70	0.135	62	0.243	−49
		1.50	0.359	159	2.19	56	0.192	59	0.223	−58
		2.00	0.378	144	1.72	43	0.248	54	0.216	−71
		2.50	0.404	130	1.44	32	0.301	49	0.210	−87
		3.00	0.431	119	1.26	22	0.352	44	0.210	−102
		4.00	0.492	99	1.03	5	0.452	33	0.227	−138
	20	0.10	0.394	−94	25.51	125	0.024	64	0.612	−44
		0.20	0.349	−131	15.10	106	0.037	64	0.387	−52
		0.30	0.339	−148	10.51	97	0.049	66	0.301	−54
		0.40	0.336	−159	8.03	91	0.062	68	0.255	−54
		0.50	0.333	−165	6.50	86	0.075	68	0.232	−54
		0.60	0.323	−175	5.44	82	0.088	69	0.204	−48
		0.70	0.325	−179	4.70	79	0.100	68	0.194	−48
		0.80	0.329	176	4.14	75	0.113	68	0.185	−50
		0.90	0.329	173	3.71	72	0.126	67	0.180	−50
		1.00	0.332	169	3.36	69	0.139	66	0.175	−52
		1.50	0.351	154	2.33	56	0.201	61	0.160	−62
		2.00	0.372	141	1.82	44	0.258	55	0.155	−77
		2.50	0.399	128	1.53	33	0.313	50	0.151	−95
		3.00	0.423	118	1.34	24	0.364	44	0.152	−111
		4.00	0.486	98	1.09	7	0.459	32	0.174	−149

Table 2. MRF917T1 Common Emitter S–Parameters

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
3.0	40	0.10	0.331	−127	26.91	116	0.020	67	0.480	−49
		0.20	0.338	−154	14.86	100	0.033	70	0.297	−52
		0.30	0.342	−164	10.16	93	0.046	72	0.239	−51
		0.40	0.347	−171	7.70	88	0.060	73	0.210	−50
		0.50	0.347	−175	6.22	84	0.074	73	0.196	−50
		0.60	0.344	177	5.21	80	0.087	73	0.176	−44
		0.70	0.346	174	4.49	77	0.100	72	0.171	−45
		0.80	0.352	170	3.96	74	0.114	71	0.164	−47
		0.90	0.352	167	3.54	71	0.127	70	0.161	−47
		1.00	0.356	164	3.21	68	0.140	69	0.157	−50
		1.50	0.377	151	2.23	55	0.202	63	0.145	−62
		2.00	0.400	138	1.75	43	0.261	57	0.142	−80
		2.50	0.426	126	1.47	33	0.317	50	0.139	−100
		3.00	0.448	115	1.29	23	0.369	44	0.141	−117
		4.00	0.504	96	1.06	7	0.465	32	0.166	−156
6.0	3.0	0.10	0.829	−34	9.23	154	0.033	71	0.936	−14
		0.20	0.720	−63	7.67	134	0.056	59	0.823	−23
		0.30	0.627	−85	6.30	120	0.069	52	0.730	−28
		0.40	0.557	−102	5.21	109	0.078	49	0.664	−31
		0.50	0.509	−115	4.44	101	0.085	47	0.619	−32
		0.60	0.456	−127	3.77	94	0.091	47	0.581	−32
		0.70	0.434	−137	3.32	88	0.096	47	0.561	−33
		0.80	0.425	−145	2.93	83	0.102	48	0.547	−34
		0.90	0.408	−153	2.67	79	0.108	49	0.534	−35
		1.00	0.402	−160	2.44	75	0.114	50	0.524	−37
		1.50	0.396	174	1.72	57	0.148	54	0.501	−46
		2.00	0.411	155	1.36	43	0.189	56	0.494	−58
		2.50	0.435	137	1.14	31	0.237	56	0.485	−71
		3.00	0.463	123	0.99	21	0.294	54	0.482	−84
		4.00	0.525	99	0.79	7	0.424	45	0.473	−117
	5.0	0.10	0.736	−43	13.73	148	0.030	69	0.888	−20
		0.20	0.602	−75	10.55	126	0.048	58	0.727	−29
		0.30	0.512	−98	8.19	113	0.059	54	0.620	−33
		0.40	0.454	−114	6.56	103	0.068	53	0.553	−35
		0.50	0.418	−127	5.47	96	0.076	53	0.512	−35
		0.60	0.377	−138	4.61	90	0.083	54	0.479	−34
		0.70	0.363	−147	4.03	85	0.091	55	0.461	−34
		0.80	0.359	−155	3.55	81	0.099	56	0.448	−35
		0.90	0.348	−162	3.21	77	0.107	57	0.438	−36
		1.00	0.346	−168	2.92	73	0.116	57	0.430	−37
		1.50	0.351	169	2.04	57	0.160	58	0.409	−46
		2.00	0.370	152	1.60	44	0.206	57	0.401	−57
		2.50	0.398	136	1.30	32	0.255	54	0.392	−69
		3.00	0.425	123	1.17	22	0.307	51	0.389	−82
		4.00	0.496	100	0.93	6	0.421	42	0.385	−113
	10	0.100	0.547	−62	21.95	136	0.025	66	0.768	−29
		0.200	0.417	−99	14.53	115	0.038	60	0.558	−37
		0.300	0.362	−120	10.49	103	0.048	61	0.460	−38
		0.400	0.334	−135	8.13	96	0.058	63	0.408	−38
		0.500	0.319	−145	6.64	90	0.069	64	0.379	−38
		0.600	0.294	−156	5.56	86	0.079	65	0.354	−34
		0.700	0.291	−163	4.82	82	0.089	65	0.343	−34
		0.800	0.293	−169	4.25	78	0.100	65	0.333	−35
		0.900	0.290	−174	3.81	75	0.110	65	0.327	−36
		1.000	0.292	−179	3.46	72	0.121	65	0.321	−37
		1.500	0.307	162	2.40	58	0.174	62	0.304	−45
		2.000	0.330	147	1.87	45	0.225	58	0.296	−56
		2.500	0.359	133	1.57	34	0.275	53	0.285	−68
		3.000	0.387	122	1.36	24	0.324	49	0.280	−80
		4.000	0.461	101	1.10	7	0.424	38	0.275	−112

Table 2. MRF917T1 Common Emitter S–Parameters (continued)

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
6.0	20	0.10	0.391	−85	27.76	125	0.020	66	0.637	−36
		0.20	0.313	−122	16.43	106	0.032	66	0.436	−39
		0.30	0.292	−140	11.44	98	0.043	68	0.365	−38
		0.40	0.284	−152	8.74	91	0.055	70	0.330	−36
		0.50	0.279	−159	7.08	87	0.067	70	0.313	−36
		0.60	0.266	−169	5.92	83	0.078	71	0.295	−32
		0.70	0.267	−174	5.11	80	0.090	70	0.289	−32
		0.80	0.272	−179	4.50	76	0.101	70	0.281	−33
		0.90	0.271	177	4.03	73	0.113	69	0.278	−34
		1.00	0.275	173	3.65	71	0.124	68	0.274	−35
		1.50	0.297	158	2.52	58	0.179	64	0.260	−43
		2.00	0.322	144	1.97	46	0.232	58	0.251	−55
		2.50	0.353	131	1.64	35	0.283	53	0.239	−68
		3.00	0.380	120	1.43	25	0.332	48	0.233	−81
		4.00	0.452	100	1.16	8	0.430	37	0.225	−113
	40	0.10	0.319	−114	27.96	116	0.017	67	0.532	−34
		0.20	0.295	−145	15.39	101	0.029	71	0.391	−31
		0.30	0.292	−157	10.51	93	0.040	73	0.353	−29
		0.40	0.295	−165	7.98	88	0.052	74	0.335	−28
		0.50	0.295	−170	6.45	85	0.064	74	0.327	−29
		0.60	0.290	−179	5.39	81	0.076	74	0.316	−26
		0.70	0.294	178	4.65	78	0.087	73	0.313	−27
		0.80	0.300	174	4.10	75	0.099	72	0.306	−29
		0.90	0.301	171	3.67	72	0.110	71	0.305	−30
		1.00	0.306	168	3.33	69	0.121	70	0.301	−32
		1.50	0.333	154	2.31	57	0.176	65	0.286	−42
		2.00	0.359	141	1.81	45	0.229	60	0.276	−54
		2.50	0.389	127	1.52	34	0.281	55	0.262	−68
		3.00	0.415	117	1.32	25	0.332	50	0.254	−81
		4.00	0.478	97	1.08	8	0.434	38	0.241	−113

Table 2. MRF917T1 Common Emitter S–Parameters (continued)

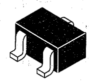
The RF Small Signal Line
NPN Silicon Low Voltage, Low Current, Low Noise, High-Frequency Transistors

MRF927T1
MRF927T3

I_C = 10 mA
LOW NOISE
HIGH FREQUENCY
TRANSISTOR

Designed for use in low voltage, low current applications at frequencies to 2.0 GHz. Specifically aimed at portable communication devices such as pagers and hand–held phones.

- High Gain (G_{Umax} 15 dB Typ @ 1.0 GHz) @ 1.0 mA
- Small, Surface–Mount Package (SC–70)
- High Current Gain–Bandwidth Product at Low Current, Low Voltage (f_τ = 8.0 GHz Typ @ 3.0 V, 5.0 mA)
- Available in Tape and Reel by Adding T1 or T3 Suffix to Part Number.
  T1 Suffix = 3,000 Units per 8 mm, 7 inch Reel.
  T3 Suffix = 10,000 Units per 8 mm, 7 inch Reel.



CASE 419–02, STYLE 3
(SC–70/SOT–323)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	10	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Emitter–Base Voltage	V_{EBO}	2.5	Vdc
Collector Current — Continuous	I_C	10	mAdc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	100 1.0	mW mW/°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C
Operating Temperature Range	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1000	°C/W

DEVICE MARKING

MRF927T1 = F

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 0.1 mA, I_B = 0 mA)	$V_{(BR)CEO}$	10	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	20	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)	$V_{(BR)EBO}$	1.5	—	—	Vdc
Emitter Cutoff Current (V_{EB} = 1.0 Vdc, I_C = 0)	I_{EBO}	—	—	0.1	μA
ON CHARACTERISTICS					
DC Current Gain (V_{CE} = 1.0 Vdc, I_C = 0.5 mA)	h_{FE}	50	—	200	—
DYNAMIC CHARACTERISTICS					
Collector–Base Capacitance (V_{CB} = 1.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	0.33	—	pF
Current–Gain Bandwidth Product (V_{CE} = 3.0 Vdc, I_E = 5.0 mA, f = 1.0 GHz)	f_τ	—	8.0	—	GHz
PERFORMANCE CHARACTERISTICS					
Noise Figure — Minimum (V_{CE} = 1.0 Vdc, I_C = 1.0 mA, f = 1000 MHz) Figure 3	NF_{min}	—	1.7	—	dB
Associated Gain at Minimum Noise Figure (V_{CE} = 1.0 Vdc, I_C = 1.0 mA, f = 1000 MHz) Figure 3	G_{NF}	—	9.8	—	dB
Maximum Unilateral Gain (V_{CE} = 1.0 Vdc, I_C = 1.0 mA, f = 1000 MHz)	G_{Umax}	—	15	—	dB
Insertion Gain (V_{CE} = 1.0 Vdc, I_C = 1.0 mA, f = 1000 MHz)	$\|S_{21}\|^2$	—	8.0	—	dB
Noise Resistance (V_{CE} = 1.0 Vdc, I_C = 1.0 mA, f = 1000 MHz)	R_N	—	62	—	Ohms

TYPICAL CHARACTERISTICS

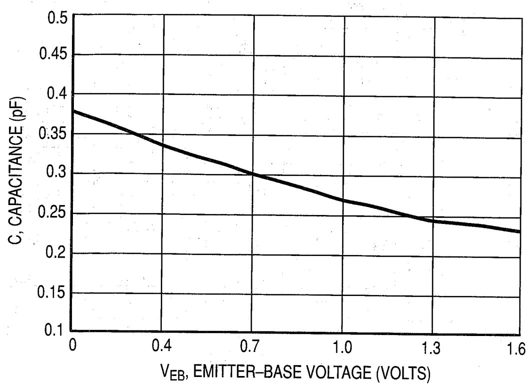


Figure 1. C_{ib} Input Capacitance versus Voltage

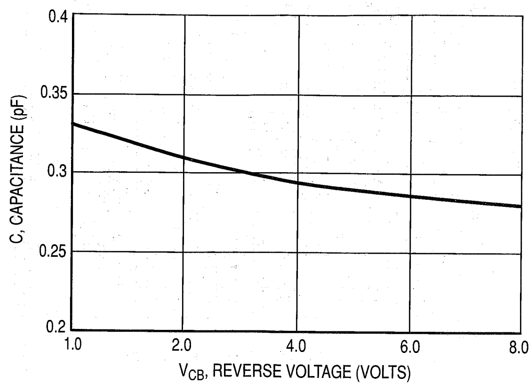
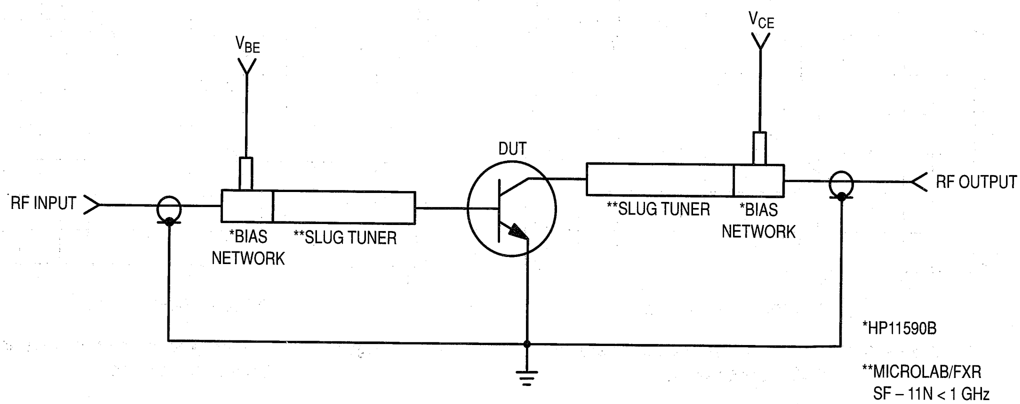


Figure 2. C_{cb}, Collector–Base Capacitance versus Voltage



*HP11590B

**MICROLAB/FXR
SF – 11N < 1 GHz
SF – 31IN ≥ 1 GHz

Figure 3. Functional Circuit Schematic

TYPICAL CHARACTERISTICS

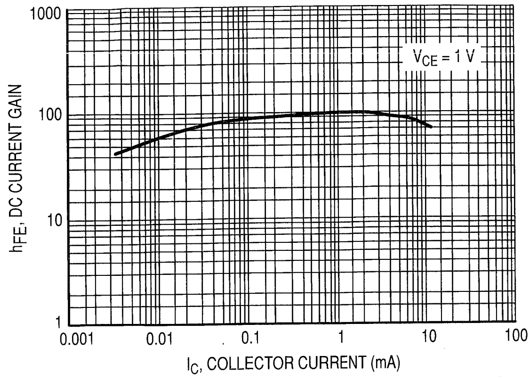


Figure 4. DC Current Gain versus Collector Current

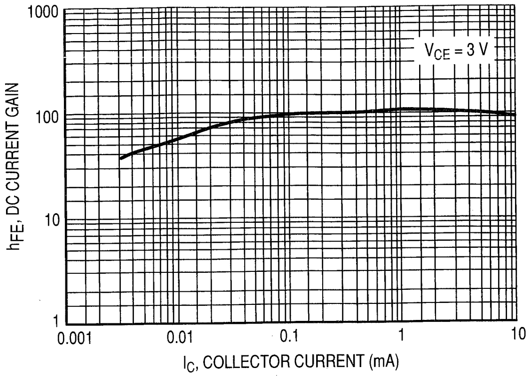


Figure 5. DC Current Gain versus Collector Current

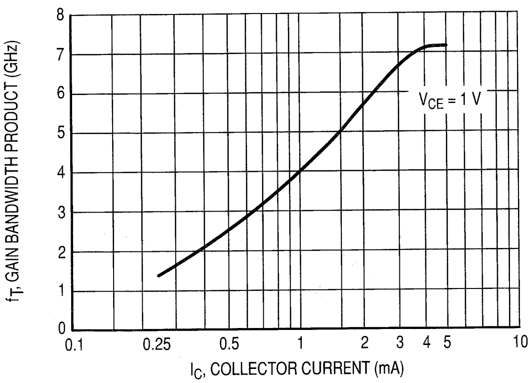


Figure 6. Gain Bandwidth Product versus Collector Current

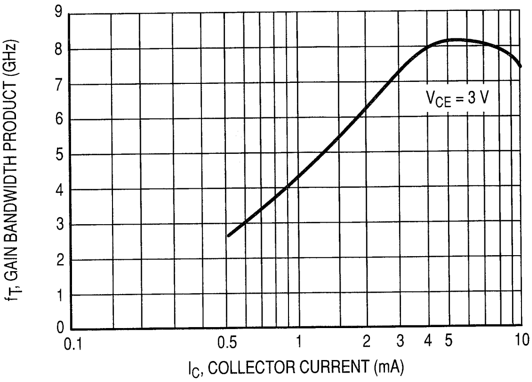


Figure 7. Gain Bandwidth Product versus Collector Current

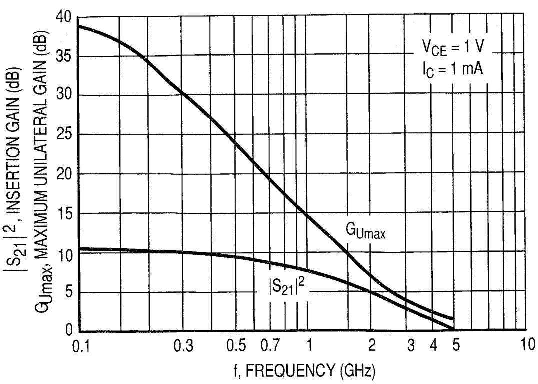


Figure 8. Forward Insertion Gain and Maximum Unilateral Gain versus Frequency

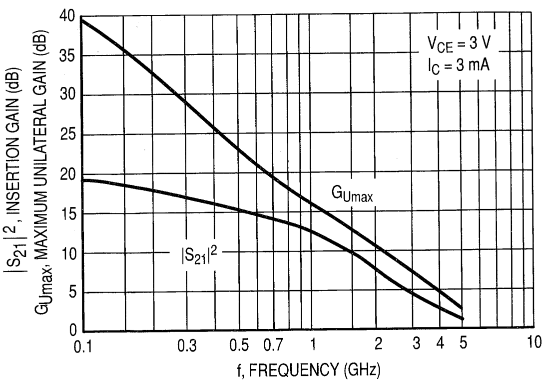


Figure 9. Forward Insertion Gain and Maximum Unilateral Gain versus Frequency

TYPICAL CHARACTERISTICS

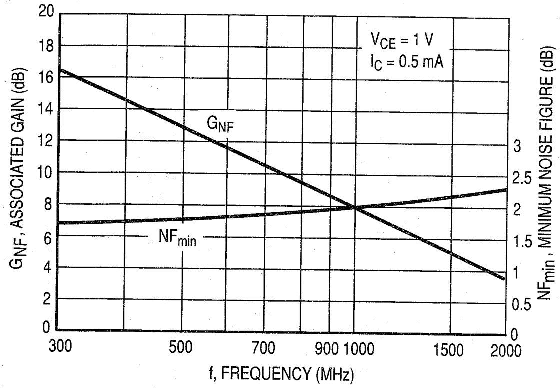


Figure 10. Minimum Noise Figure and Associated Gain versus Frequency

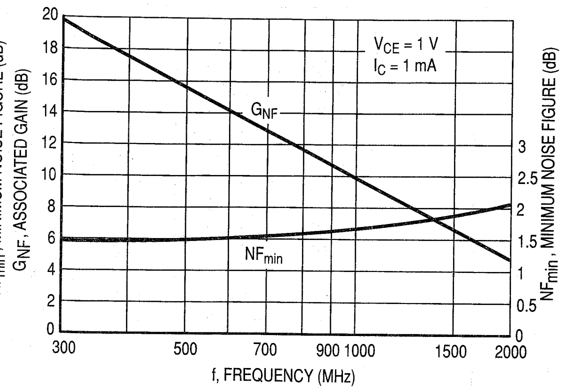


Figure 11. Minimum Noise Figure and Associated Gain versus Frequency

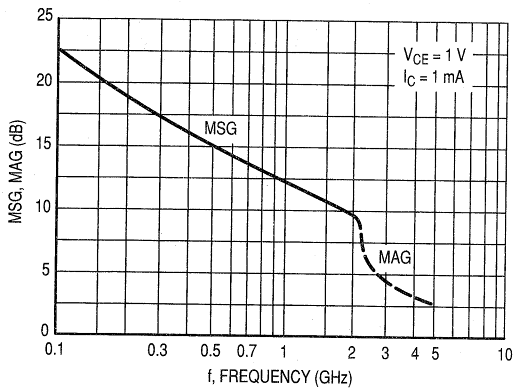


Figure 12. MSG, Maximum Stable Gain; MAG, Maximum Available Gain versus Frequency

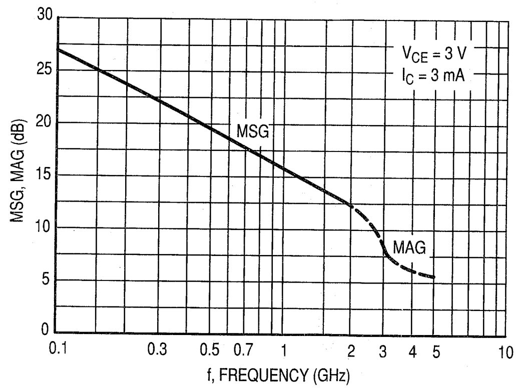


Figure 13. MSG, Maximum Stable Gain; MAG, Maximum Available Gain versus Frequency

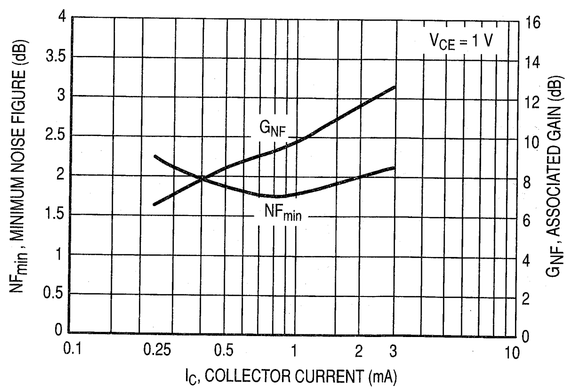


Figure 14. Noise Figure and Gain @ Minimum Noise Figure versus Collector Current

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1.0	0.25	0.10	0.992	–4	0.911	174	0.020	86	0.997	–3
		0.20	0.990	–9	0.903	169	0.039	83	0.993	–6
		0.30	0.983	–13	0.909	163	0.059	80	0.992	–8
		0.40	0.978	–17	0.904	157	0.077	77	0.988	–11
		0.50	0.973	–21	0.834	149	0.095	72	0.975	–13
		0.60	0.943	–25	0.892	144	0.111	69	0.966	–16
		0.70	0.929	–29	0.873	139	0.127	66	0.958	–19
		0.80	0.889	–33	0.901	135	0.142	63	0.949	–22
		0.90	0.895	–37	0.888	129	0.158	60	0.939	–24
		1.00	0.876	–41	0.890	124	0.171	57	0.929	–26
		1.50	0.772	–60	0.871	100	0.227	44	0.873	–38
		2.00	0.670	–78	0.835	80	0.261	34	0.823	–48
		2.50	0.564	–96	0.812	62	0.276	25	0.776	–58
		3.00	0.477	–114	0.785	48	0.276	18	0.741	–68
		3.50	0.412	–132	0.741	36	0.270	15	0.722	–77
		4.00	0.364	–151	0.701	25	0.261	14	0.711	–87
		4.50	0.308	–172	0.702	17	0.261	18	0.682	–97
		5.00	0.297	166	0.639	11	0.270	22	0.686	–107
	0.5	0.10	0.983	–5	1.788	174	0.020	86	0.994	–3
		0.20	0.977	–10	1.763	168	0.040	82	0.992	–7
		0.30	0.965	–16	1.764	162	0.059	79	0.984	–10
		0.40	0.953	–21	1.735	156	0.077	76	0.976	–13
		0.50	0.947	–26	1.637	147	0.094	70	0.954	–16
		0.60	0.901	–30	1.673	142	0.109	67	0.941	–19
		0.70	0.878	–34	1.619	137	0.124	64	0.927	–21
		0.80	0.827	–38	1.601	132	0.136	62	0.912	–24
		0.90	0.825	–43	1.594	127	0.151	58	0.893	–27
		1.00	0.796	–48	1.571	122	0.162	56	0.877	–29
		1.50	0.659	–67	1.420	99	0.207	45	0.797	–40
		2.00	0.535	–85	1.275	80	0.232	37	0.733	–49
		2.50	0.417	–102	1.177	63	0.247	32	0.678	–58
		3.00	0.332	–122	1.097	50	0.256	29	0.639	–67
		3.50	0.271	–143	1.014	38	0.265	28	0.617	–75
		4.00	0.238	–164	0.949	28	0.279	29	0.604	–84
		4.50	0.212	170	0.928	19	0.305	31	0.573	–94
		5.00	0.218	147	0.856	12	0.333	31	0.574	–105
	1.0	0.10	0.965	–7	3.383	172	0.020	85	0.990	–4
		0.20	0.952	–14	3.315	165	0.040	81	0.982	–9
		0.30	0.928	–20	3.277	157	0.057	77	0.965	–13
		0.40	0.905	–26	3.172	151	0.074	73	0.947	–16
		0.50	0.88	–33	3.027	141	0.090	67	0.910	–19
		0.60	0.819	–37	2.936	136	0.102	64	0.887	–23
		0.70	0.783	–42	2.804	130	0.115	61	0.861	–26
		0.80	0.725	–47	2.666	125	0.125	59	0.839	–28
		0.90	0.702	–52	2.623	119	0.136	56	0.810	–31
		1.00	0.664	–57	2.525	114	0.145	54	0.787	–33
		1.50	0.504	–75	2.085	93	0.181	47	0.690	–42
		2.00	0.382	–92	1.759	75	0.207	42	0.626	–50
		2.50	0.278	–108	1.548	61	0.229	40	0.577	–58
		3.00	0.21	–129	1.397	48	0.252	38	0.543	–66
		3.50	0.168	–154	1.271	38	0.276	36	0.523	–73
		4.00	0.15	–177	1.177	28	0.303	35	0.513	–82
		4.50	0.148	155	1.123	19	0.336	34	0.490	–91
		5.00	0.165	132	1.049	12	0.369	32	0.487	–101

Table 1. Common Emitter S–Parameters

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\lvert S_{11}\rvert$	∠ φ	$\lvert S_{21}\rvert$	∠ φ	$\lvert S_{12}\rvert$	∠ φ	$\lvert S_{22}\rvert$	∠ φ
1.0	2.0	0.10	0.928	–10	6.181	169	0.020	83	0.980	–6
		0.20	0.901	–19	5.967	160	0.037	78	0.959	–12
		0.30	0.856	–28	5.744	150	0.054	73	0.923	–17
		0.40	0.811	–36	5.410	142	0.068	69	0.886	–22
		0.50	0.753	–43	5.051	132	0.080	63	0.828	–25
		0.60	0.681	–48	4.679	126	0.091	61	0.790	–28
		0.70	0.632	–54	4.367	119	0.100	59	0.753	–31
		0.80	0.574	–59	4.021	114	0.108	57	0.726	–33
		0.90	0.538	–64	3.831	109	0.116	55	0.692	–35
		1.00	0.497	–68	3.595	104	0.123	54	0.667	–37
		1.50	0.349	–86	2.732	85	0.156	50	0.576	–44
		2.00	0.255	–102	2.200	70	0.186	47	0.527	–50
		2.50	0.182	–120	1.871	57	0.216	45	0.491	–58
		3.00	0.137	–143	1.647	46	0.246	42	0.469	–66
		3.50	0.115	–167	1.478	36	0.276	39	0.460	–73
		4.00	0.109	167	1.356	27	0.306	36	0.453	–81
		4.50	0.115	138	1.268	19	0.337	33	0.443	–89
		5.00	0.136	119	1.190	11	0.368	30	0.441	–98

Table 1. Common Emitter S–Parameters (continued)

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\lvert S_{11}\rvert$	∠ φ	$\lvert S_{21}\rvert$	∠ φ	$\lvert S_{12}\rvert$	∠ φ	$\lvert S_{22}\rvert$	∠ φ
3.0	0.5	0.10	0.985	–5	1.796	174	0.018	86	0.995	–3
		0.20	0.980	–10	1.776	169	0.034	83	0.993	–6
		0.30	0.969	–15	1.778	163	0.051	79	0.986	–9
		0.40	0.959	–19	1.753	157	0.066	76	0.980	–12
		0.50	0.952	–24	1.651	149	0.081	71	0.961	–14
		0.60	0.910	–28	1.693	144	0.095	68	0.949	–17
		0.70	0.888	–32	1.639	139	0.108	65	0.937	–20
		0.80	0.841	–36	1.628	134	0.119	63	0.924	–23
		0.90	0.839	–41	1.618	129	0.131	60	0.908	–25
		1.00	0.812	–45	1.596	124	0.142	57	0.894	–27
		1.50	0.681	–64	1.445	102	0.184	47	0.824	–38
		2.00	0.565	–80	1.294	83	0.210	39	0.768	–47
		2.50	0.455	–96	1.190	66	0.226	33	0.720	–56
		3.00	0.369	–112	1.106	53	0.237	30	0.687	–64
		3.50	0.308	–128	1.019	41	0.246	28	0.670	–72
		4.00	0.264	–146	0.950	30	0.256	28	0.661	–81
		4.50	0.212	–166	0.933	21	0.274	29	0.638	–89
		5.00	0.201	171	0.858	13	0.294	30	0.642	–99
	1.0	0.10	0.969	–6	3.341	173	0.017	85	0.992	–4
		0.20	0.958	–13	3.284	166	0.034	81	0.985	–8
		0.30	0.938	–19	3.255	159	0.050	78	0.972	–11
		0.40	0.917	–24	3.163	152	0.064	74	0.957	–15
		0.50	0.896	–30	3.019	143	0.078	68	0.925	–18
		0.60	0.838	–35	2.951	138	0.089	66	0.905	–21
		0.70	0.805	–40	2.823	132	0.101	63	0.883	–23
		0.80	0.750	–44	2.700	127	0.110	61	0.864	–26
		0.90	0.732	–49	2.661	122	0.121	58	0.838	–28
		1.00	0.696	–53	2.570	117	0.129	56	0.818	–31
		1.50	0.541	–71	2.139	95	0.163	48	0.731	–40
		2.00	0.424	–86	1.807	78	0.188	43	0.674	–47
		2.50	0.325	–100	1.588	63	0.210	40	0.629	–55
		3.00	0.252	–116	1.430	51	0.230	37	0.600	–63
		3.50	0.204	–132	1.294	40	0.250	36	0.589	–70
		4.00	0.170	–150	1.195	30	0.272	34	0.581	–78
		4.50	0.136	–173	1.141	21	0.297	33	0.565	–86
		5.00	0.134	162	1.063	13	0.323	32	0.566	–95

Table 2. Common Emitter S–Parameters

V_{CE} (Vdc)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
3.0	3.0	0.10	0.902	–11	8.541	168	0.017	83	0.976	–7
		0.20	0.863	–21	8.133	156	0.031	77	0.946	–13
		0.30	0.805	–31	7.647	146	0.045	73	0.901	–18
		0.40	0.746	–39	7.050	137	0.056	69	0.856	–22
		0.50	0.673	–45	6.436	127	0.066	65	0.794	–24
		0.60	0.604	–50	5.853	121	0.074	63	0.757	–27
		0.70	0.552	–55	5.378	115	0.082	61	0.721	–29
		0.80	0.499	–59	4.897	110	0.089	60	0.697	–30
		0.90	0.461	–63	4.586	105	0.096	59	0.667	–32
		1.00	0.424	–66	4.260	100	0.103	59	0.647	–33
		1.50	0.295	–80	3.141	83	0.136	56	0.578	–38
		2.00	0.215	–91	2.494	70	0.169	54	0.542	–44
		2.50	0.152	–105	2.101	58	0.201	51	0.514	–51
		3.00	0.108	–124	1.837	47	0.232	47	0.497	–59
		3.50	0.083	–146	1.641	38	0.263	44	0.490	–66
		4.00	0.071	–173	1.501	30	0.294	41	0.485	–73
		4.50	0.069	148	1.395	21	0.325	38	0.480	–81
		5.00	0.090	121	1.310	14	0.357	35	0.478	–90
	5.0	0.10	0.839	–15	12.345	164	0.016	81	0.961	–9
		0.20	0.774	–28	11.339	149	0.030	75	0.906	–16
		0.30	0.690	–38	10.154	137	0.041	71	0.840	–21
		0.40	0.614	–47	8.971	127	0.050	68	0.780	–24
		0.50	0.528	–52	7.877	119	0.058	65	0.715	–26
		0.60	0.464	–57	6.974	112	0.066	64	0.677	–27
		0.70	0.414	–61	6.267	107	0.073	63	0.646	–28
		0.80	0.370	–65	5.628	102	0.080	63	0.625	–29
		0.90	0.338	–68	5.165	98	0.087	63	0.602	–30
		1.00	0.307	–71	4.742	94	0.094	62	0.587	–31
		1.50	0.207	–83	3.389	79	0.130	61	0.536	–36
		2.00	0.148	–96	2.658	66	0.165	58	0.512	–41
		2.50	0.100	–113	2.221	56	0.200	54	0.490	–49
		3.00	0.072	–138	1.930	46	0.233	51	0.475	–56
		3.50	0.059	–168	1.720	37	0.266	47	0.470	–64
		4.00	0.062	152	1.569	29	0.299	43	0.466	–72
		4.50	0.080	118	1.451	21	0.331	40	0.462	–80
		5.00	0.107	103	1.362	14	0.365	36	0.460	–88

Table 2. Common Emitter S–Parameters (continued)

V_{CE} (Vdc)	I_C (mA)	f (MHz)	NF_{min} (dB)	Γ_o (MAG, ANG)	R_N (ohms)
1.0	0.5	300	1.65	0.81 ∠8	89
		500	1.70	0.80 ∠13	86
		900	1.85	0.77 ∠23	78
		1000	1.90	0.77 ∠25	76
		1500	2.05	0.74 ∠40	64
		2000	2.20	0.70 ∠56	50
	1.0	300	1.45	0.76 ∠7	71
		500	1.47	0.76 ∠12	69
		900	1.65	0.75 ∠21	63
		1000	1.70	0.74 ∠24	62
		1500	1.90	0.71 ∠38	53
		2000	2.05	0.67 ∠55	44

Table 3. Common–Emitter Noise Parameters

V_{CE} (Vdc)	I_C (mA)	f (MHz)	NF_{min} (dB)	Γ_o (MAG, ANG)	R_N (ohms)
3.0	1.0	300	1.60	0.72 ∠7	61
		500	1.62	0.72 ∠12	60
		900	1.64	0.70 ∠21	57
		1000	1.64	0.70 ∠24	56
		1500	1.70	0.67 ∠39	49
		2000	1.80	0.63 ∠55	41
	3.0	300	1.80	0.63 ∠7	48
		500	1.82	0.62 ∠11	47
		900	1.84	0.60 ∠19	45
		1000	1.85	0.59 ∠22	44
		1500	1.94	0.56 ∠37	40
		2000	2.12	0.51 ∠56	34

Table 3. Common–Emitter Noise Parameters (continued)

Name	Value	Name	Value	Name	Value
IS	187.1E–18	IRB	80.0E–6	TF	13.0E–12
BF	133	RBM	31	XTF	500
NF	0.9958	RE	3.3	VTF	1.1
VAF	40	RC	6	ITF	0.35
IKF	0.07	XTB	0(1)	PTF	50
ISE	5.393E–12	EG	1.11(1)	TR	2.38E–9
NE	4.933	XTI	3(1)	FC	0.9
BR	17	CJE	280.0E–15	CJS	0(1)
NR	0.9929	VJE	0.884	VJS	1(1)
VAR	2.6	MJE	0.318	MJS	0(1)
IKR	0.018	CJC	290.0E–15	AF	1(1)
ISC	28.92E–18	VJC	0.424	KF	0(1)
NC	1.049	MJC	0.108		
RB	31	XCJC	0.2		

Note
1. These parameters have not been extracted. Default values are shown.

Table 4. Spice Parameters (MRF927 Die Gummel–Poon Parameters)

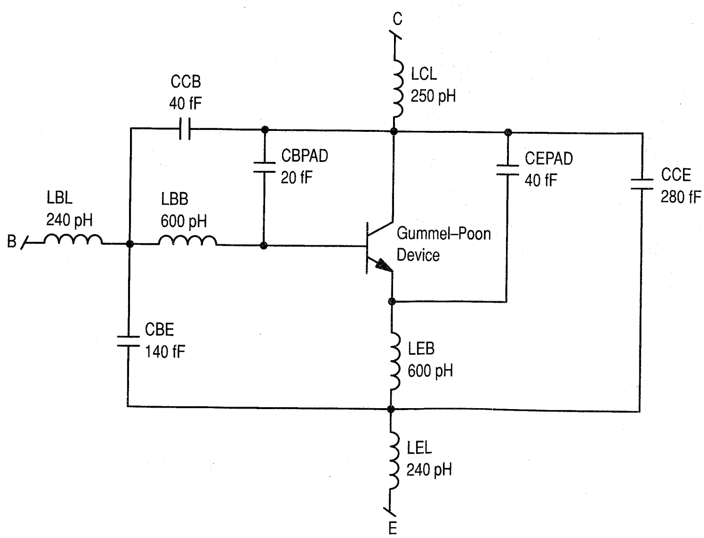
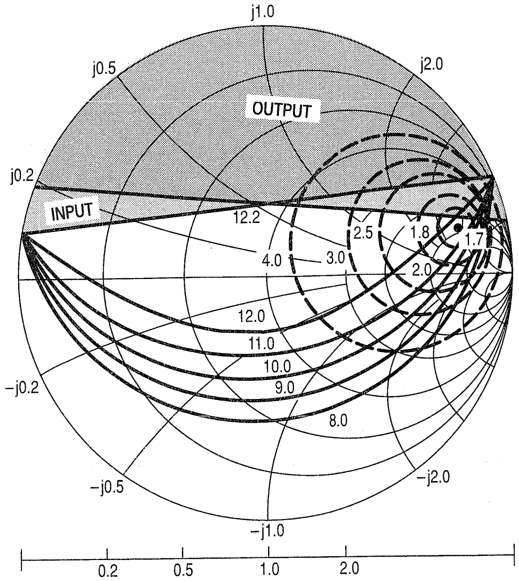


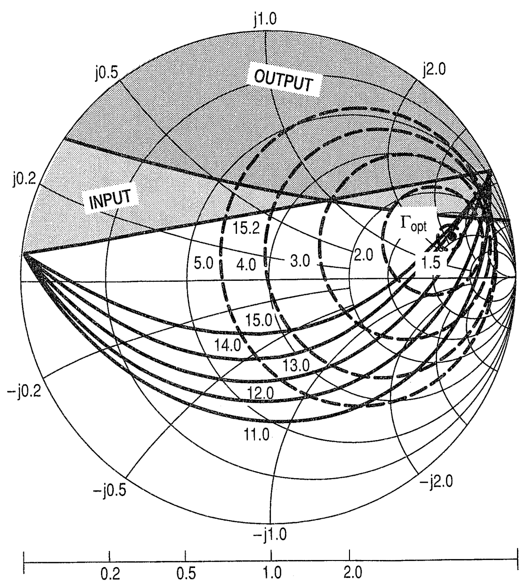
Figure 15. MRF927 SC–70 Package Equivalent Circuit



V_{CE} = 1.0 V
I_C = 0.5 mA
▨ — Potentially Unstable

f (MHz)	NF OPT (dB)	ΓMS NF OPT	Rn	K
500	1.7	0.80 ∠ 13°	86	0.25

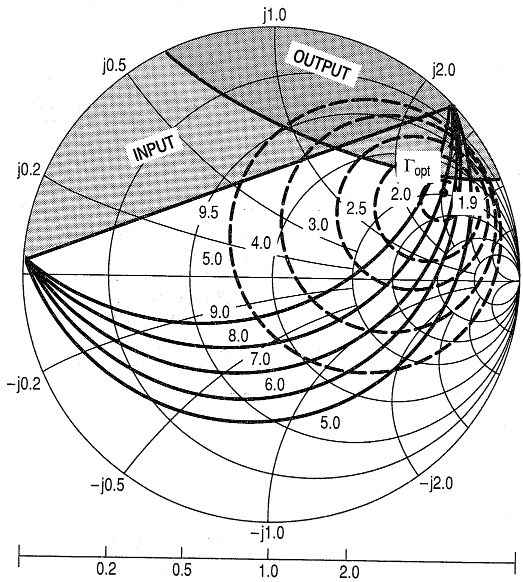
Figure 16. Constant Gain and Noise Figure Contours



V_{CE} = 1.0 V
I_C = 1.0 mA
▨ — Potentially Unstable

f (MHz)	NF OPT (dB)	ΓMS NF OPT	Rn	K
500	1.47	0.76 ∠ 12°	69	0.29

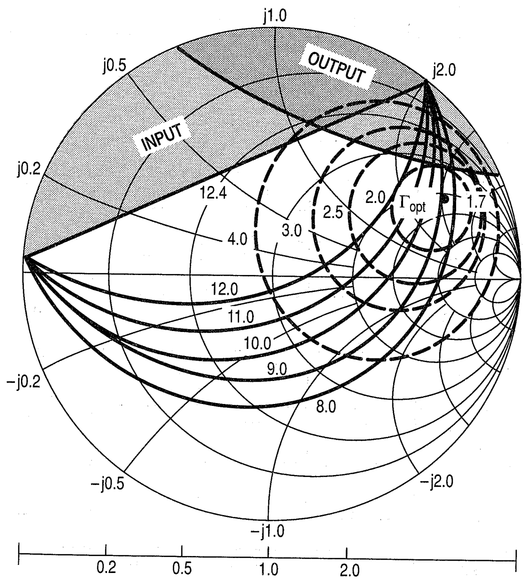
Figure 17. Constant Gain and Noise Figure Contours



V_{CE} = 1.0 V
I_C = 0.5 mA
▨ — Potentially Unstable

f (MHz)	NF OPT (dB)	ΓMS NF OPT	Rn	K
1000	1.9	0.77 ∠ 25°	76	0.43

Figure 18. Constant Gain and Noise Figure Contours



V_{CE} = 1.0 V
I_C = 1.0 mA
▨ — Potentially Unstable

f (MHz)	NF OPT (dB)	ΓMS NF OPT	Rn	K
1000	1.7	0.74 ∠ 24°	62	0.51

Figure 19. Constant Gain and Noise Figure Contours

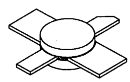
MRF1000MB

The RF Line
Microwave Pulse Power Transistors

Designed for Class A and AB common emitter amplifier applications in the low–power stages of IFF, DME, TACAN, radar transmitters, and CW systems.

- Guaranteed Performance @ 1090 MHz, 18 Vdc — Class A
  Output Power = 0.2 Watt
  Minimum Gain = 10 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input Matching for Broadband Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

0.7 W, 960–1215 MHz
CLASS A/AB
MICROWAVE POWER
TRANSISTORS
NPN SILICON



CASE 332A–03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	20	Vdc
Collector–Base Voltage	V_{CBO}	50	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	7.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	50	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	—	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—

1. These devices are designed for RF operation. The total device dissipation rating applies only when the device is operated as RF amplifiers.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

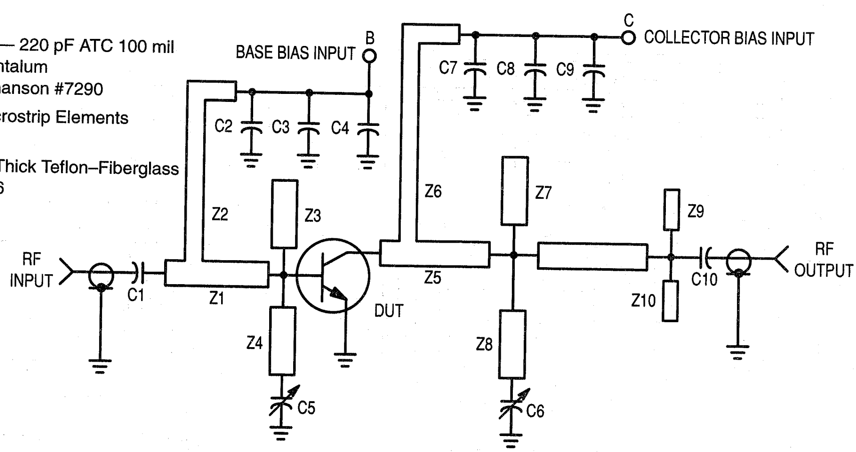
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	2.0	5.0	pF
FUNCTIONAL TESTS					
Common–Emitter Power Gain — Class A (V_{CE} = 18 Vdc, I_C = 100 mAdc, f = 1090 MHz, P_{out} = 200 mW)	G_{PE}	10	12	—	dB
Common–Emitter Power Gain — Class AB (V_{CE} = 18 Vdc, I_{CQ} = 10 mAdc, f = 1090 MHz, P_{out} = 0.7 W)	G_{PE}	—	10.7	—	dB
Load Mismatch — Class A (V_{CE} = 18 Vdc, I_C = 100 mAdc, f = 1090 MHz, P_{out} = 200 mW, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

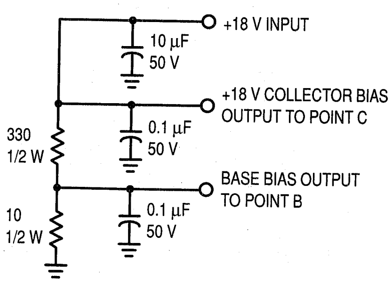
C1, C2, C3, C7, C8, C10 — 220 pF ATC 100 mil
C4, C9 — 4.7 µF 50 V Tantalum
C5, C6 — 0.8–8.0 pF Johanson #7290

Z1–Z10 — Distributed Microstrip Elements
— See Figure 8

Board Material — 0.031″ Thick Teflon–Fiberglass
ε_r = 2.56



Class AB Bias Control Circuit
18 V Output I_{CQ} 10 mA Nominal



Class A Constant Current Bias Control Circuit
I_C = 100 mA, V_{CE} = 18 V

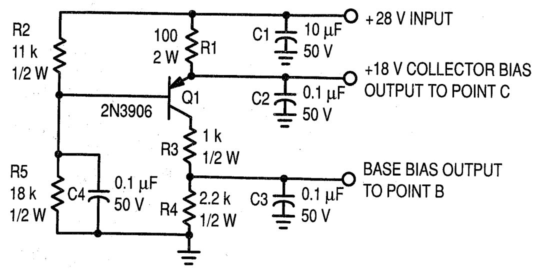


Figure 1. 1090 MHz Test Circuit

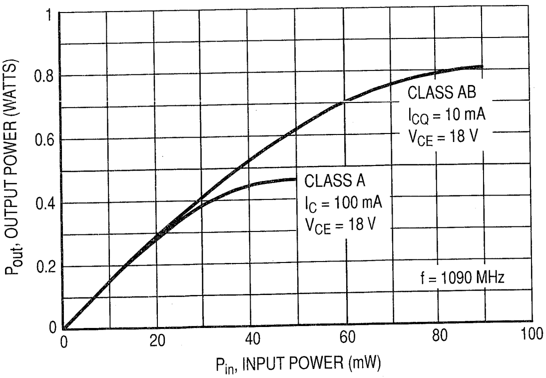


Figure 2. Output Power versus Input Power

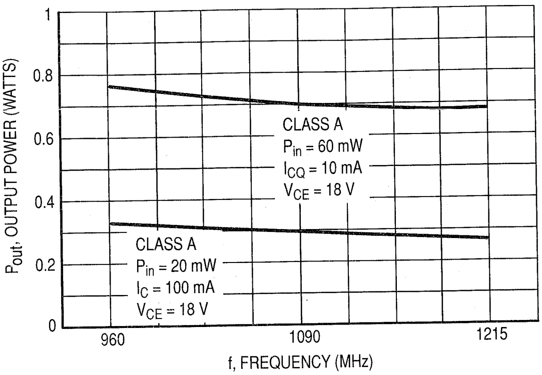


Figure 3. Output Power versus Frequency

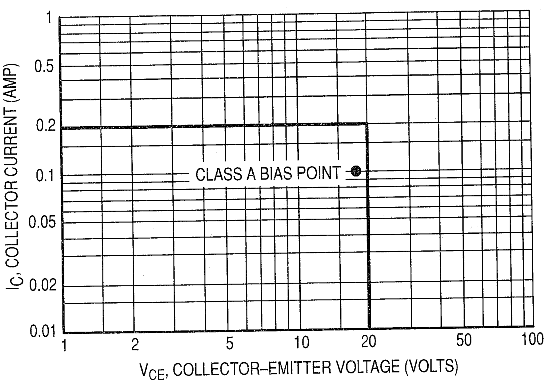


Figure 4. DC Safe Operating Area

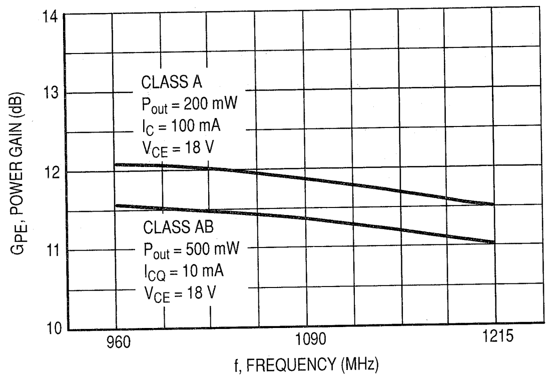
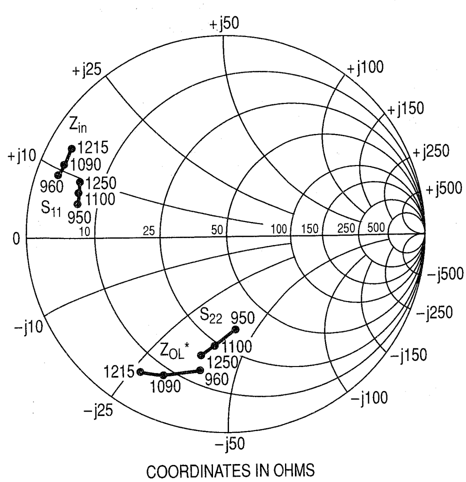


Figure 5. Power Gain versus Frequency



SERIES EQUIVALENT IMPEDANCES
P_{out} = 0.5 W, V_{CE} = 18 Vdc,
I_{CQ} = 10 mAdc, Class AB

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
960	3.0 + j9.0	16 – j40
1090	3.2 + j10	8.5 – j31
1215	2.8 + j12	7.0 – j26

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

S–PARAMETERS — V_{CE} = 18 Vdc, I_C = 100 mAdc, Class A

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
950	0.77	166	2.42	40	0.016	42	0.48	–87
1000	0.78	165	2.36	38	0.016	48	0.50	–90
1050	0.77	163	2.31	33	0.016	46	0.51	–94
1100	0.77	162	2.31	28	0.016	46	0.54	–97
1150	0.78	161	2.20	23	0.015	46	0.57	–100
1200	0.78	159	2.20	19	0.016	47	0.59	–103
1250	0.78	158	2.12	12	0.016	42	0.61	–106

Figure 6. Common–Emitter S–Parameters and Series Equivalent Input/Output Impedances

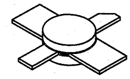
The RF Line
Microwave Pulse Power Transistors

MRF1035MB

Designed for Class B and C common base amplifier applications in short and long pulse TACAN, IFF, DME, and radar transmitters.

- Guaranteed Performance @ 1090 MHz, 50 Vdc
  Output Power = 35 Watts Peak
  Minimum Gain = 10 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input Matching for Broadband Operation

**35 W (PEAK), 960–1215 MHz
MICROWAVE POWER
TRANSISTORS
NPN SILICON**



CASE 332A–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	60	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	35 200	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	5.0	°C/W

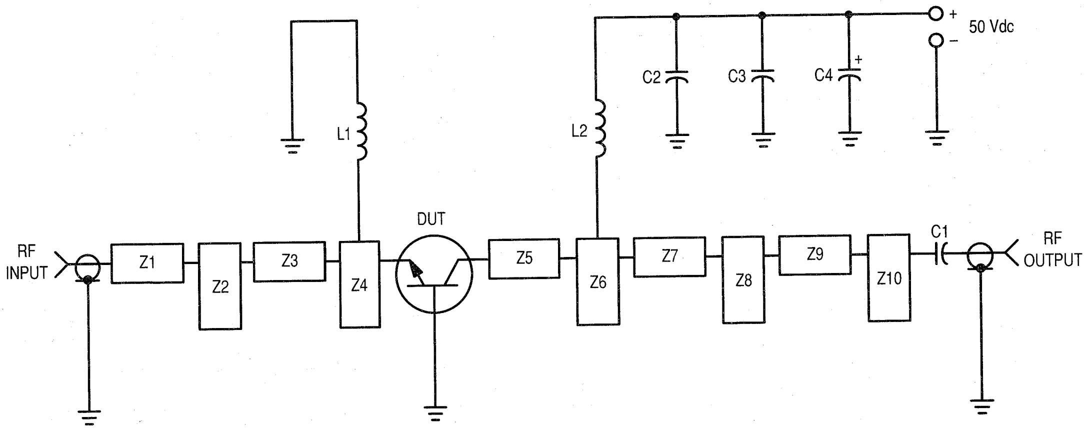
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	—	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	40	100	—

1. These devices are designed for RF operation. The total device dissipation rating applies only when the device is operated as RF amplifiers.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	10	15	pF
FUNCTIONAL TESTS (Pulse Width = 10 µs, Duty Cycle = 1%)					
Common-Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 35 W Peak, f = 1090 MHz)	G_{PB}	10	12.4	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 35 W Peak, f = 1090 MHz)	η	30	34	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 35 W Peak, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			



C1, C2 — 220 pF 100 mil Chip Capacitor
C3 — 0.1 µF
C4 — 10 µF/75 V Electrolytic
L1, L2 — 3 Turns #18 AWG, 1/8″ ID
Z1–Z10 — Microstrip, See Photomaster
Board Material — 0.031″ Glass Teflon
ε_r = 2.5

Figure 1. 1090 MHz Test Circuit

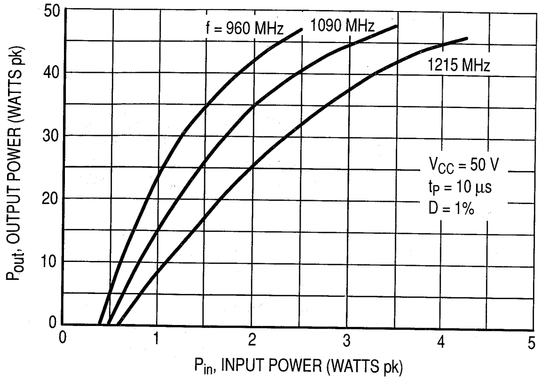


Figure 2. Output Power versus Input Power

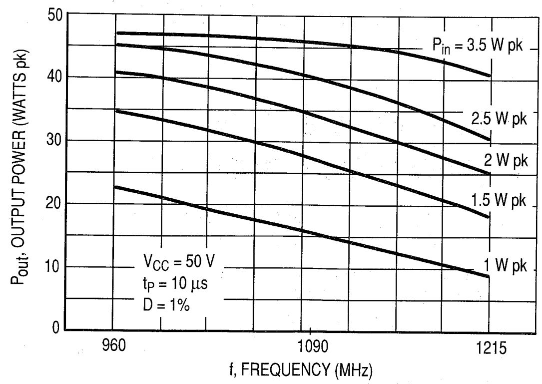


Figure 3. Output Power versus Frequency

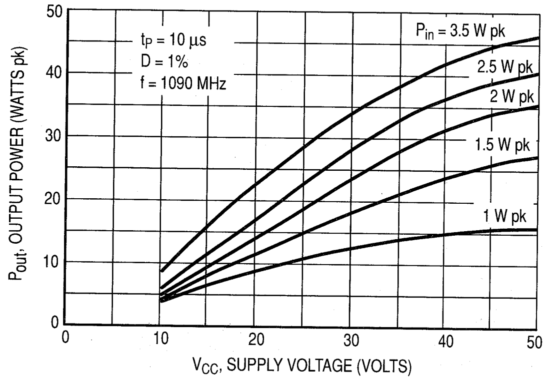


Figure 4. Output Power versus Supply Voltage

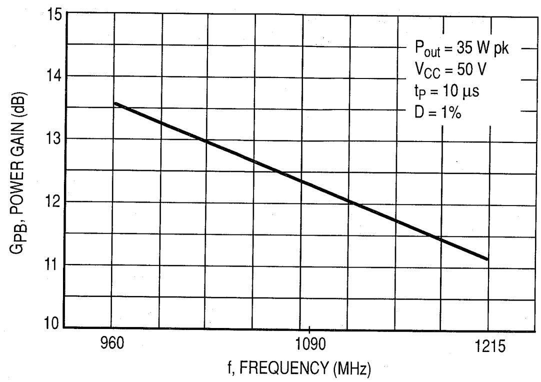
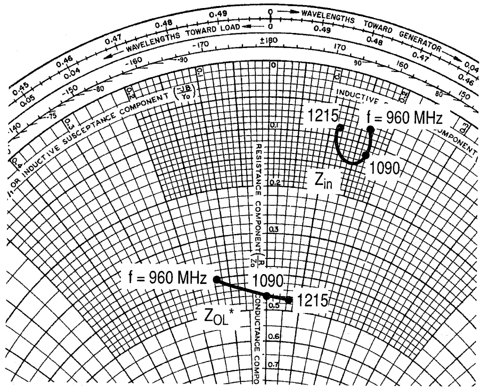


Figure 5. Power Gain versus Frequency



P_{out} = 35 W pk V_{CC} = 50 V
t_p = 10 µs   D = 1%

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
960	3.8 + j8.2	7.5 – j3.3
1090	6.0 + j8.2	9.0 + j0
1215	4.2 + j5.7	9.1 + j1.7

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

Figure 6. Series Equivalent Input/Output Impedances

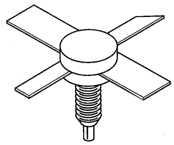
The RF Line
Microwave Pulse Power Transistors

MRF1090MA
MRF1090MB

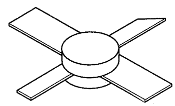
Designed for Class B and C common base amplifier applications in short pulse TACAN, IFF, and DME transmitters.

- Guaranteed Performance @ 1090 MHz, 50 Vdc
  Output Power = 90 Watts Peak
  Minimum Gain = 8.4 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized for Long Life and Resistance to Metal Migration
- Internal Input Matching for Broadband Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

90 W PEAK, 960–1215 MHz
MICROWAVE POWER
TRANSISTORS
NPN SILICON



CASE 332–04, STYLE 1
(MRF1090MA)



CASE 332A–03, STYLE 1
(MRF1090MB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CBO}	70	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current — Peak (1)	I_C	6.0	Adc
Total Device Dissipation @ T_C = 25°C (1) (2) Derate above 25°C	P_D	290 1.66	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.6	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	70	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mAdc, I_E = 0)	$V_{(BR)CBO}$	70	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (4) (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	—	—

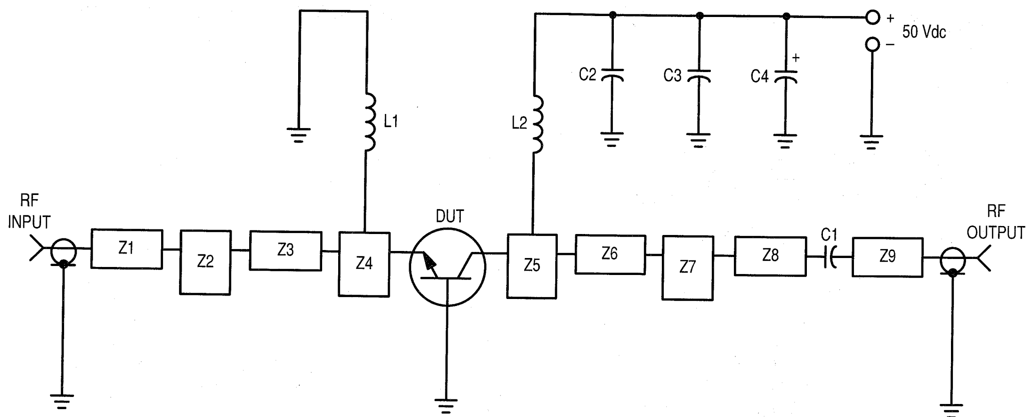
(continued)

NOTES:
1. Pulse Width = 10 μs, Duty Cycle = 1%.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the device is operated as RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.
4. 80 μs Pulse on Tektronix 576 or equivalent.

REV 8

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	12	16	pF
FUNCTIONAL TESTS (Pulse Width = 10 µs, Duty Cycle = 1.0%)					
Common–Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 90 W pk, f = 1090 MHz)	G_{PB}	8.4	10.8	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 90 W pk, f = 1090 MHz)	η	35	40	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 90 W pk, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			



C1, C2 — 220 pF Chip Capacitor, 100–mil ATC
C3 — 0.1 µF
C4 — 47 µF/75 V
L1, L2 — 3 Turns #18 AWG, 1/8″ ID
Z1 – Z9 — Distributed Microstrip Elements, See Photomaster
Board Material — 0.031″ Thick Glass Teflon, ε_r = 2.5

Figure 1. 1090 MHz Test Circuit

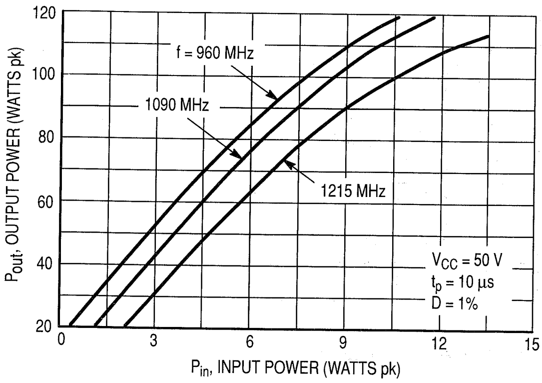


Figure 2. Output Power versus Input Power

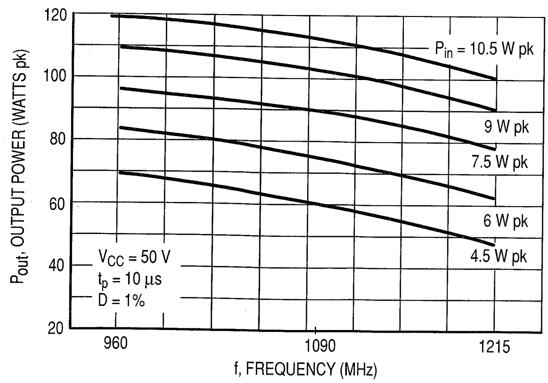


Figure 3. Output Power versus Frequency

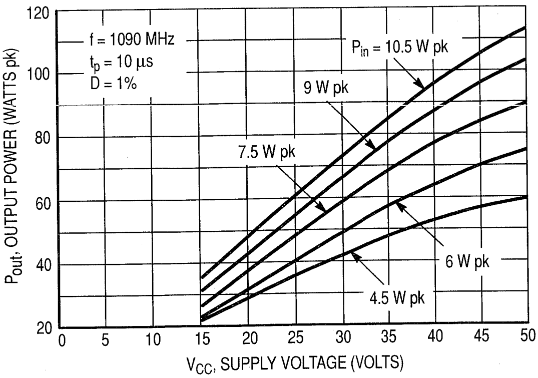


Figure 4. Output Power versus Supply Voltage

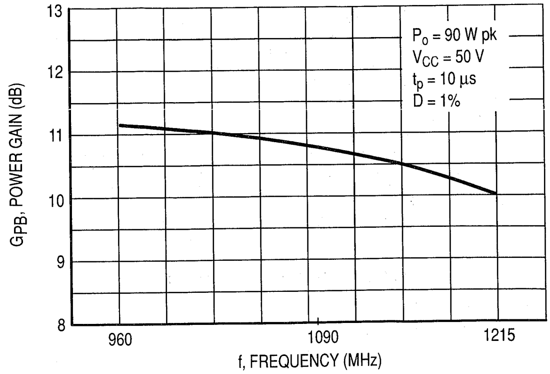
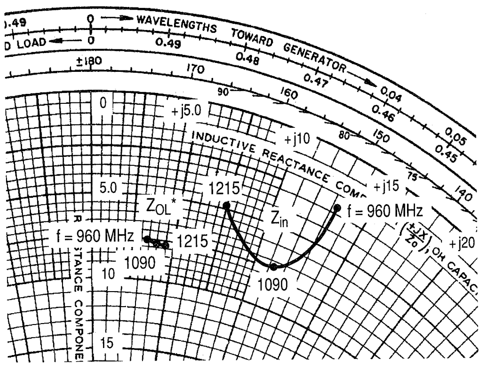


Figure 5. Power Gain versus Frequency



Coordinates in Ohms

P_{out} = 90 W pk V_{CC} = 50 V
t_p = 10 µs D = 1%

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
960	2.8 + j13.2	7.6 + j3.5
1090	7.4 + j11.4	7.6 + j4.0
1215	4.7 + j7.5	7.7 + j4.5

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

Figure 6. Series Equivalent Input/Output Impedance

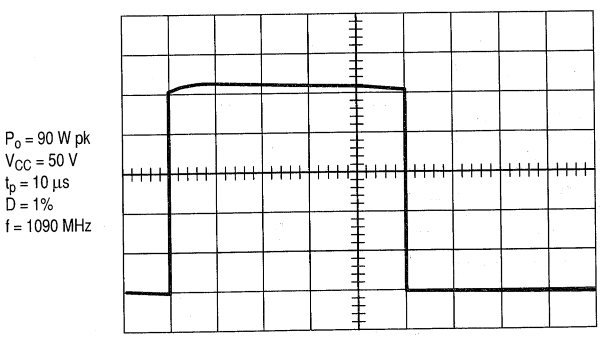


Figure 7. Typical Pulse Performance

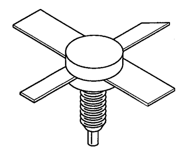
The RF Line
Microwave Pulse Power Transistors

MRF1150MA
MRF1150MB

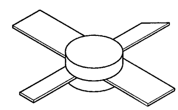
150 W PEAK, 960–1215 MHz
MICROWAVE POWER
TRANSISTORS
NPN SILICON

Designed for Class B and C common base amplifier applications in short pulse TACAN, IFF, and DME transmitters.

- Guaranteed Performance @ 1090 MHz, 50 Vdc
  Output Power = 150 Watts Peak
  Minimum Gain = 7.8 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input Matching for Broadband Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 332–04, STYLE 1
(MRF1150MA)



CASE 332A–03, STYLE 1
(MRF1150MB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CBO}	70	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Peak (1)	I_C	12	Adc
Total Device Dissipation @ T_C = 25°C (1) (2) Derate above 25°C	P_D	583 3.33	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	70	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	70	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (4) (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	—	—

(continued)

NOTES:
1. Pulse Width = 10 μs, Duty Cycle = 1%.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the device is operated as RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.
4. 80 μs Pulse on Tektronix 576 or equivalent.

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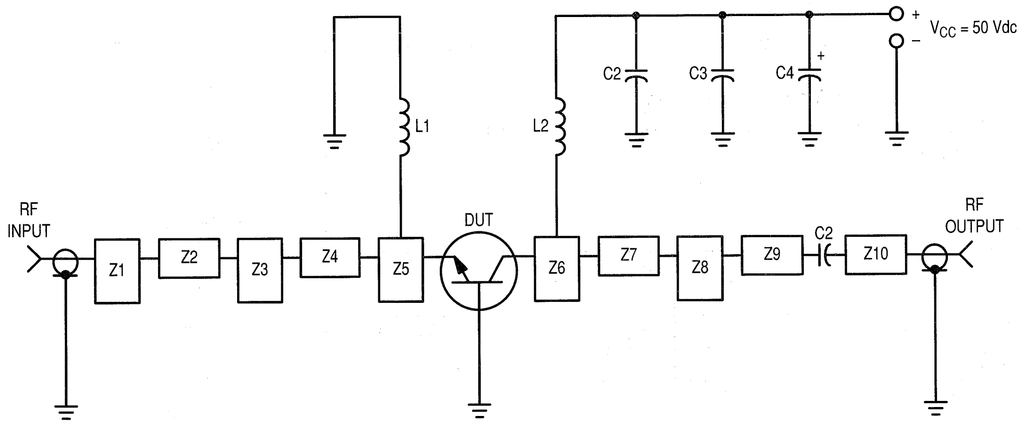
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	25	32	pF
FUNCTIONAL TESTS (Pulse Width = 10 µs, Duty Cycle = 1.0%)					
Common–Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 150 W pk, f = 1090 MHz)	G_{PB}	7.8	9.8	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 150 W pk, f = 1090 MHz)	η	35	40	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 150 W pk, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			



C1, C2 — 220 pF Chip Capacitor, 100–mil ATC
C3 — 0.1 µF/100 V
C4 — 47 µF/75 V Electrolytic
L1, L2 — 3 Turns #18 AWG, 1/8″ ID
Z1 – Z10 — Distributed Microstrip Elements — See Photomaster
Board Material — 0.031″ Thick Teflon–Fiberglass, ε_r = 2.5

Figure 1. 1090 MHz Test Circuit

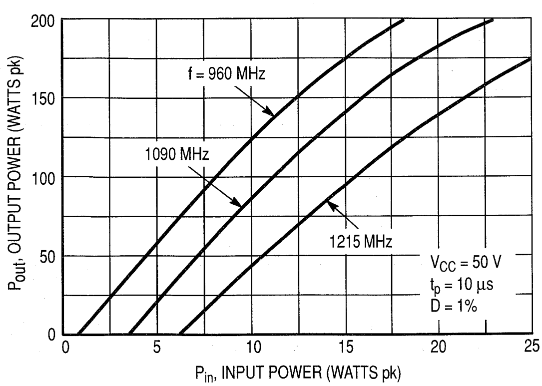


Figure 2. Output Power versus Input Power

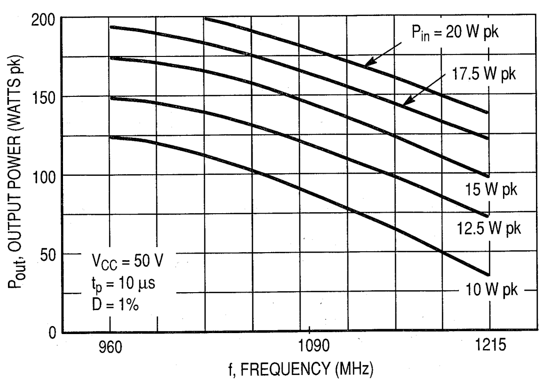


Figure 3. Output Power versus Frequency

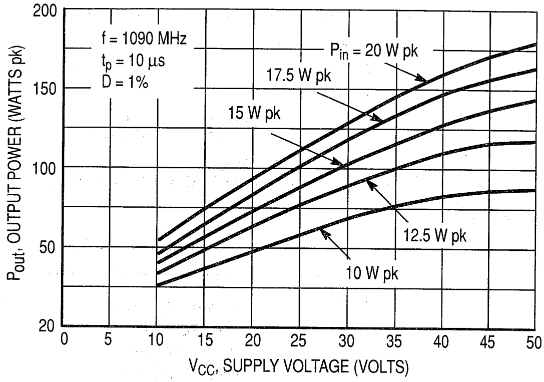


Figure 4. Output Power versus Supply Voltage

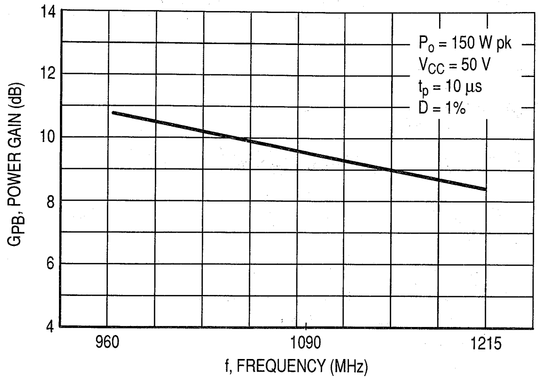
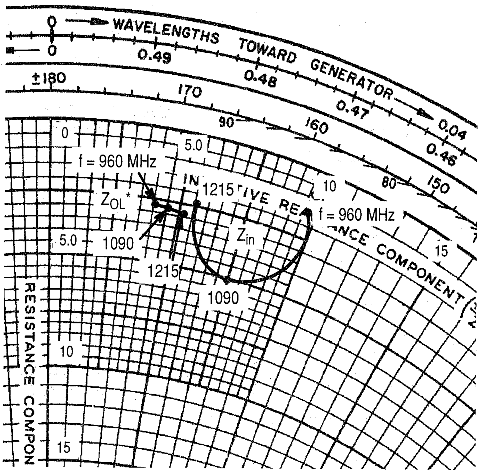


Figure 5. Power Gain versus Frequency



P_{out} = 150 W pk V_{CC} = 50 V
t_p = 10 μs D = 1%

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
960	1.5 + j9.6	2.6 + j4.1
1090	5.0 + j7.5	2.7 + j4.6
1215	2.4 + j5.6	2.8 + j5.3

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

Figure 6. Series Equivalent Input/Output Impedance

P_{out} = 150 W pk
V_{CC} = 50 V
t_p = 10 μs
D = 1%

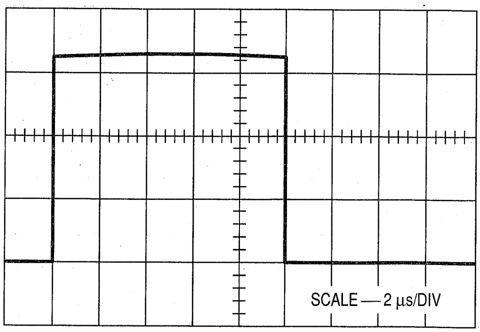


Figure 7. Typical Pulse Performance

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

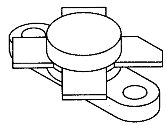
The RF Line
NPN Silicon Power Transistors

MRF1946
MRF1946A

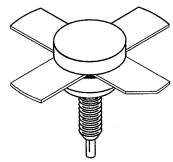
. . . designed for 12.5 volt large–signal power amplifiers in commercial and industrial equipment.

- High Common Emitter Power Gain
- Specified 12.5 V, 175 MHz Performance
  Output Power = 30 Watts
  Power Gain = 10 dB
  Efficiency = 60%
- Diffused Emitter Resistor Ballasting
- Characterized to 220 MHz
- Load Mismatch at High Line and Overdrive Conditions

30 W, 136–220 MHz
RF POWER
TRANSISTORS
NPN SILICON



CASE 211–07, STYLE 1
MRF1946



CASE 145A–09, STYLE 1
MRF1946A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	100 0.57	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W

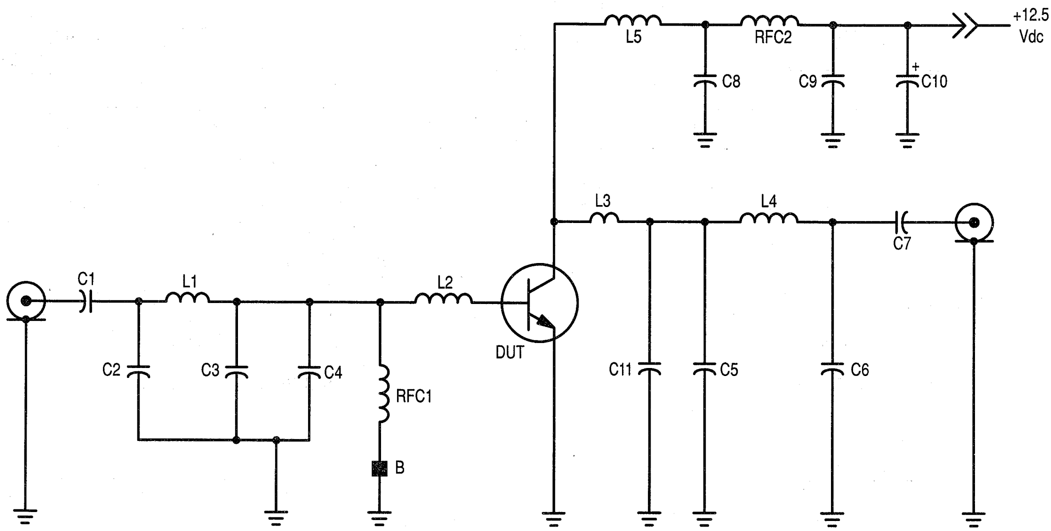
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	75	150	—

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	75	100	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 30 W, f = 175 MHz)	G_{pe}	10	11	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 30 W, f = 175 MHz)	η	60	70	—	%
Load Mismatch (V_{CC} = 15.5 Vdc, P_{in} = 2.0 dB Overdrive, Load VSWR = 30:1)	ψ	No Degradation in Power Output			



C1 — 56 pF Mini–Unelco, 3HS0006–56
C2 — 47 pF Mini–Unelco, 3HS0006–47
C3, C4 — 180 pF Chip Cap, ATC 100B181JC500
C5 — 150 pF Unelco, J101–150
C6 — 39 pF Mini–Unelco, 3HS0006–39
C7, C8 — 1000 pF Chip Cap, ATC 100B102JC50
C9 — 0.1 µF Ceramic Capacitor
C10 — 10 µF, 25 V Electrolytic Capacitor
C11 — 56 pF Mini–Unelco, 3HS0006–56

L1 — 2 Turns #18 AWG, 0.125″ ID
L2, L3 — Circuit Board and Mounting Pad Inductance
L4 — 3 Turns #18 AWG, 0.125″ ID
L5 — 6 Turns #16 Enameled, 0.250″ ID
RFC1 — 0.15 µH Molded Choke w/Ferrite Bead
RFC2 — Ferrite Choke, Fair Rite VK200–4B
Board Material — 1/32, Glass Teflon, 1 oz. Cu Plating
Bead — Ferroxcube

Figure 1. Broadband Test Circuit Schematic

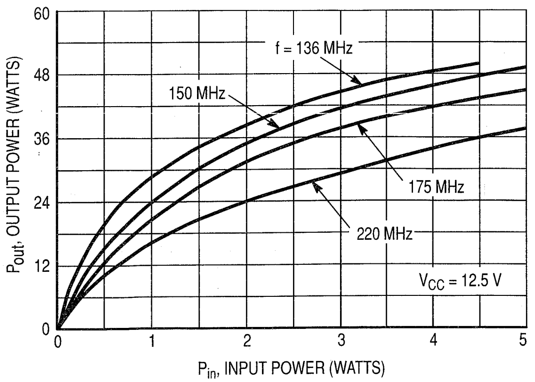


Figure 2. Output Power versus Input Power

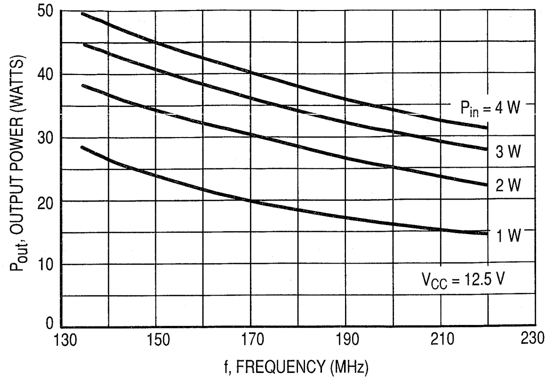


Figure 3. Output Power versus Frequency

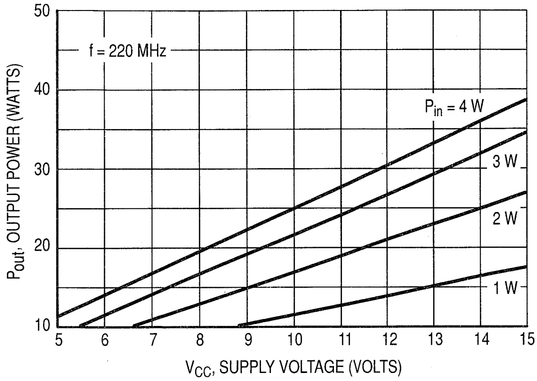


Figure 4. Output Power versus Supply Voltage

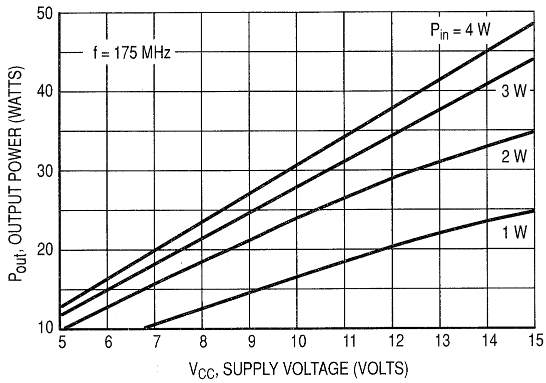


Figure 5. Output Power versus Supply Voltage

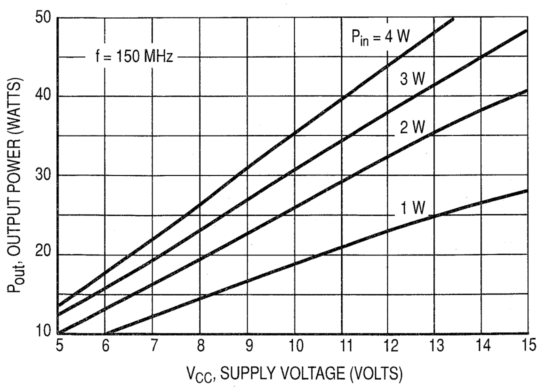


Figure 6. Output Power versus Supply Voltage

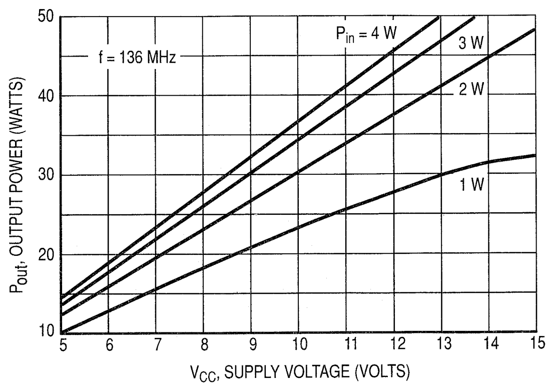


Figure 7. Output Power versus Supply Voltage

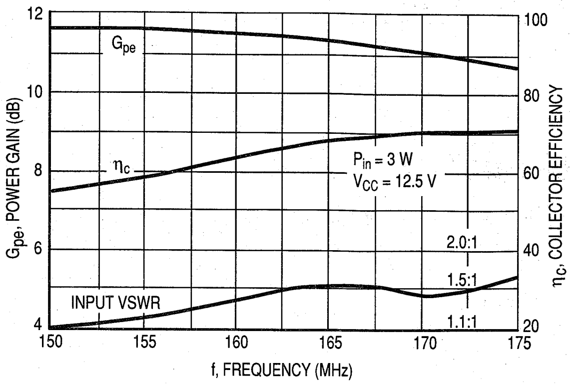
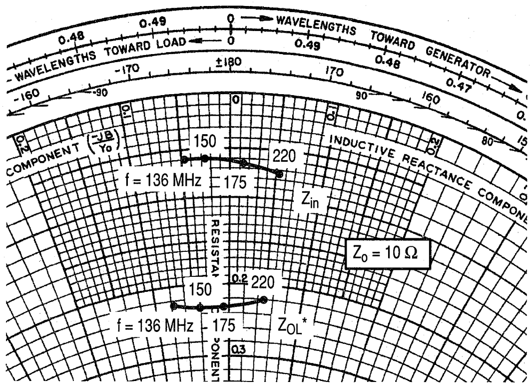


Figure 8. Typical Performance in a Broadband Circuit



V_{CC} = 12.5 Vdc, P_{out} = 30 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
136	0.60 – j0.48	2.22 – j0.74
150	0.63 – j0.26	2.30 – j0.40
175	0.62 + j0.13	2.35 – j0.04
220	0.73 + j0.57	2.20 + j0.43

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 9. Series Equivalent Input and Output Impedance

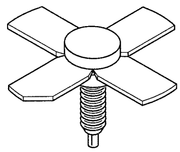
The RF Line
NPN Silicon RF Power Transistor

MRF2628

. . . designed for 12.5 volt VHF large–signal power amplifiers in commercial and industrial FM equipment.

- Compact .280 Stud Package
- Specified 12.5 V, 175 MHz Performance
  Output Power = 15 Watts
  Power Gain = 12 dB Min
  Efficiency = 60% Min
- Characterized to 220 MHz
- Load Mismatch Capability at High Line and Overdrive

**15 W 136–220 MHz
RF POWER
TRANSISTOR
NPN SILICON**



CASE 244–04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	18	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	2.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	40 0.23	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

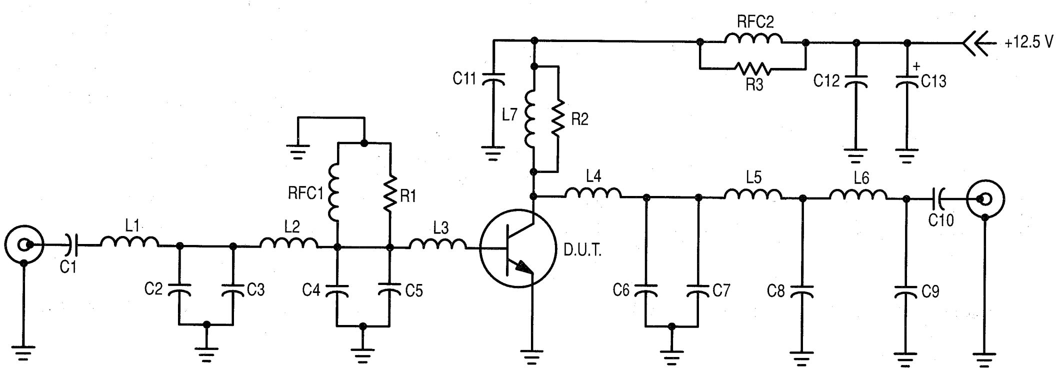
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	1.0	mAdc

(continued)

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	70	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	33	60	pF
FUNCTIONAL TESTS (Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 175 MHz)	G_{pe}	12	13	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 175 MHz)	η	60	68	—	%
Load Mismatch (V_{CC} = 15.5 Vdc, P_{in} = 2.0 dB Overdrive, Load VSWR = 30:1)	ψ	No Degradation in Output Power			



C1, C10, C11 — 1000 pF Ceramic Chip Capacitor
C2 — 27 pF Mini Unelco Capacitor
C3 — 33 pF Mini Unelco Capacitor
C4, C5 — 270 pF Unelco J101 Capacitor
C6, C9 — 18 pF Mini Unelco Capacitor
C7 — 91 pF Mini Unelco Capacitor
C8 — 68 pF Mini Unelco Capacitor
C12 — 0.1 µF Monolythic Capacitor
C13 — 100 µF, 15 V Electrolytic
L1 — 3 Turns #18 AWG, 3/16″ ID
L2 — 1–1/8″ #18 AWG into 1/2″ High Loop
L3 — Copper Pad, 0.200 x 0.400 x 0.060
L4 — 1/4″ #18 AWG into 1/8″ High Loop
L5 — 3 Turns #24 AWG Enameled, 3/32″ ID
L6 — 6 Turns #24 AWG Enameled, 3/32″ ID
L7 — 1–3/4″ #16 AWG into 3/4″ High Loop
R1 — 12 Ω, 1/2 W Carbon
R2 — 100 Ω, 1.0 W Carbon
R3 — 10 Ω, 1.0 W Carbon
RFC1 — 0.15 µH Molded Choke
RFC2 — Ferroxcube Choke, VK200–4B

Figure 1. Broadband Circuit

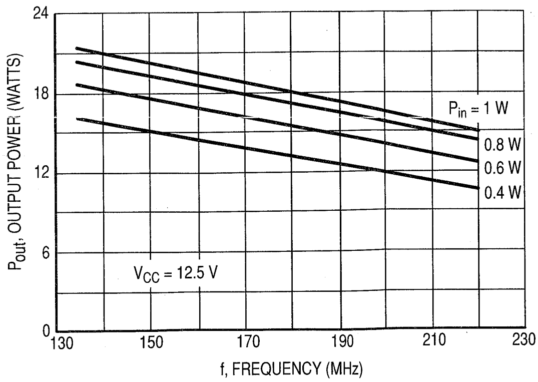


Figure 2. Output Power versus Frequency

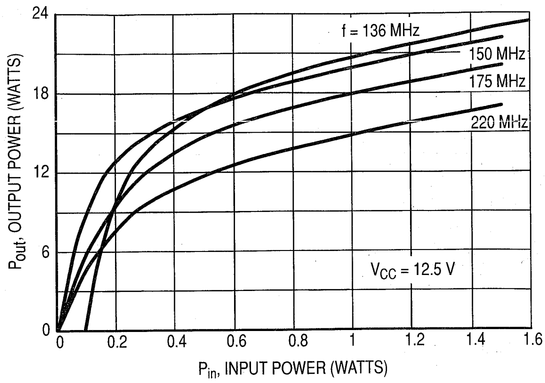


Figure 3. Output Power versus Input Power

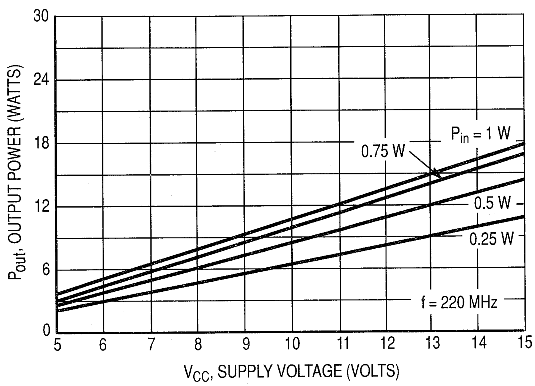


Figure 4. Output Power versus Supply Voltage

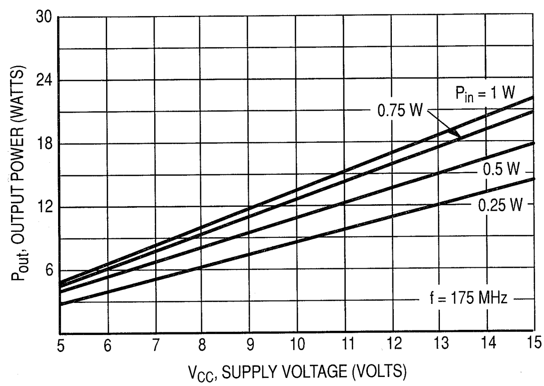


Figure 5. Output Power versus Supply Voltage

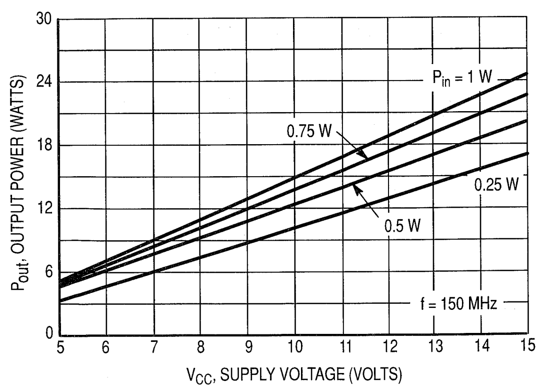


Figure 6. Output Power versus Supply Voltage

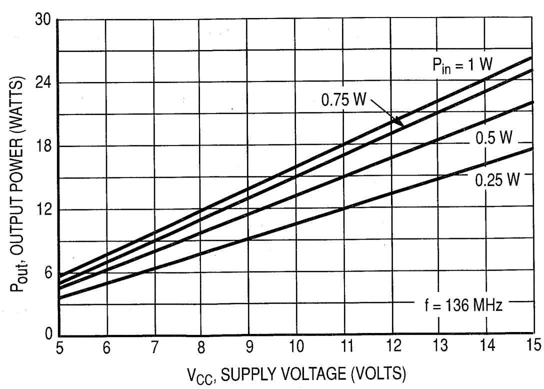


Figure 7. Output Power versus Supply Voltage

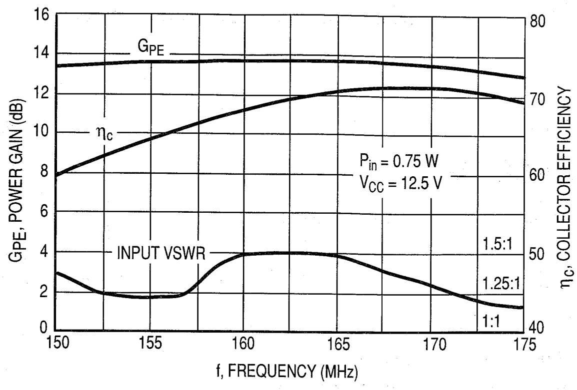
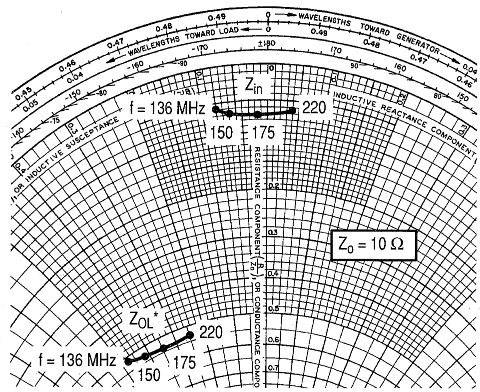


Figure 8. Typical Performance in a Broadband Circuit



V_{CC} = 12.5 V, P_{out} = 15 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
136	0.59 – j0.80	5.07 – j4.76
150	0.68 – j0.61	5.23 – j4.14
175	0.69 – j0.17	5.26 – j3.46
220	0.62 + j0.39	5.25 – j2.46

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 9. Series Equivalent Impedance

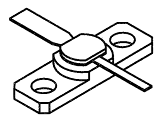
The RF Line
Microwave Linear Power Transistors

MRF3094
MRF3095

Designed for Class A, common emitter linear power amplifiers.

- Specified 20 Volt, 1.6 GHz Characteristics
  Output Power — 0.5, 0.8, 1.6 Watts
  Gain — 9.0–12 dB
- Low Parasitic Microwave Stripline Package
- Gold Metallization Diffused Emitter Ballast Resistors
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

9.0–12 dB
1.55–1.65 GHz
0.5–1.6 WATTS
MICROWAVE LINEAR
POWER TRANSISTORS



CASE 328A–03, STYLE 2

MAXIMUM RATINGS

Rating		Symbol	Limit	Unit
Collector Base Voltage		V_{CES}	50	Vdc
Emitter Base Voltage		V_{EBO}	3.5	Vdc
Collector Emitter Voltage		V_{CEO}	22	Vdc
Collector Current	MRF3094, 3095	I_C	0.4	Adc
Operating Junction Temperature		T_J	200	°C
Storage Temperature		T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
		MRF3094	MRF3095	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	40	35	°C/W

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ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = 10 mA)	MRF3094, MRF3095	$V_{(BR)CES}$	50	—	—	Vdc
Emitter Base Breakdown Voltage (I_E = 0.25 mA)	MRF3094, MRF3095	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Base Breakdown Voltage (I_C = 1.0 mA)	MRF3094, MRF3095	$V_{(BR)CBO}$	45	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 10 mA)	MRF3094, MRF3095	$V_{(BR)CEO}$	22	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 V)	MRF3094, MRF3095	I_{CBO}	—	—	0.25	mAdc
ON CHARACTERISTICS						
DC Current Gain (V_{CE} = 5.0 V, I_C = 100 mA)	MRF3094, MRF3095	h_{fe}	20	35	120	—
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 28 V, f = 1.0 MHz)	MRF3094, MRF3095	C_{ob}	—	—	3.5	pF
Functional Tests (V_{CE} = 20 V, I_C = 120 mA, P_o = 0.5 W, f = 1.6 GHz)	MRF3094	G_{PE}	10.5	11.5	—	dB
(V_{CE} = 20 V, I_C = 120 mA, P_o = 0.8 W, f = 1.6 GHz)	MRF3095		9.0	10	—	
Output Load Mismatch (V_{CE} = 20 V, I_C = 120 mA, P_o = 0.5 W, f = 1.6 GHz, Load VSWR = ∞:1)	MRF3094	ψ	No degradation in output power			
(V_{CE} = 20 V, I_C = 120 mA, P_o = 0.8 W, f = 1.6 GHz, Load VSWR = ∞:1)	MRF3095					
Gain Linearity (V_{CE} = 20 V, I_C = 120 mA, f = 1.6 GHz, P_{o1} = 0.5 W, P_{o2} = 0.5 mW)	MRF3094	L_G	—	—	−0.2 to +1.0	dB
(V_{CE} = 20 V, I_C = 120 mA, f = 1.6 GHz, P_{o1} = 0.8 W, P_{o2} = 0.8 mW)	MRF3095		—	—	−0.2 to +1.0	

TYPICAL CHARACTERISTICS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	∠ φ	Mag	∠ φ	Mag	∠ φ	Mag	∠ φ
20	100	500	0.77	−177.9	6.16	83.7	0.36	31.9	0.32	−57.1
		600	0.78	176.7	5.20	77.2	0.38	32.2	0.30	−60.3
		700	0.78	171.8	4.48	71.1	0.40	33.4	0.29	−62.6
		800	0.78	167.4	3.90	66.3	0.41	35.0	0.29	−67.3
		900	0.79	163.3	3.46	61.2	0.42	36.6	0.28	−70.8
		1000	0.79	159.3	3.11	56.4	0.46	38.1	0.29	−74.5
		1100	0.80	155.7	2.81	52.0	0.48	39.2	0.29	−79.3
		1200	0.80	152.4	2.60	47.5	0.50	40.1	0.29	−83.3
		1300	0.80	149.3	2.40	43.5	0.53	40.7	0.30	−88.3
		1400	0.80	147.1	2.18	40.6	0.57	42.2	0.30	−93.3
		1500	0.81	143.6	2.06	34.3	0.59	41.0	0.30	−97.7
		1600	0.81	140.8	1.92	30.8	0.62	41.9	0.30	−103.4
		1700	0.82	137.9	1.81	27.9	0.66	42.5	0.31	−107.6
		1800	0.82	135.2	1.67	22.7	0.68	41.9	0.32	−112.7
		1900	0.83	132.7	1.61	19.4	0.71	41.9	0.33	−117.8
		2000	0.83	130.2	1.52	16.3	0.75	41.8	0.34	−121.3

Table 1. MRF3094 Common Emitter S–Parameters

MRF3094

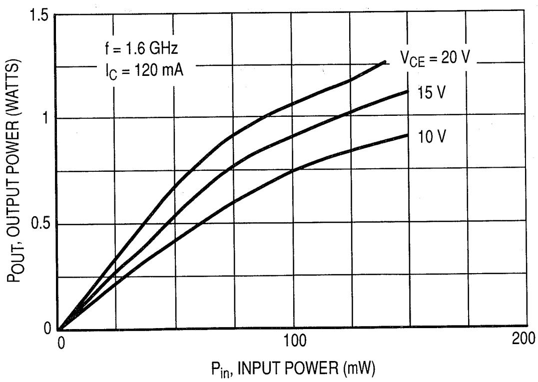


Figure 1. Output Power versus Input Power

f GHz	Z_{in} Ohms		Z_{OL}* Ohms	
	R	jx	R	jx
1.55	5.9	11.9	10.2	0.23
1.60	5.8	11.3	11.3	−2.4
1.65	5.6	10.6	12.4	−6.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and power.

Figure 2. Series Equivalent Input and Output Impedance

TYPICAL CHARACTERISTICS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	∠ φ	Mag	∠ φ	Mag	∠ φ	Mag	∠ φ
20	120	500	0.83	−177.4	4.90	71.1	0.29	21.7	0.36	−81.6
		600	0.83	179.6	4.08	64.4	0.30	22.1	0.37	−87.2
		700	0.83	176.9	3.48	59.3	0.31	23.6	0.39	−92.3
		800	0.83	175.0	3.20	52.8	0.34	23.2	0.42	−96.4
		900	0.82	171.6	2.70	48.6	0.33	25.0	0.43	−103.2
		1000	0.82	169.5	2.49	42.3	0.36	24.9	0.46	−107.6
		1100	0.83	167.4	2.26	37.0	0.38	25.2	0.48	−112.5
		1200	0.80	164.3	2.10	29.4	0.39	22.1	0.51	−117.7
		1300	0.81	162.2	1.87	27.9	0.41	25.9	0.54	−121.6
		1400	0.81	160.1	1.77	21.7	0.44	24.4	0.57	−125.3
		1500	0.80	157.8	1.63	15.2	0.45	22.4	0.58	−129.3
		1600	0.80	155.2	1.46	11.1	0.46	22.6	0.61	−131.7
		1700	0.80	152.3	1.42	9.6	0.48	23.9	0.66	−133.9
		1800	0.78	148.5	1.36	2.5	0.53	21.6	0.66	−136.6
		1900	0.77	144.5	1.25	−3.1	0.54	19.7	0.66	−139.3
		2000	0.78	141.0	1.17	−5.6	0.58	20.3	0.67	−141.9

Table 2. MRF3095 Common Emitter S–Parameters

MRF3095

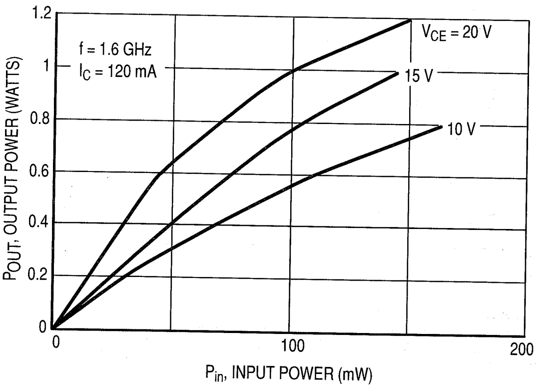


Figure 3. Output Power versus Input Power

f GHz	Z_{in} Ohms		Z_{OL}* Ohms	
	R	jx	R	jx
1.55	5.2	10.6	8.6	−22.4
1.60	4.9	9.9	9.6	−25.4
1.65	4.8	9.3	10.3	−27.8

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and power.

Figure 4. Series Equivalent Input and Output Impedance

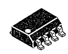
The RF Line

NPN Silicon High-Frequency Transistor

MRF3866R2

- Tape and reel packaging available for MRF3866R2:
  R2 suffix = 2,500 units per reel

I_C = 400 mA
HIGH–FREQUENCY TRANSISTORS
NPN SILICON



CASE 751–05, STYLE 1
(SO–8)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous	I_C	0.4	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C
Maximum Junction Temperature	T_{Jmax}	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, R_{BE} = 10 Ω)	$V_{(BR)CER}$	55	—	Vdc
Collector–Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, I_B = 0)	I_{CEO}	—	0.02	mAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = –1.5 Vdc (Rev.), T_C = 150°C) (V_{CE} = 55 Vdc, V_{BE} = –1.5 Vdc (Rev.)	I_{CEX}	 — —	 5.0 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 3.5 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS				
DC Current Gain (I_C = 360 mAdc, V_{CE} = 5.0 Vdc) (1) (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	 5.0 10	 — 200	—
Collector–Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 20 mAdc)	$V_{CE(sat)}$	—	1.0	Vdc
SMALL–SIGNAL CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	500	—	MHz
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	—	3.0	pF
FUNCTIONAL TEST				
Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	G_{pe}	10	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	η	45	—	%

NOTE:
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			S_{11}	∠ φ	S_{21}	∠ φ	S_{12}	∠ φ	S_{22}	∠ φ
15	50	100	0.67	−166	13.75	92	0.016	44	0.32	−27
		200	0.69	−176	6.93	81	0.024	53	0.30	−24
		300	0.70	177	4.57	73	0.032	57	0.32	−31
		400	0.71	172	3.38	67	0.042	59	0.34	−37
		500	0.72	168	2.66	61	0.049	59	0.37	−45
		600	0.72	164	2.17	54	0.056	61	0.40	−53
		700	0.72	160	1.85	49	0.061	63	0.43	−60
		800	0.72	155	1.61	44	0.068	65	0.47	−66
		900	0.71	151	1.40	39	0.075	64	0.50	−73
		1000	0.70	146	1.25	34	0.084	68	0.53	−79

Table 1. MRF3866R2 Common Emitter S–Parameters

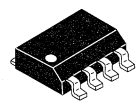
The RF Line
NPN Silicon
RF Low Power Transistor

MRF4427R2

Designed for amplifier, frequency multiplier, or oscillator applications in industrial equipment constructed with surface mount components. Suitable for use as output driver or pre–driver stages in VHF and UHF equipment.

- Low Cost SORF Plastic Surface Mount Package
- Guaranteed RF Specification — $|S_{21}|^2$
- S–Parameter Characterization
- Low Voltage Version of MRF3866
- Tape and Reel Packaging Available.
  R2 suffix = 2,500 units per reel

1.0 W, 175 MHz
HIGH–FREQUENCY
TRANSISTOR
NPN SILICON



CASE 751–05, STYLE 1
SORF
(SO–8)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	20	Vdc
Collector–Base Voltage	V_{CBO}	40	Vdc
Emitter–Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Continuous	I_C	400	mAdc
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	1.67 22.2	Watts mW/°C
Operating Junction and Storage Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	45	°C/W

DEVICE MARKING

MRF4427 = 4427

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, R_{BE} = 10 ohms)	$V_{(BR)CER}$	40	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 100 μAdc)	$V_{(BR)EBO}$	2.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 12 Vdc, I_B = 0)	I_{CEO}	—	—	20	μAdc

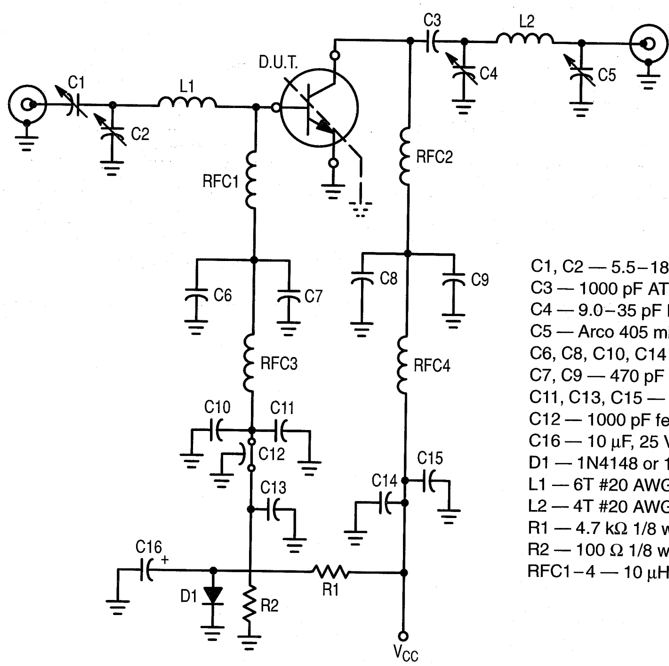
(continued)

NOTE:
1. Case temperature measured on collector lead immediately adjacent to body of package.

REV 8

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	50	200	—
(I_C = 360 mAdc, V_{CE} = 5.0 Vdc)		5.0	—	—	
Collector–Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 20 mAdc)	$V_{CE(sat)}$	—	60	—	mVdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 12 Vdc, f = 200 MHz)	f_T	—	1600	—	MHz
Output Capacitance (V_{CB} = 12 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	3.0	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (P_{in} = 15 mW, V_{CC} = 12 Vdc, f = 175 MHz)	G_{pe}	—	18	—	dB
Collector Efficiency (Figure 1) (P_{out} = 1.0 W, V_{CC} = 12 Vdc, f = 175 MHz)	η	—	60	—	%
Insertion Gain (V_{CE} = 12 Vdc, I_C = 50 mA, f = 200 MHz)	$\|S_{21}\|^2$	14	16.4	—	dB



C1, C2 — 5.5–18 pF Erie ceramic trimmer
C3 — 1000 pF ATC 100 mil chip cap.
C4 — 9.0–35 pF Erie ceramic trimmer
C5 — Arco 405 mica trimmer
C6, C8, C10, C14 — 0.1 μF Erie blue cap.
C7, C9 — 470 pF ATC 100 mil chip cap.
C11, C13, C15 — 1.0 μF Erie blue cap, non–polar
C12 — 1000 pF feedthru
C16 — 10 μF, 25 V tantalum
D1 — 1N4148 or 1N914
L1 — 6T #20 AWG on #2 drill bit
L2 — 4T #20 AWG on #4 drill bit
R1 — 4.7 kΩ 1/8 watt carbon
R2 — 100 Ω 1/8 watt carbon
RFC1–4 — 10 μH molded choke

Figure 1. 175 MHz RF Amplifier Circuit for Functional Tests

TYPICAL CHARACTERISTICS

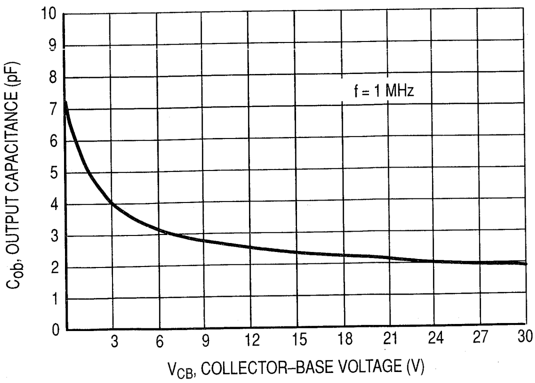


Figure 2. Collector–Base Capacitance versus Voltage

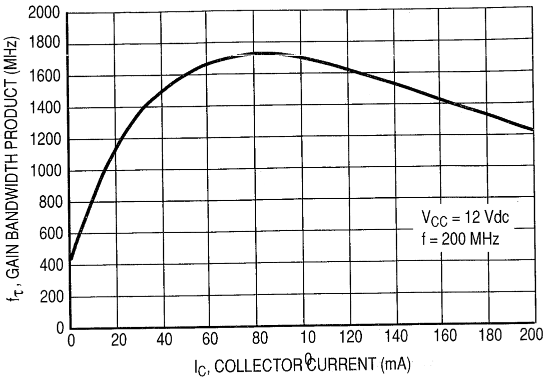


Figure 3. Gain Bandwidth Product versus Collector Current

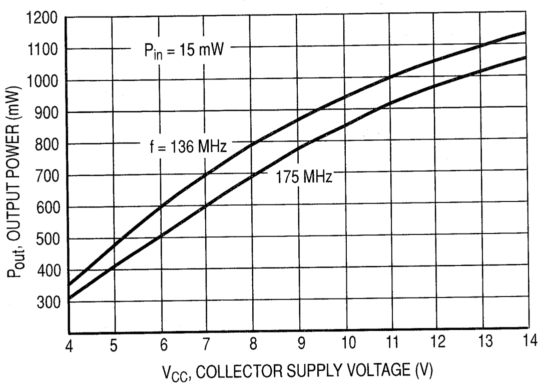


Figure 4. Output Power versus Voltage

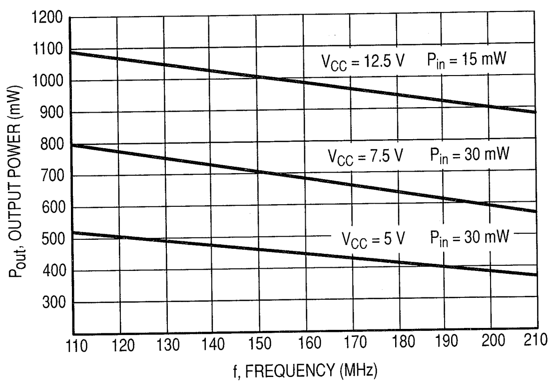


Figure 5. Output Power versus Frequency

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\lvert S_{11} \rvert$	$\angle \phi$	$\lvert S_{21} \rvert$	$\angle \phi$	$\lvert S_{12} \rvert$	$\angle \phi$	$\lvert S_{22} \rvert$	$\angle \phi$
5.0	5.0	50	0.82	−104	10.3	125	0.05	38	0.68	−34
		100	0.83	−141	6.1	103	0.06	26	0.51	−40
		200	0.81	−165	3.2	85	0.07	21	0.44	−46
		500	0.80	169	1.3	57	0.07	32	0.49	−73
		750	0.79	156	0.8	42	0.08	49	0.58	−94
		1000	0.76	144	0.6	30	0.11	61	0.65	−114
	25	50	0.77	−151	19	107	0.02	36	0.35	−75
		100	0.79	−168	9.9	94	0.03	37	0.21	−87
		200	0.79	−180	5.0	82	0.04	49	0.16	−97
		500	0.78	163	2.0	61	0.07	62	0.22	−106
		750	0.77	152	1.3	48	0.10	66	0.31	−115
		1000	0.74	141	0.9	36	0.13	66	0.37	−127
	50	50	0.77	−163	21.1	103	0.02	37	0.29	−98
		100	0.79	−174	10.7	92	0.02	50	0.19	−119
		200	0.79	177	5.4	82	0.03	62	0.16	−134
		500	0.78	162	2.2	62	0.07	67	0.20	−131
		750	0.77	151	1.4	50	0.10	69	0.26	−130
		1000	0.74	140	1.1	38	0.13	67	0.32	−139
12	5.0	50	0.83	−97	11	129	0.04	46	0.75	−26
		100	0.82	−135	6.8	107	0.05	29	0.61	−29
		200	0.81	−162	3.6	88	0.05	24	0.54	−34
		500	0.79	171	1.4	60	0.06	37	0.47	−57
		750	0.78	157	0.9	44	0.07	55	0.64	−76
		1000	0.75	145	0.7	32	0.09	68	0.70	−95
	25	50	0.73	−143	22.1	111	0.02	38	0.43	−52
		100	0.76	−164	11.7	96	0.02	39	0.29	−52
		200	0.77	−177	6.0	84	0.03	48	0.22	−53
		500	0.76	165	2.4	63	0.06	64	0.27	−69
		750	0.75	154	1.6	49	0.08	67	0.35	−84
		1000	0.72	143	1.1	38	0.11	69	0.42	−98
	50	50	0.73	−156	25.5	106	0.02	41	0.32	−67
		100	0.75	−171	13.1	94	0.02	49	0.20	−69
		200	0.76	59	6.6	83	0.03	60	0.15	−71
		500	0.75	164	2.6	64	0.06	69	0.20	−81
		750	0.74	153	1.7	51	0.09	70	0.27	−92
		1000	0.71	142	1.2	38	0.12	70	0.34	−104

Table 1. Common Emitter S–Parameters

Freq. (MHz)	P_{in} (mW)	P_{out} (mW)	V_{CC} (Volts)	Z_{in} (Ohms)	Z_{OL}* (Ohms)
136	15	—	12.5	6.2 – j11.6	—
175	15	—	12.5	4.6 – j10.4	—
136	—	1000	12.5	—	47.7 + j41.7
175	—	1000	12.5	—	47.4 – j34.4
136	30	—	7.5	5.65 – j12.6	—
175	30	—	7.5	6.25 – j12.2	—
136	—	650	7.5	—	27.6 – j32.4
175	—	650	7.5	—	27.9 – j27.6
136	30	—	5.0	6.1 – j13.3	—
175	30	—	5.0	5.9 – j12.22	—
136	—	450	5.0	—	24.8 – j22.8
175	—	450	5.0	—	28.3 – j29.3

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Table 2. Series Input/Output Impedances

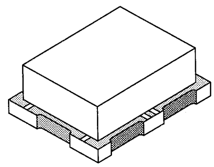
The RF MOSFET Line
RF Power Field Effect Transistor
N–Channel Enhancement–Mode

MRF5003
MRF5003R1

The MRF5003 is designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 7.5 Volt and 12.5 Volt mobile, portable, and base station FM equipment.

- Guaranteed Performance at 512 MHz, 7.5 Volts
  Output Power = 3.0 Watts
  Power Gain = 9.5 dB
  Efficiency = 45%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 512 MHz, 2.0 dB Overdrive
- Suitable for 12.5 Volt Applications
- True Surface Mount Package
- Available in Tape and Reel by Adding R1 Suffix to Part Number.
  R1 Suffix = 500 Units per 16 mm, 7 inch Reel.
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**3.0 W, 7.5 V, 512 MHz
N–CHANNEL
BROADBAND
RF POWER FET**



CASE 430–01, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	36	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 Meg Ohm)	V_{DGR}	36	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	1.7	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.07	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

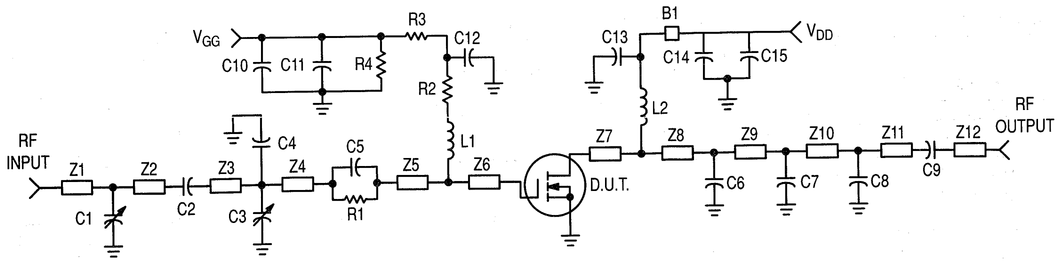
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	14	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 2.5 mAdc)	$V_{(BR)DSS}$	36	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 5.0 mAdc)	$V_{GS(th)}$	1.25	2.25	3.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.5 Adc)	$V_{DS(on)}$	—	—	0.375	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 0.5 Adc)	g_{fs}	0.6	—	—	mho
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	16.5	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	3.5	4.4	5.4	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 7.5 Vdc, P_{out} = 3.0 W, I_{DQ} = 50 mA) f = 512 MHz f = 175 MHz	G_{ps}	9.5 —	10.5 15	— —	dB
Drain Efficiency (V_{DD} = 7.5 Vdc, P_{out} = 3.0 W, I_{DQ} = 50 mA) f = 512 MHz f = 175 MHz	h	45 —	50 55	— —	%



C1, C3, C7, C8	0 to 20 pF Johanson
C2, C9	56 pF, 100 mil Chip
C4	10 pF, 100 mil Chip
C5	47 pF, Miniature Clamped Mica Capacitor
C6	22 pF, 100 mil Chip
C10, C15	10 μF, 50 V, Electrolytic
C11, C14	0.1 μF, Capacitor
C12	1000 pF, 100 mil Chip
C13	160 pF, 100 mil Chip
R1	35 Ω, 1/4 W Carbon
R2	30 Ω, 0.1 W Chip
R3	1.0 kΩ, 0.1 W Chip
R4	1.0 MΩ, 1/4 W Carbon
B1	Fair Rite Products Short Ferrite Bead (2743021446)

Board — Glass Teflon®, 31 mils

Note: Plated ceramic part locators (0.1″ x 0.15″) soldered onto Z6 and Z7.

Z1	0.350″ x 0.08″ Microstrip
Z2	0.190″ x 0.08″ Microstrip
Z3	0.800″ x 0.08″ Microstrip
Z4	0.380″ x 0.08″ Microstrip
Z5	0.150″ x 0.08″ Microstrip
Z6	0.285″ x 0.08″ Microstrip
Z7	0.340″ x 0.08″ Microstrip
Z8	0.070″ x 0.08″ Microstrip
Z9	0.280″ x 0.08″ Microstrip
Z10	0.840″ x 0.08″ Microstrip
Z11	0.180″ x 0.08″ Microstrip
Z12	0.600″ x 0.08″ Microstrip
L1	7 Turns, 0.076″ ID, #24 AWG Enamel
L2	5 Turns, 0.126″ ID, #20 AWG Enamel

Input/Output Connectors — Type N

Figure 1. 512 MHz Narrowband Test Circuit

TYPICAL CHARACTERISTICS

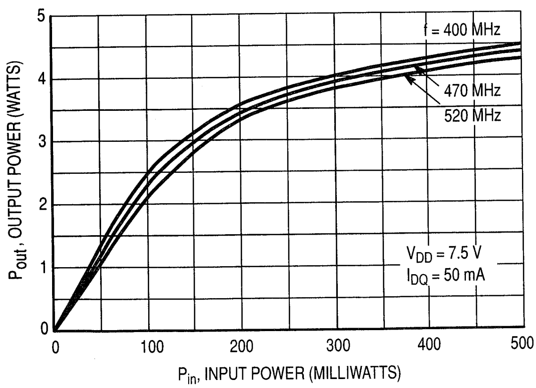


Figure 2. Output Power versus Input Power

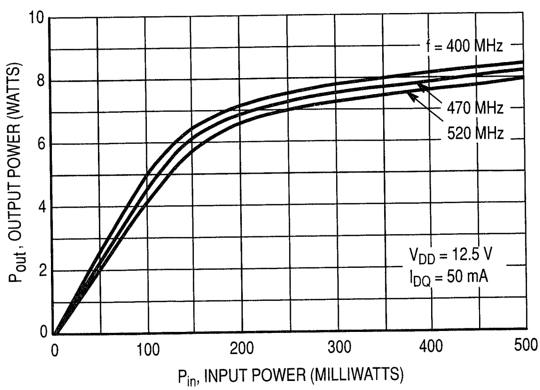


Figure 3. Output Power versus Input Power

TYPICAL CHARACTERISTICS

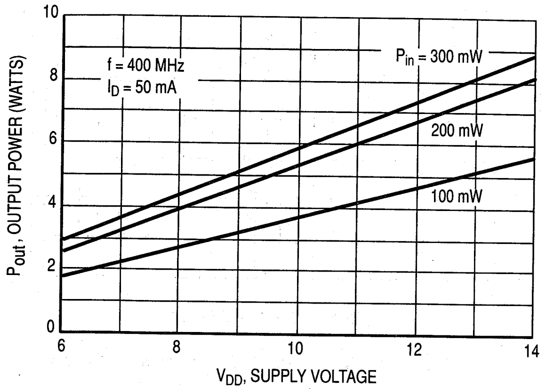


Figure 4. Output Power versus Supply Voltage

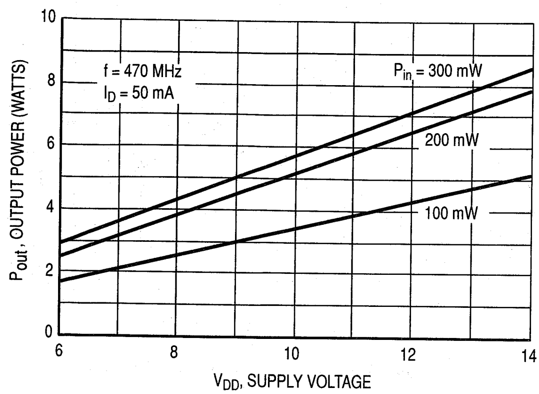


Figure 5. Output Power versus Supply Voltage

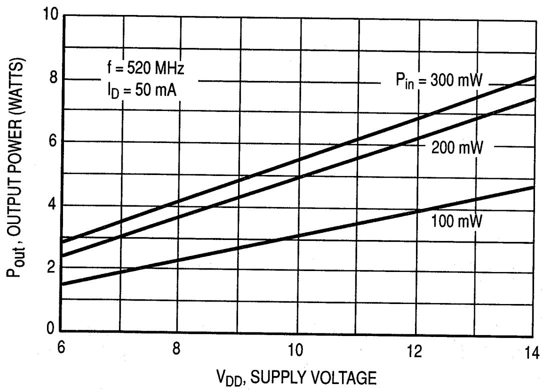


Figure 6. Output Power versus Supply Voltage

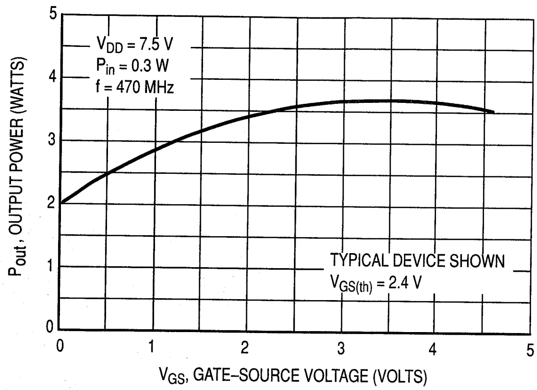


Figure 7. Output Power versus Gate Voltage

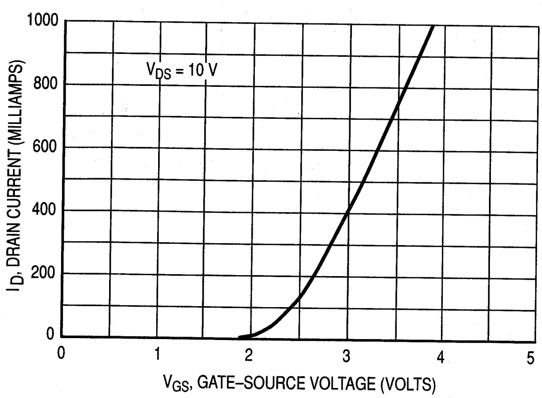


Figure 8. Drain Current versus Gate Voltage (Typical Device Shown)

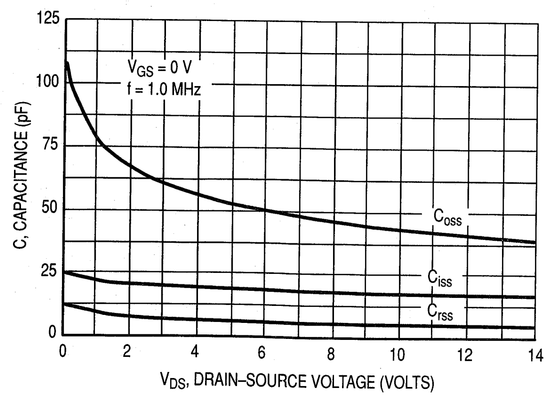


Figure 9. Capacitance versus Voltage

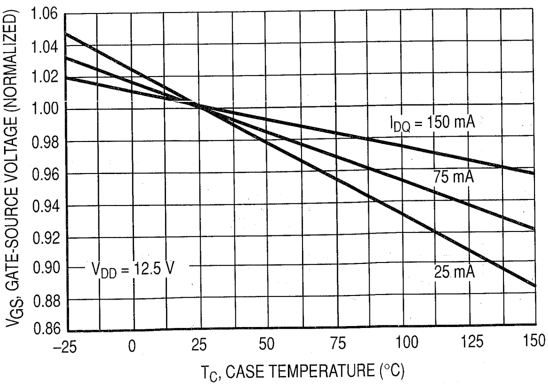


Figure 10. Gate–Source Voltage versus Case Temperature

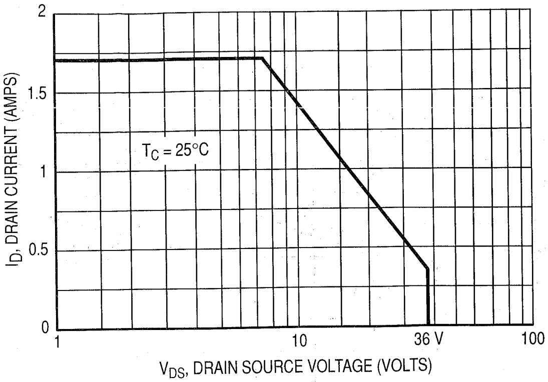
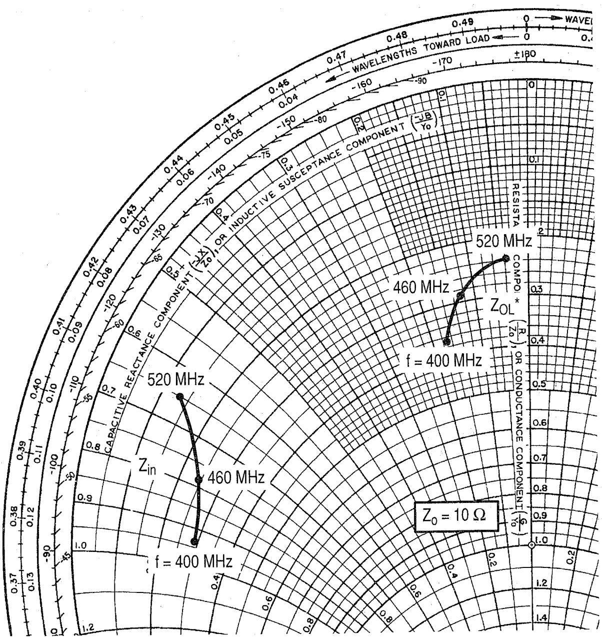


Figure 11. Maximum Rated Forward Biased Safe Operating Area



V_{DD} = 7.5 V, I_{DQ} = 50 mA, P_{out} = 3.0 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	2.8 – j9.2	3.6 – j1.7
430	2.7 – j8.5	3.3 – j1.5
460	2.5 – j7.8	2.7 – j1.1
490	2.0 – j7.2	2.5 – j0.8
520	1.3 – j6.5	2.4 – j0.5

Z_{in} = Conjugate of source impedance with parallel 35 Ω resistor and 47 pF capacitor in series with gate.

Z_{OL}* = Conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50%.

Note: Z_{ol}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

Figure 12. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DS} = 10 V)

I_D = 50 mA

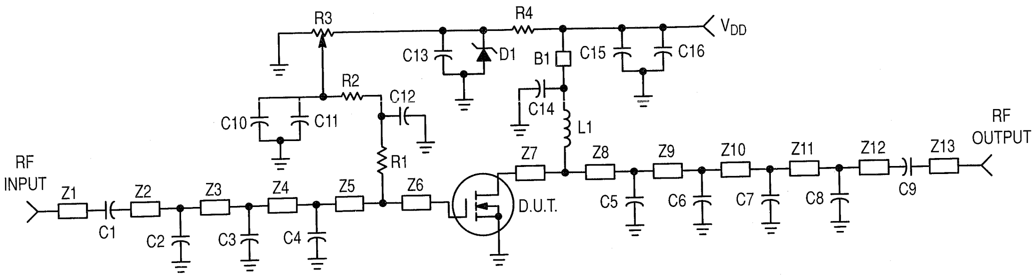
f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$|S_{11}|$	∠ φ	$|S_{21}|$	∠ φ	$|S_{12}|$	∠ φ	$|S_{22}|$	∠ φ
50	0.69	−90	10.8	117	0.07	29	0.74	−119
100	0.58	−120	6.0	96	0.08	10	0.78	−146
200	0.58	−139	3.0	75	0.08	−7	0.81	−161
300	0.64	−147	1.9	61	0.07	−16	0.84	−166
400	0.70	−152	1.3	50	0.06	−21	0.86	−169
500	0.75	−157	0.99	41	0.05	−24	0.88	−172
700	0.82	−165	0.61	28	0.03	−15	0.92	−176
850	0.86	−171	0.45	21	0.02	13	0.94	−179
1000	0.89	−176	0.34	16	0.02	47	0.95	178

I_D = 500 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$|S_{11}|$	∠ φ	$|S_{21}|$	∠ φ	$|S_{12}|$	∠ φ	$|S_{22}|$	∠ φ
50	0.76	−124	15.0	109	0.04	23	0.76	−151
100	0.72	−150	7.9	94	0.04	12	0.81	−165
200	0.72	−163	4.0	80	0.04	6	0.83	−172
300	0.73	−168	2.6	71	0.04	5	0.84	−175
400	0.75	−171	1.9	62	0.04	7	0.85	−176
500	0.77	−173	1.5	55	0.03	12	0.86	−178
700	0.81	−177	0.97	42	0.03	29	0.89	−180
850	0.84	−180	0.75	35	0.03	44	0.90	178
1000	0.86	177	0.60	29	0.04	55	0.92	176

I_D = 1.0 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$|S_{11}|$	∠ φ	$|S_{21}|$	∠ φ	$|S_{12}|$	∠ φ	$|S_{22}|$	∠ φ
50	0.80	−125	14.6	110	0.04	23	0.75	−155
100	0.76	−150	7.8	95	0.04	10	0.81	−167
200	0.76	−164	3.9	81	0.04	1	0.83	−173
300	0.77	−169	2.6	71	0.04	−3	0.84	−175
400	0.79	−172	1.9	63	0.03	−5	0.85	−176
500	0.80	−174	1.4	56	0.03	−5	0.86	−177
700	0.83	−178	0.95	43	0.03	−1	0.88	−179
850	0.85	179	0.73	35	0.02	9	0.90	179
1000	0.87	177	0.58	28	0.02	22	0.91	178



C1, C9	100 pF 100 mil Chip
C2	16 pF, 100 mil Chip
C3	24 pF, 100 mil Chip
C4	68 pF, 100 mil Chip
C5	51 pF, 100 mil Chip
C6	39 pF, 100 mil Chip
C7	6.2 pF, 100 mil Chip
C8	9.1 pF, 100 mil Chip
C10, C15	39000 pF, 100 mil Chip
C11, C16	10 μF, 50 V Electrolytic
C12	10000 pF, 100 mil Chip
B1	Fair Rite Products Short Ferrite Bead (2743021446)
C13	0.1 μF, 100 mil Chip
C14	160 pF, 100 mil Chip
R1	43 Ω, 0.1 W Chip Resistor
R2	1000 Ω, 0.1 W Chip Resistor
R3	10 kΩ Potentiometer
R4	3000 Ω, 0.1 W Chip Resistor
L1	5 Turns, 0.126″ ID, #20 AWG Enamel
Z1 to Z13	See Photomaster
D1	1N4734 Motorola Zener

Board — G10, 1/32″

Input/Output Connectors — SMA

Figure 13. Schematic of Broadband Demonstration Amplifier

PERFORMANCE CHARACTERISTICS OF BROADBAND DEMONSTRATION AMPLIFIER

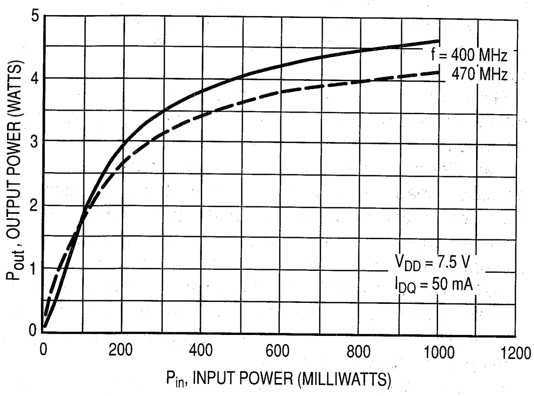


Figure 14. Output Power versus Input Power

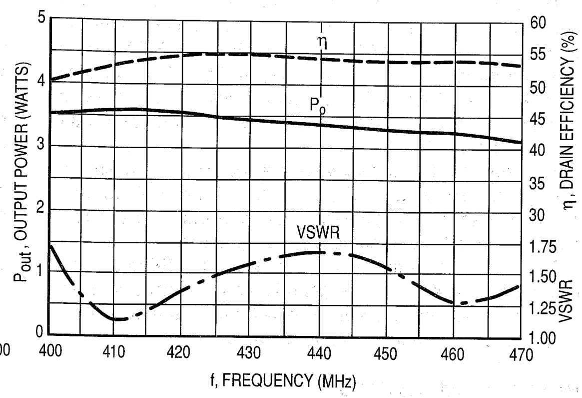


Figure 15. Output Power, Drain Efficiency and VSWR versus Frequency

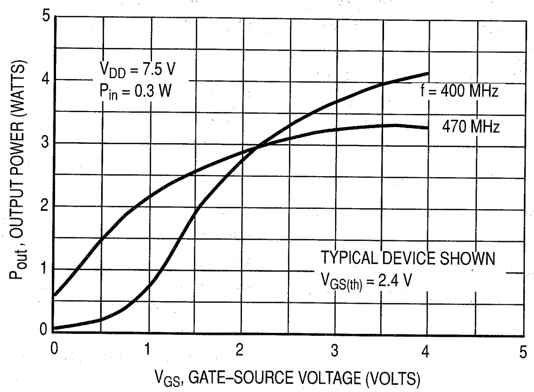


Figure 16. Output Power versus Gate Voltage

DESIGN CONSIDERATIONS

The MRF5003 is a common–source, RF power, N–Channel enhancement mode, Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design. Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts.

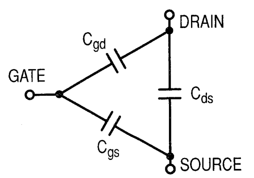
The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling.

Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since the MRF5003 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 8 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. The MRF5003 was characterized at I_{DQ} = 50 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF5003 may be controlled from its rated value down to zero (negative gain) with a low power dc control signal, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 16 is an example of output power variation with gate–source bias voltage. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 14°C/W assumes a majority of the 0.100″ x 0.200″ source contact on the back side of the package is in good contact with an appropriate heat sink. In the test fixture shown in Figure 1, the device is clamped directly to a copper pedestal. In the demonstration amplifier, the device was mounted on top of the G10 circuit board and heat removal was accomplished through several solder filled plated through holes. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5003. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors". Both small–signal S–parameters and large–signal impedances are provided. While the S–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of the MRF5003 yield a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Different stabilizing techniques were applied to the test fixture and demonstration amplifiers. The RF test fixture implements a parallel resistor and capacitor in series with the gate while the demonstration amplifier utilizes a 43 Ω shunt resistor from gate to ground. Both circuits have a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two port stability analysis with the MRF5003 S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters", for a discussion of two port network theory and stability.

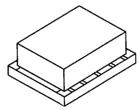
The RF MOSFET Line
RF Power Field Effect Transistor
N–Channel Enhancement–Mode

MRF5007
MRF5007R1

The MRF5007 is designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 7.5 Volt portable FM equipment.

- Guaranteed Performance at 512 MHz, 7.5 Volts
  Output Power = 7.0 Watts
  Power Gain = 10 dB Min
  Efficiency = 50% Min
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 VSWR, @ 10 Vdc, 512 MHz, 2.0 dB Overdrive
- True Surface Mount Package
- Available in Tape and Reel by Adding R1 Suffix to Part Number.
  R1 Suffix = 500 Units per 16 mm, 7 inch Reel.

7.0 W, 7.5 Vdc
512 MHz
N–CHANNEL
BROADBAND
RF POWER FET



CASE 430B–02, Style 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	25	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 Meg Ohm)	V_{DGR}	25	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	4.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.14	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

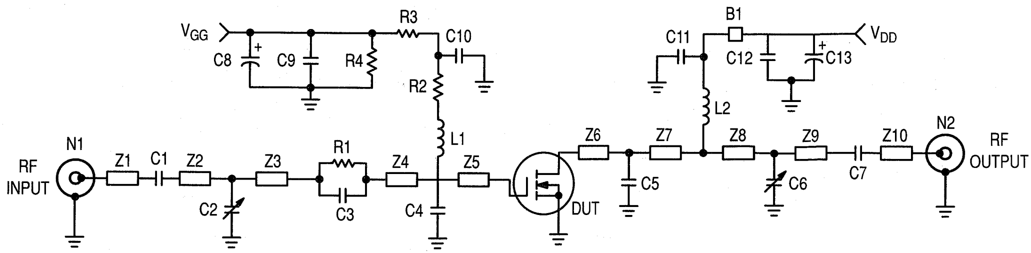
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.8	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 2.5 mAdc)	$V_{(BR)DSS}$	25	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 10 mAdc)	$V_{GS(th)}$	1.25	2.2	3.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	—	—	0.3	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1.0 Adc)	g_{fs}	0.9	—	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	32	—	pF
Output Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	63	—	pF
Reverse Transfer Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	10	13	16	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain f = 512 MHz (V_{DD} = 7.5 Vdc, P_{out} = 7.0 W, I_{DQ} = 75 mA)	G_{ps}	10	11.5	—	dB
Drain Efficiency f = 512 MHz (V_{DD} = 7.5 Vdc, P_{out} = 7.0 W, I_{DQ} = 75 mA)	η	50	55	—	%



B1	Fair Rite Products Short Ferrite Bead (2743021446)	R3	1.0 kΩ, 0.1 W Chip
C1, C7	100 pF, 100 mil Chip	R4	1.1 MΩ, 1/4 W Carbon
C2, C6	0–20 pF, Johanson	Z1, Z10	0.594″ x 0.08″ Microstrip
C3	47 pF, Miniature Clamped Mica Capacitor	Z2	0.811″ x 0.08″ Microstrip
C4	16 pF, Miniature Clamped Mica Capacitor	Z3	0.270″ x 0.08″ Microstrip
C5	21 pF, Miniature Clamped Mica Capacitor	Z4	0.122″ x 0.08″ Microstrip
C8, C13	10 μF, 50 V, Electrolytic	Z5	0.303″ x 0.08″ Microstrip
C9, C12	0.1 μF, Chip Capacitor	Z6	0.211″ x 0.08″ Microstrip
C10	1000 pF, 100 mil Chip	Z7	0.084″ x 0.08″ Microstrip
C11	140 pF, 100 mil Chip	Z8	0.060″ x 0.08″ Microstrip
L1	7 Turns, 0.076″ ID, #24 AWG Enamel	Z9	1.343″ x 0.08″ Microstrip
L2	5 Turns, 0.126″ ID, #20 AWG Enamel	Board — Glass Teflon®, 31 mils	
N1, N2	Type N Flange Mount	Note: BeCu part locators (0.147″ x 0.093″) soldered onto Z5 and Z6	
R1	39 Ω, 1/4 W Carbon		
R2	30 Ω, 0.1 W Chip		

Figure 1. 512 MHz Narrowband Test Circuit

TYPICAL CHARACTERISTICS

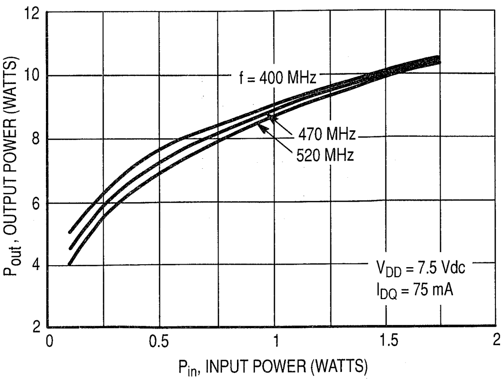


Figure 2. Output Power versus Input Power

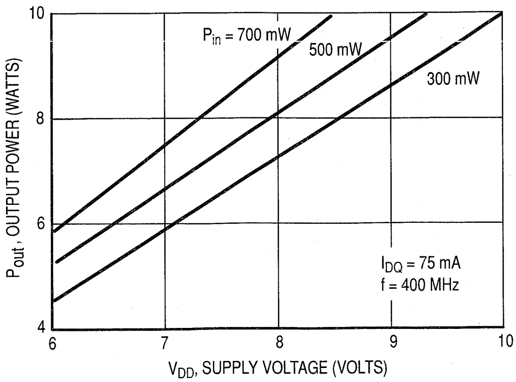


Figure 3. Output Power versus Supply Voltage

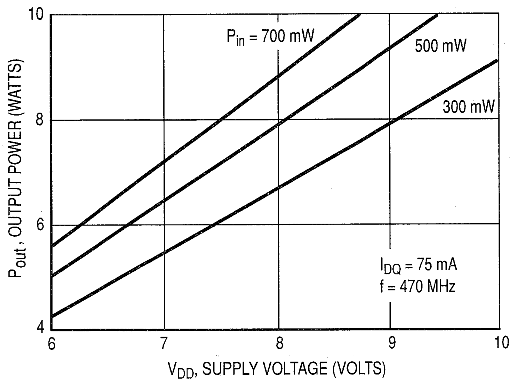


Figure 4. Output Power versus Supply Voltage

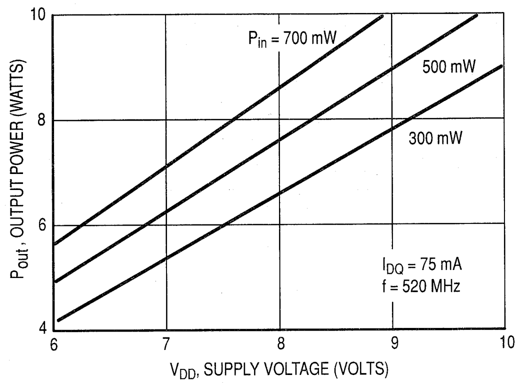


Figure 5. Output Power versus Supply Voltage

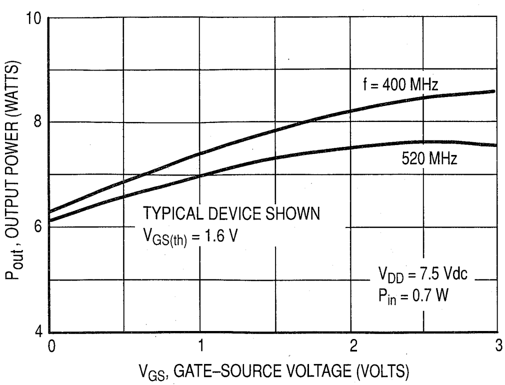


Figure 6. Output Power versus Gate Voltage

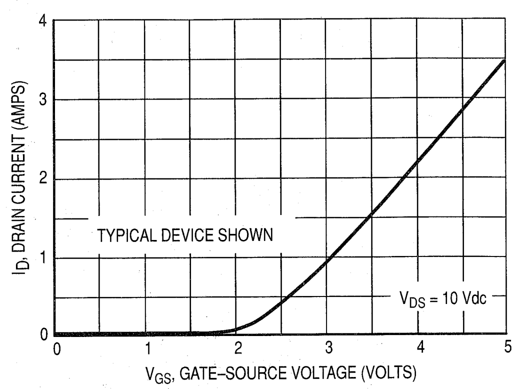


Figure 7. Drain Current versus Gate Voltage

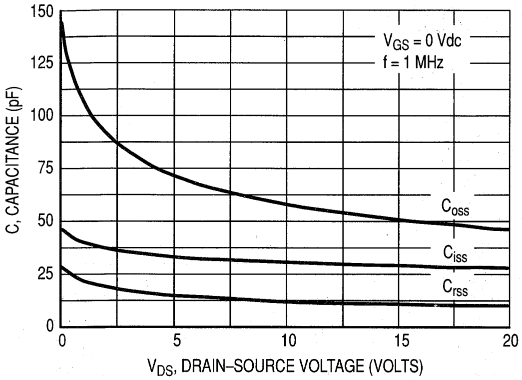


Figure 8. Capacitance versus Voltage

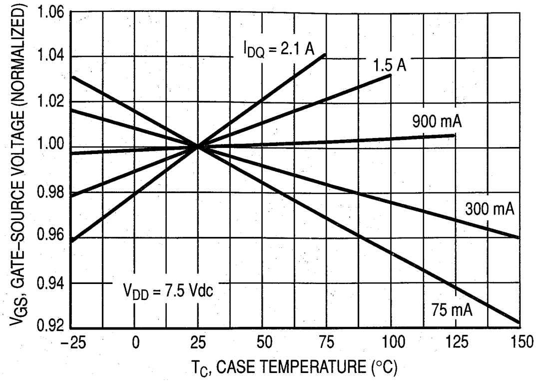


Figure 9. Gate–Source Voltage versus Case Temperature

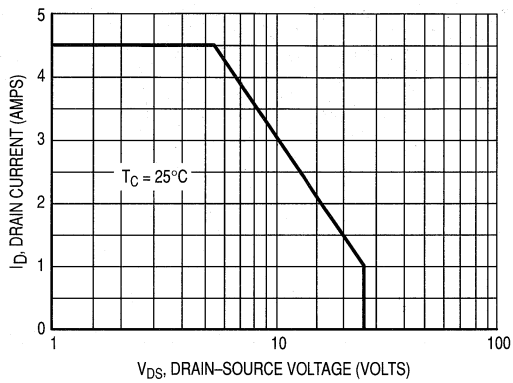
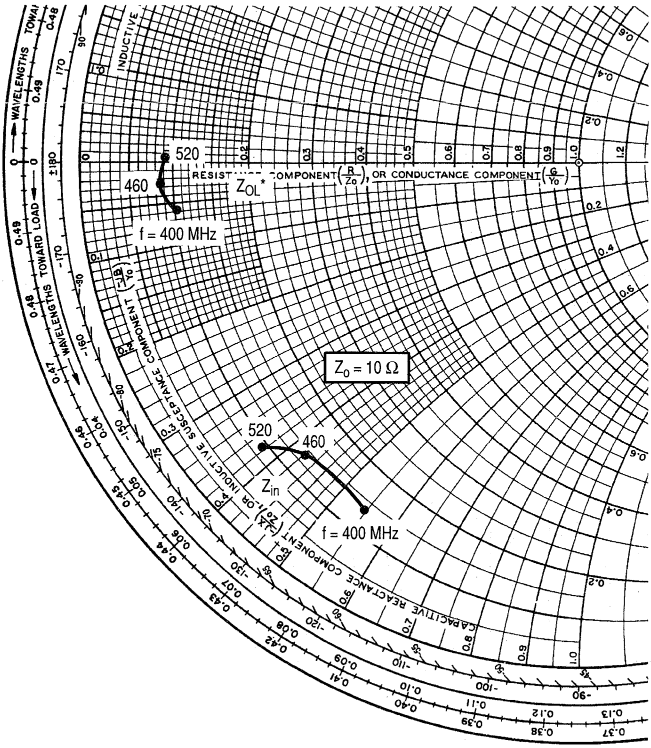


Figure 10. Maximum Rated Forward Biased Safe Operating Area



V_{DD} = 7.5 Vdc, I_{DQ} = 75 mA, P_{out} = 7.0 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	1.4 – j5.4	1.0 – j0.6
430	1.4 – j4.5	0.9 – j0.5
460	1.3 – j4.2	0.9 – j0.3
490	1.2 – j4.0	0.9 – j0.1
520	1.0 – j3.7	0.9 + j0.1

Z_{in} = Conjugate of source impedance with parallel 39 Ω resistor and 47 pF capacitor in series with gate.

Z_{OL}* = Conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50%.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

Figure 11. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DS} = 7.5 Vdc)

I_D = 75 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.75	−132	6.05	103	0.08	15	0.76	−156
100	0.73	−152	3.13	88	0.08	1	0.80	−166
200	0.75	−162	1.52	71	0.08	−13	0.83	−171
300	0.78	−164	0.95	59	0.07	−22	0.85	−172
400	0.81	−166	0.66	49	0.06	−29	0.88	−173
500	0.83	−167	0.49	40	0.06	−35	0.90	−174
700	0.87	−170	0.30	27	0.05	−43	0.93	−175
850	0.89	−171	0.22	19	0.04	−46	0.94	−177
1000	0.91	−173	0.17	13	0.03	−48	0.96	−178
1200	0.92	−174	0.13	7	0.03	−48	0.97	−180

I_D = 500 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.88	−152	6.89	100	0.03	12	0.87	−172
100	0.87	−166	3.50	91	0.03	4	0.88	−176
200	0.87	−172	1.74	81	0.03	−2	0.89	−178
300	0.87	−175	1.15	74	0.03	−6	0.89	−178
400	0.88	−176	0.84	68	0.03	−8	0.90	−179
500	0.88	−176	0.66	63	0.03	−11	0.90	−179
700	0.89	−177	0.45	53	0.03	−14	0.92	−179
850	0.90	−178	0.35	46	0.03	−15	0.92	−180
1000	0.90	−178	0.28	40	0.02	−15	0.93	179
1200	0.91	−179	0.22	34	0.02	−14	0.94	179

I_D = 1.5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.91	−155	6.67	99	0.03	11	0.91	−174
100	0.91	−167	3.38	91	0.03	5	0.92	−177
200	0.91	−174	1.69	83	0.03	1	0.92	−179
300	0.91	−176	1.12	77	0.03	−1	0.92	−179
400	0.91	−177	0.83	72	0.02	−2	0.93	−180
500	0.91	−177	0.65	67	0.02	−3	0.93	180
700	0.92	−178	0.45	57	0.02	−4	0.93	179
850	0.92	−178	0.36	51	0.02	−4	0.94	179
1000	0.93	−179	0.29	46	0.02	−3	0.94	178
1200	0.93	−179	0.23	39	0.02	0	0.95	177

DESIGN CONSIDERATIONS

The MRF5007 is a common–source, RF power, N–Channel enhancement mode, Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design. Motorola Application Note AN211A, "FETs in Theory and Practice," is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

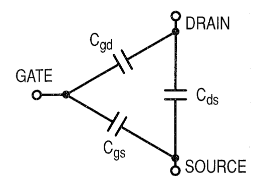
The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high — on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling.

Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since the MRF5007 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 7 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. The MRF5007 was characterized at I_{DQ} = 75 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF5007 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 6 is an example of output power variation with gate–source bias voltage. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 7.0°C/W assumes a majority of the 0.137″ x 0.185″ source contact on the back side of the package is in good contact with an appropriate heat sink. In the test fixture shown in Figure 1, the device is clamped directly to a copper pedestal. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. It is recomended that this temperature not exceed 100°C for any operating condition. Contact customer service for additional information on thermal considerations for mounting.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5007. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Both small–signal S–parameters and large–signal impedances are provided. While the S–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of the MRF5007 yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two port stability analysis with the MRF5007 S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters," for a discussion of two port network theory and stability.

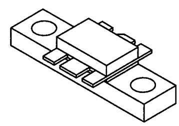
The RF MOSFET Line
RF Power Field Effect Transistor
N–Channel Enhancement–Mode

MRF5015

15 W, 512 MHz, 12.5 VOLTS
N–CHANNEL BROADBAND
RF POWER FET

Designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 12.5 volt mobile, and base station FM equipment.

- Guaranteed Performance at 512 MHz, 12.5 Volts
  - Output Power — 15 Watts
  - Power Gain — 10 dB Min
  - Efficiency — 50% Min
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 512 MHz, 2 dB Overdrive
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 319–07, STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	36	Vdc
Drain–Gate Voltage (RGS = 1 MΩ)	V_{DGR}	36	Vdc
Gate–Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	6	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.29	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

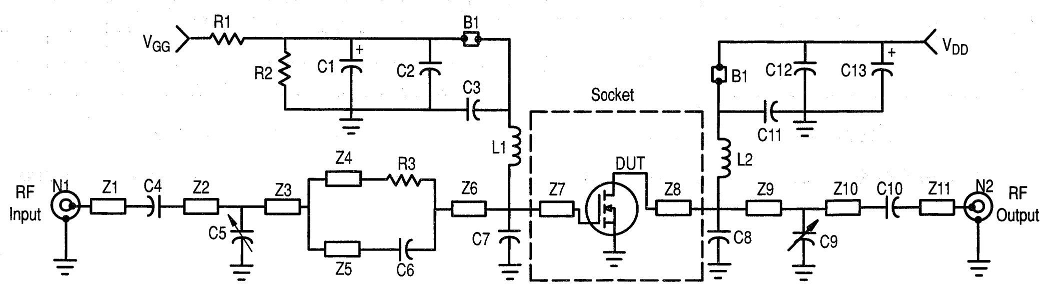
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 5 mAdc)	$V_{(BR)DSS}$	36	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	—	—	5	mAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	2	µAdc

(continued)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 10 mAdc)	$V_{GS(th)}$	1.25	2.3	3.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	—	0.375	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	1.2	—	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	33	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	74	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	7	8.8	10.8	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 15 W, I_{DQ} = 100 mA) f = 512 MHz f = 175 MHz	G_{ps}	10 —	11.5 15	— —	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 15 W, I_{DQ} = 100 mA) f = 512 MHz f = 175 MHz	η	50 —	55 55	— —	%
Load Mismatch (V_{DD} = 15.5 Vdc, 2 dB Overdrive, f = 512 MHz, Load VSWR = 20:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			



B1, B2	Ferrite Bead, Fair Rite Products	R3	160 Ω, 0.1 W Chip
C1, C13	10 µF, 50 V, Electrolytic	Z1, Z11	Transmission Line*
C2, C12	0.1 µF, Chip Capacitor	Z2	Transmission Line*
C3, C4, C10, C11	120 pF, Chip Capacitor	Z3	Transmission Line*
C5, C9	0 to 20 pF, Trimmer Capacitor	Z4	Transmission Line*
C6	36 pF, Chip Capacitor	Z5	Transmission Line*
C7	43 pF, Chip Capacitor	Z6	Transmission Line*
C8	30 pF, Chip Capacitor	Z7, Z8	Transmission Line+
L1, L2	7 Turns, 24 AWG 0.116″ ID	Z9	Transmission Line*
N1, N2	Type N Flange Mount	Z10	Transmission Line*
R1	1 kΩ, 1/4 W, Carbon	Board	Glass Teflon® 0.060″
R2	470 kΩ, 1/4 W, Carbon		+ Part of Capacitor Mount Socket
			*See Photomaster

Figure 1. 512 MHz Narrowband Test Circuit Electrical Schematic

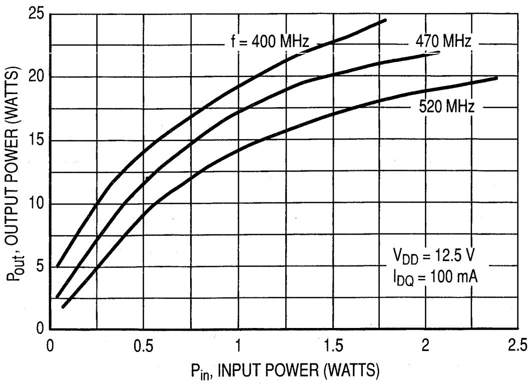


Figure 2. Output Power versus Input Power

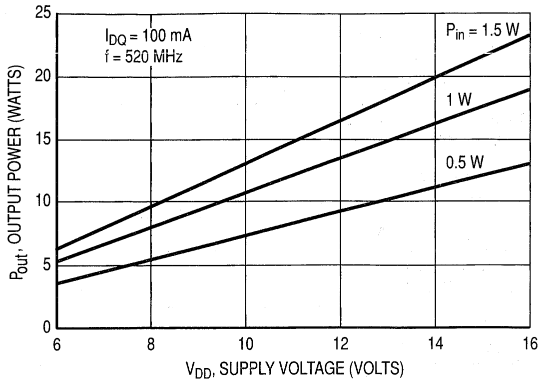


Figure 3. Output Power versus Supply Voltage

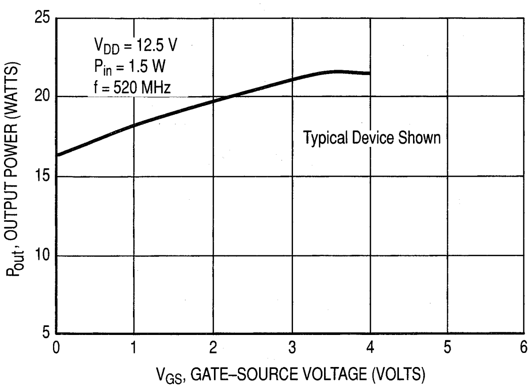


Figure 4. Output Power versus Gate Voltage

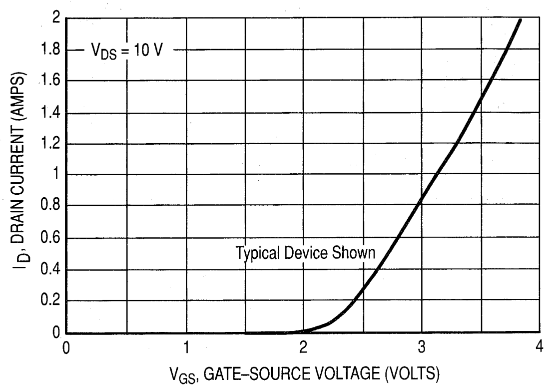


Figure 5. Drain Current versus Gate Voltage

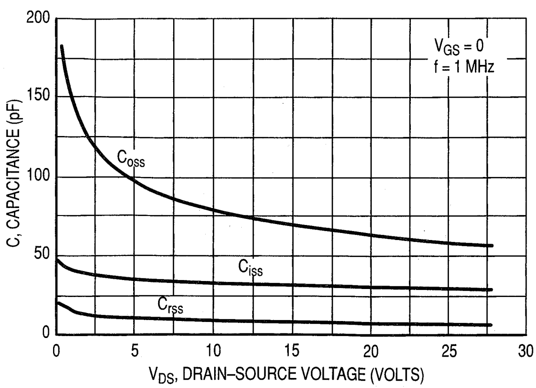


Figure 6. Capacitance versus Voltage

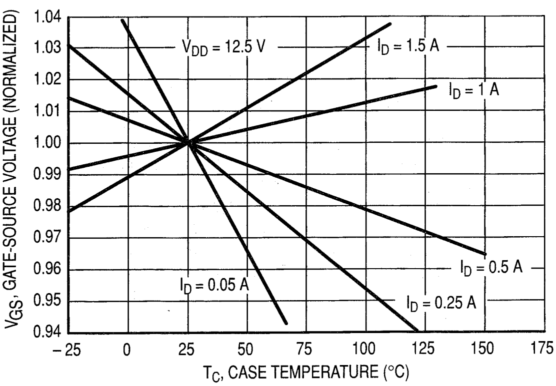


Figure 7. Gate–Source Voltage versus Case Temperature

TYPICAL CHARACTERISTICS

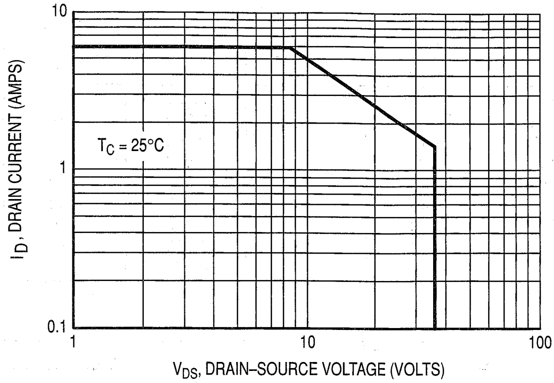
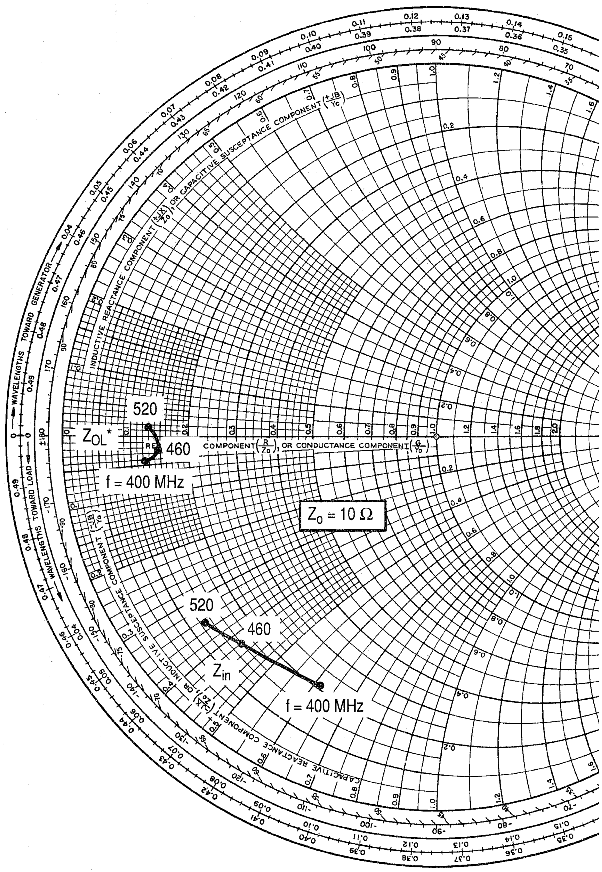


Figure 8. DC Safe Operating Area



V_{DD} = 12.5 V, I_{DQ} = 100 mA, P_{out} = 15 W

f (MHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
400	2.0 – j6.1	1.3 – j0.4
420	1.8 – j5.3	1.4 – j0.4
440	1.6 – j4.7	1.5 – j0.4
460	1.5 – j4.2	1.5 – j0.3
480	1.4 – j3.8	1.5 – j0.2
500	1.3 – j3.6	1.4 – j0.1
520	1.2 – j3.5	1.3 + j0.1

Z_{in} = Conjugate of source impedance with parallel 160 Ω resistor and 36 pF capacitor in series with gate.

Z_{OL*} = Conjugate of the load impedance at given output power, voltage and frequency that produces maximum gain.

Figure 9. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DS} = 12.5 V)

I_D = 50 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.63	–123	8	100	0.063	11	0.79	–149
100	0.62	–142	4	82	0.063	– 6	0.82	–162
200	0.70	–152	1.8	61	0.056	– 23	0.86	–169
300	0.78	–157	1.1	47	0.046	– 35	0.90	–171
400	0.84	–162	0.70	36	0.037	– 42	0.93	–174
500	0.88	–165	0.49	28	0.029	– 46	0.94	–175
700	0.93	–171	0.28	17	0.016	– 45	0.97	–179
850	0.95	–175	0.20	13	0.010	– 31	0.97	179
1000	0.96	–178	0.15	10	0.007	11	0.98	178

I_D = 100 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.67	–136	9.1	99	0.047	10	0.82	–158
100	0.66	–153	4.6	84	0.048	–3	0.85	–168
200	0.71	–160	2.2	66	0.043	–17	0.87	–172
300	0.77	–163	1.3	54	0.037	– 26	0.90	–174
400	0.82	–165	0.89	44	0.031	– 32	0.92	–175
500	0.86	–168	0.64	36	0.025	– 35	0.94	–177
700	0.91	–173	0.37	25	0.015	– 30	0.96	–179
850	0.93	–176	0.27	20	0.010	–11	0.97	179
1000	0.95	–179	0.20	16	0.009	25	0.98	177

I_D = 500 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.81	–150	11.1	98	0.027	11	0.85	–168
100	0.81	–164	5.6	86	0.027	2	0.87	–174
200	0.82	–170	2.7	73	0.025	– 5	0.88	–176
300	0.84	–173	1.7	63	0.023	– 9	0.89	–177
400	0.86	–174	1.2	55	0.020	– 9	0.91	–178
500	0.88	–175	0.92	47	0.018	– 7	0.92	–179
700	0.91	–178	0.57	35	0.013	7	0.94	180
850	0.93	180	0.43	29	0.013	26	0.95	178
1000	0.94	178	0.33	23	0.014	44	0.96	177

I_D = 2.5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.86	–144	10.1	101	0.022	15	0.85	–171
100	0.85	–161	5.2	88	0.022	5	0.87	–175
200	0.86	–170	2.5	74	0.021	–1	0.89	–177
300	0.87	–173	1.6	64	0.019	– 4	0.90	–178
400	0.89	–175	1.1	55	0.017	– 2	0.91	–178
500	0.91	–176	0.84	48	0.015	2	0.93	–179
700	0.93	–179	0.52	37	0.013	22	0.95	179
850	0.94	179	0.39	30	0.014	39	0.96	178
1000	0.95	177	0.30	26	0.016	52	0.96	176

DESIGN CONSIDERATIONS

The MRF5015 is a common–source, RF power, N–Channel enhancement mode, Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design. Motorola Application Note AN211A, "FETs in Theory and Practice," is suggested reading for those not familiar with the construction and characteristics of FETs.

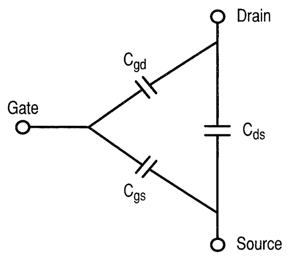
This device was designed primarily for 12.5 volt VHF and UHF power amplifier applications. The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



$C_{iss} = C_{gd} + C_{gs}$
$C_{oss} = C_{gd} + C_{ds}$
$C_{rss} = C_{gd}$

DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{ds(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{ds(on)}$. For MOSFETs, $V_{ds(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high, on the order of 10^9 Ω, resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating – Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination – The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating must be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection – These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling networks.

Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since the MRF5015 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 5 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. The MRF5015 was characterized at I_{DQ} = 100 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws essentially no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF5015 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 4 is an example of output power variation with gate–source bias voltage with P_{in} held constant. This characteristic is very dependent on frequency and load line.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5015. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Both small–signal S–parameters and large–signal impedances are provided. While the S–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of MRF5015 yield a device quite capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Different stabilizing techniques may be required depending on the desired gain and bandwidth of the application. The RF test fixture implements a parallel resistor and capacitor in series with the gate to improve stability and input impedance Q.

Two port stability analysis with the MRF5015 S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters," for a discussion of two port network theory and stability.

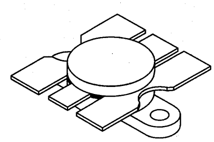
The RF MOSFET Line
RF Power Field Effect Transistor
N–Channel Enhancement–Mode

MRF5035

Designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 12.5 volt mobile, and base station FM equipment.

- Guaranteed Performance at 512 MHz, 12.5 Volt
  Output Power — 35 Watts
  Power Gain — 6.5 dB Min
  Efficiency — 50% Min
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 Load VSWR, @ 15.5 Volt, 512 MHz, 2 dB Overdrive
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**35 W, 12.5 VOLTS, 512 MHz
N–CHANNEL BROADBAND
RF POWER FET**



CASE 316–01, STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	36	Vdc
Drain–Gate Voltage (RGS = 1 MΩ)	V_{DGR}	36	Vdc
Gate–Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	97 0.56	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 20 mAdc)	$V_{(BR)DSS}$	36	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	—	—	5	mAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	5	µAdc

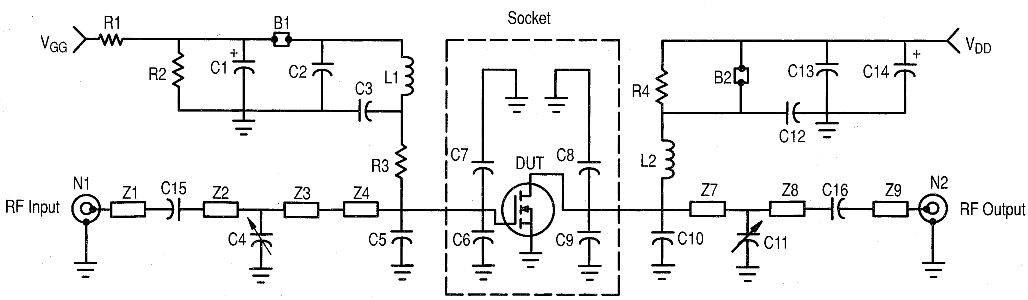
(continued)

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 25 mAdc)	$V_{GS(th)}$	1.25	2.3	3.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3 Adc)	$V_{DS(on)}$	—	—	0.422	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	3.2	—	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	88	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	197	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	18	24	29	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 35 W, I_{DQ} = 400 mA) f = 512 MHz f = 175 MHz	G_{ps}	6.5 —	7.5 12	— —	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 35 W, I_{DQ} = 400 mA) f = 512 MHz f = 175 MHz	η	50 —	55 55	— —	%
Load Mismatch (V_{DD} = 15.5 Vdc, 2 dB Overdrive, f = 512 MHz, Load VSWR = 20:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			



Components List

B1, B2	Short Ferrite Bead, Fair Rite Products	N1, N2	Type N Flange Mount
C1, C14	10 µF, 50 V, Electrolytic	R1	1 kΩ, 1/4 W, Carbon
C2	1500 pF, Chip Capacitor	R2	1 MΩ, 1/4 W, Carbon
C3	140 pF, Chip Capacitor	R3	100 Ω, 1/4 W, Carbon
C4, C11	0–10pF, Trimmer Capacitor	R4	110 Ω, 1/4 W, Carbon
C5	30 pF, Chip Capacitor	Z1, Z9	Transmission Line*
C6, C7	43 pF, Chip Capacitor	Z2	Transmission Line*
C8, C9	36 pF, Chip Capacitor	Z3	Transmission Line*
C10	3.6 pF, Chip Capacitor	Z4	Transmission Line*
C12, C15, C16	120 pF, Chip Capacitor	Z7	Transmission Line*
C13	0.1 µF, Chip Capacitor	Z8	Transmission Line*
L1	5 Turns, 18 AWG, 0.116″ ID	Board	Glass Teflon® 0.060″
L2	8 Turns, 20 AWG, 0.125″ ID		*See Photomaster for Dimensions

Figure 1. 512 MHz Narrowband Test Circuit Electrical Schematic

TYPICAL CHARACTERISTICS

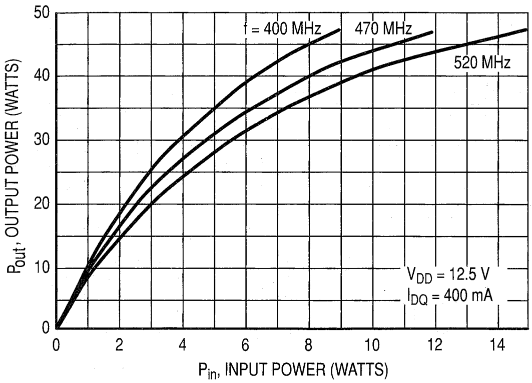


Figure 2. Output Power versus Input Power

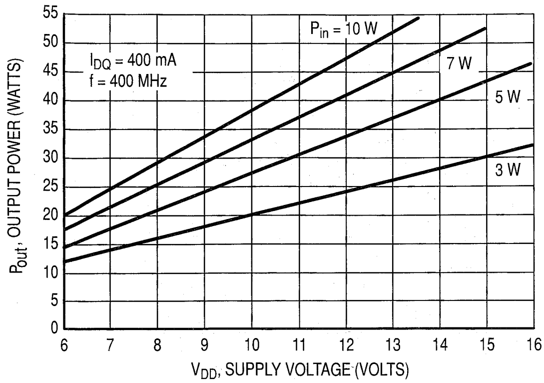


Figure 3. Output Power versus Supply Voltage

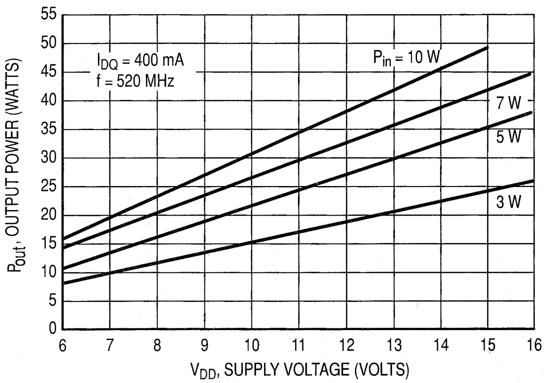


Figure 4. Output Power versus Supply Voltage

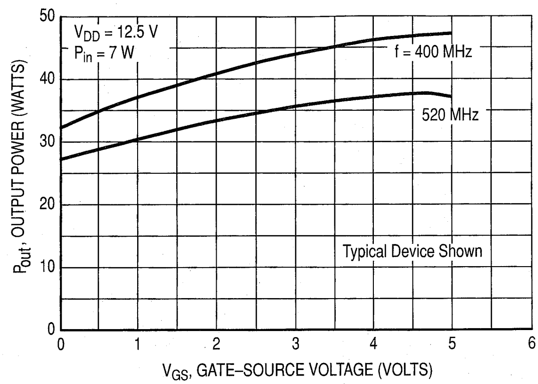


Figure 5. Output Power versus Gate Voltage

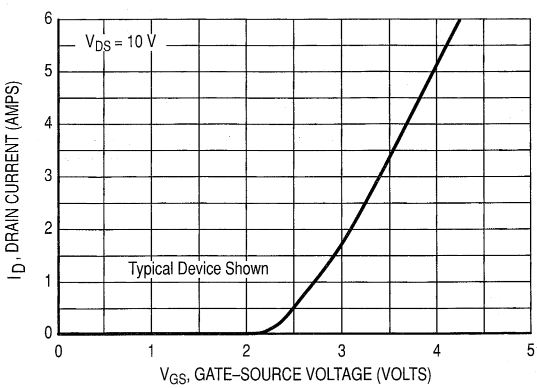


Figure 6. Drain Current versus Gate Voltage

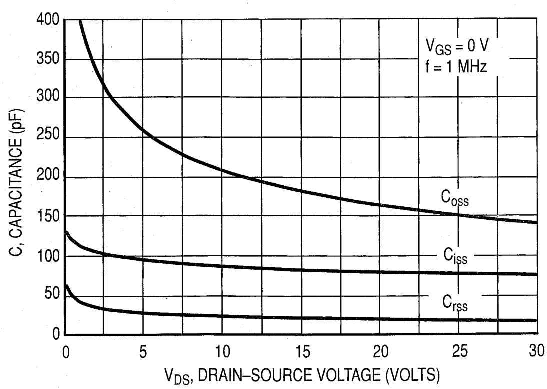


Figure 7. Capacitance versus Voltage

TYPICAL CHARACTERISTICS

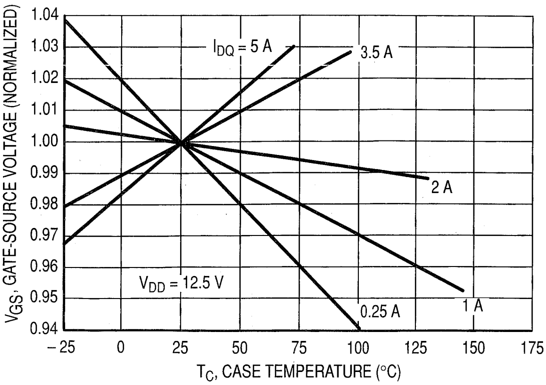


Figure 8. Gate–Source Voltage versus Case Temperature

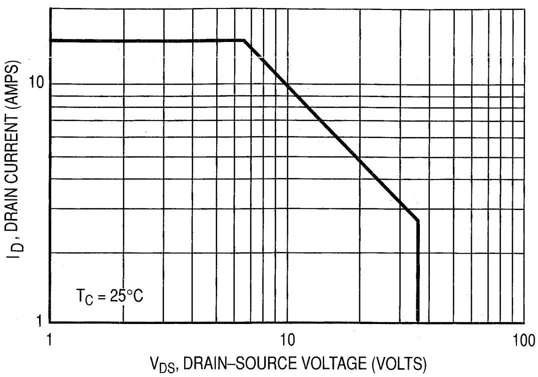
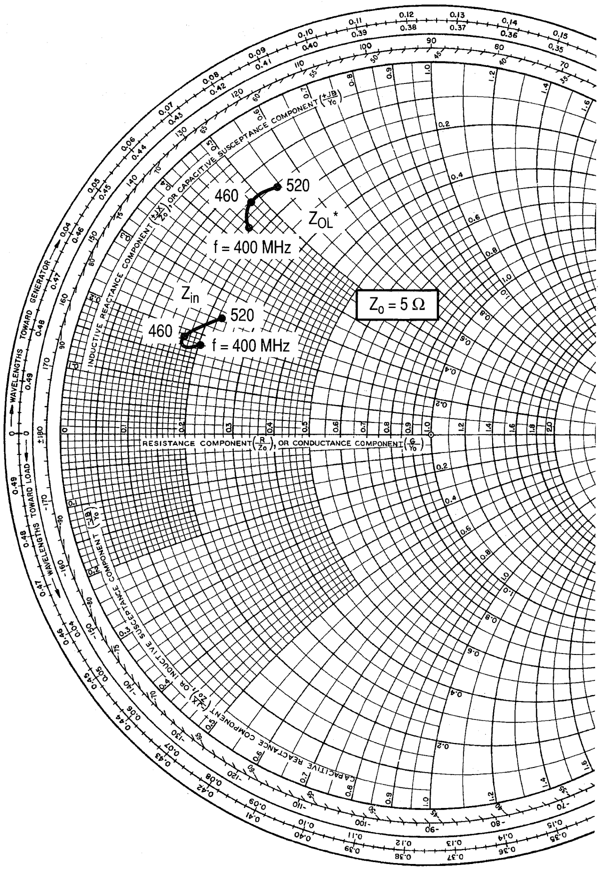


Figure 9. DC Safe Operating Area



V_{DD} = 12.5 V, I_{DQ} = 400 mA, P_{in} = 7.8 W,
Tune for Maximum Output Power

f (MHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
400	1.0 + j0.89	0.87 + j2.1
420	0.90 + j0.83	0.79 + j2.2
440	0.83 + j0.81	0.73 + j2.3
460	0.82 + j0.83	0.71 + j2.4
480	0.87 + j0.90	0.71 + j2.5
500	0.97 + j1.0	0.74 + j2.6
520	1.1 + j1.2	0.80 + j2.7

Z_{in} = Conjugate of source impedance.

Z_{OL}* = Conjugate of the load impedance at given input power, voltage and frequency that produces maximum output power.

Figure 10. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DS} = 12.5 V)

I_D = 100 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
25	0.74	–153	6.9	94	0.039	6	0.87	–169
50	0.74	–164	3.4	82	0.039	– 5	0.89	–174
100	0.77	–168	1.6	67	0.036	–16	0.90	–176
150	0.81	–170	1	56	0.032	– 25	0.92	–178
200	0.85	–171	0.69	46	0.028	– 31	0.93	–179
300	0.90	–174	0.38	32	0.019	– 36	0.96	179
400	0.93	–178	0.24	22	0.013	– 30	0.97	177
450	0.94	–179	0.20	19	0.010	– 22	0.97	175
500	0.95	179	0.17	16	0.008	– 8	0.98	174
600	0.96	176	0.12	13	0.008	27	0.98	172

I_D = 400 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
25	0.88	–163	7.8	94	0.018	7	0.93	–175
50	0.88	–172	3.9	87	0.018	3	0.93	–178
100	0.88	–176	1.9	77	0.018	–1	0.94	–180
150	0.89	–178	1.3	70	0.017	– 2	0.94	179
200	0.89	–179	0.91	63	0.016	–1	0.94	178
300	0.91	180	0.57	51	0.014	3	0.95	177
400	0.92	178	0.39	41	0.012	14	0.96	175
450	0.93	177	0.33	37	0.012	22	0.96	174
500	0.94	176	0.29	33	0.012	29	0.97	173
600	0.95	174	0.22	27	0.014	42	0.97	171

I_D = 1 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
25	0.92	–165	7.8	95	0.013	9	0.94	–177
50	0.91	–173	3.9	88	0.013	6	0.95	–179
100	0.92	–177	1.9	81	0.013	7	0.95	179
150	0.92	–179	1.3	75	0.013	9	0.95	179
200	0.92	180	0.95	69	0.012	12	0.95	178
300	0.93	178	0.61	59	0.012	21	0.96	176
400	0.94	176	0.43	50	0.013	32	0.96	174
450	0.94	175	0.38	46	0.013	37	0.97	174
500	0.94	174	0.33	43	0.014	42	0.97	173
600	0.95	173	0.26	36	0.016	49	0.97	171

I_D = 5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
25	0.94	–164	7.2	95	0.010	10	0.95	–178
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200	0.94	179	0.89	70	0.011	21	0.96	177
300	0.95	177	0.57	61	0.011	31	0.96	176
400	0.95	176	0.42	52	0.013	41	0.97	174
450	0.95	175	0.36	48	0.013	45	0.97	173
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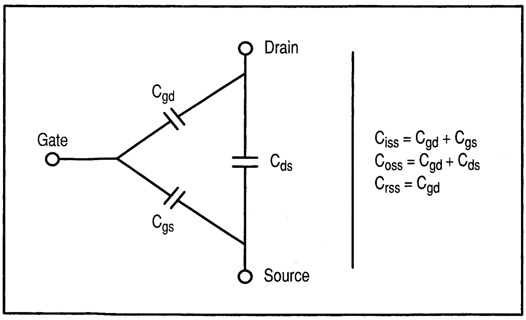

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One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{ds(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{ds(on)}$. For MOSFETs, $V_{ds(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high, on the order of $10^9\ \Omega$, resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating – Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination – The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating must be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection – These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling networks.

Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since the MRF5035 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 6 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. The MRF5035 was characterized at I_{DQ} = 400 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws essentially no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF5035 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 5 is an example of output power variation with gate–source bias voltage with P_{in} held constant. This characteristic is very dependent on frequency and load line.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5035. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Both small–signal S–parameters and large–signal impedances are provided. While the S–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the high gain of the MRF5035 yield a device quite capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Different stabilizing techniques may be required depending on the desired gain and bandwidth of the application. The RF test fixture implements a resistor in shunt with the gate to improve stability. Two port stability analysis with the MRF5035 S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters," for a discussion of two port network theory and stability.

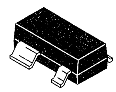
The RF Line
NPN Silicon High-Frequency Transistor

MRF5811LT1

**I_C = 200 mA
LOW NOISE
HIGH–FREQUENCY
TRANSISTOR
NPN SILICON**

Designed for high current, low power amplifiers up to 1.0 GHz.

- Low Noise (2.0 dB @ 500 MHz)
- Low Intermodulation Distortion
- High Gain
- State–of–the–Art Technology
  - Fine Line Geometry
  - Arsenic Emitters
  - Gold Top Metallization
  - Nichrome Thin–Film Ballasting Resistors
- Excellent Dynamic Range
- Fully Characterized
- High Current–Gain Bandwidth Product
- Available in Tape and Reel by Adding T1 Suffix to Part Number. T1 Suffix = 3,000 Units per 8 mm, 7 inch Reel.



**CASE 318A–05, STYLE 1
(SOT–143)**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	18	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	2.5	Vdc
Collector Current — Continuous	I_C	200	mAdc
Thermal Resistance θJC (1)	$R_{\theta JC}$	106	°C/W
Total Device Dissipation @ T_C = 75°C Derate above T_C = 75°C	P_D	0.71 9.4	Watts mW/°C
Storage Junction Temperature Range	T_{stg}	– 55 to +150	°C
Maximum Junction Temperature	T_{Jmax}	150	°C

DEVICE MARKING

MRF5811L = 20

NOTES:
1. Case temperature measured on collector lead immediately adjacent to body of package.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 1.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.5	—	—	Vdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, V_{BE} = 0)	I_{EBO}	—	—	100	µAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	100	µAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	50	—	200	—
DYNAMIC CHARACTERISTICS					
Collector–Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	2.0	—	pF
Collector–Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	1.2	2.0	pF
Current–Gain Bandwidth Product (2) (I_C = 75 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	f_T	—	5.0	—	GHz
FUNCTIONAL TESTS					
Noise Figure (Minimum), Figure 3 (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 500 MHz)	NF_{min}	—	2.0	3.0	dB
Noise Figure (50 Ohm Insertion) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 500 MHz)	$NF_{50\,\Omega}$	—	2.5	—	dB
Power Gain at Optimum Noise Figure, Figure 3 (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 500 MHz)	G_{NF}	—	18.4	—	dB
Insertion Gain (I_C = 50 mAdc, V_{CE} = 6.0 Vdc, f = 500 MHz)	$\lvert S_{21}\rvert^2$	—	14.2	—	dB
Maximum Unilateral Gain (2) (I_C = 50 mAdc, V_{CE} = 6.0 Vdc, f = 500 MHz)	$G_{U\,max}$	—	18	—	dB

NOTES:

1. 300 µs pulse on Tektronix 576 or equivalent.
2. $G_{Umax} = \dfrac{\lvert S_{21}\rvert^2}{(1-\lvert S_{11}\rvert^2)(1-\lvert S_{22}\rvert^2)}$

TYPICAL CHARACTERISTICS

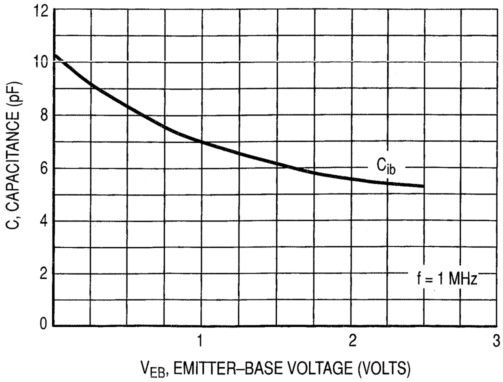


Figure 1. C_{ib} Input Capacitance versus Voltage

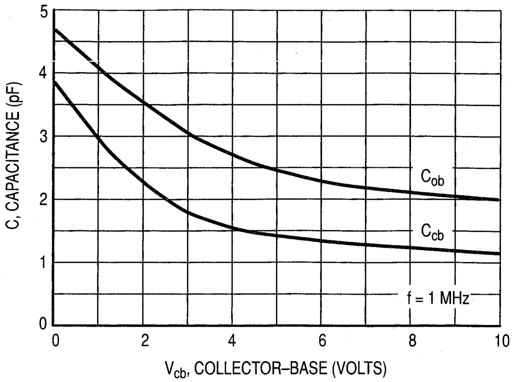


Figure 2. C_{cb}, C_{ob} Collector–Base Capacitance versus Voltage

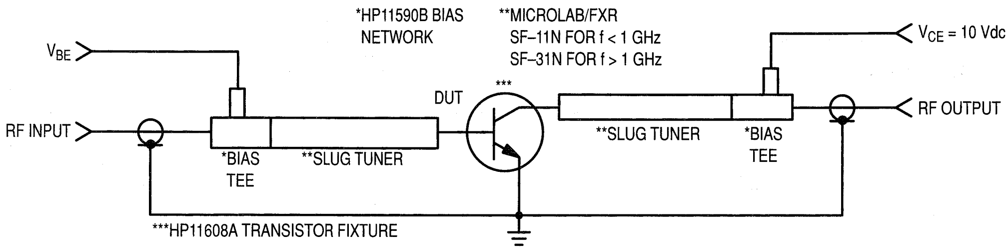


Figure 3. MRF5811L Functional Circuit Schematic

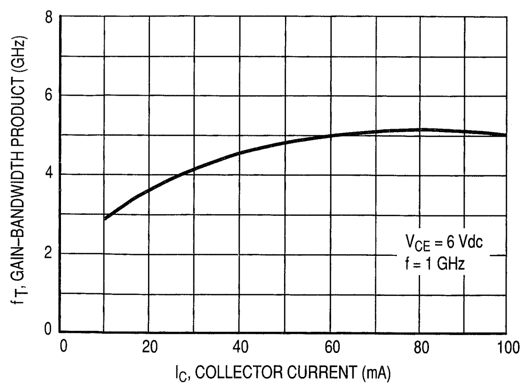


Figure 4. Gain–Bandwidth Product versus Collector Current

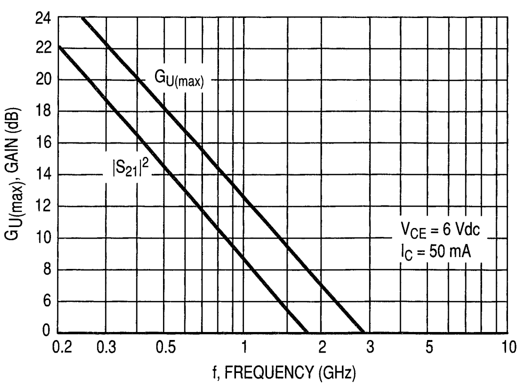


Figure 5. $G_{U(max)}$ Maximum Unilateral Gain, $|S_{21}|^2$ versus Frequency

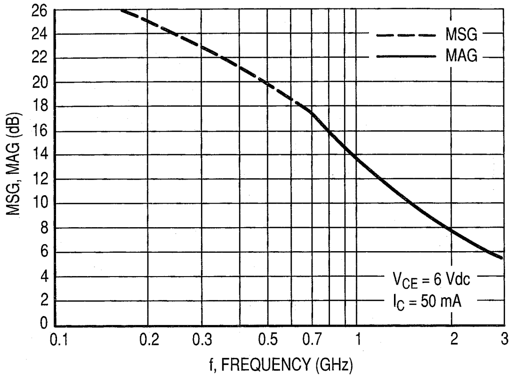


Figure 6. MSG — Maximum Stable Gain, MAG — Maximum Available Gain versus Frequency

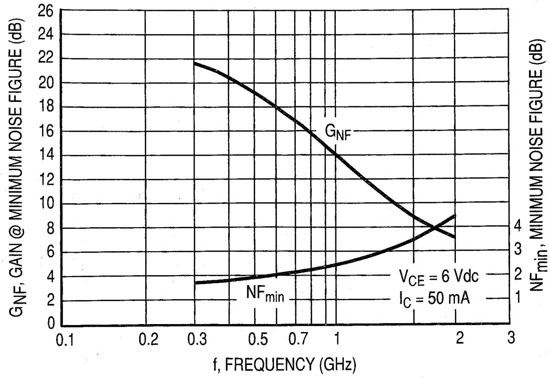


Figure 7. Minimum Noise Figure and Gain @ Minimum Noise Figure versus Frequency

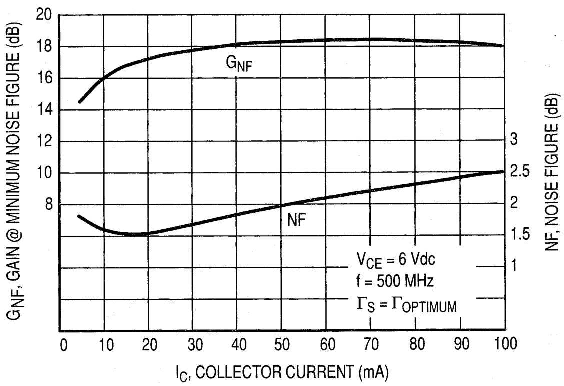


Figure 8. Noise Figure and Gain @ Minimum Noise Figure versus Collector Current

V_{CE} (Vdc)	I_C (mA)	f (MHz)	NF_{min} (dB)	|Gam Opt|	< Gam Opt	Rn
6.0	10	500	1.64	0.49	164	3.5
		1000	2.81	0.68	–173	3.5
	50	500	2.0	0.51	177	3.9
		1000	2.85	0.61	–168	4.7

Table 1. Common Emitter Noise Parameters

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
3.0	25	0.10	0.734	−132	17.54	115	0.045	37	0.544	–89
		0.20	0.765	−157	9.66	99	0.051	30	0.395	–120
		0.30	0.771	−168	6.59	90	0.056	32	0.354	–135
		0.40	0.773	−174	4.98	84	0.060	34	0.340	–143
		0.50	0.768	−180	4.01	81	0.065	38	0.319	–150
		0.60	0.768	176	3.36	76	0.070	41	0.319	–153
		0.70	0.769	173	2.89	73	0.076	43	0.321	–155
		0.80	0.771	170	2.55	69	0.081	44	0.325	–157
		0.90	0.770	167	2.27	65	0.088	46	0.329	–158
		1.00	0.771	165	2.06	62	0.094	47	0.335	–159
		1.50	0.773	152	1.41	47	0.127	49	0.367	–163
		2.00	0.777	140	1.08	33	0.162	48	0.408	–167
		2.50	0.786	129	0.87	22	0.194	45	0.461	–171
		3.00	0.793	118	0.75	12	0.229	40	0.498	–177
		3.50	0.803	108	0.65	4	0.262	35	0.530	177
		4.00	0.812	100	0.58	–2	0.294	30	0.563	169
		4.50	0.811	91	0.53	–7	0.328	24	0.587	162
		5.00	0.816	83	0.50	–11	0.355	18	0.616	154
	50	0.10	0.732	−141	19.19	112	0.039	36	0.542	–105
		0.20	0.764	−163	10.33	97	0.045	34	0.44	–136
		0.30	0.771	−172	7.01	90	0.050	37	0.416	–149
		0.40	0.772	−177	5.29	84	0.056	40	0.408	–156
		0.50	0.768	178	4.26	81	0.062	44	0.392	–162
		0.60	0.768	174	3.57	77	0.069	47	0.392	–165
		0.70	0.769	171	3.08	74	0.076	49	0.393	–167
		0.80	0.770	168	2.71	70	0.083	50	0.395	–169
		0.90	0.769	166	2.42	67	0.090	51	0.396	–170
		1.00	0.769	163	2.19	64	0.098	51	0.399	–172
		1.50	0.769	151	1.51	50	0.135	51	0.414	–176
		2.00	0.771	139	1.17	37	0.171	48	0.434	–180
		2.50	0.778	128	0.96	26	0.204	44	0.467	178
		3.00	0.783	118	0.83	16	0.237	39	0.487	173
		3.50	0.792	108	0.73	7	0.268	33	0.506	168
		4.00	0.802	100	0.66	0	0.297	28	0.53	162
		4.50	0.800	91	0.60	–6	0.328	22	0.546	156
		5.00	0.808	83	0.56	–12	0.353	16	0.572	149
	75	0.10	0.738	−145	19.35	110	0.036	35	0.54	–112
		0.20	0.769	−165	10.31	96	0.042	35	0.458	–142
		0.30	0.774	−173	6.98	89	0.048	39	0.44	–153
		0.40	0.776	−178	5.26	84	0.054	43	0.434	–160
		0.50	0.772	177	4.24	81	0.061	47	0.42	–166
		0.60	0.772	173	3.55	77	0.068	49	0.42	–169
		0.70	0.773	170	3.06	74	0.076	51	0.421	–171
		0.80	0.773	168	2.69	71	0.084	52	0.422	–172
		0.90	0.772	165	2.41	67	0.091	53	0.423	–174
		1.00	0.772	162	2.18	65	0.099	53	0.426	–175
		1.50	0.771	150	1.50	50	0.138	52	0.436	–180
		2.00	0.772	139	1.17	38	0.175	48	0.451	176
		2.50	0.778	128	0.96	27	0.208	44	0.478	174
		3.00	0.783	117	0.83	17	0.241	38	0.493	169
		3.50	0.790	108	0.74	8	0.271	33	0.507	165
		4.00	0.800	99	0.67	1	0.299	27	0.526	158
		4.50	0.798	91	0.62	–5	0.329	21	0.538	153
		5.00	0.806	83	0.57	–11	0.353	15	0.561	147

Table 2. Common Emitter S–Parameters

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
3.0	100	0.10	0.747	–149	18.83	109	0.035	35	0.531	–117
		0.20	0.775	–167	9.95	95	0.041	35	0.463	–145
		0.30	0.781	–175	6.72	88	0.047	40	0.448	–156
		0.40	0.782	–179	5.07	83	0.053	44	0.444	–162
		0.50	0.779	176	4.08	81	0.061	48	0.431	–168
		0.60	0.778	173	3.42	77	0.068	50	0.431	–170
		0.70	0.779	170	2.95	74	0.076	52	0.432	–172
		0.80	0.779	167	2.60	70	0.084	53	0.434	–174
		0.90	0.778	164	2.32	67	0.092	53	0.434	–175
		1.00	0.778	162	2.10	64	0.100	54	0.436	–177
		1.50	0.776	150	1.45	50	0.139	52	0.445	179
		2.00	0.777	138	1.13	38	0.177	48	0.46	175
		2.50	0.782	127	0.93	27	0.209	44	0.485	173
		3.00	0.786	117	0.81	17	0.243	38	0.498	168
		3.50	0.794	107	0.72	9	0.273	32	0.51	163
		4.00	0.802	99	0.65	1	0.301	27	0.528	157
		4.50	0.800	91	0.60	–5	0.330	21	0.539	152
		5.00	0.807	83	0.56	–11	0.354	15	0.56	145
6.0	25	0.10	0.715	–122	19.96	119	0.039	40	0.562	–72
		0.20	0.742	–151	11.31	101	0.046	33	0.364	–98
		0.30	0.748	–164	7.76	92	0.050	33	0.298	–112
		0.40	0.750	–171	5.89	86	0.054	36	0.271	–120
		0.50	0.743	–177	4.73	82	0.058	39	0.24	–127
		0.60	0.744	179	3.97	78	0.063	42	0.237	–131
		0.70	0.746	175	3.42	74	0.068	44	0.239	–134
		0.80	0.748	172	3.00	70	0.074	46	0.243	–135
		0.90	0.747	169	2.68	66	0.079	47	0.248	–137
		1.00	0.748	166	2.42	63	0.085	49	0.255	–139
		1.50	0.753	153	1.64	47	0.115	52	0.3	–144
		2.00	0.760	141	1.25	33	0.148	51	0.352	–150
		2.50	0.772	130	1.00	21	0.180	49	0.417	–155
		3.00	0.783	119	0.84	11	0.215	44	0.464	–163
		3.50	0.795	109	0.72	2	0.249	40	0.505	–170
		4.00	0.807	101	0.63	–5	0.283	34	0.545	–179
		4.50	0.808	92	0.56	–10	0.319	28	0.576	173
		5.00	0.815	84	0.51	–14	0.349	22	0.609	164
	50	0.10	0.706	–131	22.47	116	0.034	40	0.527	–86
		0.20	0.734	–157	12.38	99	0.041	36	0.37	–117
		0.30	0.740	–168	8.44	91	0.046	38	0.325	–132
		0.40	0.742	–174	6.38	86	0.051	42	0.308	–140
		0.50	0.736	–179	5.13	82	0.057	46	0.283	–147
		0.60	0.737	177	4.30	78	0.063	48	0.281	–151
		0.70	0.738	173	3.70	74	0.069	50	0.282	–154
		0.80	0.740	170	3.26	71	0.075	51	0.285	–155
		0.90	0.739	168	2.90	68	0.082	52	0.287	–157
		1.00	0.740	165	2.63	65	0.089	53	0.291	–158
		1.50	0.742	152	1.79	50	0.123	53	0.315	–162
		2.00	0.748	141	1.37	36	0.158	50	0.348	–165
		2.50	0.758	129	1.11	25	0.189	47	0.395	–168
		3.00	0.768	119	0.94	14	0.222	42	0.427	–173
		3.50	0.780	109	0.81	5	0.253	37	0.458	–178
		4.00	0.793	101	0.72	–3	0.283	32	0.491	175
		4.50	0.795	92	0.65	–9	0.316	26	0.518	169
		5.00	0.805	84	0.58	–15	0.343	20	0.552	161

Table 2. Common Emitter S–Parameters (continued)

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
6.0	75	0.10	0.710	–135	22.99	114	0.033	39	0.505	–93
		0.20	0.735	–159	12.49	98	0.039	37	0.367	–123
		0.30	0.741	–169	8.49	90	0.044	40	0.33	–137
		0.40	0.742	–175	6.42	85	0.050	44	0.317	–145
		0.50	0.737	180	5.16	82	0.056	48	0.295	–153
		0.60	0.737	176	4.32	78	0.062	50	0.294	–156
		0.70	0.739	173	3.72	74	0.069	52	0.295	–158
		0.80	0.740	170	3.27	71	0.076	53	0.297	–160
		0.90	0.739	167	2.92	68	0.083	54	0.298	–161
		1.00	0.740	164	2.64	65	0.090	54	0.302	–162
		1.50	0.742	152	1.80	50	0.125	53	0.322	–166
		2.00	0.747	140	1.38	37	0.160	50	0.349	–169
		2.50	0.757	129	1.12	25	0.191	47	0.392	–171
		3.00	0.766	119	0.95	15	0.224	42	0.42	–176
		3.50	0.778	109	0.82	5	0.254	36	0.448	180
		4.00	0.791	100	0.73	–3	0.284	31	0.479	173
		4.50	0.793	92	0.66	–9	0.315	26	0.504	167
		5.00	0.803	84	0.60	–15	0.342	20	0.536	160
	100	0.10	0.718	–138	22.70	112	0.032	38	0.481	–96
		0.20	0.740	–161	12.22	97	0.038	37	0.354	–126
		0.30	0.745	–170	8.28	90	0.043	41	0.321	–140
		0.40	0.746	–176	6.25	84	0.049	45	0.309	–147
		0.50	0.741	179	5.03	81	0.055	49	0.29	–154
		0.60	0.741	175	4.21	77	0.062	51	0.289	–157
		0.70	0.743	172	3.62	74	0.069	53	0.29	–159
		0.80	0.744	169	3.19	70	0.076	54	0.293	–161
		0.90	0.743	166	2.84	67	0.083	54	0.294	–162
		1.00	0.744	164	2.57	64	0.090	55	0.298	–163
		1.50	0.745	151	1.75	49	0.126	54	0.318	–166
		2.00	0.750	140	1.35	36	0.160	51	0.347	–169
		2.50	0.760	129	1.09	25	0.192	47	0.39	–171
		3.00	0.769	118	0.93	14	0.224	42	0.418	–175
		3.50	0.781	109	0.80	5	0.255	37	0.447	180
		4.00	0.793	100	0.71	–3	0.284	31	0.478	173
		4.50	0.794	91	0.64	–9	0.316	26	0.502	167
		5.00	0.804	84	0.58	–15	0.342	20	0.534	160

Table 2. Common Emitter S–Parameters (continued)

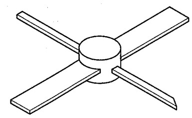
The RF Line
NPN Silicon RF Power Transistor

MRF6401

**0.5 W, 1.0 to 2.0 GHz
RF LINEAR
POWER TRANSISTOR**

The MRF6401 is designed for Class A common emitter, linear power amplifiers in the 1.0–2.0 GHz frequency range. It has been specifically designed for use in Personal Communications Network (PCN) base station and INMARSAT Standard M applications.

- Specified 20 Volts, 1.66 GHz Characteristics:
  Output Power — 0.5 Watts
  Gain — 10 dB Min
  Class A Operation
- Specified 20 Volts, 1.88 GHz Characteristics:
  Output Power — 0.5 Watts
  Gain — 9.0 dB Min
  Class A Operation
- Circuit Board Photomaster Available by Ordering Document MRF6401PHT/D from Motorola Literature Distribution.



**CASE 305C–02, STYLE 1
SOE200–PILL**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	22	Vdc
Collector–Base Voltage	V_{CBO}	45	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.8 0.033	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	30	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

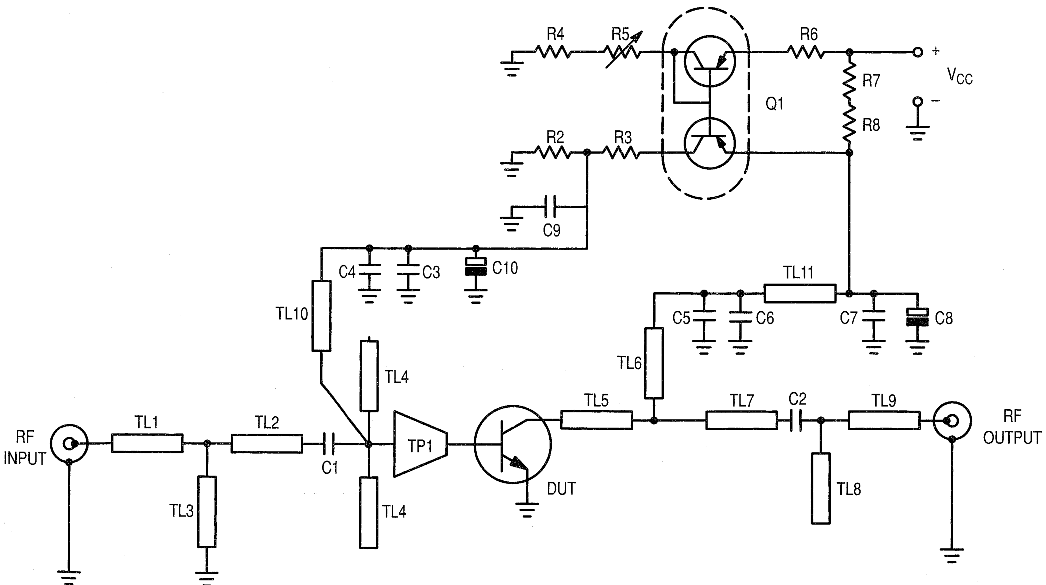
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mAdc, R_B = 75 Ω)	$V_{(BR)CER}$	28	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.25 mAdc)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 1 mAdc)	$V_{(BR)CBO}$	45	—	—	Vdc

(1) Thermal resistance is determined under specified RF operating condition.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 V, I_E = 0, f = 1 MHz)	C_{ob}	—	1.4	—	pF
FUNCTIONAL TESTS (V_{CC} = 20 V, I_{CQ} = 80 mA)					
Common–Emitter Amplifier Power Gain (f = 1660 MHz, P_{out} = 0.5 W) (f = 1880 MHz, P_{out} = 0.5 W)	G_p	 10 9	 11 10	 — —	dB
Load Mismatch (f = 1660 MHz, f = 1880 MHz, P_{out} = 0.5 W, Load VSWR = 20:1, all phase angles at frequency of test)	ψ	No Degradation in Output Power			
Intermodulation Distortion (P_{out} = 0.5 W PEP, f1 = 1659.2 MHz, f2 = 1660 MHz) (P_{out} = 0.5 W PEP, f1 = 1879.2 MHz, f2 = 1880 MHz)	IMD	 –30 –30	 –35 –35	 — —	dBc



C1	1.5 pF, ATC Chip Capacitor 100A	R2	470 Ω, Chip Resistor 0805
C2	3.9 pF, ATC Chip Capacitor 100A	R3	4.7 kΩ, Chip Resistor 0805
C3	56 pF, ATC Chip Capacitor 100A	R4	8.2 kΩ, Chip Resistor 0805
C4, C6, C7, C9	15 nF, Chip Capacitor 0805	R5	5 kΩ, SMD Potentiometer
C5	47 pF, ATC Chip Capacitor 100A	R6	680 Ω, Chip Resistor 0805
C8	4.7 μF, 35 V, Capacitor	R7, R8	7.5 Ω, Chip Resistor 0805
C10	10 μF, 16 V, Capacitor	TL1 to TL11	μStrip Lines; See Photomaster Document, MRF6401PHT/D
C11	100 pF, ATC Chip Capacitor 100A	TP1	μStrip Taper; See Photomaster Document, MRF6401PHT/D
Q1	Transistor, BCV62		

Figure 1. 1600–2000 MHz Broadband Application Amplifier Schematic

TYPICAL CHARACTERISTICS

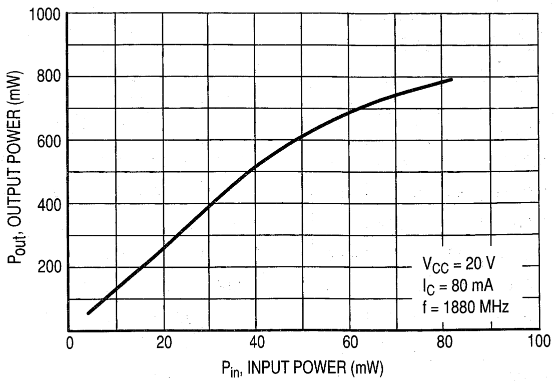


Figure 2. Output Power versus Input Power

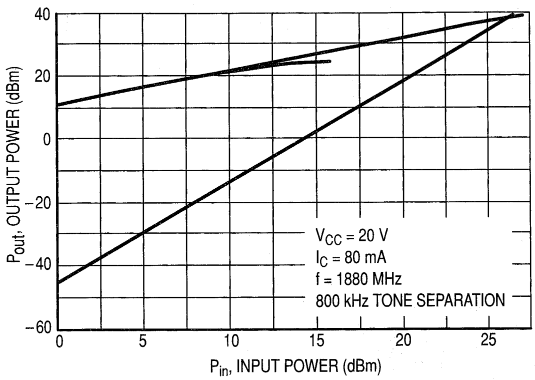


Figure 3. Third Order Intercept

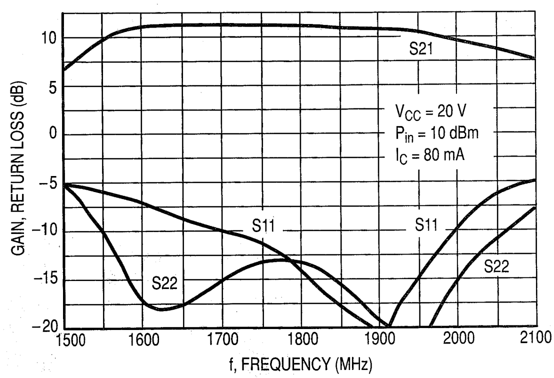


Figure 4. Performance in Broadband Test Fixture

Table 1. Common Emitter S–Parameters

V_{CC} = 20 V, I_C = 80 mA

POLAR S–PARAMETERS IN 50 Ω SYSTEM								
f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
100	0.626	–118	28.4	127	0.0186	45	0.649	–40
200	0.718	–149	17.1	106	0.0230	35	0.434	–49
400	0.754	–171	9.10	88	0.0271	35	0.303	–53
600	0.761	179	6.15	77	0.0312	38	0.272	–56
800	0.762	171	4.65	68	0.0359	42	0.266	–62
1000	0.763	165	3.73	60	0.0409	44	0.271	–68
1200	0.758	159	3.13	52	0.0469	44	0.286	–75
1400	0.753	155	2.60	44	0.0490	46	0.291	–87
1600	0.765	150	2.30	39	0.0574	50	0.288	–93
1800	0.769	144	2.06	32	0.0665	49	0.303	–97
1900	0.768	142	1.98	29	0.0714	48	0.312	–100
2000	0.767	139	1.88	25	0.0756	48	0.322	–103

V_{CC} = 20 V, I_C = 50 mA

POLAR S–PARAMETERS IN 50 Ω SYSTEM								
f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
100	0.618	–113	26.2	130	0.0195	45	0.678	–36
200	0.713	–145	16.2	108	0.0251	34	0.465	–47
400	0.758	–168	8.78	89.2	0.0288	32	0.331	–51
600	0.763	180	5.94	78	0.0323	35	0.297	–55
800	0.761	169	4.49	68	0.0363	39	0.290	–61
1000	0.764	166	3.61	60	0.0415	41	0.294	–68
1200	0.758	160	3.02	52	0.0467	42	0.310	–75
1400	0.757	155	2.52	44.5	0.0486	45	0.313	–87
1600	0.768	150	2.22	39	0.0566	48	0.311	–92
1800	0.772	145	2	32	0.0655	48	0.328	–97
1900	0.770	142	1.91	28	0.0705	47	0.335	–101
2000	0.772	140	1.81	25	0.0745	47	0.345	–104

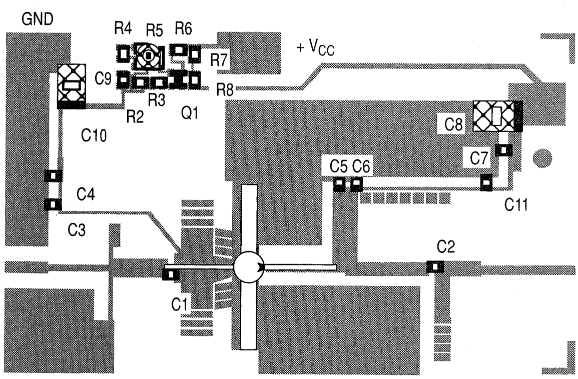


Figure 5. Test Circuit Components Layout

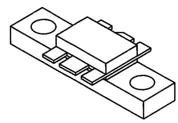
The RF Line
NPN Silicon
RF Power Transistor

MRF6402

4.5 W, 1.88 GHz
RF POWER TRANSISTOR
NPN SILICON

The MRF6402 is designed for 1.8 GHz Personal Communications Network (PCN) base stations applications. It incorporates high value emitter ballast resistors, gold metallizations and offers a high degree of reliability and ruggedness. For ease of design, this transistor has an internally matched input.

- To be used in Class AB for PCN and Cellular Radio Applications
- Specified 26 V, 1.88 GHz Characteristics
  Output Power — 4.5 Watts
  Gain — 10 dB Typ
  Efficiency — 45% Typ
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



CASE 319–07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CER}	40	Vdc
Collector–Base Voltage	V_{CBO}	45	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector–Current — Continuous	I_C	0.7	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.2	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mA, R_{BE} = 75 Ω)	$V_{(BR)CER}$	40	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5 mAdc)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 10 mAdc)	$V_{(BR)CBO}$	40	—	—	Vdc
Collector–Emitter Leakage (V_{CE} = 26 V, R_{BE} = 75 Ω)	I_{CER}	—	—	5	mA

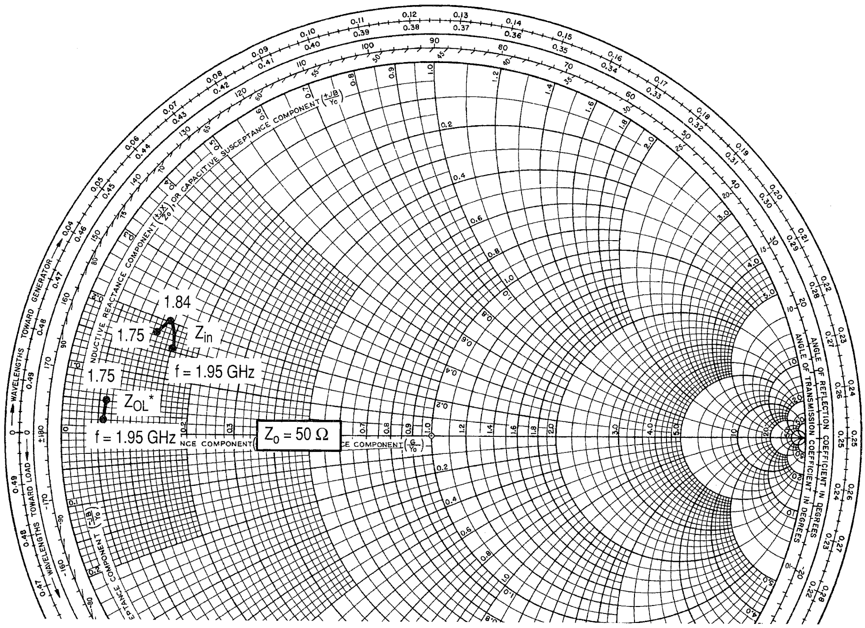
(1) Thermal resistance is determined under specified RF operating condition.

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 20 Vdc)	h_{FE}	50	—	200	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 V, I_E = 0, f = 1 MHz)	C_{ob}	—	6	—	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 V, P_{out} = 4 W, I_{CQ} = 40 mA, f = 1.88 GHz)	G_p	9	10	—	dB
Collector Efficiency (V_{CC} = 26 V, P_{out} = 4 W, f = 1.88 GHz)	η	40	43	—	%
Load Mismatch (V_{CC} = 26 V, P_{out} = 4.5 W, I_{CQ} = 40 mA, f = 1.88 GHz, Load VSWR = 3:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation in Output Power			



f (GHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
1.75	0.12 + j0.18	0.06 + j0.05
1.84	0.13 + j0.2	0.06 + j0.04
1.95	0.15 + j0.16	0.06 + j0.02

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 1. Input and Output Impedances with Circuit Tuned for Maximum Gain @ V_{CE} = 26 V, I_{CQ} = 40 mA, P_{out} = 4.5 W

TYPICAL CHARACTERISTICS

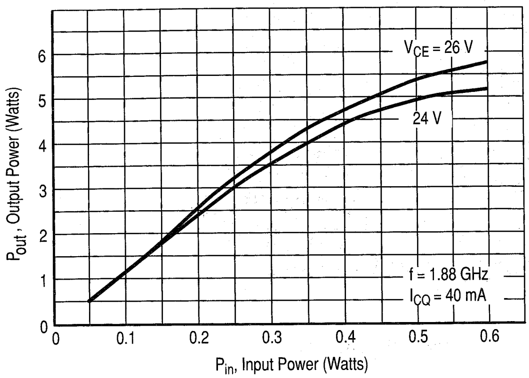


Figure 2. Typical Output Power versus Input Power

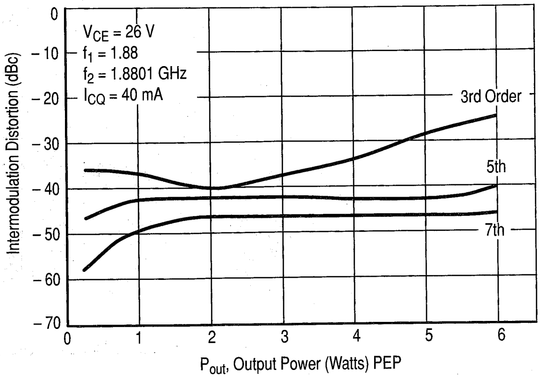
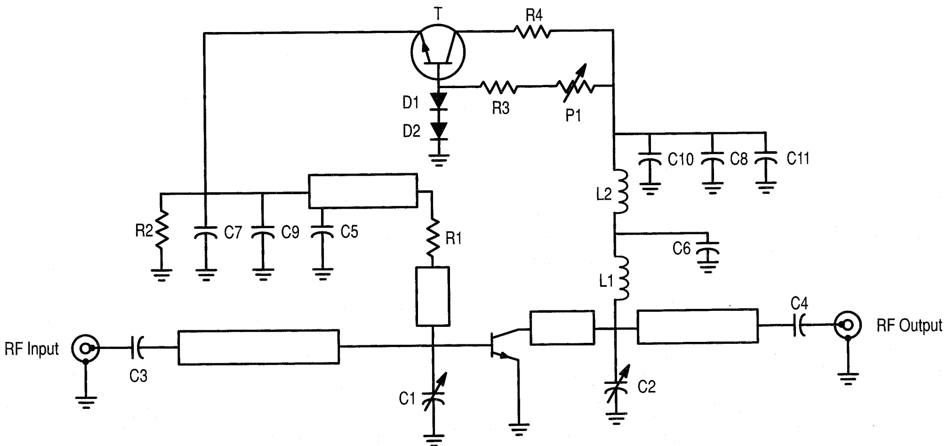


Figure 3. IMD versus Output Power



C1, C2	1 to 5 pF, Trimmer Capacitor, Johanson		L1	2 Turns, Wire 0.5 mm, ID 2 mm
C3, C4	100A, 68 pF, Chip Capacitor, ATC		L2	Ferrite Bead, SMD Fair–Rite
C5, C6	100A, 82 pF, Chip Capacitor, ATC		P1	10 kΩ, Trimmer
C7, C8	15 nF, Chip Capacitor, 0805		R1	2.2 Ω, Chip Resistor, 0805
C9, C10	330 pF, Chip Capacitor, 0805		R2	56 Ω, Chip Resistor, 1206
C11	4.7 µF, 35 V, Capacitor		R3	1.2 kΩ, 1/4 W, 5%, Resistor
D1, D2	Diode, 1N4148		R4	100 Ω, 3 W, Power Resistor
			T	Transistor, BD135

Figure 4. 1.80–1.88 GHz Test Circuit Electrical Schematic

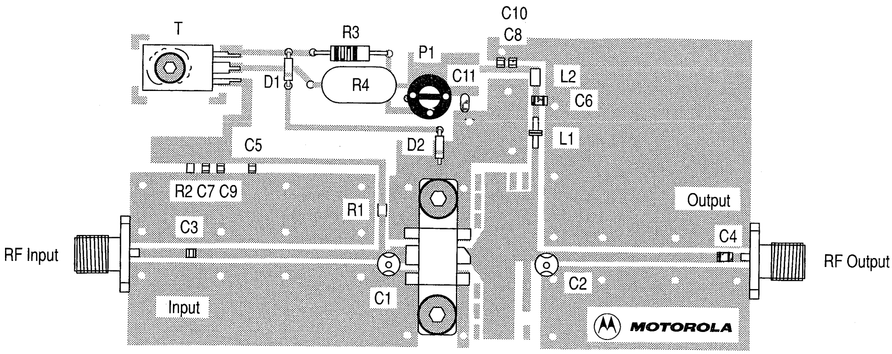


Figure 5. Test Circuit Components View and Parts List

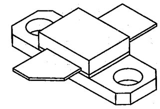
The RF Line
NPN Silicon RF Power Transistor

MRF6404
MRF6404K

The MRF6404 is designed for 26 volts microwave large signal, common emitter, class AB linear amplifier applications operating in the range 1.8 to 2.0 GHz.

- Specified 26 Volts, 1.88 GHz Characteristics
  Output Power — 30 Watts
  Gain — 7.5 dB Min @ 30 Watts
  Efficiency — 38% Min @ 30 Watts
- Characterized with Series Equivalent Large–Signal Parameters from
  1.8 to 2.0 GHz
- To be used in Class AB for DCS1800 and PCS1900/Cellular Radio
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration

30 W, 1.88 GHz
RF POWER TRANSISTOR
NPN SILICON



CASE 395C–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	24	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Collector–Current — Continuous	I_C	10	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	1.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

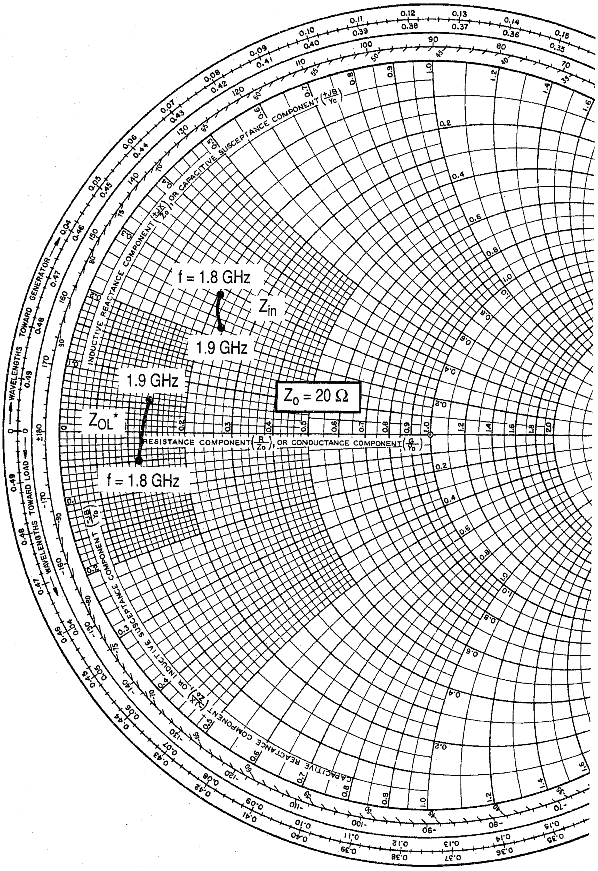
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mA, I_B = 0)	$V_{(BR)CEO}$	24	29	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc)	$V_{(BR)EBO}$	4	5	—	Vdc
Collector–Base Breakdown Voltage (I_C = 50 mAdc)	$V_{(BR)CES}$	60	68	—	Vdc
Collector–Base Breakdown Voltage (I_C = 50 mAdc, R_{BE} = 75 Ω)	$V_{(BR)CER}$	40	56	—	Vdc
Collector Cutoff Current (V_{CE} = 30 V, V_{BE} = 0)	I_{CES}	—	—	10	mA
ON CHARACTERISTICS					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	50	120	—

(1) Thermal resistance is determined under specified RF operating condition.

REV 2

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 V, I_E = 0, f = 1 MHz) For information only. This part is collector matched.	C_{ob}	30	38	—	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 V, P_{out} = 30 W, I_{CQ} = 150 mA, f = 1.88 GHz)	G_{pe}	7.5	8.5	—	dB
Common–Emitter Amplifier Power Gain (V_{CC} = 26 V, P_{out} = 28 W, I_{CQ} = 150 mA) (f = 1.99 GHz)	G_{pe}	7	8	—	dB
Collector Efficiency	η				%
(V_{CC} = 26 V, P_{out} = 30 W, f = 1.88 GHz)		38	43	—	
(V_{CC} = 26 V, P_{out} = 28 W, f = 1.99 GHz)		35	40	—	
Output Power at 1 dBc	P_{1dBc}				Watts
(V_{CC} = 26 V, f = 1.88 GHz)		30	35	—	
(V_{CC} = 26 V, f = 1.99 GHz)		28	33	—	
Output Mismatch Stress: VSWR = 3:1 (all phase angles) (V_{CC} = 26 Vdc, P_{out} = 25 W, I_{CQ} = 150 mA, f = 1.88 GHz)	Ψ	No Degradation in Output Power			



DCS EVALUATION

f (GHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
1.8	4.3 + j6.1	2.7 – j1.0
1.85	4.6 + j5.3	2.9 + j0.3
1.9	4.8 + j5.0	3.0 + j1.2

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 1. Input and Output Impedances with Circuit Tuned for Maximum Gain @ V_{CC} = 26 V, I_{CQ} = 150 mA, P_{out} = 30 W

TYPICAL CHARACTERISTICS

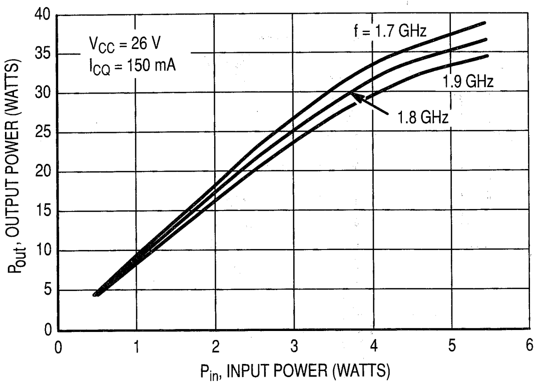


Figure 2. Output Power versus Input Power

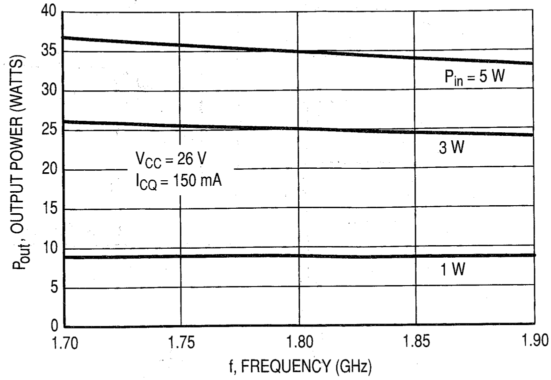


Figure 3. Output Power versus Frequency

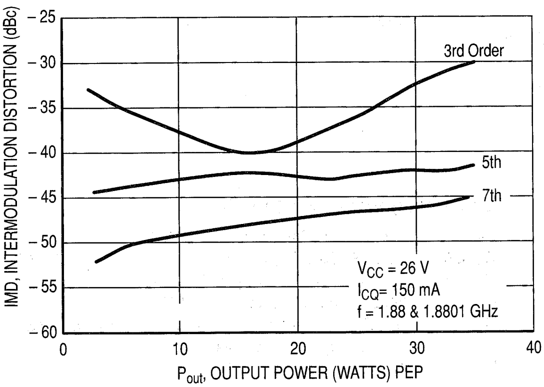


Figure 4. Intermodulation versus Output Power

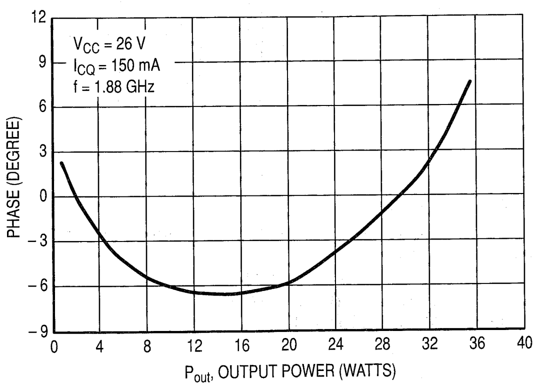
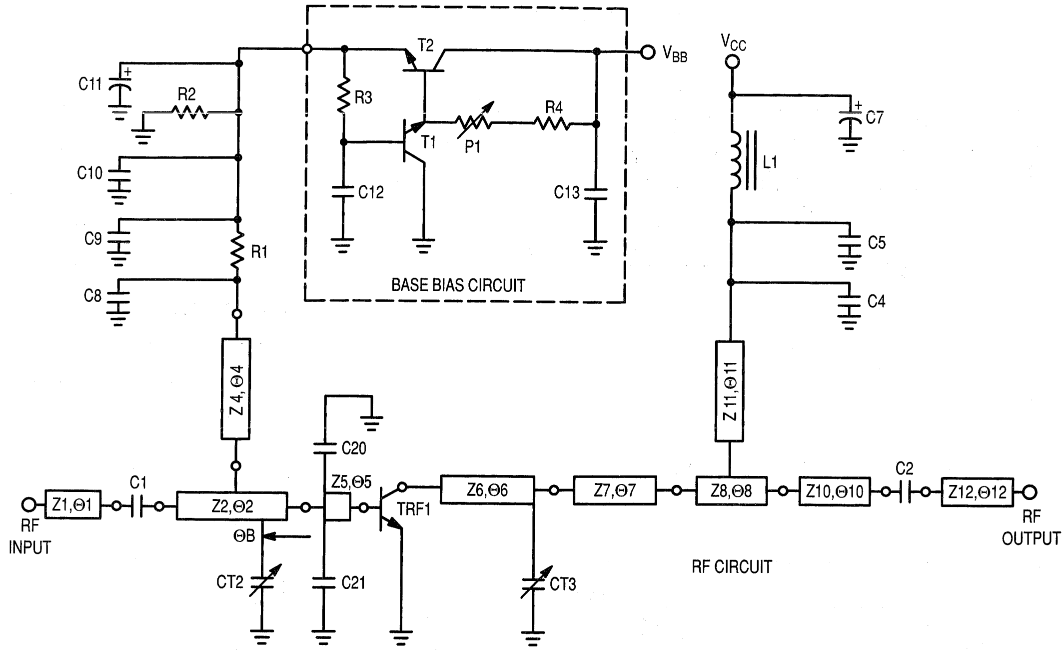


Figure 5. AM/PM Conversion



Base Bias Circuit

C12, C13	15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
P1	1 KΩ, Trimmer
R3	47 Ω, Chip Resistor, 0805
R4	330 Ω, Chip Resistor, 0805
T1,T2	Motorola MJD 31C

Decoupling Base Bias Circuit

C4	68 pF, Chip Capacitor, ATC 100A
C5, C9	330 pF, Chip Capacitor, Vitramon (0805 A331 JXB)
C7, C11	4.7 µF, 63 V, Electrolytic Capacitor
C8	68 pF, Chip Capacitor, ATC 100A
C10	15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
R1	1.5 Ω, Chip Resistor, 0805
R2	56 Ω, Chip Resistor, 1206

RF Circuit

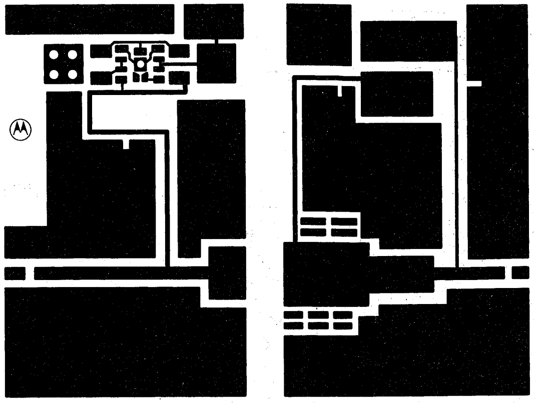
C1, C2	68 pF, Chip Capacitor, ATC 100A
C20, C21	1.3 pF, Chip Capacitor, ATC 100A
CT2	Trimmer Capacitor, Gigatrim, Ref 37281
CT3	Trimmer Capacitor, Gigatrim, Ref 37291
TRF1	MRF6404

PC Board Material:
ε_r = 2.55, H = 0.508 mm, T = 0.035 mm

All Electrical Lengths Are Referenced from λg @ f = 1.9 GHz

Z1 : 50 Ω	Θ1 : 10°
Z2 : 50 Ω	Θ2 : 74.5° ΘB : 16.5°
Z4 : 74 Ω	Θ4 : 68°
Z5 : 12.8 Ω	Θ5 : 21°
Z6 : 10.4 Ω	Θ6 : 49.5°
Z7 : 18 Ω	Θ7 : 36.5°
Z8 : 45 Ω	Θ8 : 20°
Z10 : 50 Ω	Θ10 : 10°
Z11 : 74 Ω	Θ11 : 74.5°
Z12 : 50 Ω	Θ12 : 10°

Figure 6. 1.80–1.88 GHz Test Circuit Electrical Schematic and Components List



(Not to Scale)

Teflon® Glass 0.5 mm – Double Side 35 µm Cu.

Figure 7. 1.80–1.88 GHz PCN Test Circuit Photomaster

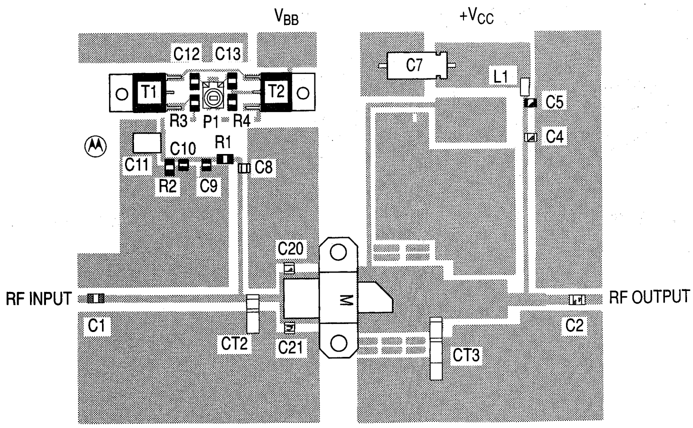
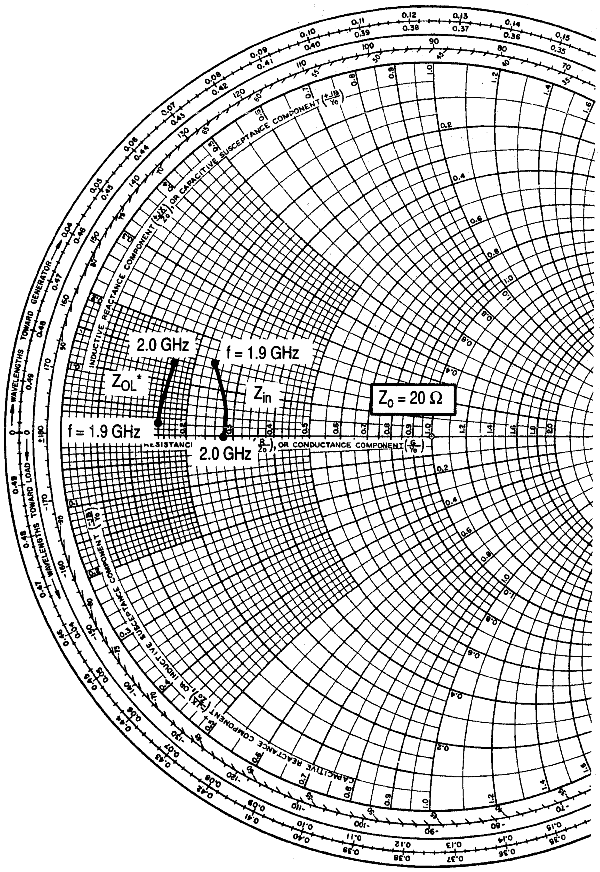


Figure 8. 1.80–1.88 GHz PCN Test Circuit Components Layout



PCS EVALUATION

f (GHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
1.90	4.9 + j3.0	3.2 + j0.5
1.93	5.4 + j2.5	3.3 + j1.2
1.97	5.6 + j1.4	3.4 + j1.5
2.00	5.4 – j0.2	3.6 + j2.5

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 9. Input and Output Impedances with Circuit Tuned for Maximum Gain @ V_{CC} = 26 V, I_{CQ} = 150 mA, P_{out} = 28 W

TYPICAL CHARACTERISTICS

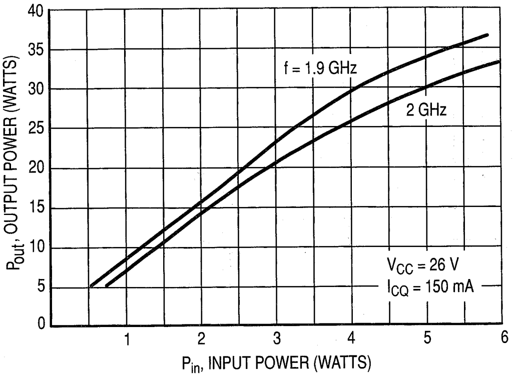


Figure 10. Output Power versus Input Power

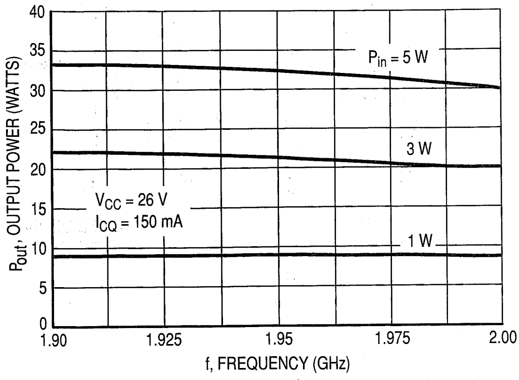


Figure 11. Output Power versus Frequency

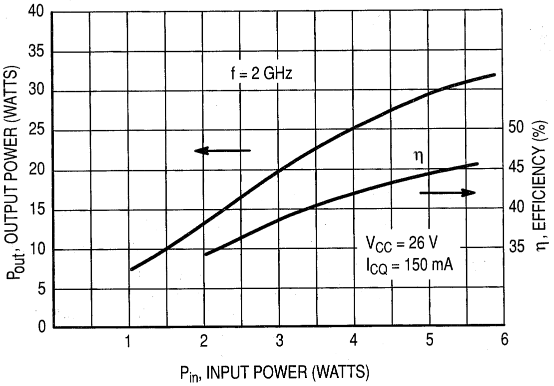


Figure 12. Output Power and Efficiency versus Input Power

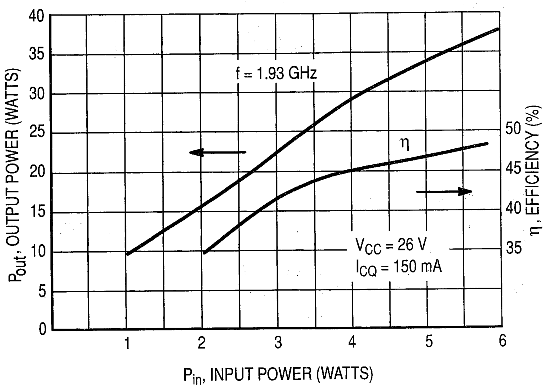


Figure 13. Output Power and Efficiency versus Input Power

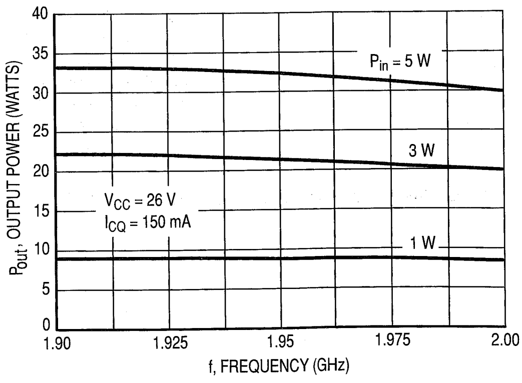
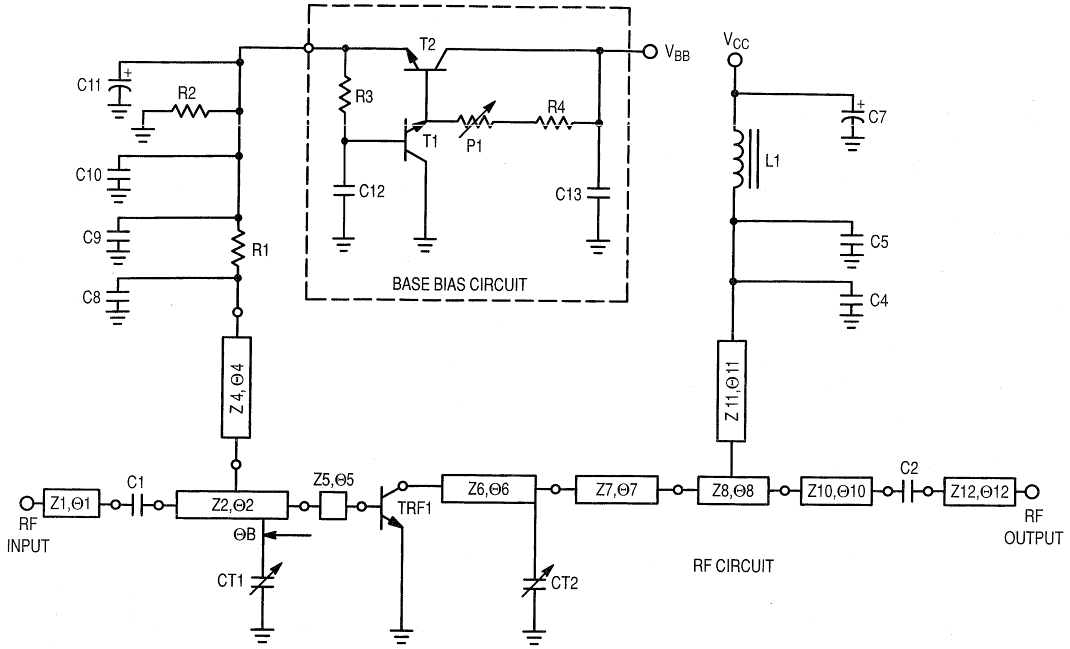


Figure 14. Output Power versus Frequency



Base Bias Circuit

C12, C13	15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
P1	1 KΩ, Trimmer
R3	47 Ω, Chip Resistor, 0805
R4	330 Ω, Chip Resistor, 0805
T1,T2	Motorola MJD 31C

Decoupling Base Bias Circuit

C4	68 pF, Chip Capacitor, ATC 100A
C5, C9	330 pF, Chip Capacitor, Vitramon (0805 A331 JXB)
C7, C11	4.7 μF, 63 V, Electrolytic Capacitor
C8	68 pF, Chip Capacitor, ATC 100A
C10	15 nF, Chip Capacitor, Vitramon (0805 A153 JXB)
R1	1.2 Ω, Chip Resistor, 0805
R2	56 Ω, Chip Resistor, 1206

RF Circuit

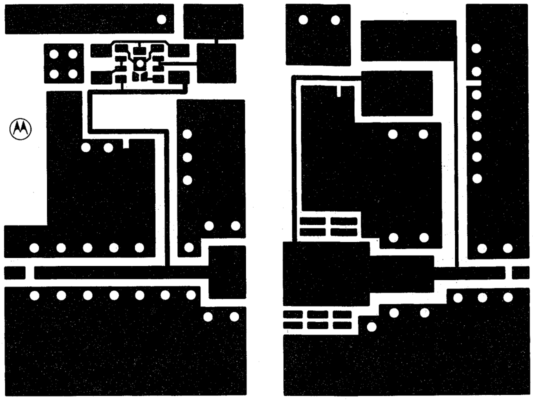
C1, C2	68 pF, Chip Capacitor, ATC 100A
C20, C21	1.3 pF, Chip Capacitor, ATC 100A
CT1, CT2	Trimmer Capacitor, Gigatrim, Ref 37271
TRF1	MRF6404

PC Board Material:
ε_r = 2.55, H = 0.508 mm, T = 0.035 mm

All Electrical Lengths Are Referenced from λg @ f = 1.9 GHz

Z1 : 50 Ω	Θ1 : 10°	
Z2 : 50 Ω	Θ2 : 74.5°	ΘB : 16.5°
Z4 : 74 Ω	Θ4 : 68°	
Z5 : 12.8 Ω	Θ5 : 21°	
Z6 : 10.4 Ω	Θ6 : 49.5°	
Z7 : 18 Ω	Θ7 : 36.5°	
Z8 : 45 Ω	Θ8 : 20°	
Z10 : 50 Ω	Θ10 : 10°	
Z11 : 74 Ω	Θ11 : 60°	
Z12 : 50 Ω	Θ12 : 10°	

Figure 15. 1.9–2.0 GHz Test Circuit Electrical Schematic and Components List



Teflon® Glass 0.5 mm – Double Side 35 µm Cu.

Figure 16. 1.9–2.0 GHz Test Circuit Photomaster

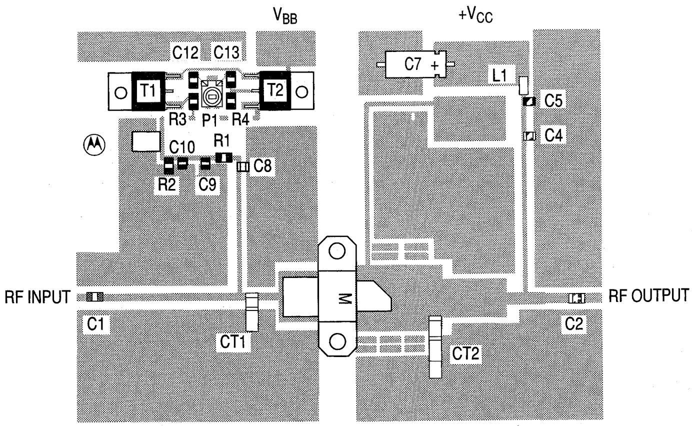


Figure 17. 1.9–2.0 GHz Test Circuit Components Layout

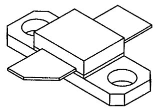
MRF6408

The RF Line
NPN Silicon
RF Power Transistor

Designed for PCN and PCS base station applications, the MRF6408 incorporates high value emitter ballast resistors, gold metallizations and offers a high degree of reliability and ruggedness.

- To be used in class AB for PCN–PCS / Cellular Radio
- Specified 26 Volts, 1.88 GHz Characteristics
  Output Power = 12 Watts CW
  Typical Gain = 8.8 dB
  Typical Efficiency = 42%
- Specified 26 Volts, 1.99 GHz Characteristics
  Output Power = 12 Watts CW
  Typical Gain = 8.3 dB
  Typical Efficiency = 39%
- Circuit Board Photomaster Available by Ordering Document MRF6408PHT/D from Motorola Literature Distribution.

**12 W, 2.0 GHz
RF POWER TRANSISTOR
NPN SILICON**



CASE 395C–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	24	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Collector–Current — Continuous	I_C	5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 0.35	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	2.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	24	30	—	Vdc
Emitter–Base Breakdown Voltage (I_B = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	5	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	64	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	6	mA

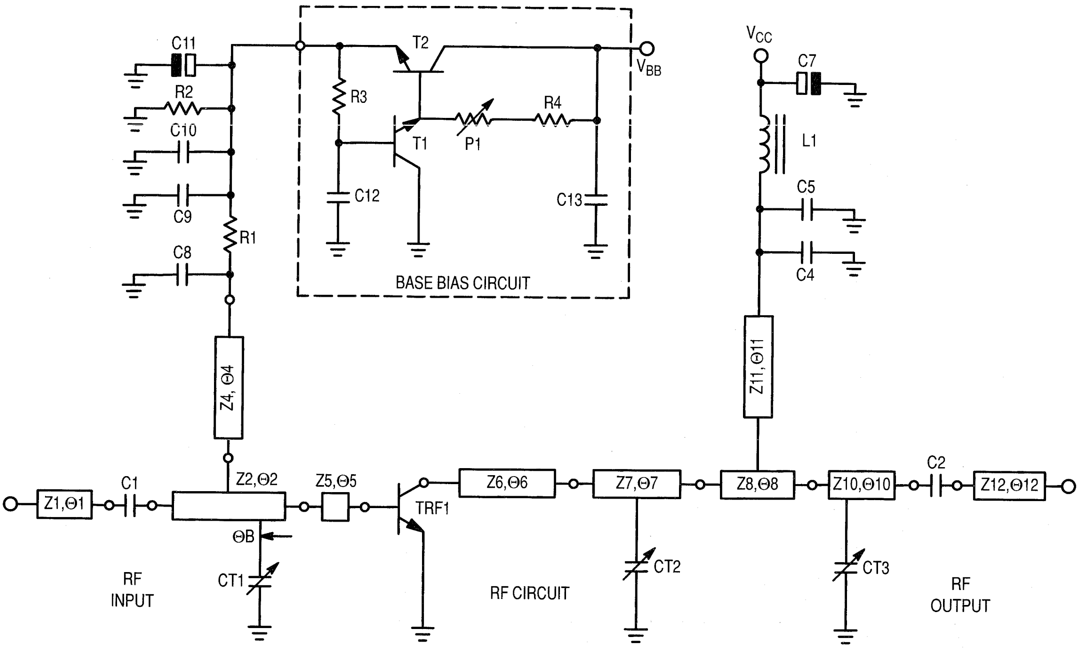
(1) Thermal resistance is determined under specified RF operating condition.

REV 2

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	35	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (2) (V_{CB} = 26 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	18	—	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 12 W (CW), I_{CQ} = 100 mA, f = 1.88 GHz)	G_{pe}	7.8	8.8	—	dB
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 12 W (CW), I_{CQ} = 100 mA, f = 1.99 GHz)	G_{pe}	7.5	8.3	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 12 W (CW), I_{CQ} = 100 mA, f = 1.88 GHz)	η	37	42	—	%
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 12 W (CW), I_{CQ} = 100 mA, f = 1.99 GHz)	η	34	39	—	%
Output Power at 1 dB Compression Point (V_{CC} = 26 Vdc, I_{CQ} = 100 mA, f = 1.88 GHz)	P @ 1 dB	15	—	—	W
Output Power at 1 dB Compression Point (V_{CC} = 26 Vdc, I_{CQ} = 100 mA, f = 1.99 GHz)	P @ 1 dB	14	—	—	W
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 12 W (PEP), I_{CQ} = 100 mA, f1 = 1880 MHz, f2 = 1880.1 MHz)	IMD	—	−35	−30	dBc
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 12 W (PEP), I_{CQ} = 100 mA, f1 = 1990 MHz, f2 = 1990.1 MHz)	IMD	—	−35	−30	dBc
Load Mismatch (V_{CC} = 26 Vdc, P_{out} = 12 W (CW), I_{CQ} = 100 mA, f = 1.99 GHz, Load VSWR = 3:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			

(2) For information only. This part is collector matched.



C4	47 pF, Chip Capacitor, ATC100A	P1	1 kΩ, Trimmer Resistor
C5, C9	330 pF, 0805 Chip Capacitor, Vitramon JXB	R1	1 Ω, 1206 Chip Resistor
C7	4.7 µF 63 V, Electrolytic Capacitor	R2	56 Ω, 1206 Chip Resistor
C10, C12, C13	15 nF, 0805 Chip Capacitor, Vitramon JXB	R3	47 Ω, 0805 Chip Resistor
C11	100 µF 16 V, Electrolytic Capacitor	R4	330 Ω, 0805 Chip Resistor
L1	SMD Ferrite Bead, Fair–Rite 2743021447	T1, T2	MJD31C, NPN Transistor, Motorola

Test Circuits Bias and Decoupling Components List

C1, C2	33 pF, Chip Capacitor, ATC100A
CT1	Trimmer Capacitor, Gigatrim 37281
CT2	Trimmer Capacitor, Gigatrim 37281
CT3	Trimmer Capacitor, Gigatrim 37281
Z1	50 Ω Θ1 = 10°
Z2	50 Ω Θ2 = 74.5° ΘB = 16.5°
Z4	74 Ω Θ4 = 68°
Z5	12.8 Ω Θ5 = 21°
Z6	10.4 Ω Θ6 = 49.5°
Z7	18 Ω Θ7 = 36.5°
Z8	45 Ω Θ8 = 20°
Z10	50 Ω Θ10 = 10°
Z11	74 Ω Θ11 = 74.5°
Z12	50 Ω Θ12 = 10°

1.88 GHz Test Circuit RF Components List

C1, C2	33 pF, Chip Capacitor, ATC100A
CT1	Trimmer Capacitor, Gigatrim 37281
CT2	Trimmer Capacitor, Gigatrim 37281
CT3	Not Used
Z1	50 Ω Θ1 = 10°
Z2	50 Ω Θ2 = 74.5° ΘB = 16.5°
Z4	74 Ω Θ4 = 68°
Z5	12.8 Ω Θ5 = 21°
Z6	10.4 Ω Θ6 = 49.5°
Z7	18 Ω Θ7 = 36.5°
Z8	45 Ω Θ8 = 20°
Z10	50 Ω Θ10 = 10°
Z11	74 Ω Θ11 = 60°
Z12	50 Ω Θ12 = 10°

1.99 GHz Test Circuit RF Components List

Electrical Lengths are referenced from I_G @ f = 1.9 GHz

Figure 1. Test Circuits Schematic

TYPICAL CHARACTERISTICS

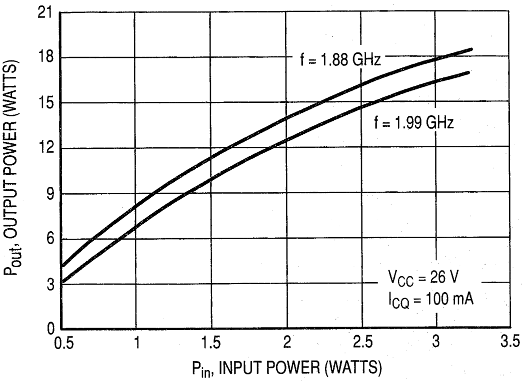


Figure 2. Output Power versus Input Power (CW)

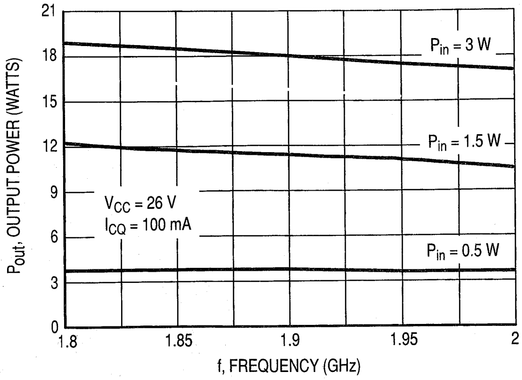


Figure 3. Output Power (CW) versus Frequency

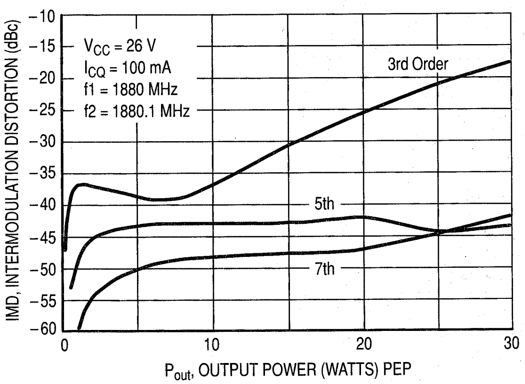


Figure 4. Intermodulation Distortion versus Output Power

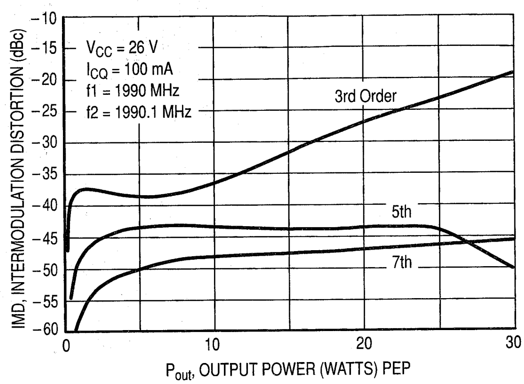


Figure 5. Intermodulation Distortion versus Output Power

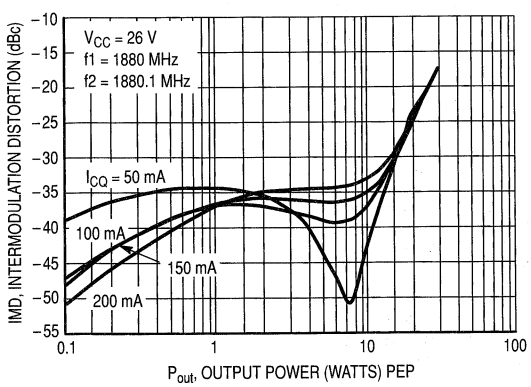


Figure 6. Intermodulation Distortion versus Output Power

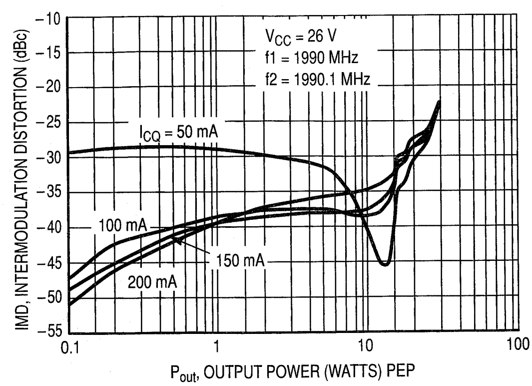
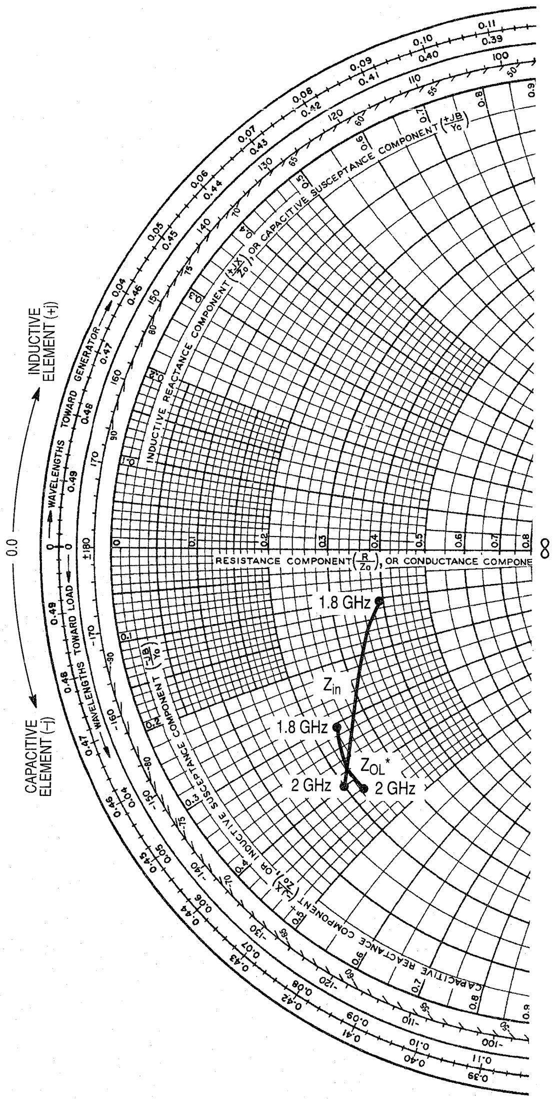


Figure 7. Intermodulation Distortion versus Output Power



Normalized to 20 Ω

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
1800	7.5 – j2.5	5.1 – j4.5
1900	6.5 – j4	4.6 – j5.1
2000	4 – j5.9	4.1 – j6.4

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage current and frequency.

Figure 8. Input and Output Impedances with Circuit Tuned for Maximum Gain @ V_{CC} = 26 V, I_{CQ} = 100 mA, P_{out} = 12 W (CW)

V_{CE} (Vdc)	I_C (Adc)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\lvert S_{11} \rvert$	$\angle \phi$	$\lvert S_{21} \rvert$	$\angle \phi$	$\lvert S_{12} \rvert$	$\angle \phi$	$\lvert S_{22} \rvert$	$\angle \phi$
26	1.0	1000	0.987	176	0.502	−179	0.012	136	0.898	172
		1050	0.986	176	0.478	−177	0.012	136	0.886	172
		1100	0.984	175	0.570	179	0.014	138	0.874	172
		1150	0.982	175	0.553	−177	0.014	137	0.859	171
		1200	0.979	174	0.623	176	0.017	140	0.844	171
		1250	0.974	173	0.660	177	0.017	140	0.826	171
		1300	0.970	172	0.757	176	0.021	138	0.807	171
		1350	0.962	171	0.790	170	0.021	138	0.785	171
		1400	0.950	170	0.932	169	0.025	132	0.760	171
		1450	0.932	169	0.996	161	0.028	131	0.727	172
		1500	0.899	167	1.272	154	0.031	123	0.690	173
		1550	0.845	165	1.407	145	0.035	113	0.649	177
		1600	0.761	165	1.587	132	0.041	100	0.628	−176
		1650	0.670	170	1.763	109	0.041	076	0.672	−168
		1700	0.667	−179	1.671	092	0.039	055	0.776	−166
		1750	0.746	−173	1.390	069	0.030	035	0.861	−168
		1800	0.823	−173	1.184	061	0.024	013	0.897	−172
		1850	0.875	−174	0.901	046	0.018	001	0.911	−175
		1900	0.907	−176	0.755	044	0.015	−012	0.909	−177
		1950	0.928	−177	0.614	038	0.013	−022	0.921	−179
		2000	0.941	−178	0.484	036	0.010	−037	0.901	−179

Table 1. Small Signal S–Parameters

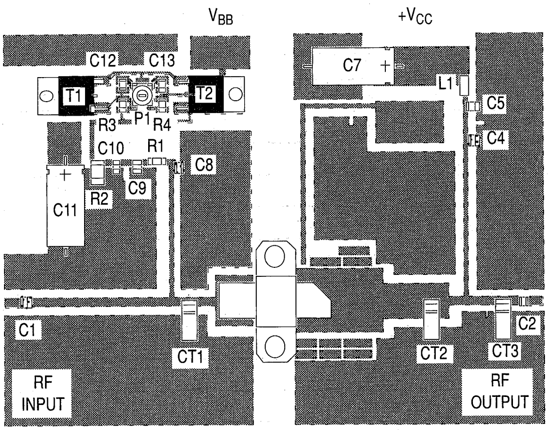


Figure 9. 1.88 GHz Test Circuit Components Layout

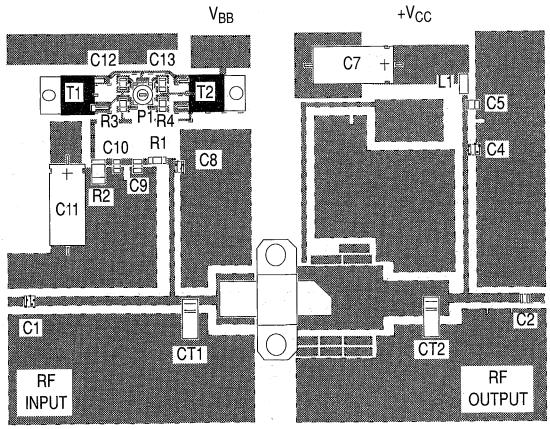


Figure 10. 1.99 GHz Test Circuit Components Layout

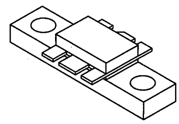
The RF Line
NPN Silicon
RF Power Transistor

MRF6409

The MRF6409 is designed for GSM base stations applications. It incorporates high value emitter ballast resistors, gold metallizations and offers a high degree of reliability and ruggedness.

- To be used in Class AB
- Specified 26 Volts, 960 MHz Characteristics
  Output Power — 20 Watts CW
  Gain — 11 dB Typ
  Efficiency — 60% Typ

20 W, 960 MHz
RF POWER TRANSISTOR
NPN SILICON



CASE 319–07, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	24	Vdc
Collector–Emitter Voltage	V_{CES}	55	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current — Continuous	I_C	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	45 0.26	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	3.8	°C/W

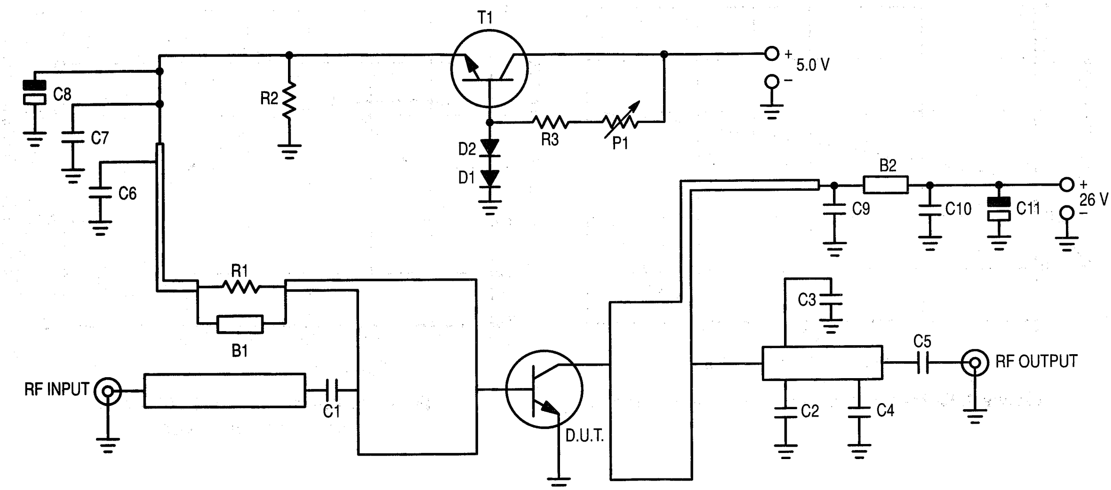
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	24	30	—	Vdc
Emitter–Base Breakdown Voltage (I_B = 5.0 mAdc, I_C =0)	$V_{(BR)EBO}$	4.0	5.0	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	60	—	Vdc
Collector–Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	6.0	mA

(1) Thermal resistance is determined under specified RF operating condition.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	35	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	18	—	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 20 W (CW), I_{CQ} = 50 mA, f = 960 MHz)	G_{pe}	10	11	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 20 W (CW), I_{CQ} = 50 mA, f = 960 MHz)	η	50	60	—	%
Load Mismatch (V_{CC} = 26 Vdc, P_{out} = 15 W (CW), I_{CQ} = 50 mA, f = 960 MHz, Load VSWR = 3:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation in Output Power			



B1, B2	Ferrite Bead	C11	4.7 µF, 50 V, Tantalum Capacitor
C1	3.3 pF, Chip Capacitor, High Q	D1, D2	Diode BAS16 Type or Equivalent
C2, C3	4.7 pF, Chip Capacitor, High Q	P1	1.0 kΩ, Trimmer
C4	2.2 pF, Chip Capacitor, High Q	R1	3.3 Ω, Chip Resistor
C5	82 pF, Chip Capacitor, High Q	R2	68 Ω, Chip Resistor
C6, C9	330 pF, Chip Capacitor, High Q	R3	2.2 kΩ, Resistor
C7, C10	0.1 µF, Chip Capacitor	T1	NPN Transistor
C8	22 µF, 16 V, Tantalum Capacitor	Board	Glass Teflon®, ε_r = 2.55, H = 1/50 inch

Figure 1. Test Circuit Electrical Schematic

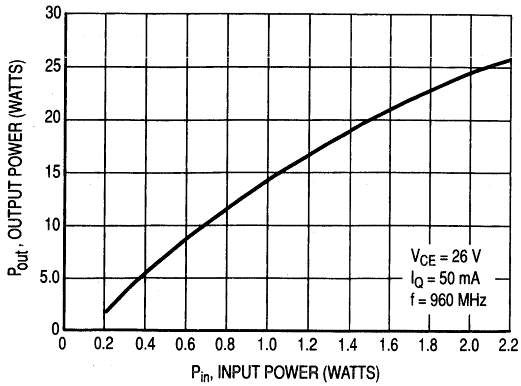


Figure 2. Output Power versus Input Power (CW)

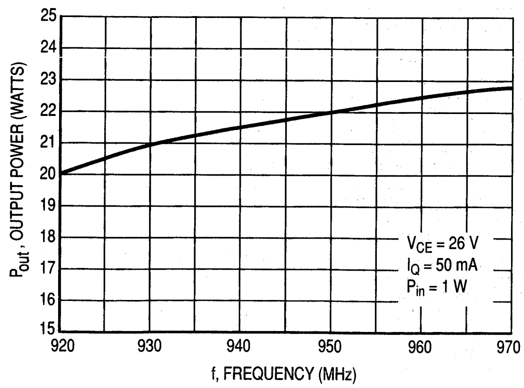


Figure 3. Output Power versus Frequency (CW)

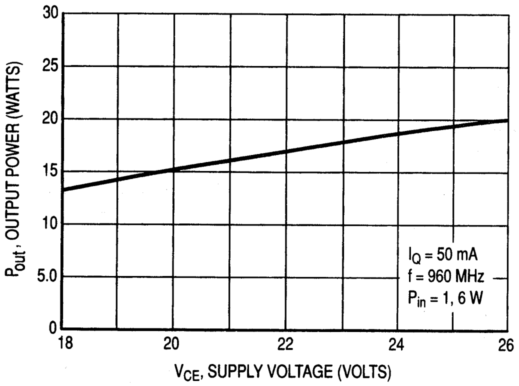


Figure 4. Output Power versus Supply Voltage (CW)

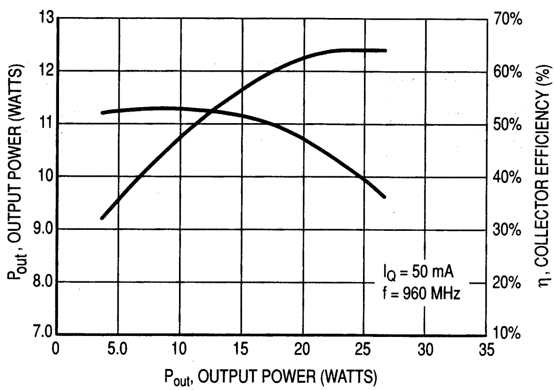


Figure 5. Power Gain and Efficiency versus Output Power

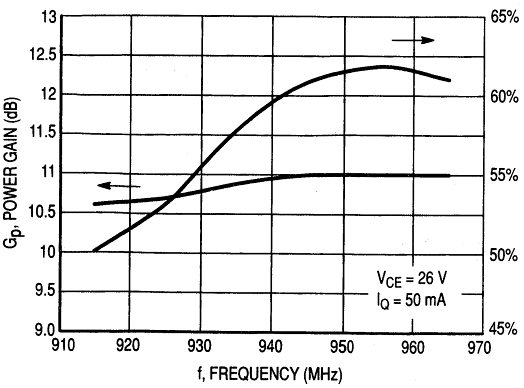


Figure 6. Typical Broadband Performances

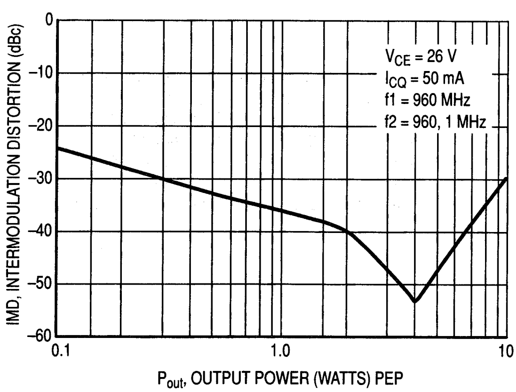
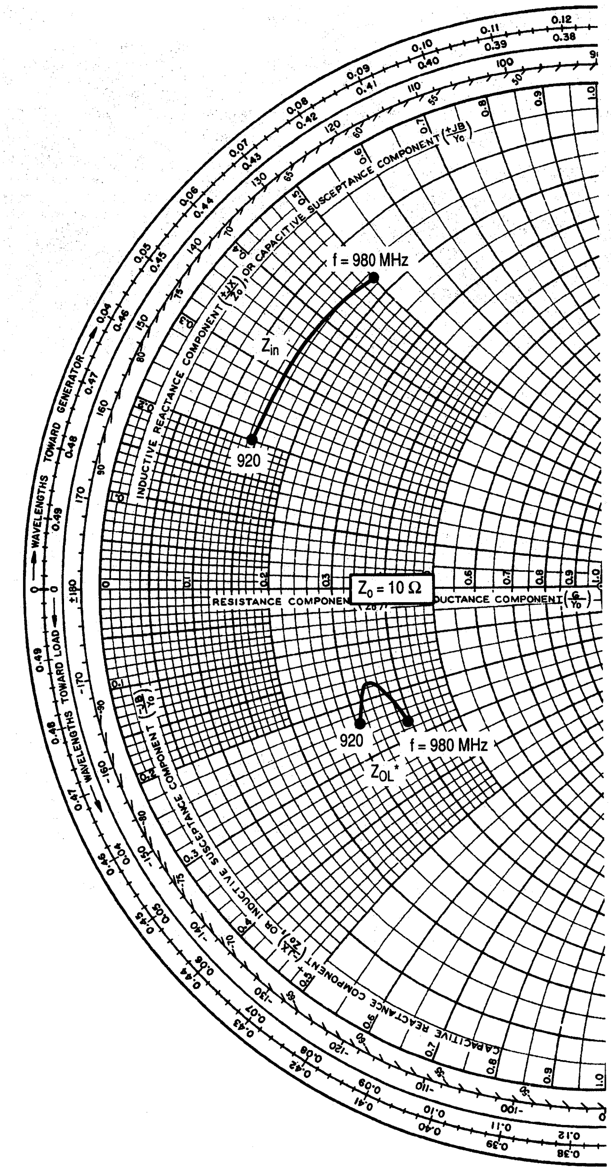


Figure 7. Intermodulation Distortion versus Output Power



f (MHz)	Z_{in} (Ω)	Z_{OL}* (Ω)
920	1.4 + j3.0	3.2 – j2.5
940	1.5 + j3.9	3.5 – j1.88
960	1.5 + j4.2	3.9 – j2.5
980	1.6 + j4.4	4.0 – j2.8

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 8. Input and Output Impedances with Circuit Tuned for Maximum Gain @ V_{CC} = 26 V, I_{CQ} = 50 mA, P_{out} = 20 W (CW)

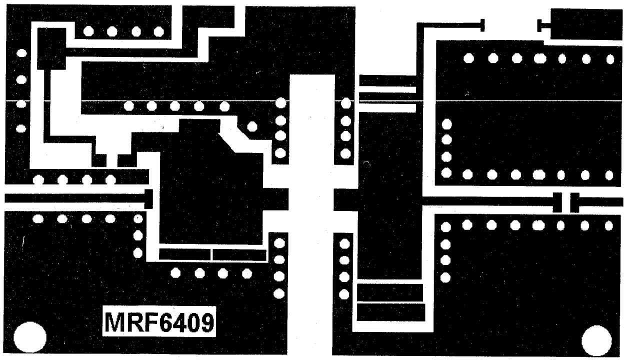


Figure 9. 960 MHz Test Circuit RF, Photomaster Scale 1:1 (Reduced 25% in printed data book, DL110/D)

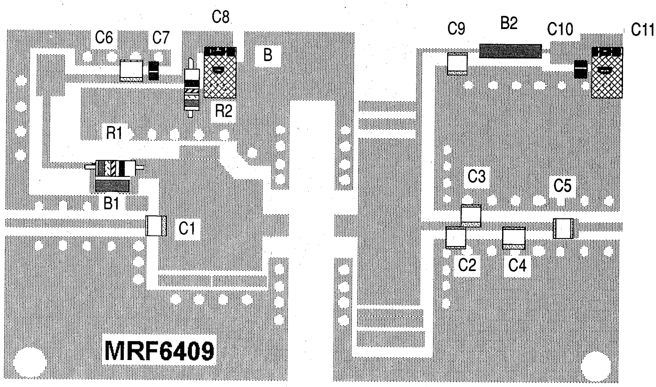


Figure 10. 960 MHz Test Circuit RF, Photomaster Scale 1:1 and Components Location (Reduced 25% in printed data book, DL110/D)

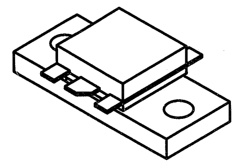
The RF Line
NPN Silicon RF Power Transistor

MRF6414

The MRF6414 is designed for 26 volt UHF large signal, common emitter, class AB linear amplifier applications.

- Specified 26 Volt, 960 MHz Characteristics
  Output Power = 50 Watts
  Minimum Gain = 8.5 dB @ 960 MHz, Class AB
  Minimum Efficiency = 50% @ 960 MHz, 50 Watts
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit Board Photomaster Available by Ordering Document MRF6414PHT/D from Motorola Literature Distribution.

50 W, 960 MHz
RF POWER TRANSISTOR
NPN SILICON



CASE 333A–02, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	28	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Collector–Current — Continuous	I_C	6	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	134 0.77	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.3	°C/W

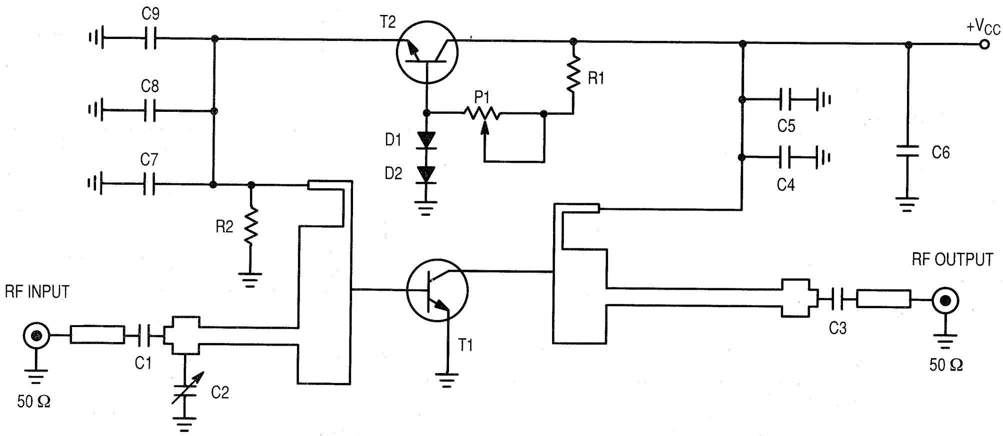
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	28	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector–Emitter Leakage Current (V_{CE} = 30 Vdc, R_{BE} = 75 Ω)	I_{CER}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	30	—	120	—

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1 MHz) (1)	C_{ob}	—	45	—	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 50 W, I_{CQ} = 200 mA, f = 960 MHz)	G_{pe}	8.5	—	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 50 W, I_{CQ} = 200 mA, f = 960 MHz)	η	50	55	—	%
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 50 W, I_{CQ} = 200 mA, f = 960 MHz) VSWR = 3:1; all phase angles at frequency of test	Ψ	No Degradation in Output Power			

(1) For information only. It is not measurable in MRF6414 because of internal matching network.



C1, C3	100 pF, Chip Capacitor, Hight Q		P1	1 kΩ, Trimmer
C2, C7	330 pF, Chip Capacitor, 0805		R1	1 kΩ, Resistor
C5, C8	10 nF, Chip Capacitor, 0805		R2	58 Ω, Resistor, 0805
C6	15 µF, Capacitor, 63 V		T1	MRF6414
C9	100 µF, Capacitor, 16 V		T2	Transistor NPN Type BD135
D1, D2	Diode 1N4007			

Figure 1. 960 MHz Test Circuit Schematic

TYPICAL CHARACTERISTICS

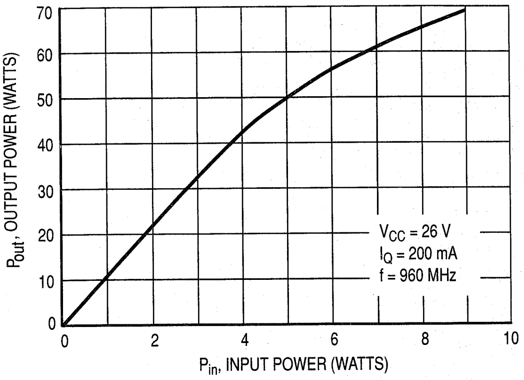


Figure 2. Output Power versus Input Power (Typical)

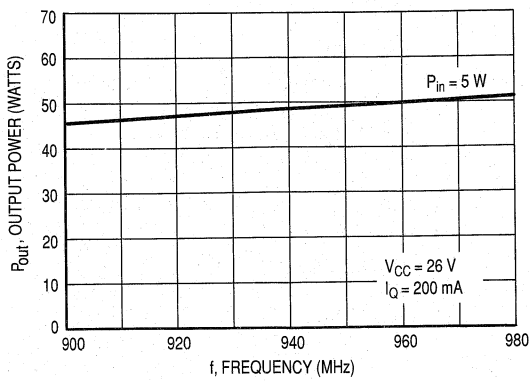


Figure 3. Output Power versus Frequency

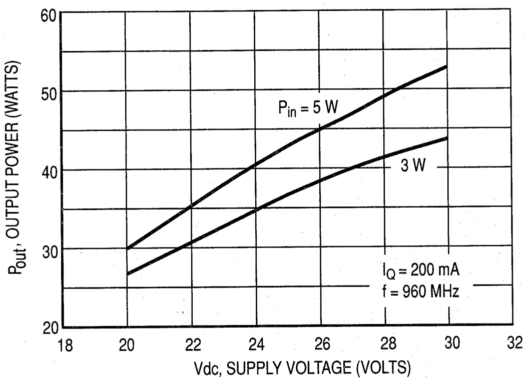


Figure 4. Output Power versus Supply Voltage

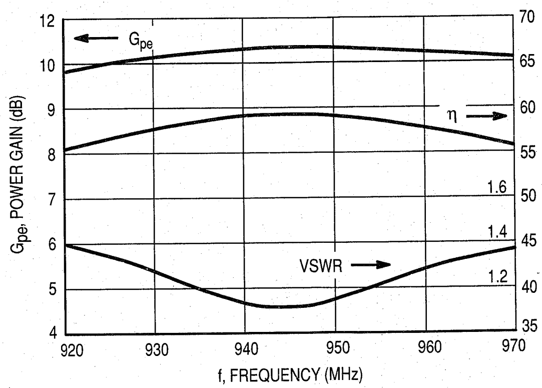


Figure 5. Typical Broadband Amplifier

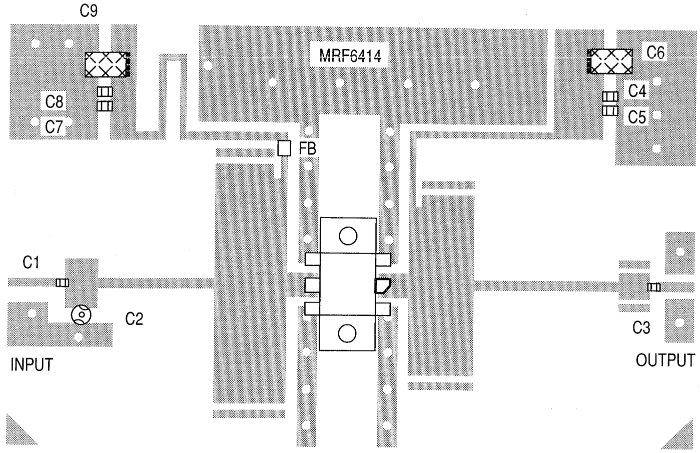
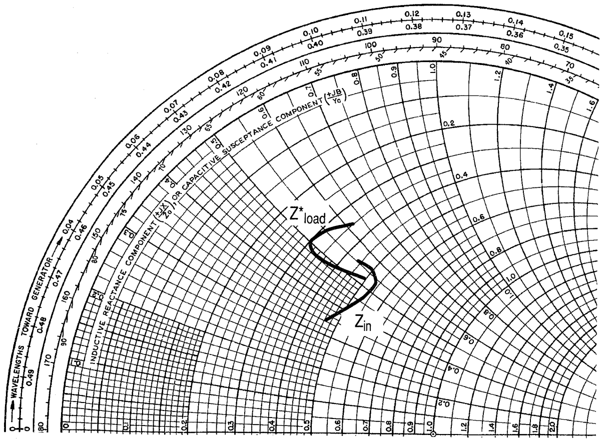


Figure 6. 960 MHz Test Circuit Components Layout



Normalized to 10 Ω

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
900	4.4 + j4.6	4.7 + j4.7
935	5.1 + j4.8	4.0 + j3.9
960	5.4 + j3.6	3.7 + j4.5
980	4.7 + j2.5	3.4 + j4.7

Z_{OL}*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

Figure 7. Input and Output Impedances with Circuit Tuned for Maximum Gain @ V_{CC} = 26 V, I_Q = 200 mA, P_{out} = 50 W

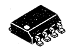
The RF Line
NPN Silicon RF Low Power Transistor

MRF8372R1, R2

Designed primarily for wideband large signal predriver stages in 800 MHz and UHF frequency ranges.

- Specified @ 12.5 V, 870 MHz Characteristics
  Output Power = 750 mW
  Minimum Gain = 8.0 dB
  Efficiency 60% (Typ)
- State–of–the–Art Technology
  Fine Line Geometry
  Gold Top Metal and Wires
  Silicon Nitride Passivated
  Ion Implanted Arsenic Emitters
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.
- Order MRF8372 in tape and reel packaging by adding suffix:
  R1 suffix = 500 units per reel
  R2 suffix = 2,500 units per reel

750 mW, 870 MHz
RF LOW POWER
TRANSISTOR
NPN SILICON



CASE 751–05, STYLE 1
SORF (SO–8)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	16	Vdc
Collector–Base Voltage	V_{CBO}	36	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_C = 75°C (1) Derate above 75°C	P_D	1.67 22.2	Watts mW/°C
Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C
Maximum Junction Temperature	T_{Jmax}	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	45	°C/W

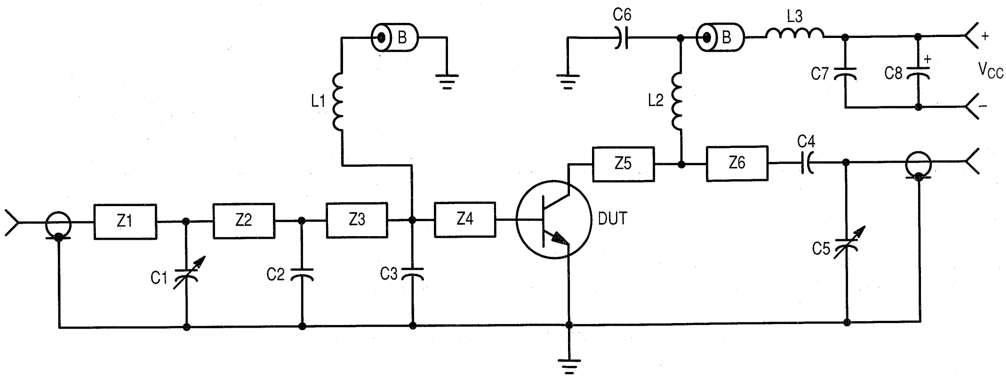
DEVICE MARKING

MRF8372 = 8372

NOTE:
1. Case temperature measured on collector lead immediately adjacent to body of package.

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage ($I_C = 5.0$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector–Emitter Breakdown Voltage ($I_C = 5.0$ mAdc, $V_{BE} = 0$)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter–Base Breakdown Voltage ($I_E = 0.1$ mAdc, $I_C = 0$)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 15$ Vdc, $V_{BE} = 0$, $T_C = 25°C$)	I_{CES}	—	—	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain ($I_C = 50$ mAdc, $V_{CE} = 10$ Vdc)	h_{FE}	30	90	200	—
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 15$ Vdc, $I_E = 0$, f = 1.0 MHz)	C_{ob}	—	1.8	2.5	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain ($V_{CC} = 12.5$ Vdc, $P_{out} = 0.75$ W, f = 870 MHz)	G_{pe}	8.0	10	—	dB
Collector Efficiency ($V_{CC} = 12.5$ Vdc, $P_{out} = 0.75$ W, f = 870 MHz)	η	55	60	—	%



C1, C5 — 0.8–8.0 pF Johanson Gigatrim
C2, C3 — 10 pF Ceramic Chip Capacitor
C6 — 91 pF Clamped Mica, Mini–Underwood
C4 — 47 pF Ceramic Chip Capacitor
C7 — 91 pF Clamped Mica, Mini–Underwood
C8 — 1.0 µF 25 V Tantalum
B — Bead, Ferroxcube 56–590–65/3B

L1, L2 — 4 Turns, #21 AWG, 5/32″ ID
L3 — 7 Turns, #21 AWG, 5/32″ ID
Z1, Z2 — 1″ x 0.078″ Microstrip, Z_o = 50 Ohms
Z3 — 0.25″ x 0.078″ Microstrip, Z_o = 50 Ohms
Z4 — 0.15″ x 0.078″ Microstrip, Z_o = 50 Ohms
Z5 — 0.30″ x 0.078″ Microstrip, Z_o = 50 Ohms
Z6 — 1.63″ x 0.078″ Microstrip, Z_o = 50 Ohms
PCB — 1/32″ Glass Teflon, ε_r = 2.56

Figure 1. 800–900 MHz Broadband Circuit

800/900 MHz BAND DATA

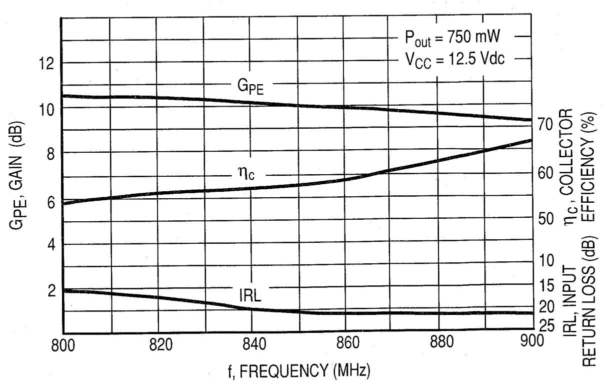


Figure 2. Typical Broadband Performance

f Frequency MHz	Z_{in} Ohms		Z_{OL}* Ohms	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 150 mW	P_{in} = 100 mW	P_{out} = 806 MHz = 820 mW P_{out} = 870 MHz = 635 mW P_{out} = 960 MHz = 530 mW	P_{out} = 806 MHz = 1.05 mW P_{out} = 870 MHz = 855 mW P_{out} = 960 MHz = 580 mW
806	8.0 + j1.9	4.0 + j1.2	24.7 – j19.2	20.9 – j31.0
870	5.2 + j3.5	6.0 + j1.9	36.9 – j20.5	32.1 – j26.6
960	6.8 + j4.0	6.1 + j2.5	39.3 – j18.5	36.3 – j25.7

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

Table 1. Series Equivalent Input/Output Impedance

TYPICAL CHARACTERISTICS
800/900 MHz BAND DATA (continued)

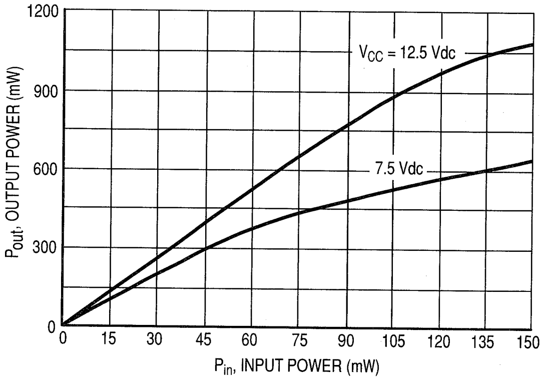


Figure 3. Output Power versus Input Power
f = 870 MHz

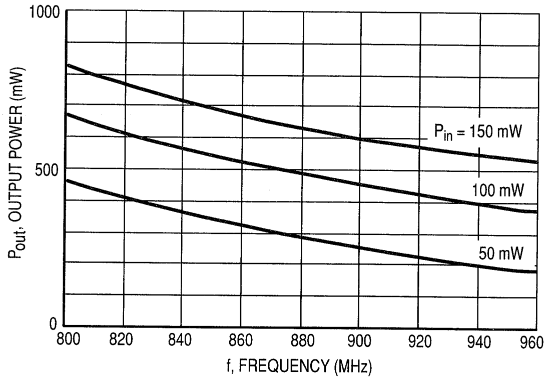


Figure 4. Output Power versus Frequency
V_{CC} = 7.5 Vdc

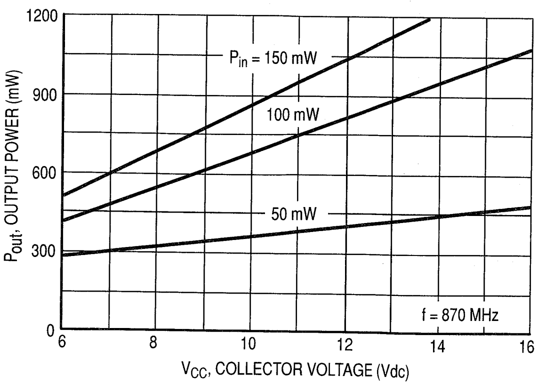


Figure 5. Output Power versus Collector Voltage

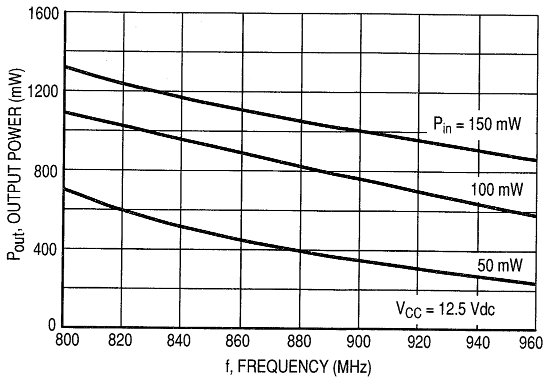


Figure 6. Output Power versus Frequency

TYPICAL CHARACTERISTICS
800/900 MHz BAND DATA (continued)

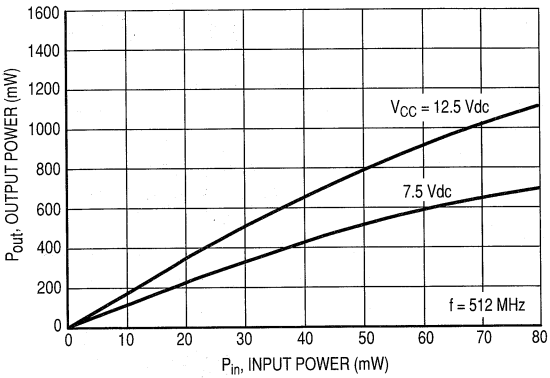


Figure 7. Output Power versus Input Power

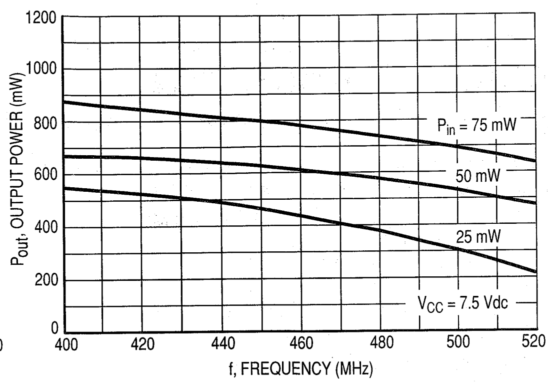


Figure 8. Output Power versus Frequency

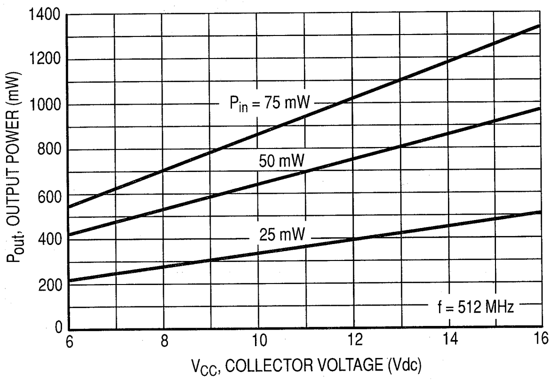


Figure 9. Output Power versus Collector Voltage

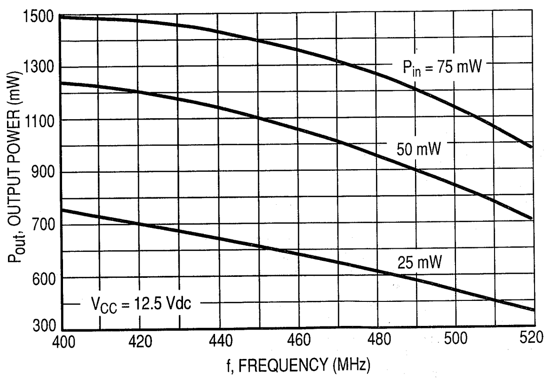


Figure 10. Output Power versus Frequency

Advance Information

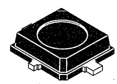
The RF Small Signal Line

Silicon Lateral FET

N–Channel Enhancement–Mode MOSFET

MRF9745T1

**30 dBm, 900 MHz
HIGH FREQUENCY
POWER TRANSISTOR
LDMOS FET**



**CASE 449–02, STYLE 1
(PLD–1)**

Designed for use in low voltage, moderate power amplifiers such as portable analog and digital cellular radios and PC RF modems.

- Performance Specifications at 5.8 V, 900 MHz:
  Output Power = 30 dBm Min
  Power Gain = 10 dB Typ
  Efficiency = 50% Min
- Guaranteed Ruggedness at Load VSWR = 20:1
- New Plastic Surface Mount Package
- Available in Tape and Reel Packaging.
  T1 Suffix = 1,000 Units per 8 mm, 7 inch Reel
- Device Marking = 9745

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	35	Vdc
Drain–Gate Voltage (R_{GS} = 1 MΩ)	V_{DGO}	25	Vdc
Gate–Source Voltage	V_{GS}	±10	Vdc
Drain Current – Continuous	I_D	2	Adc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	10 100	W mW/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Temperature Range	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Leakage Current (V_{DS} = 35 V, V_{GS} = 0)	I_{DSS}	–	–	10	µAdc
Gate–Source Leakage Current (V_{GS} = 5 V, V_{DS} = 0)	I_{GSS}	–	–	1	µAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 1

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 6 V, I_D = 25 μA)	$V_{GS(th)}$	1	2	3	Vdc
Forward Transconductance (V_{DS} = 6 V, I_D = 200 mA)	g_{fs}	–	550	–	mmhos
Resistance Drain–Source (V_{GS} = 4 V, I_D = 100 mA)	$R_{DS(on)}$	–	1	2.5	Ω
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 6 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	14	–	pF
Output Capacitance (V_{DS} = 6 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	–	11	–	pF
Feedback Capacitance (V_{DS} = 6 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	–	1.8	–	pF
FUNCTIONAL CHARACTERISTICS					
Power Gain (V_{DD} = 5.8 Vdc, P_{in} = 20 dBm, I_{DQ} = 150 mA, f = 900 MHz)	G_{ps}	9.5	10	–	dB
Drain Efficiency (V_{DD} = 5.8 Vdc, P_{in} = 20 dBm, I_{DQ} = 150 mA, f = 900 MHz)	η_D	50	55	–	%
Ruggedness Test (V_{DD} = 5.8 Vdc, P_{in} = 20 dBm, I_{DQ} = 150 mA, f = 900 MHz, Load VSWR = 20:1, All Phase Angles at Frequency Test)	Ψ	No Degradation in Output Power after Test			

Table 1. Large Signal Impedance
V_{DD} = 5.8 V, P_{in} = 20 dBm, I_{DQ} = 150 mA

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
850	7.0 – j6.4	6.1 – j5.1
900	5.2 – j6.5	5.9 – j4.6
950	5.2 – j6.0	6.1 – j4.7

Z_{OL}* is the conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Advance Information

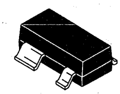
The RF Small Signal Line

Gallium Arsenide

N–Channel Depletion–Mode MESFET

MRF9811T1

**21 dBm, 5.8 V
HIGH FREQUENCY
GaAs FET TRANSISTOR**



**CASE 318A–05, STYLE 7
(SOT–143)**

Designed for use in driver stages of moderate power RF amplifiers to 2 GHz. Typical applications are cellular radios and personal communication transmitters such as AMPS, ETACS, NMT, GSM, PCN, JDC and DECT.

- Performance Specifications at 900 MHz, 5.8 V:
  Output Power = 21 dBm
  Power Gain = 14 dB Min
  Drain Efficiency = 55% Min
- Plastic Surface Mount Package
- Order MRF9811T1 for Tape and Reel Packaging.
  T1 Suffix = 3,000 Units per 8 mm, 7 inch Reel.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	10	Vdc
Gate–Source Voltage	V_{GS}	±5	Vdc
Drain Current — Continuous	I_D	0.7	Adc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	0.77 7.7	W mW/°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	130	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Gate–Drain Breakdown Voltage (I_{GD} = 0.25 mA, Source Open)	$V_{(BR)GDO}$	15	–	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 1.5 Vdc, V_{GS} = 0)	I_{DSS}	0.35	–	–	Adc
Gate–Source Leakage Current (V_{GS} = –5.0 Vdc, Drain Open)	I_{GSO}	–	0.5	10	µAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 5.8 Vdc, I_D = 0.25 A)	$V_{GS(th)}$	–	–2	–	Vdc
Forward Transconductance (V_{DS} = 5.8 Vdc, I_D = 30 mA)	g_{fs}	–	90	–	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 5.8 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	2	–	pF
Output Capacitance (V_{DS} = 5.8 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	–	3.5	–	pF
FUNCTIONAL CHARACTERISTICS (In specified test circuit shown on data sheet)					
Common Source Output Power (V_{DS} = 5.8 V, I_{DQ} = 30 mA, P_{in} = 7 dBm, f = 900 MHz)	G_{ps}	14	–	–	dB
Drain Efficiency (V_{DS} = 5.8 V, I_{DQ} = 30 mA, P_{in} = 7 dBm, f = 900 MHz)	η_D	55	–	–	%

Advance Information

The RF Small Signal Line

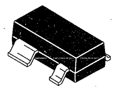
GaAs MESFET AGC Amplifier

MRF9820T1

The MRF9820T1 is a high performance GaAs AGC amplifier suitable for use in low noise front end amplifier or downconverter applications. The device contains two enhancement mode MESFETs connected in cascode to allow access to both gates for gain control or injection of LO signals. This device is well suited for low voltage, low current front–end applications such as paging, cellular, GSM, DECT, and other portable wireless systems.

- Low Noise Figure: 1.5 dB @ 940 MHz, 1 mA
- Built In ESD Protection
- Does Not Require a Negative Supply Voltage
- RF Power Gain 16 dB @ 940 MHz, 1 mA
- High Third Order Intercept Point
- Industry Standard SOT–143 Surface Mount Package
- Order MRF9820T1 for Tape and Reel Packaging.
  T1 Suffix = 3,000 Units per 8 mm, 7 inch Reel.

**SURFACE MOUNT
LOW NOISE
ENHANCEMENT MODE
GaAs CASCODE**



**CASE 318A–05, STYLE 11
(SOT–143)**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	6	Vdc
Gate 1–Source Voltage	V_{G1S}	–4	Vdc
Gate 2–Source Voltage	V_{G2S}	–4	Vdc
Drain Current — Continuous	I_D	I_{DSS}	—
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	231 4.3	mW mW/°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Operating Channel Temperature	T_{ch}	150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance, Channel to Case	$R_{\theta ch-C}$	325	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Gate 1 Leakage Current (V_{DS} = 2 V, V_{G1S} = 0.425 V, V_{G2S} = 1 V)	I_{G1S}	4	µA
Gate 2 Leakage Current (V_{DS} = 2 V, V_{G1S} = 0.5 V, V_{G2S} = 0.425 V)	I_{G2S}	4	µA
Threshold Voltage (V_{DS} = 3 V, V_{G2S} = 1 V, I_D = 1 mA)	V_{th}	275 (min) 425 (max)	mV
Gate 1–to–Source Cutoff Voltage (V_{DS} = 2 V, V_{G2S} = 1 V, I_D = 200 µA)	$V_{G1S(off)}$	100 (min) 360 (max)	mV
Gate 2–to–Source Cutoff Voltage (V_{DS} = 2 V, V_{G1S} = 0.5 V, I_D = 200 µA)	$V_{G2S(off)}$	10 (min) 370 (max)	mV
Forward Transconductance (V_{DS} = 2 V, V_{G2S} = 1 V, I_D = 1 mA)	g_m	9 (min)	mS
Drain–to–Source Leakage Current (V_{DS} = 2 V, V_{G1S} = 0 V, V_{G2S} = 0 V)	$I_{DS(off)}$	2 (max)	µA

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

PERFORMANCE CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
RF Power Gain (V_{DS} = 3 V, V_{G2} = 1.7 V, I_D = 1 mA, f = 940 MHz)	G_{ps}	14 (min)	dB
Noise Figure (V_{DS} = 3 V, V_{G2} = 1.7 V, I_D = 1 mA, f = 940 MHz)	NF	1.5 (typ) 2.0 (max)	dB
Input Third Order Intercept Point	IIP3	–3 (typ) –8 (min)	dBm

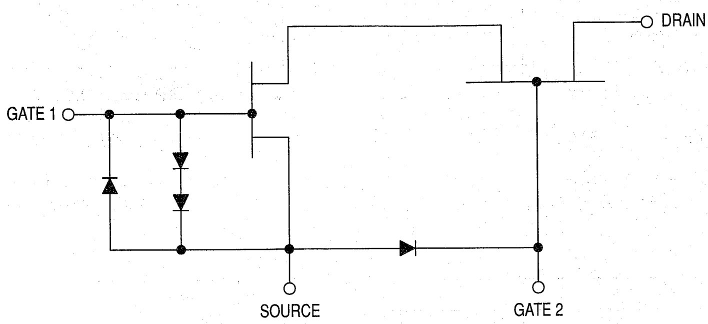


Figure 1. Electrical Schematic of GaAs AGC Amplifier

TYPICAL CHARACTERISTICS

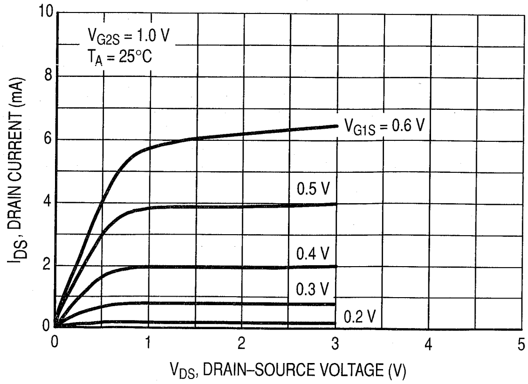


Figure 2. Drain Current versus V_{DS}; Stepping V_{G1S}

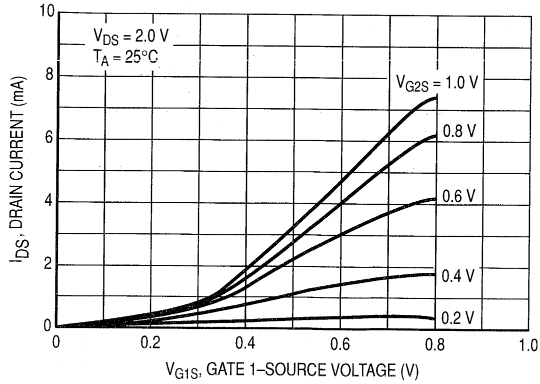


Figure 3. Drain Current versus V_{G1S}; Stepping V_{G2S}

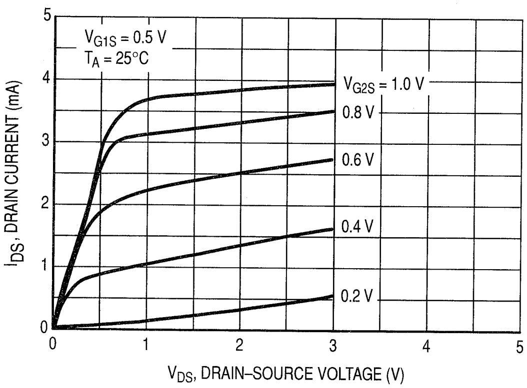


Figure 4. Drain Current versus V_{DS}; Stepping V_{G2S}

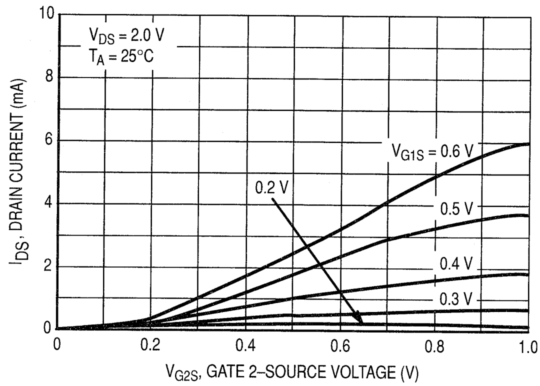


Figure 5. Drain Current versus V_{G2S}; Stepping V_{G1S}

Advance Information

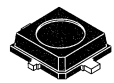
MRF9822T1

The RF Small Signal Line
Gallium Arsenide PHEMT
Pseudomorphic High Electron Mobility Transistor

31 dBm, 850 MHz
HIGH FREQUENCY
POWER TRANSISTOR
GaAs PHEMT

Designed for use in low voltage, moderate power amplifiers such as portable analog and digital cellular radios and PC RF modems.

- Performance Specifications at 3.5 V, 850 MHz:
  Output Power = 31 dBm Min
  Power Gain = 11 dB Typ
  Efficiency = 70% Min
- Guaranteed Ruggedness at Load VSWR = 20:1
- New Plastic Surface Mount Package
- Available in Tape and Reel Packaging Options:
  T1 suffix = 1,000 Units per Reel
- Device Marking = 9822



CASE 449–02, STYLE 1
(PLD–1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Gate Voltage	V_{DGO}	12	Vdc
Gate–Source Voltage	V_{GS}	– 6	Vdc
Drain Current – Continuous	I_D	3	Adc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	10 100	W mW/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Temperature Range	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

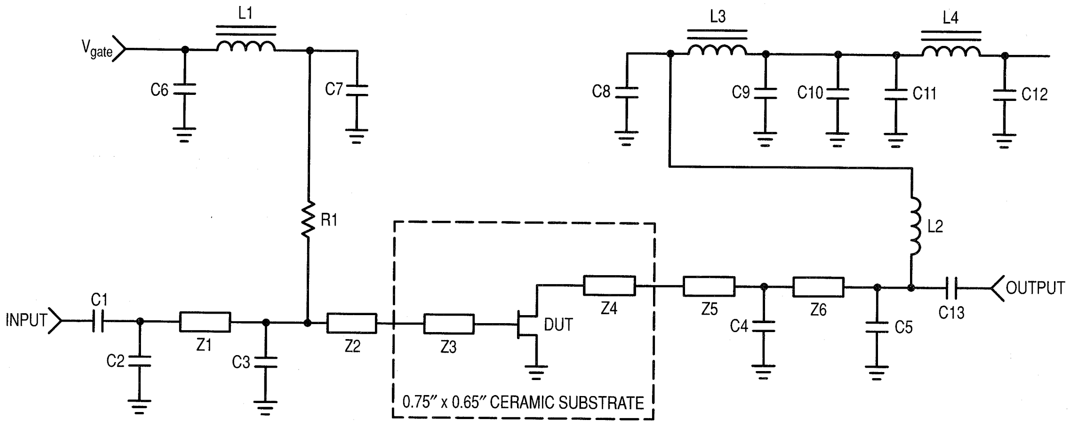
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Gate Breakdown Voltage (I_D = 1.5 mA)	BV_{GDO}	12	–	–	Vdc
Off–state Leakage Current (V_{DS} = 5.5 V, V_{GS} = –2. 6 V)	$I_{DS(off)}$	–	–	3	mA
Gate–Source Leakage Current (V_{GS} = –2. 6 V)	I_{GSS}	–	–	10	µAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 3.5 V, I_D = 150 mA)	$V_{GS(th)}$	–1.5	–	–0.5	Vdc
Forward Transconductance (V_{DS} = 6 V, I_D = 200 mA)	g_{fs}	–	1.5	–	mhos
Saturation Drain–Current (V_{GS} = 0.0 V, V_{DS} = 1.5 V)	I_{DSS}	1.8	2.5	–	A
FUNCTIONAL CHARACTERISTICS					
Power Gain (V_{DD} = 3.5 Vdc, P_{in} = 20 dBm, I_{DQ} = 150 mA, f = 850 MHz)	G_{ps}	10.5	11	–	dB
Drain Efficiency (V_{DD} = 3.5 Vdc, P_{in} = 20 dBm, I_{DQ} = 150 mA, f = 850 MHz)	η_D	65	70	–	%



C1, C13	1000 pF, ATC "B" Series	L2	7 Turns, AWG #18, 0.09″ I.D., Close Wound
C2	2.7 pF, ATC "B" Series	L3	3 Ferrite Beads on 1/2″ AWG #16
C3	2.7 pF, ATC "B" Series	R1	680 Ω, 1/8 Watt Leaded
C4	7.5 pF, ATC "B" Series	Z1	0.075″ x 0.790″ Microstrip
C5	33 pF, ATC "B" Series	Z2	0.075″ x 0.09″ Microstrip
C6, C12	47 µF, Ceramic	Z3, Z4	0.075″ x 0.25″ Microstrip
C7, C8, C9, C10, C11	0.05 µF Chip	Z5	0.075″ x 0.09″ Microstrip
L1, L4	VK–200 4 Turn Ferrite Bead	Z6	0.075″ x 0.53″ Microstrip

Substrate Material: 0.05, Teflon/Glass, ε_r = 2.55, 2 oz. cu.

Figure 1. 850 MHz Test Fixture Schematic

Table 1. Large Signal Impedance
V_{DD} = 3.5 V, P_{in} = 20 dBm, I_{DQ} = 150 mA

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
850	5.0 – j6.3	5.5 – j1.2

Z_{OL}* is the conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

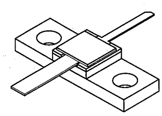
The RF Line
Microwave Power Transistor

MRF10005

. . . designed for CW and long pulsed common base amplifier applications, such as JTIDS and Mode S, in the 0.96 to 1.215 GHz frequency range at high overall duty cycles.

- Guaranteed Performance @ 1.215 GHz, 28 Vdc
  Output Power = 5.0 Watts CW
  Minimum Gain = 8.5 dB, 10.3 dB (Typ)
- RF Performance Curves given for 28 Vdc and 36 Vdc Operation
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input Matching for Broadband Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

5.0 W, 960–1215 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON



CASE 336E–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	55	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous (1)	I_C	1.25	mAdc
Total Device Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	25 143	Watt mW/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

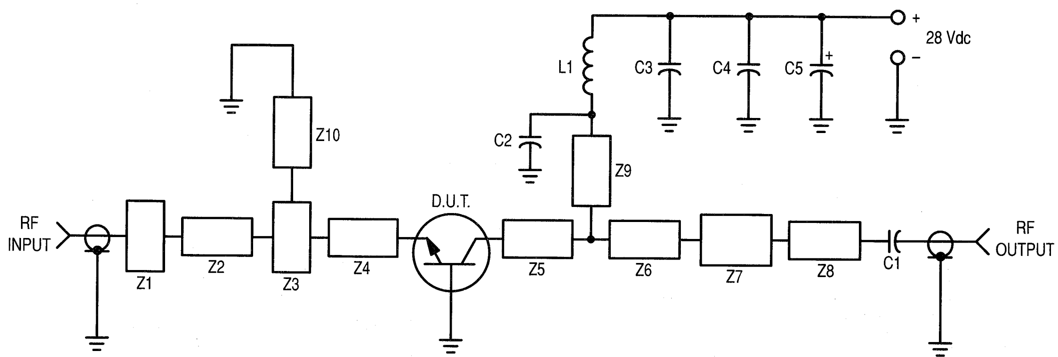
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	7.0	°C/W

NOTES:
1. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
2. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

REV 6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.5 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	7.0	10	pF
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 1215 MHz)	G_{PB}	8.5	10.3	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 1215 MHz)	η	45	55	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 1215 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1, C2, C3 — 220 pF 100 mil Chip Capacitor
C4 — 0.1 µF
C5 — 47 µF/50 V Electrolytic
L1 — 3 turn #18 AWG, 1/8″ ID, 0.18″ Long

Z1–Z10 — Microstrip, see details below
Board Material — 0.030″ Glass Teflon, 2.0 oz. Copper, ε_r = 2.55

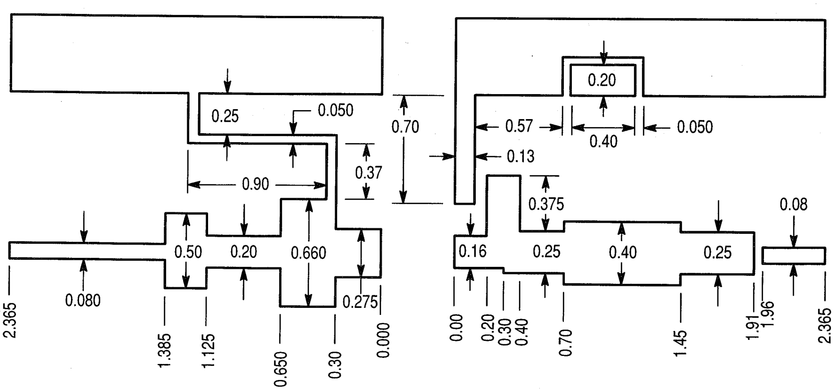


Figure 1. Test Circuit

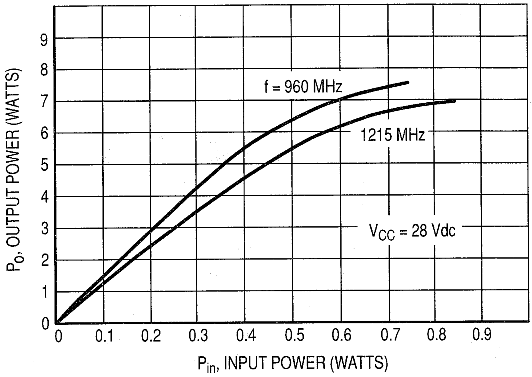


Figure 2. Output Power versus Input Power

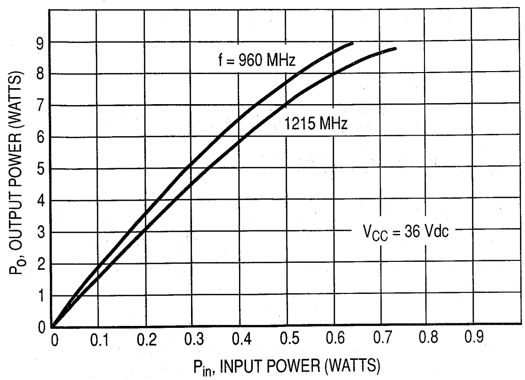
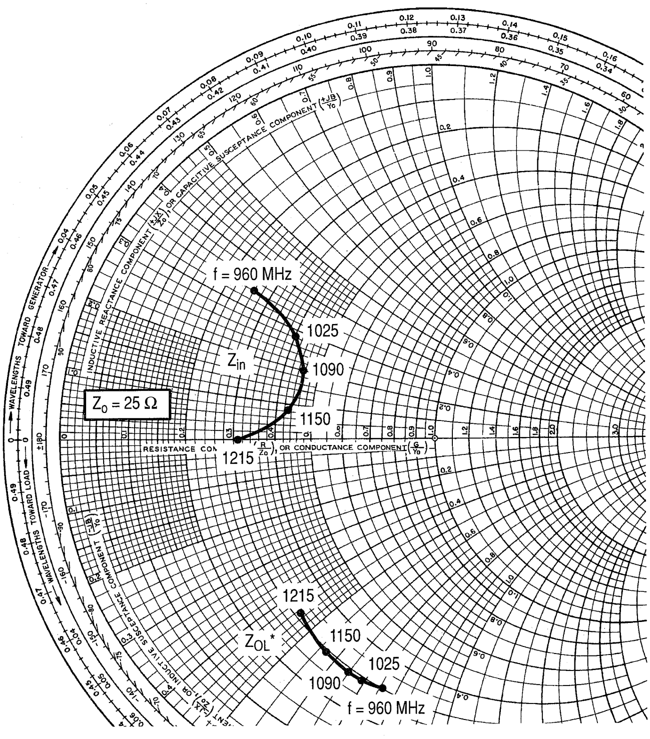


Figure 3. Output Power versus Input Power



P_{out} = 5 W, V_{CC} = 28 V

f MHz	Z_{in} OHMS	Z_{OL}* OHMS
960	6.5 + j8.5	7.4 – j18.9
1025	10.0 + j7.0	7.2 – j17.4
1090	11.2 + j4.9	7.1 – j16.3
1150	10.8 + j2.0	7.15 – j14.3
1215	7.8 + j0.0	7.8 – j11.2

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 4. Series Equivalent Input/Output Impedances

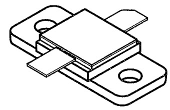
The RF Line
Microwave Long Pulse Power Transistor

MRF10031

Designed for 960–1215 MHz long or short pulse common base amplifier applications such as JTIDS and Mode–S transmitters.

- Guaranteed Performance @ 960 MHz, 36 Vdc
  Output Power = 30 Watts Peak
  Minimum Gain = 9.0 dB Min (9.5 dB Typ)
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input Matching for Broadband Operation

**30 W (PEAK)
960–1215 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON**



CASE 376B–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	55	Vdc
Collector–Base Voltage (1)	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous (1)	I_C	3.0	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	110 0.625	Watts mW/°C
Storage Temperature Range	T_{stg}	– 65 to + 200	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

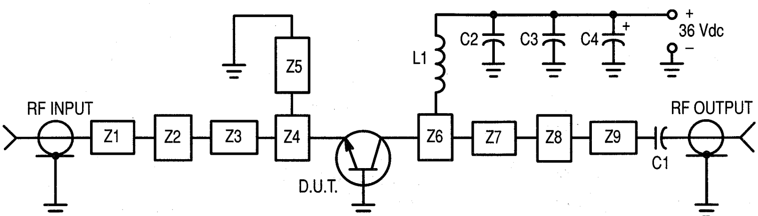
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	1.6	°C/W

NOTES:
1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as pulsed RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques. (Worst case θ_{JC} value measured @ 23% duty cycle)

REV 6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 36 Vdc, I_E = 0)	I_{CBO}	—	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS (10 μs Pulses @ 50% duty cycle for 3.5 ms; overall duty cycle – 25%)					
Common–Base Amplifier Power Gain (V_{CC} = 36 Vdc, P_{out} = 30 W Peak, f = 960 MHz)	G_{PB}	9.0	9.5	—	dB
Collector Efficiency (V_{CC} = 36 Vdc, P_{out} = 30 W Peak, f = 960 MHz)	η	40	45	—	%
Load Mismatch (V_{CC} = 36 Vdc, P_{out} = 30 W Peak, f = 960 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 75 pF 100 Mil Chip Capacitor
C2 — 39 pF 100 Mil Chip Capacitor
C3 — 0.1 μF
C4 — 1000 μF, 50 Vdc, Electrolytic
L1 — 3 Turns #18 AWG, 1/8″ ID, 0.18 Long

Z1–Z9 — Microstrip, See Details
Board Material — Teflon, Glass Laminate
Dielectric Thickness = 0.030″
ε_r = 2.55, 2 Oz. Copper

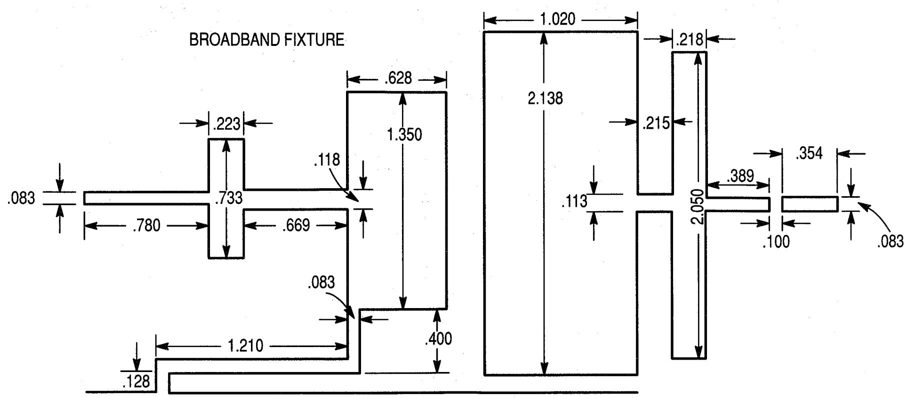


Figure 1. Test Circuit

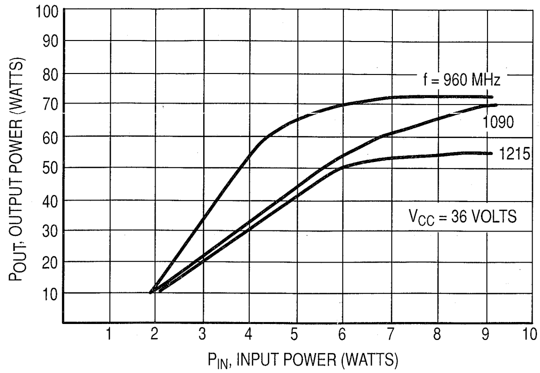
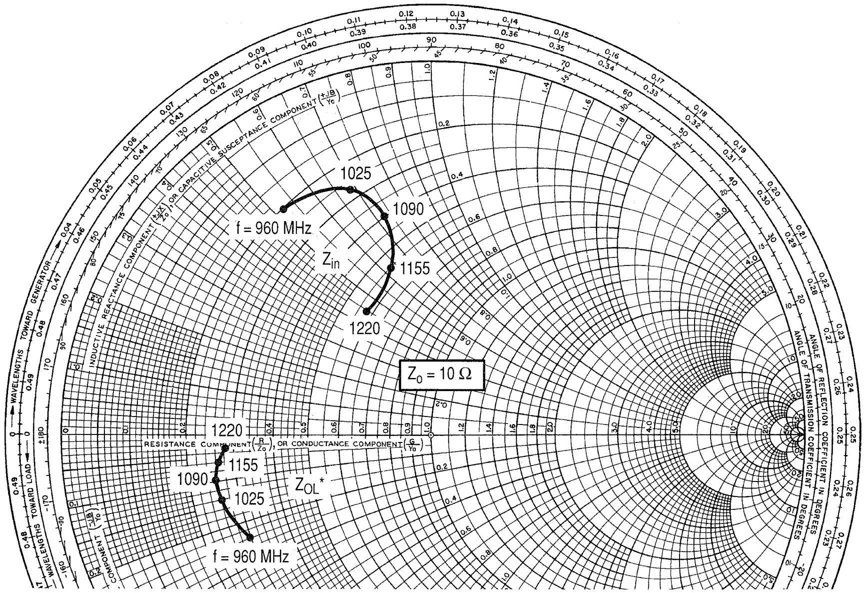


Figure 2. Output Power versus Input Power



P_{out} = 30 W Pk V_{CC} = 36 V

f MHz	Zin Ohms	Z_{OL}* Ohms
960	2.05 + j5.2	2.9 – j2.35
1025	2.67 + j6.34	2.55 – j1.3
1090	4.0 + j7.1	2.52 – j0.9
1155	5.5 + j6.2	2.6 – j0.6
1220	5.7 + j4.3	2.8 – j0.3

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

Figure 3. Series Equivalent Input/Output Impedances

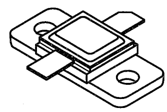
The RF Line
Microwave Pulse Power Transistor

MRF10070

**70 W (PEAK)
1025 –1150 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON**

Designed for 1025–1150 MHz pulse common base amplifier applications such as TCAS, TACAN and Mode–S transmitters.

- Guaranteed Performance @ 1090 MHz
  Output Power = 70 Watts Peak
  Gain = 9.0 dB Min
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Characterized with 10 μs, 10% Duty Cycle Pulses
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input and Output Matching
- Hermetically Sealed Package
- Recommended Driver for MRF10500 Transistor or a Pair of MRF10350 Transistors



CASE 376C–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	65	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Peak (1)	I_C	8.8	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	438 2.5	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to + 200	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

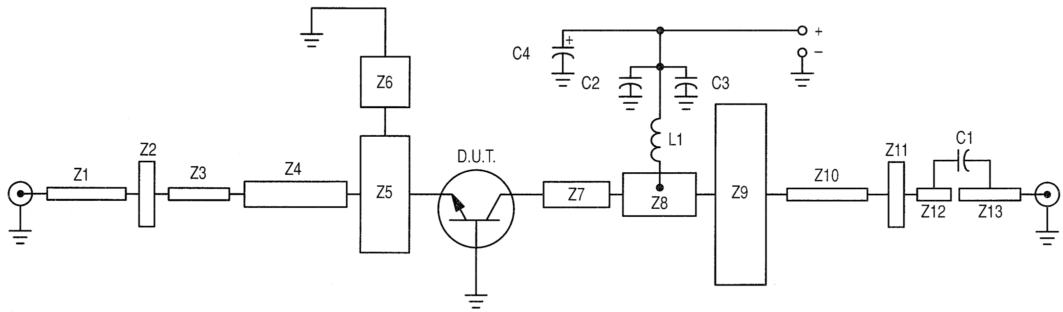
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.4	°C/W

NOTES:
1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as pulsed RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques. (Worst case θ_{JC} value measured @ 10 μs, 10%.)

REV 6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 60 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 60 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	—	—	25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 70 W Peak, f = 1090 MHz)	G_{PB}	9.0	10	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 70 W Peak, f = 1090 MHz)	η	40	—	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 70 W Peak, f = 1090 MHz, Load VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power Before or After Test			



C1 — 82 pF 100 mil Chip Capacitor
C2 — 82 pF 100 mil Chip Capacitor
C3 — 0.1 μF
C4 — 100 μF/100 Vdc Electrolytic
L1 — 3 turns #18 AWG, 1/8″ ID, 0.18″ Long

Z1 – Z13 — Microstrip, see details below
Board Material — 0.030″ Glass Teflon®; 2 oz. Cu clad; both sides; ϵ_r = 2.55

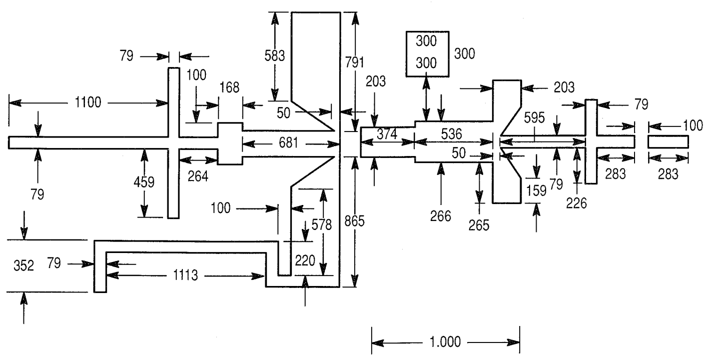


Figure 1. Test Circuit

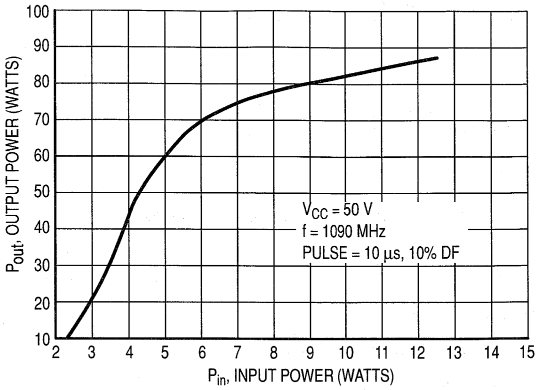
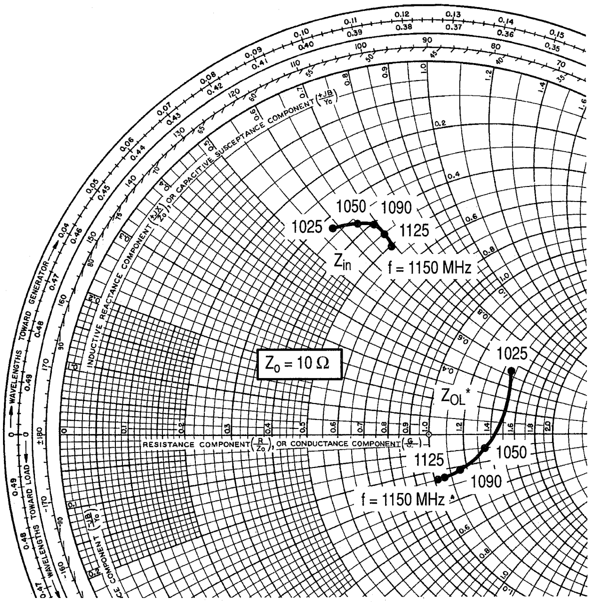


Figure 2. Output Power versus Input Power



P_{out} = 70 W Pk V_{CC} = 50 V

f MHz	ZIN OHMS	Z_{OL}* (Z_{OUT}) OHMS
1025	3.3 + j5.8	14.3 + j5.6
1050	3.6 + j6.5	13.3 – j1.0
1090	4.0 + j6.9	11.3 – j2.1
1125	4.5 + j6.9	10.4 – j2.5
1150	5.0 + j6.9	10.2 – j2.6

Z_{OL}* is the conjugate of the optimum load impedance into which the device operates at a given output power voltage and frequency.

Figure 3. Series Equivalent Input/Output Impedances

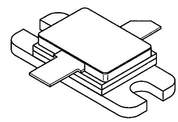
The RF Line
Microwave Long Pulse Power Transistor

MRF10120

Designed for 960–1215 MHz long pulse common base amplifier applications such as JTIDS and Mode S transmitters.

- Guaranteed Performance @ 1.215 GHz, 36 Vdc
  Output Power = 120 Watts Peak
  Gain = 8.0 dB Min., 9.2 dB (Typ)
- 100% Tested for Load Mismatch at All Phase Angles with 3:1 VSWR
- Hermetically Sealed Industry Standard Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input and Output Matching for Broadband Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

120 W (PEAK), 960–1215 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON



CASE 355C–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	55	Vdc
Collector–Base Voltage	V_{CBO}	55	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Peak (1)	I_C	15	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	380 2.17	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +200	°C
Junction Temperature	T_J	200	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.46	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 60 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 60 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 36 Vdc, I_E = 0)	I_{CBO}	—	—	25	mAdc

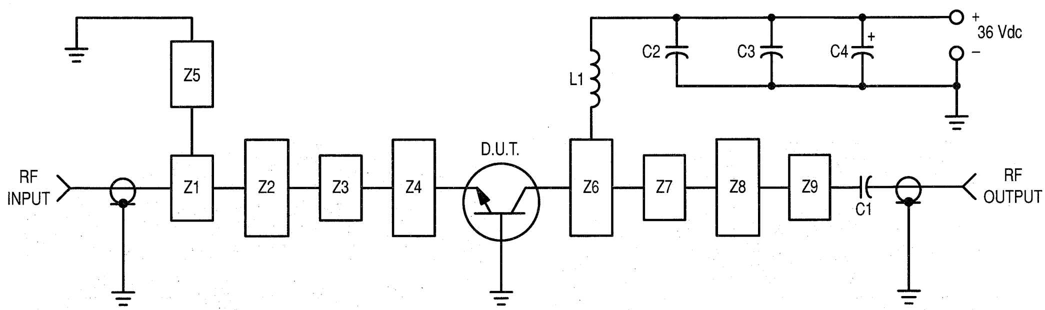
NOTES:
1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the device is operated as RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS (7.0 µs Pulses @ 54% duty cycle for 3.4 ms; then off for 4.5 ms; overall duty cycle = 23%)					
Common–Base Amplifier Power Gain (V_{CC} = 36 Vdc, P_{out} = 120 W Peak, f = 1215 MHz)	G_{PB}	8.0	9.2	—	dB
Collector Efficiency (V_{CC} = 36 Vdc, P_{out} = 120 W Peak, f = 1215 MHz)	η	50	55	—	%
Load Mismatch (V_{CC} = 36 Vdc, P_{out} = 120 W Peak, f = 1215 MHz, VSWR = 3:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 270 pF 100 Mil Chip Capacitor
C2 — 220 pF 100 Mil Chip Capacitor
C3 — 0.1 µF
C4 — 47 µF 50 V Electrolytic
L1 — 3 Turns #18 AWG, 1/8″ ID, 0.18 Long

Z1 – Z9 — Microstrip, See Details
Board Material — Teflon®/Glass Laminate, Dielectric Thickness = 0.030″, ε_r = 2.55, 2 Oz. Copper

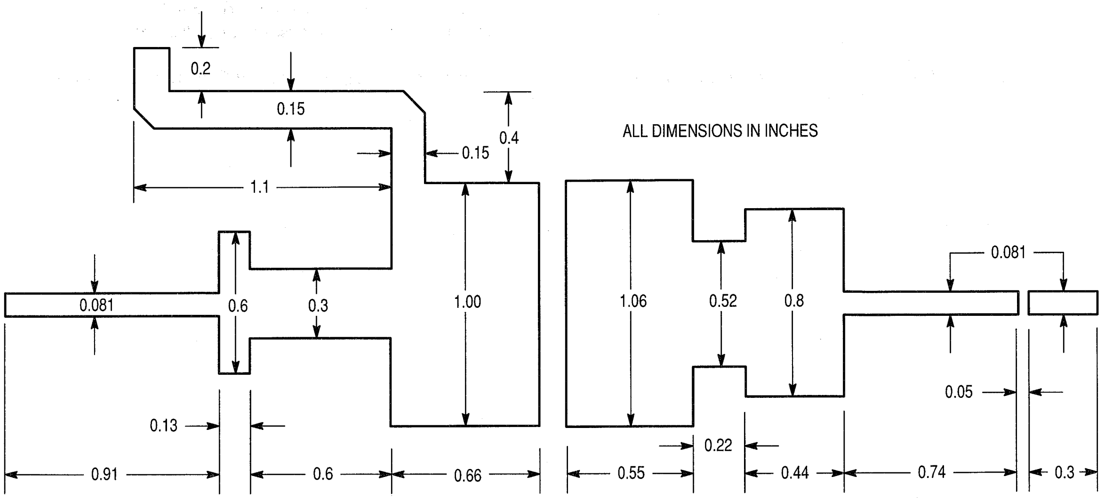


Figure 1. Test Circuit

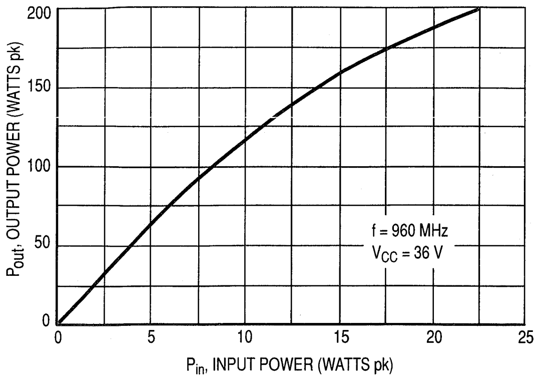


Figure 2. Output Power versus Input Power

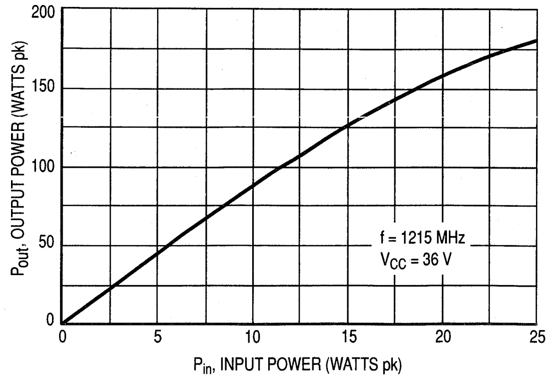
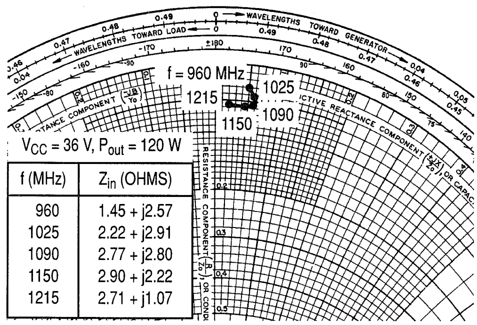
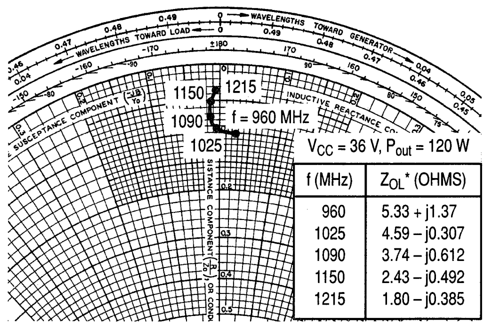


Figure 3. Output Power versus Input Power



f (MHz)	Z_{in} (OHMS)
960	1.45 + j2.57
1025	2.22 + j2.91
1090	2.77 + j2.80
1150	2.90 + j2.22
1215	2.71 + j1.07

Figure 4. Series Equivalent Input Impedances



f (MHz)	Z_{OL}* (OHMS)
960	5.33 + j1.37
1025	4.59 – j0.307
1090	3.74 – j0.612
1150	2.43 – j0.492
1215	1.80 – j0.385

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 5. Series Equivalent Output Impedance

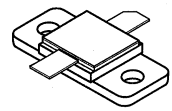
The RF Line
Microwave Pulse Power Transistor

MRF10150

. . . designed for 1025–1150 MHz pulse common base amplifier applications such as TCAS, TACAN and Mode–S transmitters.

- Guaranteed Performance @ 1090 MHz
  Output Power = 150 Watts Peak
  Gain = 9.5 dB Min, 10.0 dB (Typ)
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input and Output Matching
- Characterized with 10 µs, 10% Duty Cycle Pulses
- Recommended Driver for a Pair of MRF10500 Transistors

**150 W (PEAK)
1025–1150 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON**



CASE 376B–02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	65	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Peak (1)	I_C	14	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	700 4.0	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Junction Temperature	T_J	200	°C

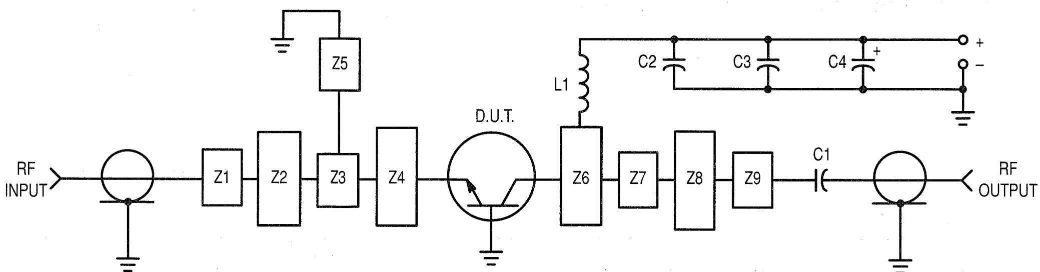
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.25	°C/W

NOTES:
1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as pulsed RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques. (Worst case θ_{JC} value measured @ 10 µs, 10%.)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 60 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 60 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 36 Vdc, I_E = 0)	I_{CBO}	—	—	25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 150 W Peak, f = 1090 MHz)	G_{PB}	9.5	10	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 150 W Peak, f = 1090 MHz)	η	40	—	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 150 W Peak, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 82 pF 100 Mil Chip Capacitor
C2 — 39 pF 100 Mil Chip Capacitor
C3 — 0.1 µF
C4 — 100 µF, 100 Vdc, Electrolytic
L1 — 3 Turns #18 AWG, 1/8″ ID, 0.18 Long

Z1–Z9 — Microstrip, See Details
Board Material — Teflon Glass Laminate
Dielectric Thickness = 0.030″
ε_r = 2.55, 2 Oz. Copper

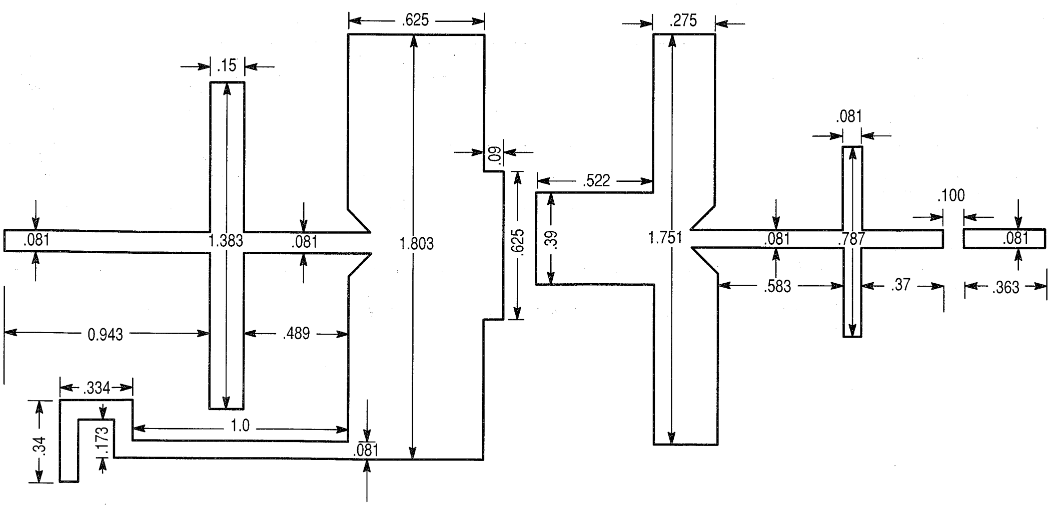


Figure 1. Test Circuit

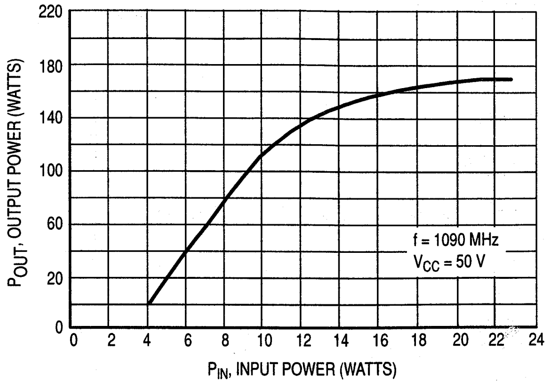
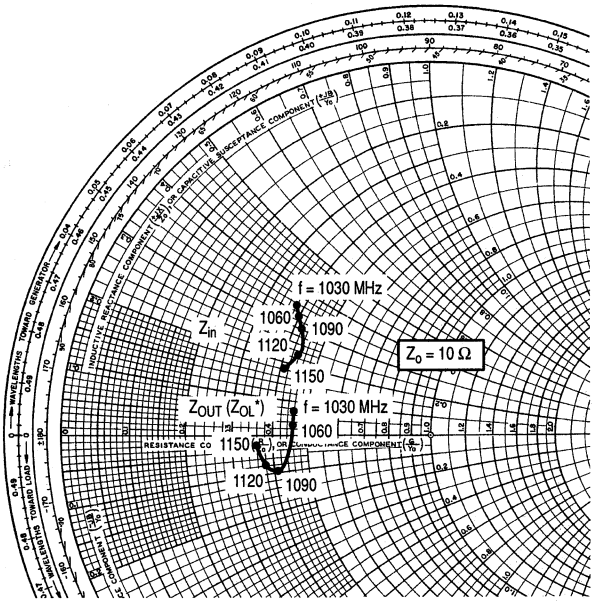


Figure 2. Output Power versus Input Power



P_{OUT} = 150 W Pk V_{CC} = 50 V

f MHz	Z_{in} OHMS	Z_{OL}* (Z_{OUT}) OHMS
1030	3.8 + j3.5	4.6 + j0.7
1060	4.0 + j3.3	4.6 + j0.3
1090	4.2 + j3.0	4.1 – j1.0
1120	4.4 + j2.3	3.8 – j0.8
1150	4.1 + j1.8	3.6 – j0.3

Z_{OL}* is the conjugate of the optimum load impedance into which the device operates at a given output power voltage and frequency.

Figure 3. Series Equivalent Input/Output Impedances

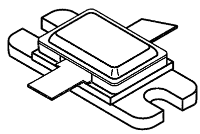
The RF Line
Microwave Pulse Power Transistor

MRF10350

Designed for 1025–1150 MHz pulse common base amplifier applications such as TCAS, TACAN and Mode–S transmitters.

- Guaranteed Performance @ 1090 MHz
  Output Power = 350 Watts Peak
  Gain = 8.5 dB Min, 9.0 dB (Typ)
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input and Output Matching
- Characterized using Mode–S Pulse Format

350 W (PEAK)
1025–1150 MHz
MICROWAVE POWER
TRANSISTOR
NPN SILICON



CASE 355E–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	65	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Peak (1)	I_C	31	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	1590 9.1	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +200	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

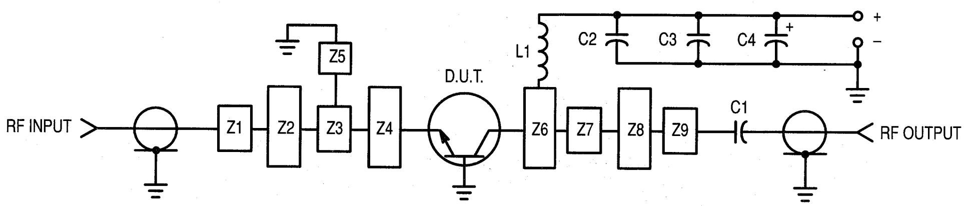
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.11	°C/W

NOTES:
1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as pulsed RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques. (Worst Case θ_{JC} measured using Mode–S pulse train, 128 µs burst 0.5 µs on, 0.5 µs off repeating at 6.4 ms interval.)

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 60 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 60 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 36 Vdc, I_E = 0)	I_{CBO}	—	—	25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 350 W Peak, f = 1090 MHz)	G_{PB}	8.5	9.0	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 350 W Peak, f = 1090 MHz)	η	40	—	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 350 W Peak, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 75 pF 100 Mil Chip Capacitor
C2 — 39 pF 100 Mil Chip Capacitor
C3 — 0.1 µF
C4 — 100 µF, 100 Vdc, Electrolytic
L1 — 3 Turns #18 AWG, 1/8″ ID, 0.18 Long

Z1–Z9 — Microstrip, See Details
Board Material — Teflon, Glass Laminate
Dielectric Thickness = 0.030″
ε_r = 2.55, 2 Oz. Copper

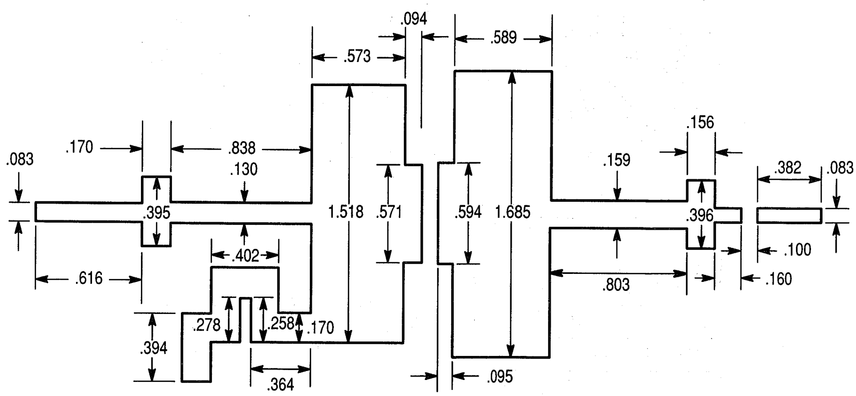
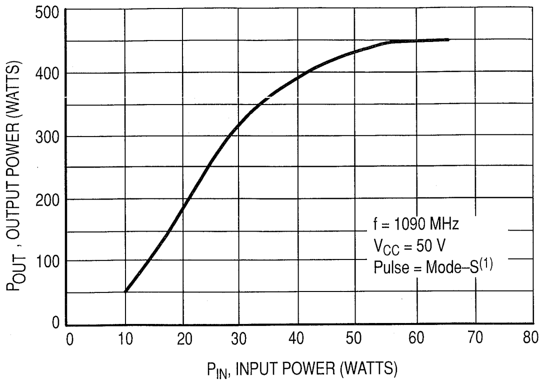
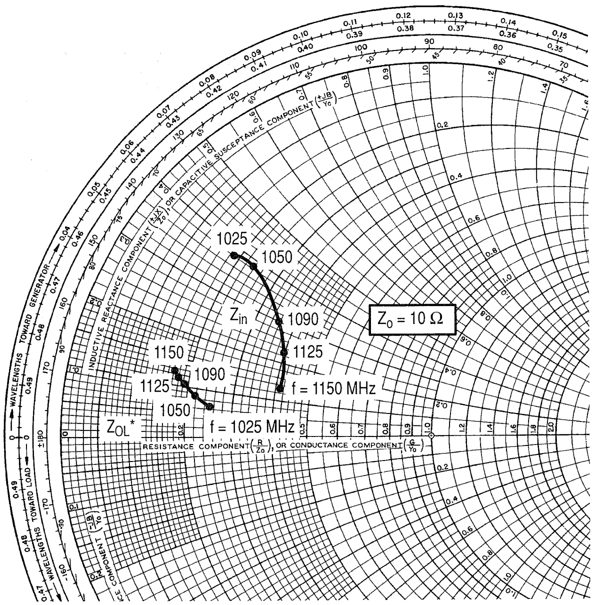


Figure 1. Test Circuit



(1) 128 µs burst 0.5 µs on, 0.5 µs off repeating at 6.4 ms interval.

Figure 2. Output Power versus Input Power



P_{OUT} = 350 W Pk V_{CC} = 50 V

f MHz	Z_{in} OHMS	Z_{OL}* (1) OHMS
1025	1.92 + j3.80	2.52 + j0.70
1050	2.44 + j3.92	2.18 + j0.85
1090	3.55 + j3.02	1.94 + j1.13
1125	4.11 + j2.27	1.80 + j1.22
1150	4.13 + j1.35	1.71 + j1.31

Z_{OL}* is the conjugate of the optimum load impedance into which the device operates at a given output power voltage and frequency.

Figure 3. Series Equivalent Input/Output Impedances

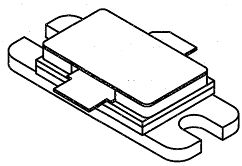
The RF Line
Microwave Pulse Power Transistors

. . . designed for 1025–1150 MHz pulse common base amplifier applications such as TCAS, TACAN and Mode–S transmitters.

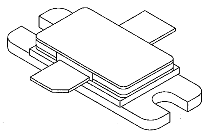
- Guaranteed Performance @ 1090 MHz
  Output Power = 500 Watts Peak
  Gain = 8.5 dB Min, 9.0 dB (Typ)
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Package
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Internal Input and Output Matching
- Characterized with 10 μs, 1% Duty Cycle Pulses

MRF10500
MRF10501

500 W (PEAK)
1025–1150 MHz
MICROWAVE POWER
TRANSISTORS
NPN SILICON



CASE 355D–02, STYLE 1
MRF10500



CASE 355H–01, STYLE 1
MRF10501

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	65	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Peak (1)	I_C	29	Adc
Total Device Dissipation @ T_C = 25°C (1), (2) Derate above 25°C	P_D	1460 8.3	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +200	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

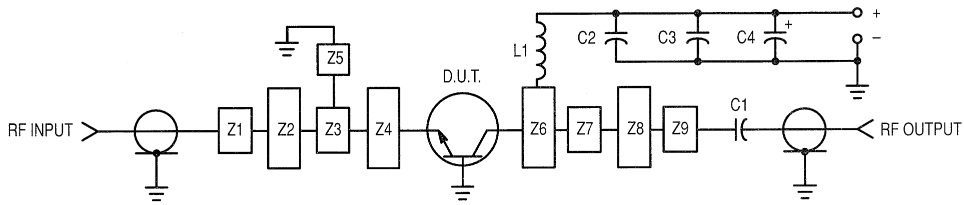
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.12	°C/W

NOTES:
1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as pulsed RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques. (Worst case θ_{JC} value measured @ 32 μs, 2%.)

REV 6

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 60 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 60 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 36 Vdc, I_E = 0)	I_{CBO}	—	—	25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 500 W Peak, f = 1090 MHz)	G_{PB}	8.5	9.0	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 500 W Peak, f = 1090 MHz)	η	40	45	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 500 W Peak, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 82 pF 100 Mil Chip Capacitor
C2 — 39 pF 100 Mil Chip Capacitor
C3 — 0.1 µF
C4 — 100 µF, 100 Vdc, Electrolytic
L1 — 3 Turns #18 AWG, 1/8″ ID, 0.18 Long

Z1–Z9 — Microstrip, See Details
Board Material — Teflon, Glass Laminate
Dielectric Thickness = 0.030″
ε_r = 2.55, 2 Oz. Copper

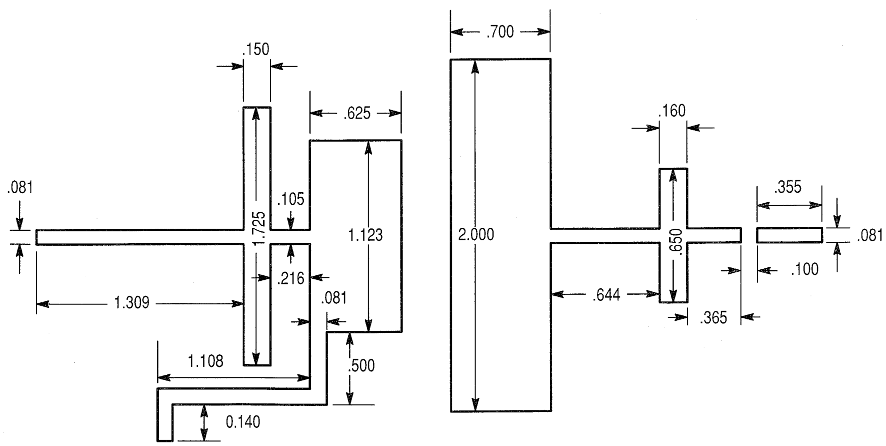


Figure 1. Test Circuit

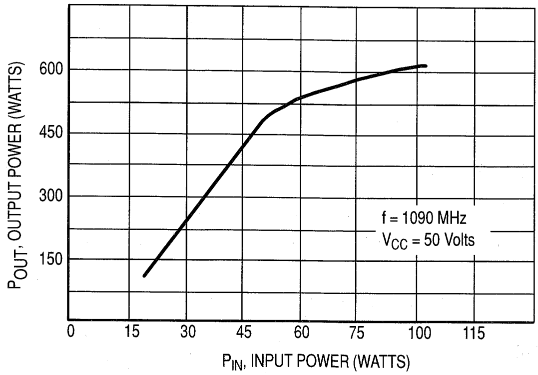
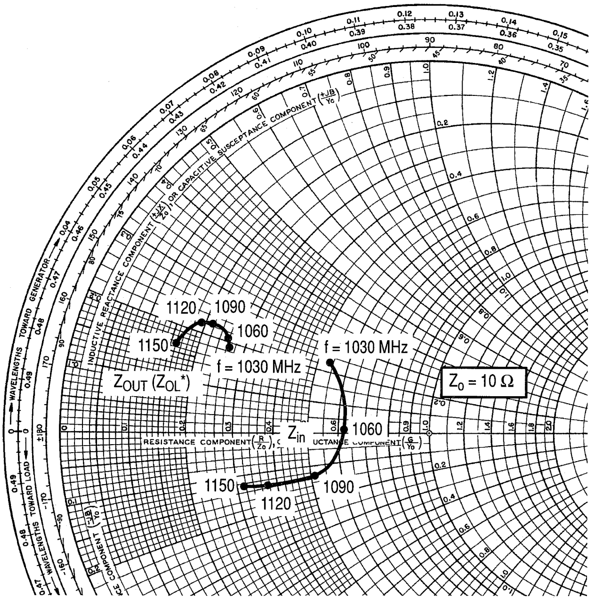


Figure 2. Output Power versus Input Power



P_{OUT} = 500 W Pk V_{CC} = 50 V

f MHz	Z_{in} OHMS	Z_{OL}* (Z_{OUT}) OHMS
1030	5.3 + j2.25	2.6 + j1.89
1060	6.2 + j0.2	2.56 + j2.0
1090	5.2 – j1.4	2.12 + j2.2
1120	3.7 – j1.35	1.9 + j2.15
1150	3.15 – j1.3	1.6 + j1.62

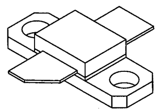
Z_{OL}* is the conjugate of the optimum load impedance into which the device operates at a given output power voltage and frequency.

Figure 3. Series Equivalent Input/Output Impedances

The RF Line
NPN Silicon RF Power Transistor

MRF15030

30 W, 1.5 GHz
RF POWER TRANSISTOR
NPN SILICON



CASE 395C–01, STYLE 1

Designed for 26 volts microwave large–signal, common emitter, class A and class AB linear amplifier applications in industrial and commercial FM/AM equipment operating in the range 1400–1600 MHz.

- Specified 26 Volts, 1490 MHz, Class AB Characteristics:
  Output Power — 30 Watts
  Gain — 9 dB Min @ 30 Watts (PEP)
  Efficiency — 30% Min @ 30 Watts (PEP)
  Intermodulation Distortion — –30 dBc Max @ 30 Watts (PEP)
- Third Order Intercept Point — 53.5 dBm Typ @ 1490 MHz, V_{CE} = 24 Vdc, I_C = 2.5 Adc
- Characterized with Series Equivalent Large–Signal Parameters from 1400–1600 MHz
- Characterized with Small Signal S–Parameters from 1000–2000 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at all Phase Angles with 3:1 Load VSWR @ 28 Vdc, at Rated Output Power
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Collector–Current — Continuous	I_C	10	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.71	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.40	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	25	29	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	64	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, R_{BE} = 100 Ω)	$V_{(BR)CER}$	30	52	—	Vdc

(continued)

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS — continued					
Emitter–Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	5	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	35	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	38	—	pF
FUNCTIONAL TESTS (Figure 12)					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 30 W (PEP), I_{CQ} = 125 mA, f_1 = 1490 MHz, f_2 = 1490.1 MHz)	G_{pe}	9.0	9.6	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 30 W (PEP), I_{CQ} = 125 mA, f_1 = 1490 MHz, f_2 = 1490.1 MHz)	η	30	34	—	%
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 30 W (PEP), I_{CQ} = 125 mA, f_1 = 1490 MHz, f_2 = 1490.1 MHz)	IMD	—	– 34	– 30	dBc
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 30 W (PEP), I_{CQ} = 125 mA, f_1 = 1490 MHz, f_2 = 1490.1 MHz)	IRL	12	15	—	dB
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 30 W (PEP), I_{CQ} = 125 mA, f_1 = 1490 MHz, f_2 = 1490.1 MHz, Load VSWR = 3:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			

TYPICAL CHARACTERISTICS

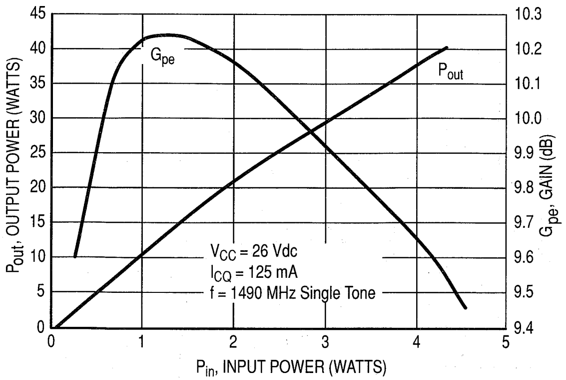


Figure 1. Output Power & Power Gain versus Input Power

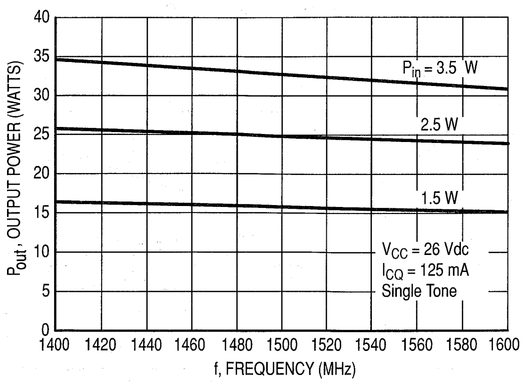


Figure 2. Output Power versus Frequency

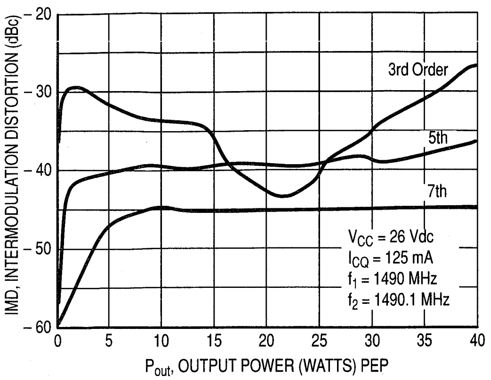


Figure 3. Intermodulation Distortion versus Output Power

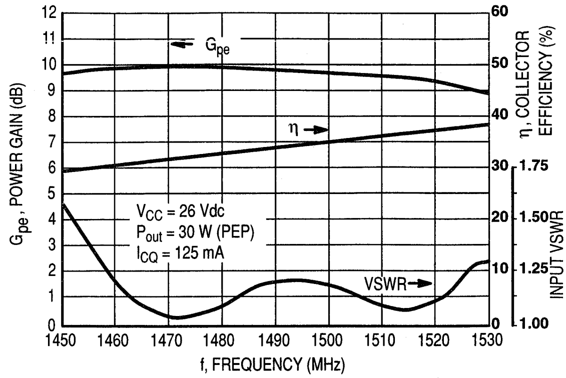


Figure 4. Performance in Broadband Circuit

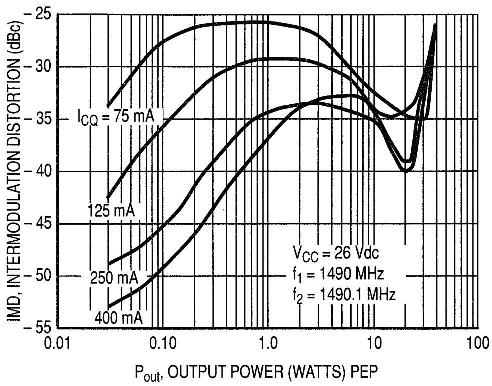


Figure 5. Intermodulation Distortion versus Output Power

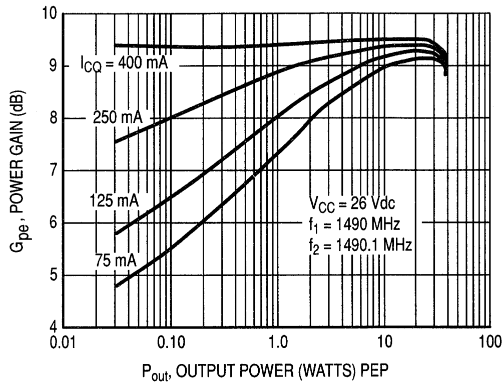


Figure 6. Power Gain versus Output Power

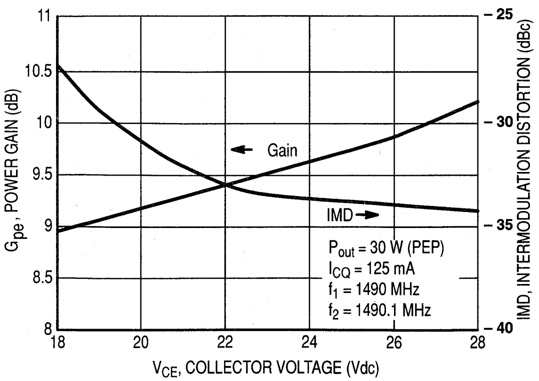


Figure 7. Power Gain and Intermodulation Distortion versus Collector Voltage

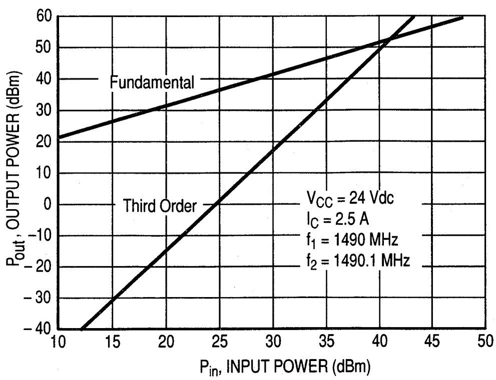


Figure 8. Class A Third Order Intercept Point

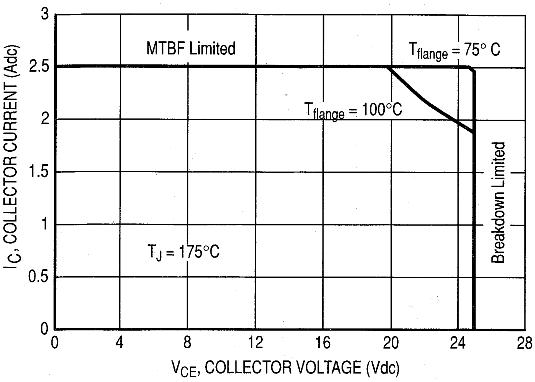


Figure 9. DC Safe Operating Area

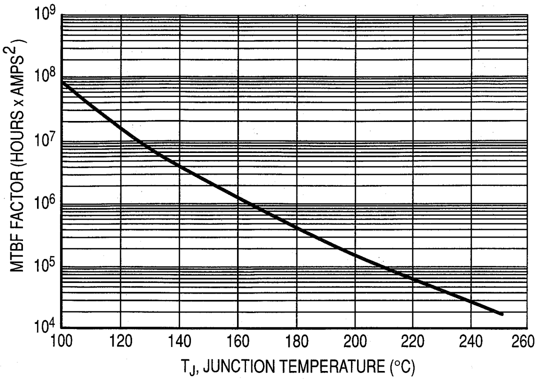
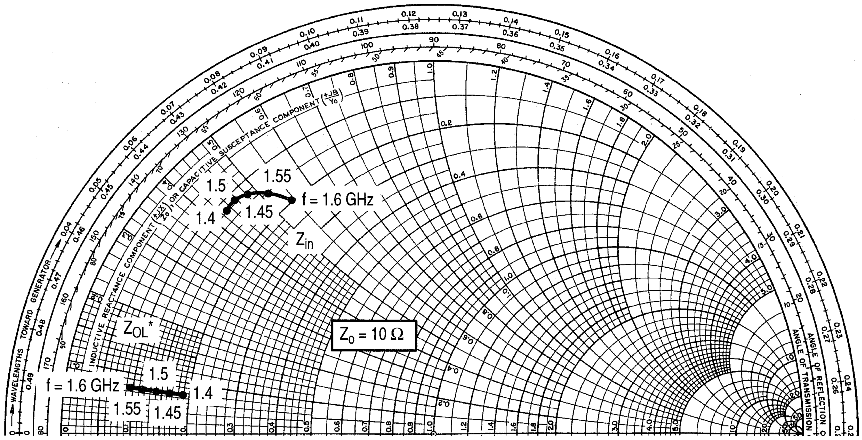


Figure 10. MTBF Factor versus Junction Temperature

The above graph displays calculated MTBF in hours x ampere^2 emitter current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTBF Factor by $I_C{}^2$ for MTBF in a particular application.



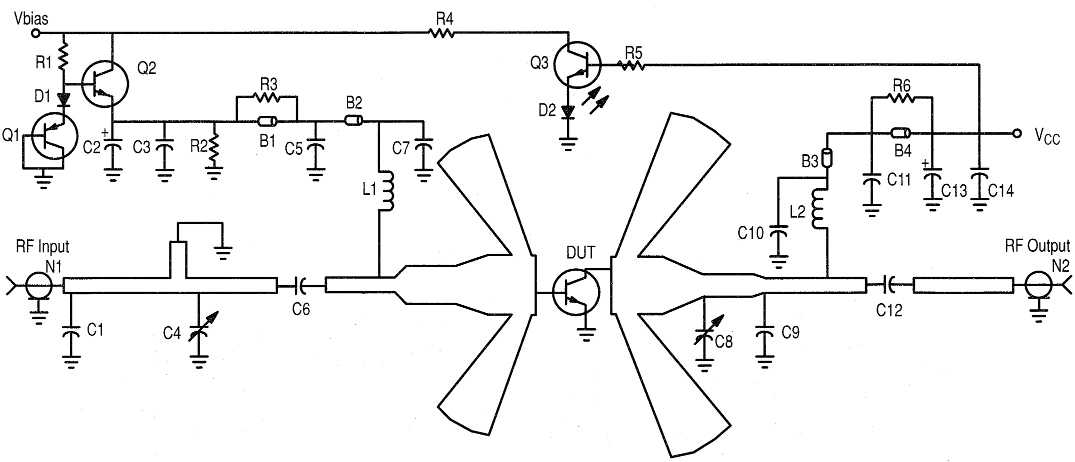
f (GHz)	Z_{in} (Ω)	Z^*_{OL} (Ω)
1.40	1.15 + j4.25	1.87 + j0.78
1.45	1.15 + j4.55	1.67 + j0.78
1.50	1.20 + j4.80	1.47 + j0.78
1.55	1.45 + j5.15	1.27 + j0.78
1.60	1.89 + j5.25	1.00 + j0.78

Z^*_{OL} = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 11. Input and Output Impedances with Circuit Tuned for Maximum Gain @ P_{out} = 30 Watts (PEP), V_{CC} = 26 Volts, I_{CQ} = 125 mA, and Driven by Two Equal Amplitude Tones with Separation of 100 KHz

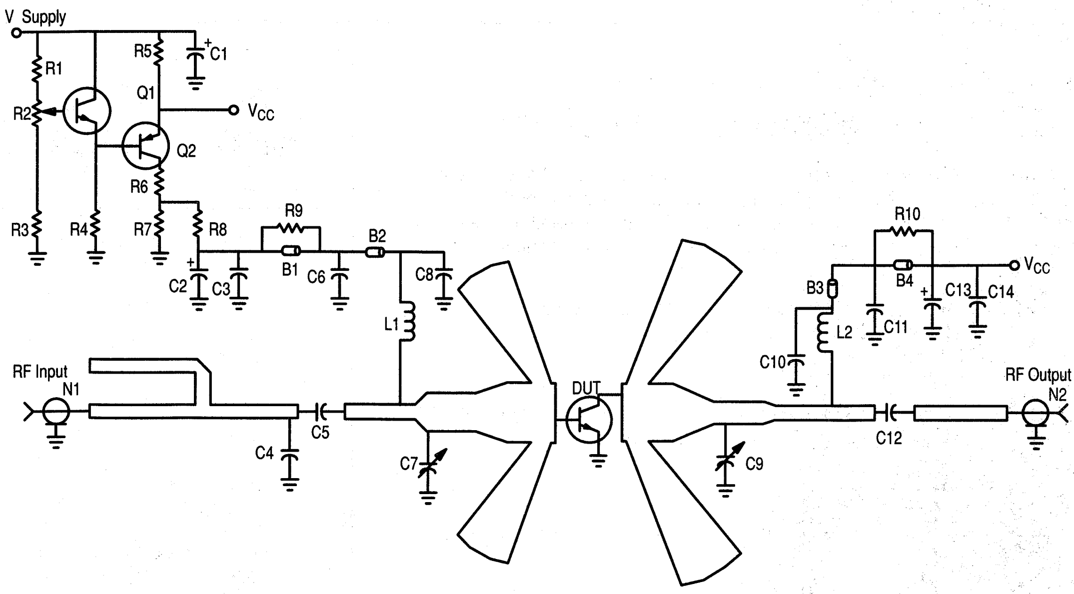
Table 1. Small Signal S Parameters at V_{CE} = 24 Vdc, I_C = 2.5 Adc

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1000	0.983	173	0.366	49	0.006	36	0.890	178
1050	0.984	172	0.367	46	0.007	33	0.893	178
1100	0.978	172	0.367	43	0.007	33	0.888	178
1150	0.975	171	0.373	40	0.007	30	0.885	178
1200	0.975	171	0.382	36	0.008	31	0.886	177
1250	0.969	170	0.391	33	0.007	27	0.881	177
1300	0.963	169	0.408	29	0.008	21	0.879	177
1350	0.955	169	0.428	25	0.009	20	0.879	177
1400	0.945	168	0.452	20	0.008	7	0.873	177
1450	0.933	167	0.487	13	0.009	1	0.875	178
1500	0.915	166	0.525	6	0.009	– 8	0.875	178
1550	0.889	166	0.572	– 3	0.009	–18	0.877	178
1600	0.856	166	0.618	–16	0.009	– 35	0.887	178
1650	0.833	168	0.654	– 30	0.010	– 54	0.901	178
1700	0.820	171	0.654	– 48	0.010	– 86	0.918	178
1750	0.839	174	0.600	– 66	0.010	–120	0.930	177
1800	0.872	175	0.517	– 81	0.010	–152	0.932	176
1850	0.909	176	0.435	– 94	0.010	–176	0.925	174
1900	0.937	175	0.357	–104	0.011	159	0.924	173
1950	0.957	174	0.296	–112	0.012	148	0.917	173
2000	0.970	173	0.247	–119	0.012	136	0.915	173



B1, B4	Long Bead, Fair Rite	D1	Surface Mount Diode, Motorola
B2, B3	Short Bead, Fair Rite	D2	Light Emitting Diode, Industrial Devices
C1	0.3 pF, B Case Chip Capacitor, ATC	L1, L2	3 Turn, 20 AWG, 0.126″ ID Choke
C2	220 μF, Electrolytic Capacitor, Mallory	N1, N2	Type N Flange Mount RF Connector, Omni Spectra
C3, C14	0.1 μF, Chip Capacitor, Kemit	Q1	Transistor PNP Motorola (BD136)
C4, C8	0.8 to 8 pF, Variable Capacitor, Johanson	Q2, Q3	Surface Mount Transistor, NPN, Motorola (MJD47)
C5, C11	1800 pF, Chip Capacitor, Kemit	R1	2 x 330 Ω, 1/8 Watt Chip Resistors in Parallel, Rohm
C6, C12	18 pF, B Case Chip Capacitor, ATC	R2	100 Ω, 1/8 Watt, Chip Resistor, Rohm
C7, C10	51 pF, Chip Capacitor, Murata Erie	R3, R6	4 x 38 Ω, 1/8 Watt, Chip Resistors in Parallel, Rohm
C9	1.7 pF, B Case Chip Capacitor, ATC	R4	39 Ω, 1/8 Watt, Chip Resistor, Rohm
C13	470 μF, Electrolytic Capacitor, Mallory	R5	22 KΩ, 1/8 Watt, Chip Resistor, Rohm
		Board	Glass Teflon®, Arlon GX–0300–55–22, ε_r = 2.55

Figure 12. Class AB Broadband Test Fixture Electrical Schematic



B1, B4	Long Bead, Fair Rite	Q1	Transistor NPN Motorola (BD135)
B2, B3	Short Bead, Fair Rite	Q2	Transistor PNP Motorola (BD136)
C1, C2	100 µF, Electrolytic Capacitor, Mallory	R1	250 Ω, 1/8 Watt, Chip Resistor Rohm
C3, C14	0.1 µF, Chip Capacitor, Kemit	R2	500 Ω, 1/4 Watt Potentiometer, State of the Art
C4	1.3 pF, B Case Chip Capacitor, ATC	R3	4.7 KΩ, 1/8 Watt, Chip Resistor, Rohm
C5, C12	18 pF, B Case Chip Capacitor, ATC	R4	2 x 4.7 KΩ, 1/8 Watt, Chip Resistors in Parallel, Rohm
C6, C11	1800 pF, Chip Capacitor, Kemit	R5	1.0 Ω, 10 Watt, Resistor, Dale
C7, C9	0.8 to 8 pF, Variable Capacitor, Johanson	R6	38 Ω, 1.0 Watt, Resistor
C8, C10	51 pF, Chip Capacitor, Murata Erie	R7	75 Ω, 1/8 Watt, Chip Resistor, Rohm
C13	470 µF, Electrolytic Capacitor, Mallory	R8	2 x 10 Ω, 1/8 Watt, Chip Resistors in Parallel, Rohm
L1, L2	3 Turn, 20 AWG, 0.126″ ID Choke	R9, R10	4 x 38 Ω, 1/8 Watt, Chip Resistors in Parallel, Rohm
N1, N2	Type N Flange Mount RF Connector, Omni Spectra	Board	Glass Teflon®, Arlon GX–0300–55–22, $\varepsilon_r = 2.55$

Figure 13. Class A Test Fixture Electrical Schematic

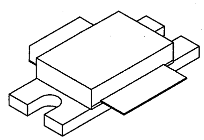
The RF Sub–Micron Bipolar Line
RF Power Bipolar Transistors

MRF15060
MRF15060S

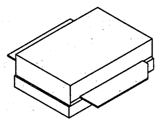
**60 W, 1.49 GHz
RF POWER
BIPOLAR
TRANSISTORS**

Designed for broadband commercial and industrial applications at frequencies from 1400 to 1600 MHz. The high gain and broadband performance of these devices makes them ideal for large–signal, common–emitter class A and class AB amplifier applications in 26 volt amplitude modulated and multi–carrier base station equipment.

- Guaranteed Two–Tone Performance at 1490 MHz, 26 Volts
  Output Power — 60 Watts (PEP)
  Power Gain — 10 dB
  Efficiency — 33%
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 3:1 VSWR @ 26 Vdc, 1490 MHz, 60 Watts (PEP) Output Power



**CASE 451–04, STYLE 1
(MRF15060)**



**CASE 451A–01, STYLE 1
(MRF15060S)**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	60	Adc
Collector Current – Continuous	I_C	8	Adc
Total Device Dissipation @ T_C = 70°C Derate above 70°C	P_D	185 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

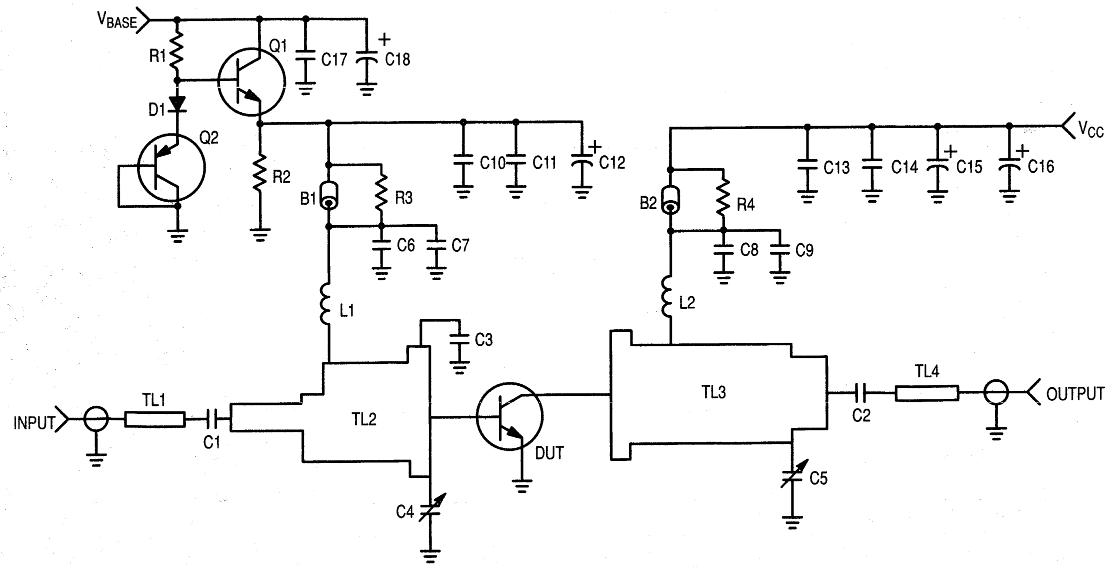
THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	25	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0 mAdc)	$V_{(BR)EBO}$	3	3.5	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	40	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1.0 MHz) (1)	C_{ob}	—	55	—	pF
FUNCTIONAL TESTS (In Motorola Test Circuit. See Figure 1)					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 1490.0 MHz, f_2 = 1490.1 MHz)	G_{pe}	10	11.7	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 1490.0 MHz, f_2 = 1490.1 MHz)	η	33	38	—	dB
3rd Order Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 1490.0 MHz, f_2 = 1490.1 MHz)	IMD	—	– 32	– 28	dB
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 1490.0 MHz, f_2 = 1490.1 MHz)	IRL	12	20	—	dB
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 1490.0 MHz, f_2 = 1490.1 MHz, VSWR = 3:1, at All Phase Angles)	ψ	No Degradation in Output Power			

NOTE: For information only. This part is collector matched.



B1, B2	Short RF Bead Fair Rite–2743019447	D1	Diode, 1N4003
C1, C2, C6, C8	18 pF, Chip Capacitor	L1, L2	3 Turns, 20 AWG, IDIA 0.102″ (17.7 nH)
C3	3.9 pF, Chip Capacitor	Q1	Transistor, NPN BD135
C4, C5	0.6–4.5 pF, Variable Capacitor	Q2	Transistor, PNP BD136
C7, C9	100 pF, Chip Capacitor	R1	120 Ω, 1/4 W Resistor
C10, C13	1000 pF, Chip Capacitor	R2	51 Ω, 1/4 W, Chip Resistor
C11, C14, C17	0.1 μF, 50 Vdc Ceramic Capacitor	R3, R4	4 x 39 Ω, 1/8 W Chip Resistors
C12, C15, C18	10 μF, 50 Vdc Electrolytic Capacitor	TL1–TL4	Microstrip Line See Photomaster
C16	250 μF, 50 Vdc Electrolytic Capacitor	Board	1/32″ Glass Teflon®, Arlon GX–0300–55–22, $\varepsilon_r = 2.55$

Figure 1. MRF15060 RF Test Fixture Schematic

TYPICAL CHARACTERISTICS

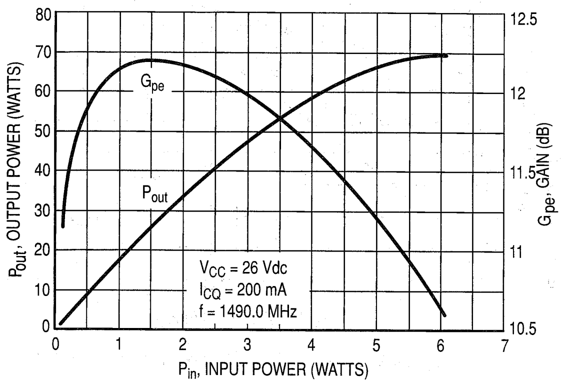


Figure 2. Output Power & Power Gain versus Input Power

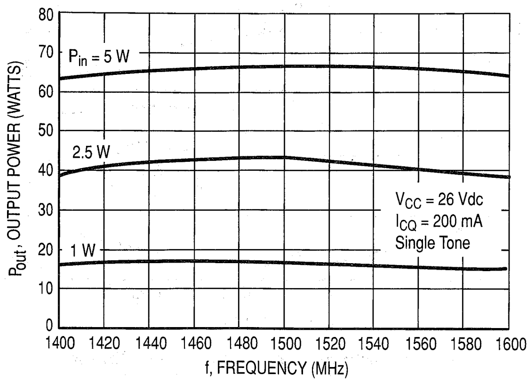


Figure 3. Output Power versus Frequency

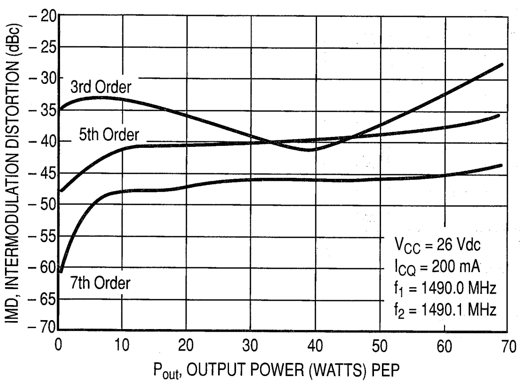


Figure 4. Intermodulation Distortion versus Output Power

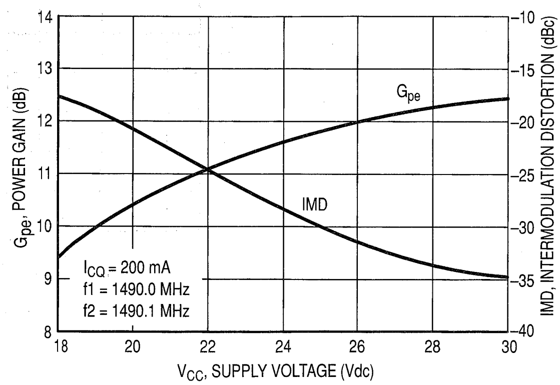


Figure 5. Power Gain and Intermodulation Distortion versus Supply Voltage

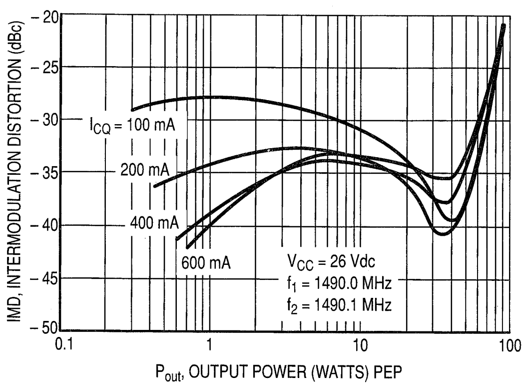


Figure 6. Intermodulation Distortion versus Output Power

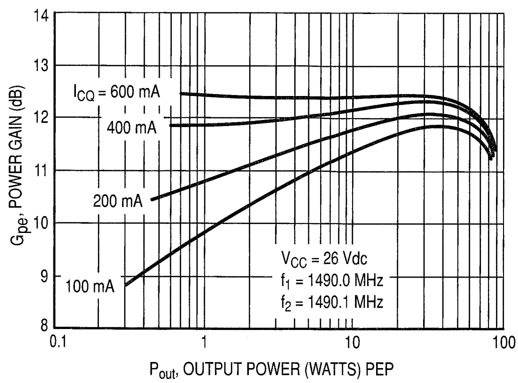


Figure 7. Power Gain versus Output Power

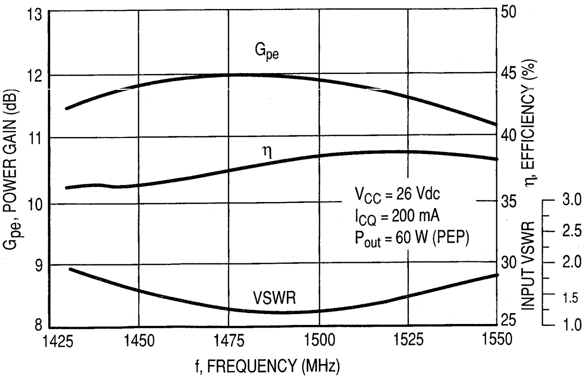


Figure 8. Performance in Broadband Circuit

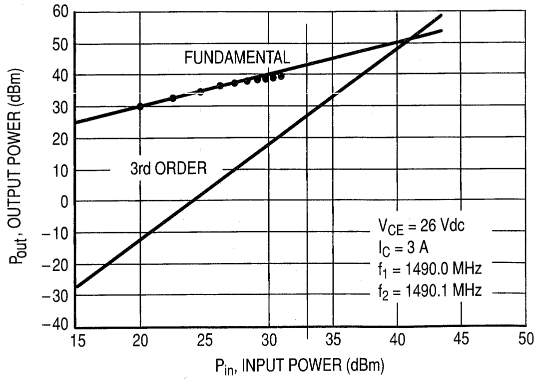


Figure 9. Class A Third Order Intercept Point

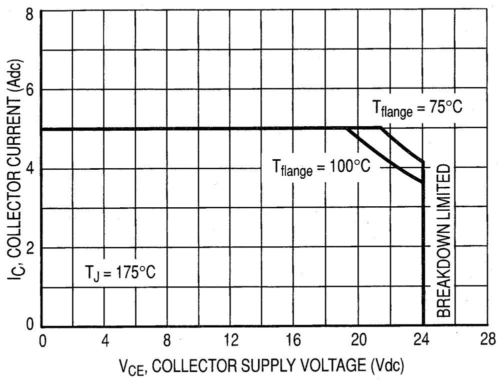
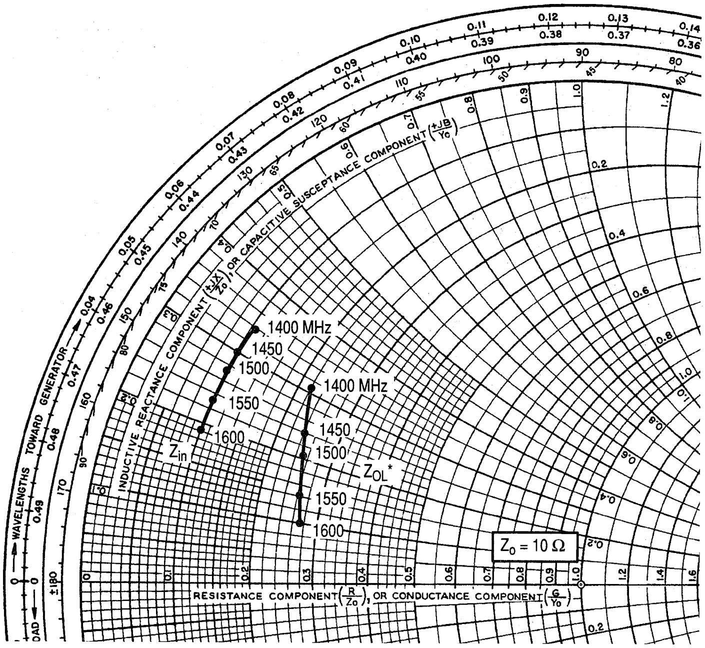


Figure 10. DC Safe Operating Area



V_{CC} = 26 Vdc, I_{CQ} = 200 mA, P_{out} = 60 Watts PEP

f MHz	Z_{in}(1) Ohms	Z_{OL}* Ohms
1400	1.07 + j3.4	2.25 + j3.1
1450	1.04 + j3.0	2.37 + j2.4
1500	1.01 + j2.7	2.46 + j2.1
1550	0.99 + j2.3	2.54 + j1.4
1600	0.97 + j1.9	2.66 + j1.0

Z_{in}(1) = Conjugate of fixture base impedance.

Z_{OL}* = Conjugate of the optimum load impedance at given output power, voltage, bias current and frequency.

Figure 11. Series Equivalent Input and Output Impedence

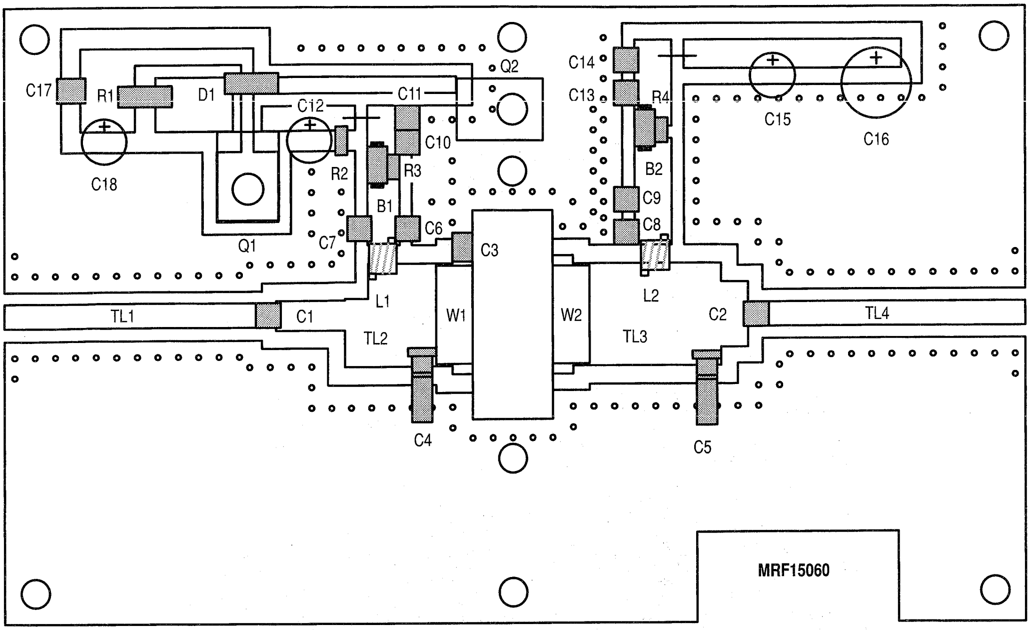


Figure 12. MRF15060 Component Parts Layout

Table 1. Typical Common Emitter S–Parameters (V_{CC} = 26 V)

I_D = 3.0 A

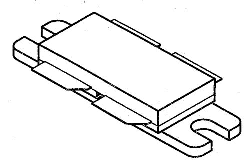
f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠φ	$\|S_{21}\|$	∠φ	$\|S_{12}\|$	∠φ	$\|S_{22}\|$	∠φ
1000	0.964	163	0.28	93	0.018	73	0.991	178
1050	0.958	162	0.30	87	0.018	76	0.989	178
1100	0.957	161	0.31	82	0.017	81	0.987	179
1150	0.956	160	0.34	76	0.022	73	0.982	179
1200	0.955	158	0.38	70	0.023	67	0.969	179
1250	0.953	157	0.42	62	0.022	57	0.956	180
1300	0.941	155	0.47	53	0.019	60	0.937	180
1350	0.922	154	0.55	43	0.015	64	0.915	-180
1400	0.920	153	0.67	28	0.013	66	0.891	-180
1450	0.901	152	0.80	6	0.012	71	0.880	-180
1500	0.903	151	0.83	-24	0.007	76	0.911	-179
1550	0.906	152	0.70	-54	0.008	89	0.954	-180
1600	0.913	153	0.51	-75	0.009	92	0.971	-180
1650	0.921	154	0.38	-89	0.010	95	0.973	-179
1700	0.946	154	0.29	-98	0.012	97	0.974	-179
1750	0.974	155	0.34	-107	0.014	105	0.976	-178
1800	0.968	154	0.19	-115	0.016	116	0.977	-178
1850	0.966	153	0.16	-121	0.018	138	0.978	-177
1900	0.947	152	0.14	-128	0.021	143	0.980	-177
1950	0.918	151	0.12	-138	0.027	151	0.982	-177
2000	0.912	150	0.09	-146	0.031	159	0.985	-176

Advance Information

The RF Line
NPN Silicon RF Power Transistor

MRF15090

90 W, 1.5 GHz
RF POWER TRANSISTOR
NPN SILICON



CASE 375A–01, STYLE 1

Designed for 26 volts microwave large–signal, common emitter, class A and class AB linear amplifier applications in industrial and commercial FM/AM equipment operating in the range 1400–1600 MHz.

- Specified 26 Volts, 1490 MHz, Class AB Characteristics
  Output Power — 90 Watts (PEP)
  Gain — 7.5 dB Min @ 90 Watts (PEP)
  Collector Efficiency — 30% Min @ 90 Watts (PEP)
  Intermodulation Distortion — –28 dBc Max @ 90 Watts (PEP)
- Third Order Intercept Point — 56.5 dBm Typ @ 1490 MHz, V_{CE} = 24 Vdc, I_C = 5 Adc
- Characterized with Series Equivalent Large–Signal Parameters from 1400–1600 MHz
- Characterized with Small–Signal S–Parameters from 1000–2000 MHz
- Silicon Nitride Passivated
- 100% Tested for Load Mismatch Stress at All Phase Angles with 3:1 Load VSWR @ 28 Vdc, and Rated Output Power
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Collector–Current — Continuous @ $T_{J(max)}$ = 150°C	I_C	15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	25	28	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	65	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, R_{BE} = 100 Ω)	$V_{(BR)CER}$	30	—	—	Vdc

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 6

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS — continued					
Emitter–Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	4.8	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	40	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1 MHz) – For Information Only. This Part Is Collector Matched.	C_{ob}	—	52	—	pF
FUNCTIONAL TESTS (Figure 12)					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 90 W (PEP), I_{CQ} = 250 mA, f_1 = 1490 MHz, f_2 = 1490.1 MHz)	G_{pe}	7.5	8.3	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 90 W (PEP), I_{CQ} = 250 mA, f_1 = 1490 MHz, f_2 = 1490.1 MHz)	η	30	36	—	%
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 90 W (PEP), I_{CQ} = 250 mA, f_1 = 1490 MHz, f_2 = 1490.1 MHz)	IMD	—	– 32	– 28	dBc
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 90 W (PEP), I_{CQ} = 250 mA, f_1 = 1490 MHz, f_2 = 1490.1 MHz)	IRL	12	15	—	dB
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 90 W (PEP), I_{CQ} = 250 mA, f_1 = 1490 MHz, f_2 = 1490.1 MHz, Load VSWR = 3:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			

TYPICAL CHARACTERISTICS

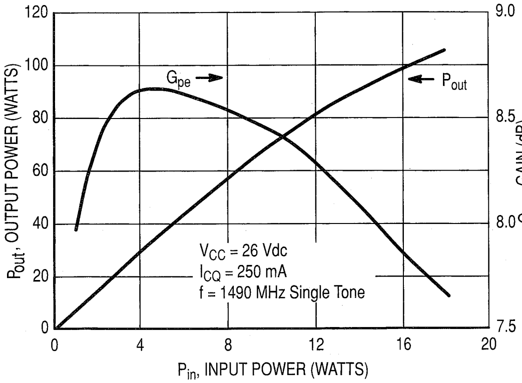


Figure 1. Output Power & Power Gain versus Input Power

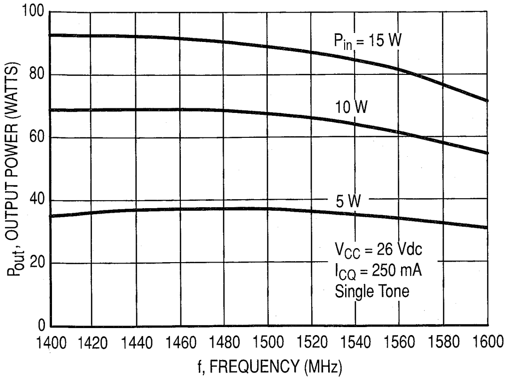


Figure 2. Output Power versus Frequency

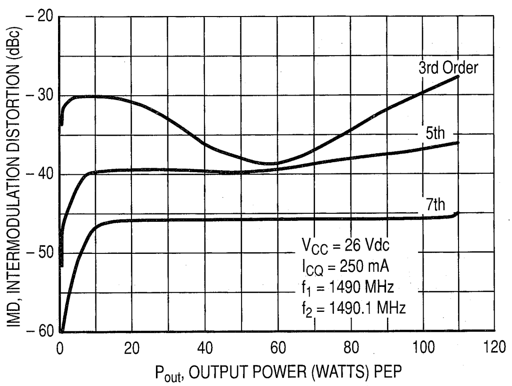


Figure 3. Intermodulation Distortion versus Output Power

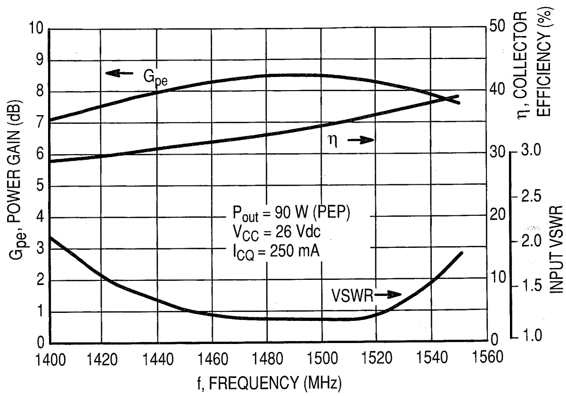


Figure 4. Performance in Broadband Circuit

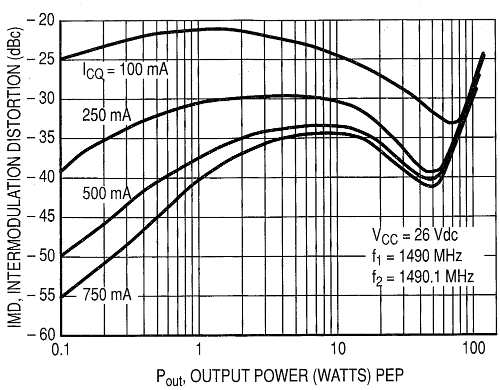


Figure 5. Intermodulation Distortion versus Output Power

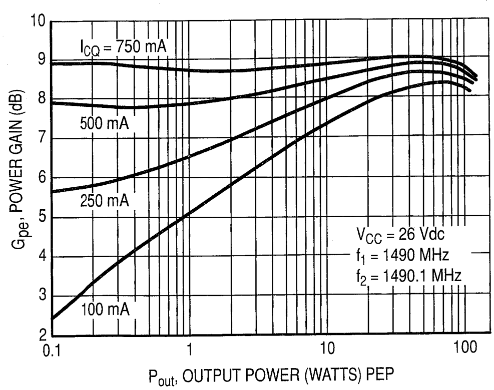


Figure 6. Power Gain versus Output Power

TYPICAL CHARACTERISTICS

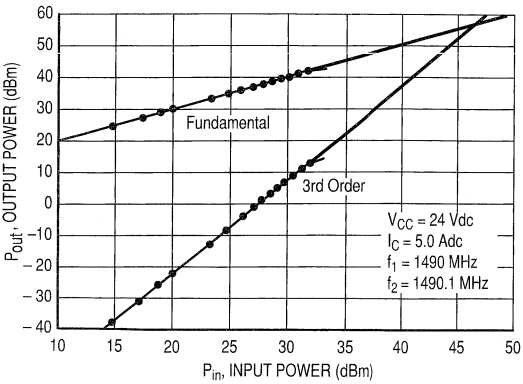


Figure 7. Class A Third Order Intercept Point

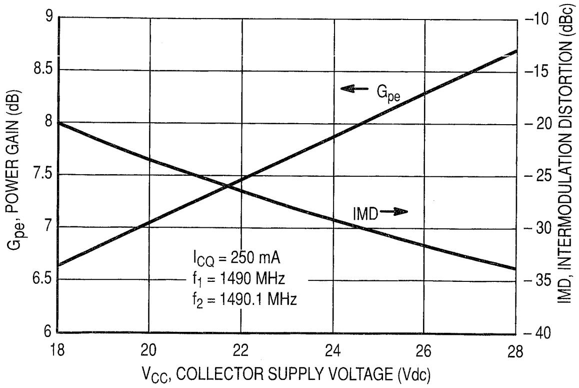


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage

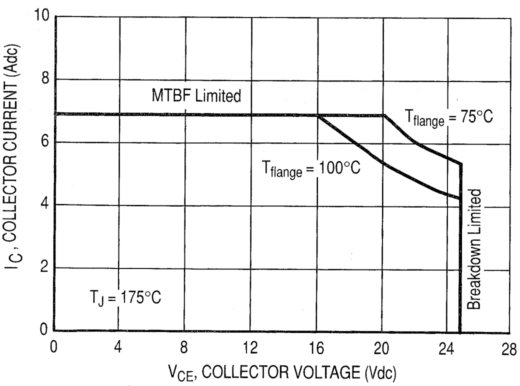


Figure 9. DC Safe Operating Area

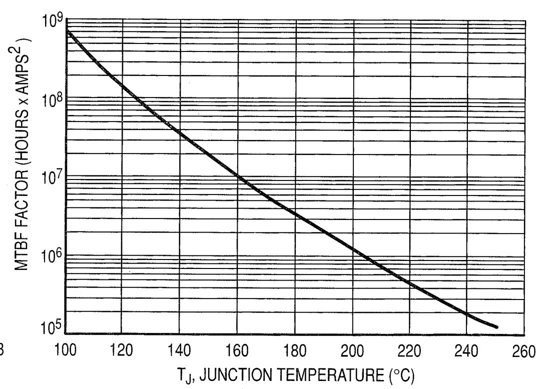
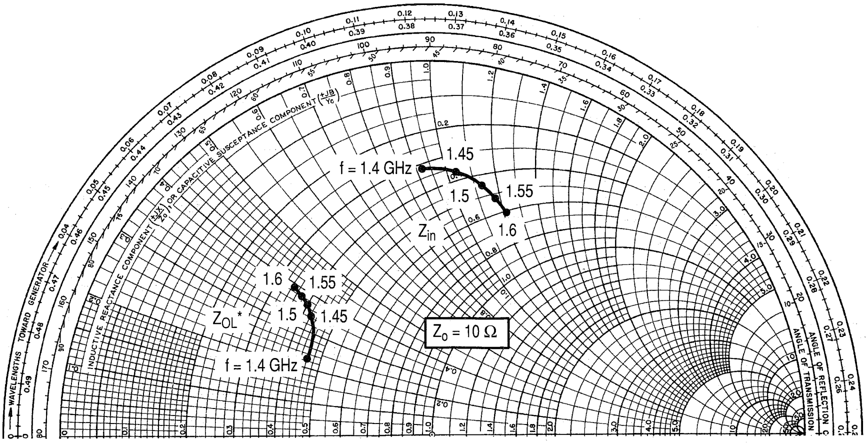


Figure 10. MTBF Factor versus Junction Temperature

The graph above displays calculated MTBF in hours x ampere^2 emitter current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTBF Factor by I_C^2 for MTBF in a particular application.



f (MHz)	Zin (Ω)	ZOL* (Ω)
1400	3.28 + j9.07	4.62 + j2.23
1450	3.85 + j10.4	4.35 + j3.41
1500	4.55 + j11.4	4.08 + j3.60
1550	5.45 + j11.9	3.80 + j3.78
1600	6.20 + j12.2	3.55 + j3.84

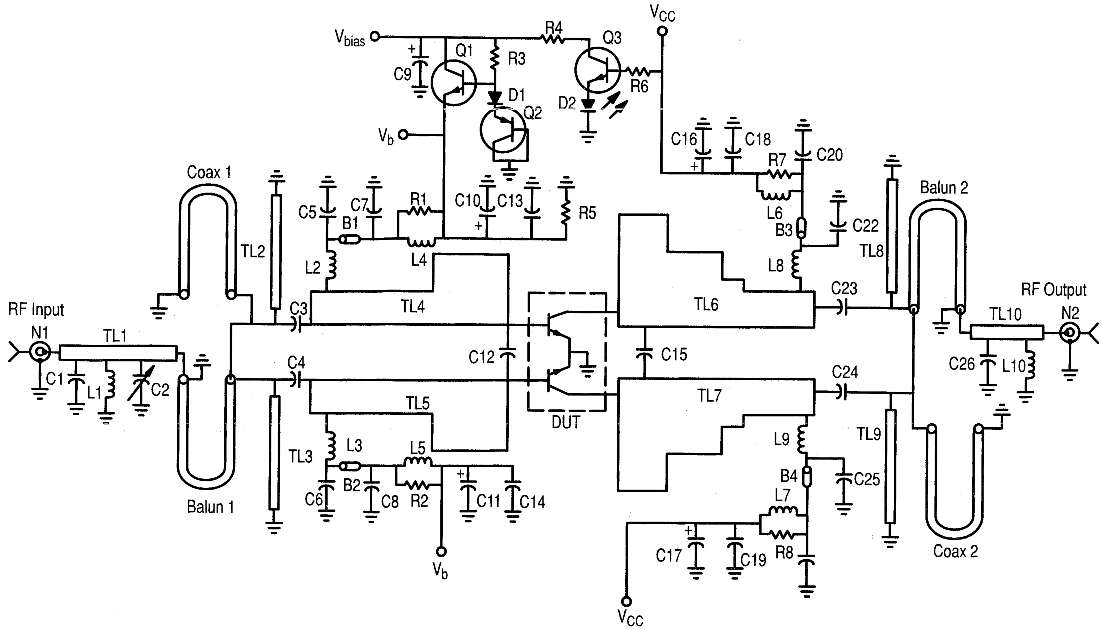
Z_{in} = Input impedance is a balanced base to base measurement.

Z_{OL}^* = Conjugate of optimum load impedance collector to collector into which the device operates at a given output power, bias current, voltage and frequency.

Figure 11. Input and Output Impedances with Circuit Tuned for Maximum Gain @ P_{out} = 90 Watts (PEP), V_{CC} = 26 Volts, I_{CQ} = 250 mA, and Driven by Two Equal Amplitude Tones with Separation of 100 KHz

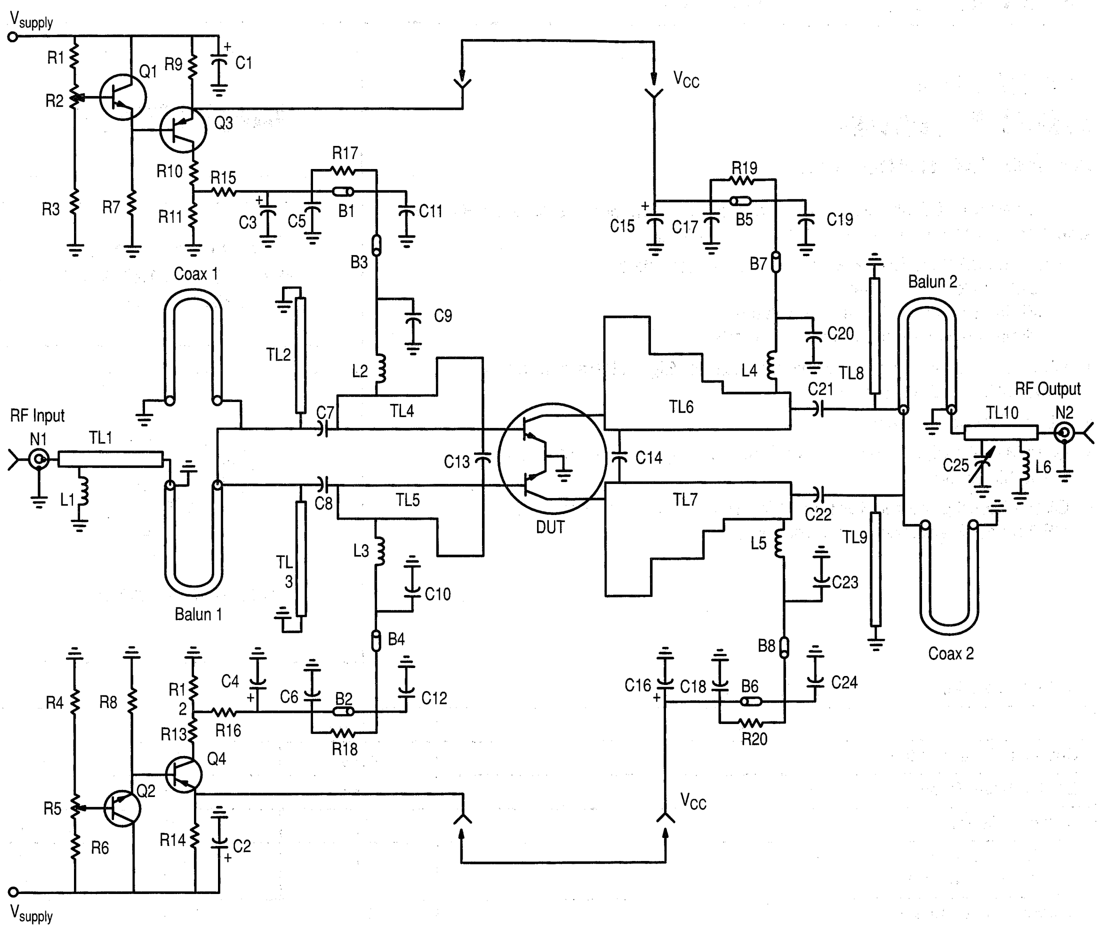
Table 1. Common Emitter S–Parameters (for One Side of Push–Pull MRF15090) at V_{CE} = 24 Vdc, I_C = 2.5 Adc

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1000	0.999	172	0.164	108	0.006	72	0.957	173
1050	0.999	171	0.179	103	0.007	69	0.956	172
1100	0.994	170	0.196	97	0.007	66	0.948	172
1150	0.992	170	0.216	92	0.008	63	0.940	171
1200	0.994	169	0.241	86	0.008	62	0.935	171
1250	0.986	168	0.269	80	0.009	57	0.924	170
1300	0.982	167	0.306	73	0.010	51	0.915	170
1350	0.973	166	0.351	66	0.011	45	0.905	170
1400	0.957	164	0.408	56	0.012	33	0.888	170
1450	0.938	163	0.483	44	0.013	22	0.876	170
1500	0.903	162	0.571	29	0.014	7	0.859	171
1550	0.857	163	0.651	10	0.014	–13	0.855	173
1600	0.821	165	0.673	–14	0.013	– 40	0.877	174
1650	0.837	169	0.623	– 37	0.011	– 67	0.902	174
1700	0.872	170	0.529	– 56	0.009	–104	0.922	173
1750	0.901	170	0.437	–70	0.008	–138	0.931	172
1800	0.920	170	0.363	– 81	0.007	–165	0.932	171
1850	0.940	169	0.309	– 90	0.008	173	0.930	170
1900	0.954	169	0.265	– 98	0.008	150	0.932	169
1950	0.965	168	0.232	–104	0.009	139	0.930	169
2000	0.971	167	0.205	–110	0.010	132	0.929	168



B1, B2, B3, B4	Ferrite Bead, Ferroxcube	L1	1 Turn, 24 AWG, 0.042″ ID Choke
C1	2.7 pF, B Case Chip Capacitor, ATC	L2, L3, L8, L9	3 Turn, 20 AWG, 0.126″ ID Choke
C2	0.6–4.0 pF, Variable Capacitor, Johanson	L4, L5, L6, L7	12 Turns, 22 AWG, 0.140″ ID Choke
C3, C4, C23, C24	18 pF, B Case Chip Capacitor, ATC	L10	3 Turns, 24 AWG, 0.046″ ID Choke
C5, C6, C22, C25	51 pF, Chip Capacitor, Murata Erie	N1, N2	Type N Flange Mount RF Connector, Omni Spectra
C7, C8, C20, C21	1800 pF, Chip Capacitor, Kemit	Q1, Q3	Transistor, NPN, Motorola (MJD47)
C9, C10, C11	100 μF, Electrolytic Capacitor, Mallory	Q2	Transistor PNP Motorola (BD136)
C12	5.1 pF, A Case Chip Capacitor, ATC	R1, R2, R7, R8	10 Ω, 1/2 W, Resistor
C13, C14, C18, C19	0.1 μF, Chip Capacitor, Kemit	R3	150 Ω, 1/2 W, Resistor
C15	1.1 pF, B Case Chip Capacitor, ATC	R4	2 x 66 Ω, 1/8 W, Chip Resistors in Parallel, Rohm
C16, C17	470 μF, Electrolytic Capacitor, Mallory	R5	93 Ω, 1/8 W, Chip Resistor, Rohm
C26	0.3 pF, B Case Chip Capacitor, ATC	R6	22 KΩ, 1/8 W, Chip Resistor, Rohm
D1	Diode, Motorola (MUR5120T3)	TL1 to TL10	See Photomaster
D2	Light Emitting Diode, Industrial Devices	Board	Glass Teflon®, Arlon GX–0300–55–22, ε_r = 2.55

Figure 12. Class AB Test Fixture Electrical Schematic



B1, B2, B5, B6	Long Bead, Fair Rite	N1, N2	Type N Flange Mount RF Connector, Omni Spectra
B3, B4, B7, B8	Short Bead, Fair Rite	Q1, Q2	Transistor NPN Motorola (BD135)
C1, C2, C3, C4	100 μF, Electrolytic Capacitor, Mallory	Q3, Q4	Transistor PNP Motorola (BD136)
C5, C6, C17, C18	0.1 μF, Chip Capacitor, Kemit	R1, R6	250 Ω, 1/8 W, Chip Resistor, Rohm
C7, C8, C21, C22	18 pF, B Case Chip Capacitor, ATC	R2, R5	500 Ω, 1/4 W, Potentiometer, State of the Art
C9, C10, C20, C23	51 pF, Chip Capacitor, Murata Erie	R3, R4	4.7 Ω, 1/8 W, Chip Resistor, Rohm
C11, C12, C19, C24	1800 pF, Chip Capacitor, Kemit	R7, R8	2 x 4.7 KΩ, 1/8 W, Chip Resistors in Parallel, Rohm
C13	4.3 pF, B Case Chip Capacitor, ATC		
C14	2.0 pF, B Case Chip Capacitor, ATC	R9, R14	1.0 Ω, 10 W, Resistor, Dale
C15, C16	470 μF, Electrolytic Capacitor, Mallory	R10, R13	38 Ω, 1 W, Resistor
C25	0.6–4 pF Variable Capacitor, Johanson	R11, R12	75 Ω, 1/8 W, Chip Resistor, Rohm
L1	3 Turns, 24 AWG, 0.046″ ID Choke	R15, R16	2 x 10 Ω, 1/8 W, Chip Resistors in Parallel, Rohm
L2, L3, L4, L5	3 Turns, 20 AWG, 0.126″ ID Choke	R17, R18, R19, R20	4 x 38 Ω, 1/8 W, Chip Resistors in Parallel, Rohm
L6	2 Turns, 24 AWG, 0.042″ ID Choke	Board	Glass Teflon®, Arlon GX–0300–55–22, $\varepsilon_r = 2.55$

Figure 13. Class A Test Fixture Electrical Schematic

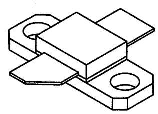
The RF Line
NPN Silicon
RF Power Transistor

MRF16006

Designed for 28 Volt microwave large–signal, common base, Class–C CW amplifier applications in the range 1600 – 1640 MHz.

- Specified 28 Volt, 1.6 GHz Class–C Characteristics
  Output Power = 6 Watts
  Minimum Gain = 7.4 dB, @ 6 Watts
  Minimum Efficiency = 40% @ 6 Watts
- Characterized with Series Equivalent Large–Signal Parameters from 1500 MHz to 1700 MHz
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

6.0 WATTS, 1.6 GHz
RF POWER TRANSISTOR
NPN SILICON



CASE 395C–01, STYLE 2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current	I_C	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	26 0.15	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

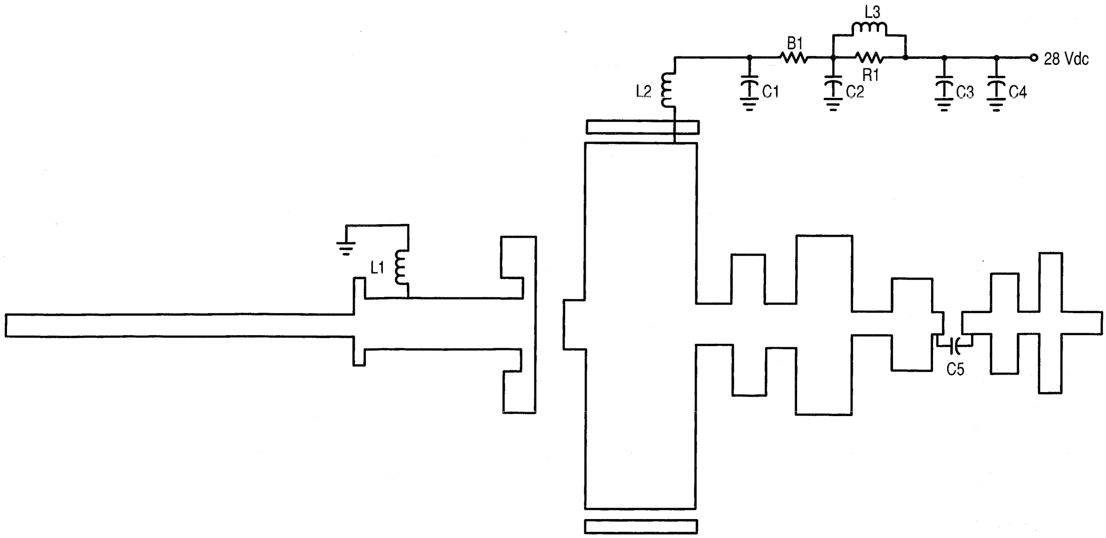
Thermal Resistance — Junction to Case (1) (2)	$R_{\theta JC}$	6.8	°C/W

(1) Thermal measurement performed using CW RF operating condition.
(2) Thermal resistance is determined under specified RF operating conditions by infrared measurement techniques.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

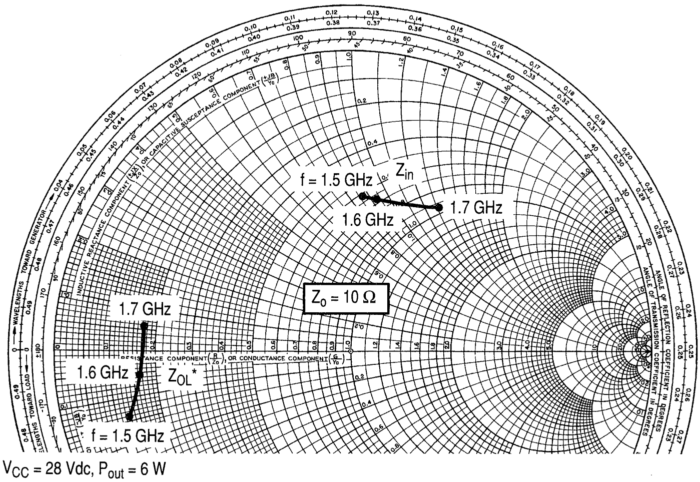
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 40 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 40 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 2.5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (VCE = 28 Vdc, V_{BE} = 0)	I_{CES}	—	—	2.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 0.2 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB}= 28 Vdc, f = 1.0 MHz)	C_{ob}	11	—	—	pf
FUNCTIONAL TESTS					
Common–Base Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 6 Watts, f = 1600/1640 MHz)	G_{pe}	7.4	—	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 6 Watts, f = 1600/1640 MHz)	η	40	45	—	%
Return Loss (V_{CC} = 28 Vdc, P_{out} = 6 Watts, f = 1600/1640 MHz)	I_{RL}	—	8.0	—	dB
Output Mismatch Stress (V_{CC} = 28 Vdc, P_{out} = 6 Watts, f = 1600 MHz, Load VSWR = 3:1 all phase angles at frequency of test)	ψ	No Degradation in Output Power			



Board Material – Teflon® Glass Laminate Dielectric
Thickness – 0.30″, ε_r = 2.55″, 2.0 oz. Copper

B1	Fair Rite Bead on #24 Wire	C4	47 µF, 50 V, Electrolytic Cap
C1, C5	100 pF, B Case, ATC Chip Cap	L1, L2	3 Turns, #18, 0.133″ ID, 0.15″ Long
C2	0.1 µF, Dipped Mica Cap	L3	9 Turns, #24 Enamel
C3	0.1 µF, Chip Cap	R1	82 Ω, 1.0 W, Carbon Resistor

Figure 1. MRF16006 Test Fixture Schematic



V_{CC} = 28 Vdc, P_{out} = 6 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
1500	6.28 + j 8.53	1.22 – j 1.37
1600	7.04 + j 9.00	1.58 – j 0.53
1700	9.55 + j 12.86	1.71 + j 0.39

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 2. Series Equivalent Input/Output Impedance

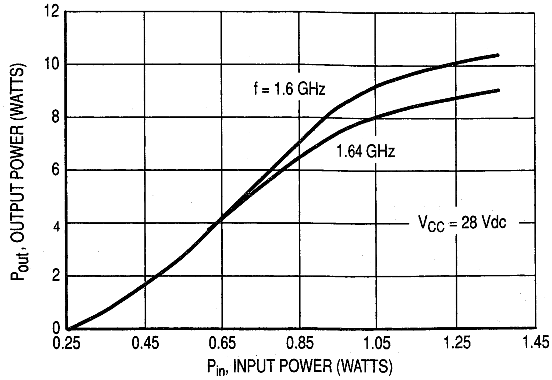


Figure 3. Output Power versus Input Power

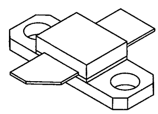
The RF Line
NPN Silicon
RF Power Transistor

MRF16030

Designed for 28 Volt microwave large–signal, common base, Class–C CW amplifier applications in the range 1600 – 1640 MHz.

- Specified 28 Volt, 1.6 GHz Class–C Characteristics
  Output Power = 30 Watts
  Minimum Gain = 7.5 dB, @ 30 Watts
  Minimum Efficiency = 40% @ 30 Watts
- Characterized with Series Equivalent Large–Signal Parameters from 1500 MHz to 1700 MHz
- Silicon Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

30 WATTS, 1.6 GHz
RF POWER TRANSISTOR
NPN SILICON



CASE 395C–01, STYLE 2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	60	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector–Current	I_C	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	103 0.58	Watts °C/W
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

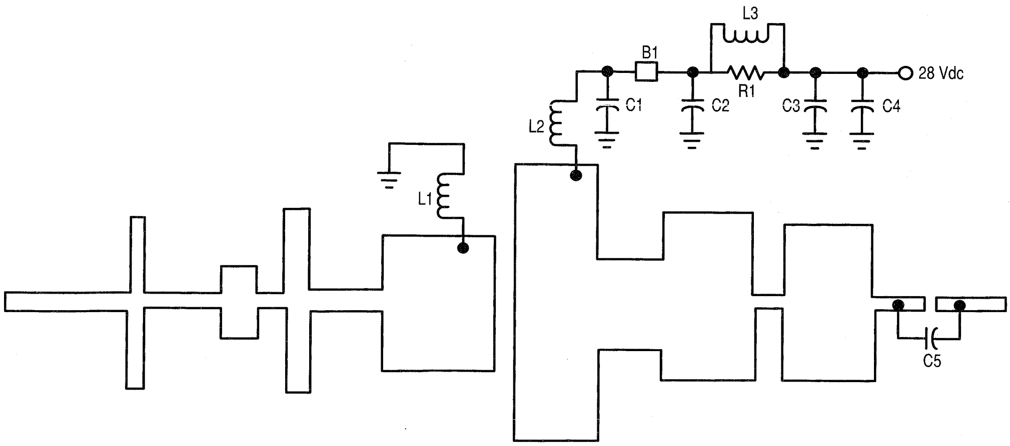
Thermal Resistance — Junction to Case (1) (2)	$R_{\theta JC}$	1.7	°C/W

(1) Thermal measurement performed using CW RF operating condition.
(2) Thermal resistance is determined under specified RF operating conditions by infrared measurement techniques.

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

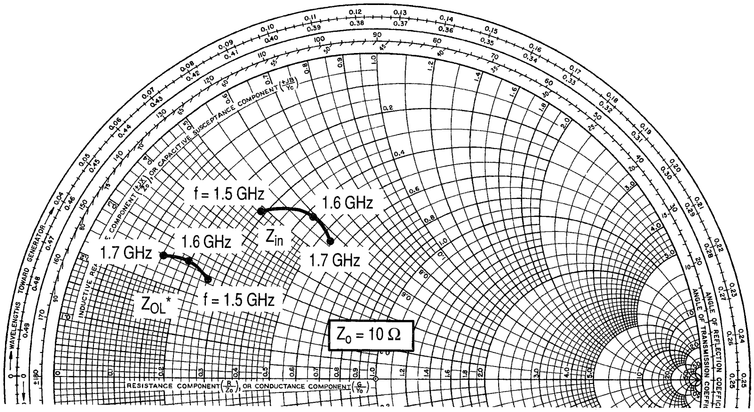
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_{CE} = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	35	80	—
FUNCTIONAL TESTS					
Collector–Base Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 30 Watts, f = 1600/1640 MHz)	G_{pe}	7.5	7.7	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 30 Watts, f = 1600/1640 MHz)	η	40	45	—	%
Input Return Loss (V_{CC} = 28 Vdc, P_{out} = 30 Watts, f = 1600/1640 MHz)	I_{RL}	8.0	—	—	dB
Output Mismatch Stress V_{CC} = 28 Vdc, P_{out} = 30 Watts, f = 1600 MHz, Load VSWR = 3:1, All phase angles at frequency of test	Ψ	No Degradation in Output Power			



Board Material – Teflon® Glass Laminate Dielectric
Thickness = 0.30″, ε_r = 2.55″, 2.0 oz. Copper

B1	Fair Rite Bead on #24 Wire	C4	47 µF, 50 V, Electrolytic
C1, C5	100 pF, B Case, ATC Chip Cap	L1, L2	3 Turns, #18, 0.133″ ID, 0.15″ Long
C2	0.1 µF, Dipped Mica Cap	L3	9 Turns, #24 Enamel
C3	0.1 µF, Chip Cap	R1	82 Ω, 1.0 W, Carbon

Figure 1. MRF16030 Test Fixture Schematic



V_{CC} = 28 Vdc, P_{out} = 30 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
1500	3.05 + j 4.88	2.66 + j 2.53
1600	4.32 + j 6.00	1.79 + j 2.80
1700	5.62 + j 5.79	1.51 + j 2.64

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

Figure 2. Series Equivalent Input/Output Impedance

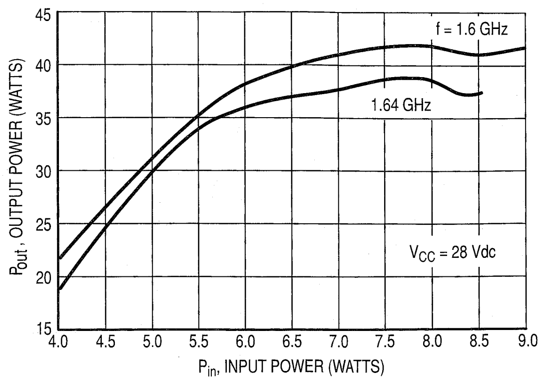
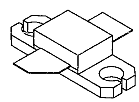


Figure 3. Output Power versus Input Power

The RF Sub–Micron Bipolar Line
RF Power Bipolar Transistor

MRF20030

30 W, 2.0 GHz
NPN SILICON
BROADBAND
RF POWER TRANSISTOR



CASE 395D–03, STYLE 1

Designed for broadband commercial and industrial applications at frequencies from 1800 to 2000 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common–emitter class A and class AB amplifier applications. Suitable for frequency modulated, amplitude modulated and multi–carrier base station RF power amplifiers.

- Specified 26 Volts, 2.0 GHz, Class AB, Two–Tones Characteristics
  Output Power — 30 Watts (PEP)
  Power Gain — 9.8 dB
  Efficiency — 34%
  Intermodulation Distortion — –28 dBc
- Typical 26 Volts, 1.88 GHz, Class AB, CW Characteristics
  Output Power — 30 Watts
  Power Gain — 10.5 dB
  Efficiency — 40%
- Excellent Thermal Stability
- Capable of Handling 3:1 VSWR @ 26 Vdc, 2000 MHz, 30 Watts (PEP) Output Power
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Designed for FM, TDMA, CDMA, and Multi–Carrier Applications

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	30	Vdc
Emitter–Base Voltage	V_{EB}	–3	Vdc
Collector Current – Continuous	I_C	4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.71	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	1.4	°C/W

(1) Thermal resistance is determined under specified RF operating condition.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

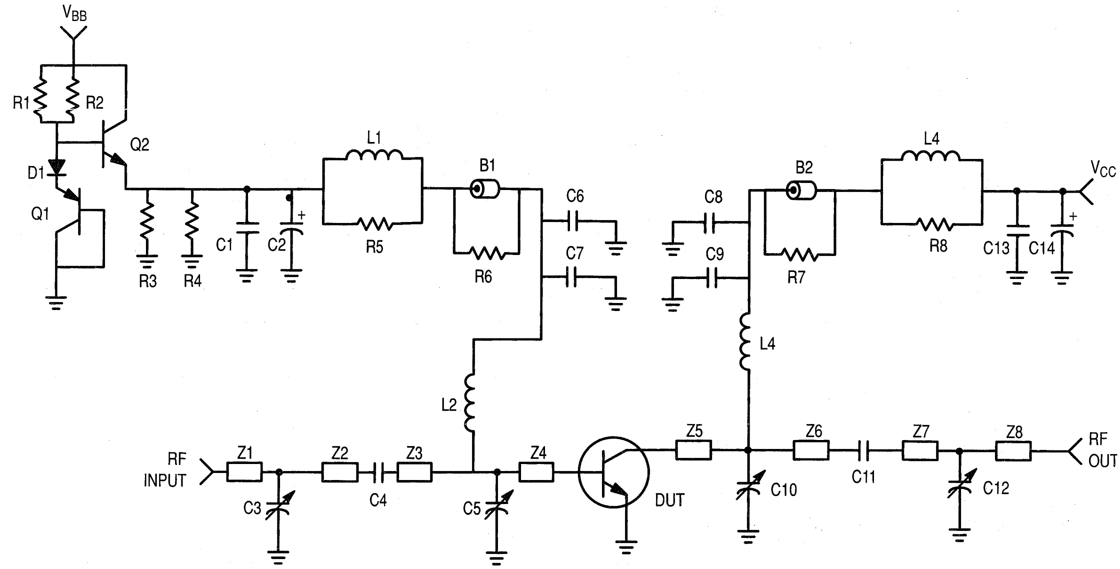
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	25	26	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	70	—	Vdc
Collector–Base Breakdown Voltage (I_C = 25 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	70	—	Vdc

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

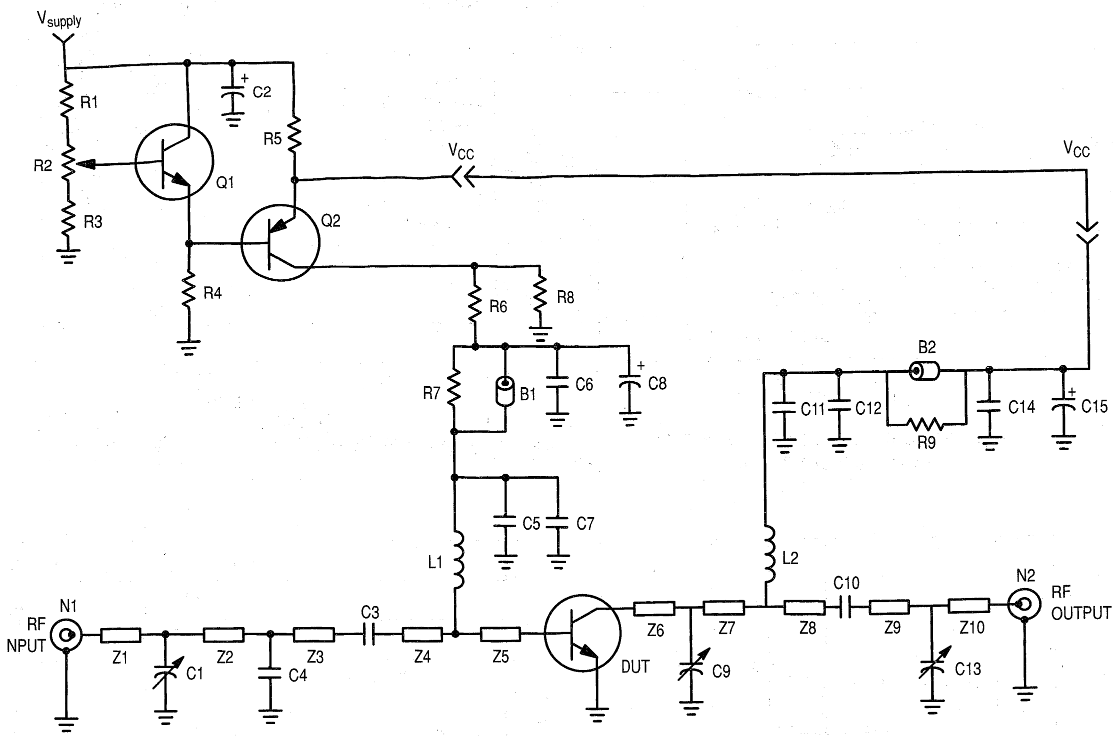
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Emitter–Base Breakdown Voltage (I_B = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	3	3.8	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (V_{CE} = 5 Vdc, I_{CE} = 1 Adc)	h_{FE}	20	40	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1.0 MHz) (1)	C_{ob}	—	28	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 30 Watts, I_{CQ} = 120 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	G_{pe}	9.8	10.5	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 120 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	η	34	38	—	%
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 120 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	IMD	—	– 33	– 28	dBc
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 125 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	IRL	10	17	—	dB
Load Mismatch (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 120 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz, Load VSWR = 3:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 125 mA, f_1 = 1930.0 MHz, f_2 = 1930.1 MHz)	G_{pe}	—	10.5	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 125 mA, f_1 = 1930.0 MHz, f_2 = 1930.1 MHz)	η	—	34	—	%
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 125 mA, f_1 = 1930.0 MHz, f_2 = 1930.1 MHz)	IMD	—	– 35	—	dBc
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 30 Watts (PEP), I_{CQ} = 125 mA, f_1 = 1930.0 MHz, f_2 = 1930.1 MHz)	IRL	—	14	—	dB
GUARANTEED BUT NOT TESTED (In Motorola Test Fixture)					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 30 Watts, I_{CQ} = 125 mA, f = 1880 MHz)	G_{pe}	—	10.5	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 30 Watts , I_{CQ} = 125 mA, f = 1880 MHz)	η	—	40	—	%
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 30 Watts , I_{CQ} = 125 mA, f = 1880 MHz)	IRL	—	14	—	dB
Output Mismatch Stress (V_{CC} = 25 Vdc, P_{out} = 30 Watts, I_{CQ} = 125 mA, f = 1880 MHz, VSWR = 3:1, All Phase Angles at Frequency of Test)	ψ	Typically No Degradation in Output Power			

(1) For Information Only. This Part Is Collector Matched.



B1, B2	Ferrite Bead, P/N 5659065/3B, Ferroxcube	N1, N2	Type N Flange Mount RF Connector MA/COM 3052–1648–10
C1, C13	0.1 μF, Chip Capacitor, Kermet		
C2	100 μF, 50 V, Electrolytic Capacitor, Mallory	R1, R2	130 Ω, 1/8 W Chip Resistor, Rohm
C3, C5, C12	0.6–4 pF, Variable Capacitor, Johanson, Gigatrim	R3, R4	100 Ω, 1/8 W Chip Resistor, Rohm
C4, C11	10 pF, B Case Chip Capacitor, ATC	R5, R8	10 Ω, 1/2 W Resistor
C6, C8	24 pF, B Case Chip Capacitor, ATC	R6, R7	10 Ω, 1/8 W Chip Resistor, Rohm (10J)
C7, C9	75 pF, B Case Chip Capacitor, ATC	Q1	Transistor, PNP Motorola (BD136)
C10	0.4–2.5 pF, Variable Capacitor, Johanson, Gigatrim	Q2	Transistor, NPN Motorola (MJD47)
C14	470 μF, 63 V, Electrolytic Capacitor, Mallory	Board	30 Mil Glass Teflon®, Arlon GX–0300–55–22, $\varepsilon_r = 2.55$
D1	Diode, Motorola (MUR3160T3)		
L1, L4	12 Turns, 22 AWG, IDIA. 0.195″		
L2, L3	0.750″ 20 AWG		

Figure 1. Class AB Test Fixture Electrical Schematic



B1, B2	Long Bead, Fair Rite	Q1	Transistor, NPN, Motorola (BD135)
C1, C9, C13	0.6–4 pF, Variable Capacitor, Johanson, Gigatrim	Q2	Transistor, PNP, Motorola (BD136)
C2, C8	100 µF, 50 V, Electrolytic Capacitor, Mallory	R1	250 Ω, Chip Resistor, 1/8 Watt, Rohm
C3, C10	18 pF B Case Chip Capacitor, ATC	R2	500 Ω, 1/4 Watt, Potentiometer
C4	1.3 pF, B Case Chip Capacitor, ATC	R3	4.7 kΩ, Chip Resistor, 1/8 Watt, Rohm
C5, C11	24 pF, B Case Chip Capacitor, ATC	R4	2 x 4.7 kΩ, Chip Resistor, 1/8 Watt, Rohm
C6, C14	0.1 µF, Chip Capacitor, Kermet	R5	1.0 Ω, 10 Watt, Resistor, DALE
C7, C12	75 pF, B Case Chip Capacitor, ATC	R6	39 Ω, 1 Watt, Resistor
C15	470 µF, 63 V, Electrolytic Capacitor, Mallory	R7, R9	4 x 39 Ω, Chip Resistors, 1/8 Watt, Rohm
L1, L2	0.75 in., 20 AWG	R8	75 Ω, Chip Resistor, 1/8 Watt, Rohm
N1, N2	Type N Flange Mount RF Connector, MA/COM	Board	30 Mil Glass Teflon®, Arlon GX–0300–55–22, $\varepsilon_r = 2.55$

Figure 2. Class A Test Fixture Electrical Schematic

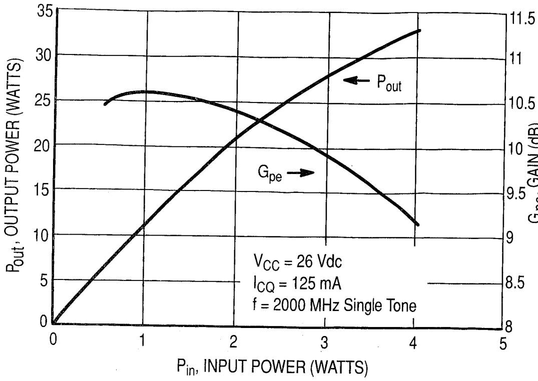


Figure 3. Output Power & Power Gain versus Input Power

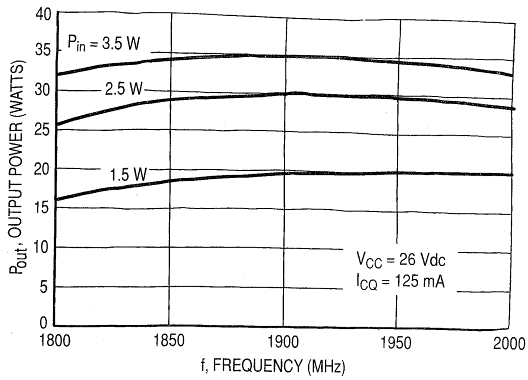


Figure 4. Output Power versus Frequency

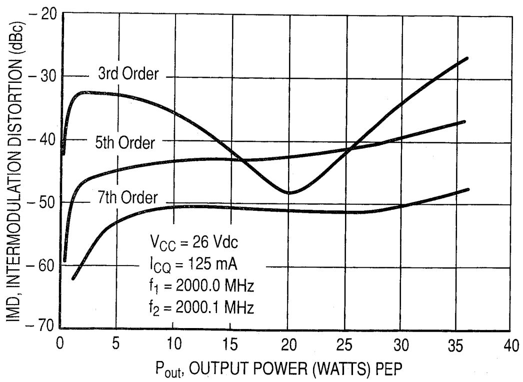


Figure 5. Intermodulation Distortion versus Output Power

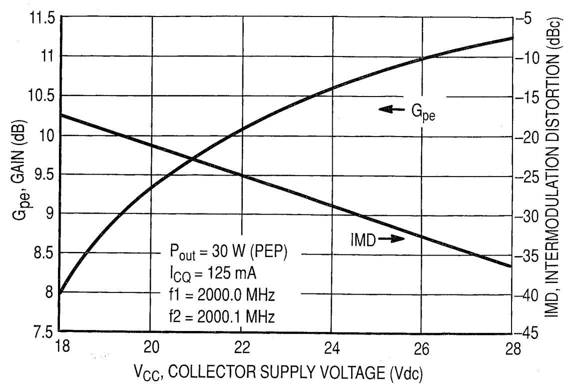


Figure 6. Power Gain and Intermodulation Distortion versus Supply Voltage

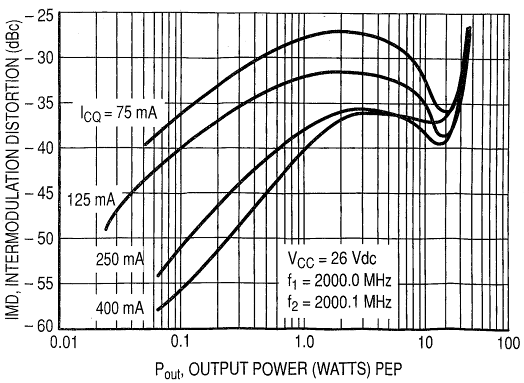


Figure 7. Intermodulation Distortion versus Output Power

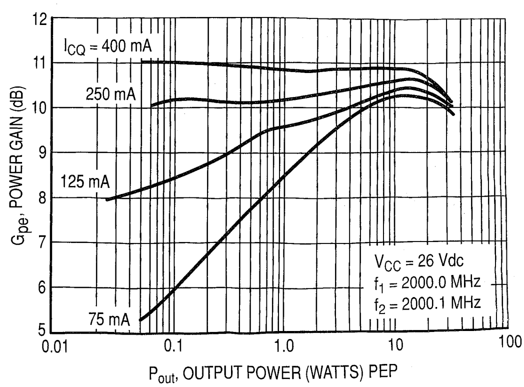


Figure 8. Power Gain versus Output Power

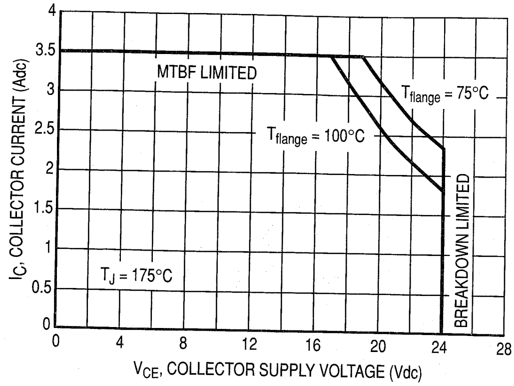


Figure 9. DC Class A Safe Operating Area

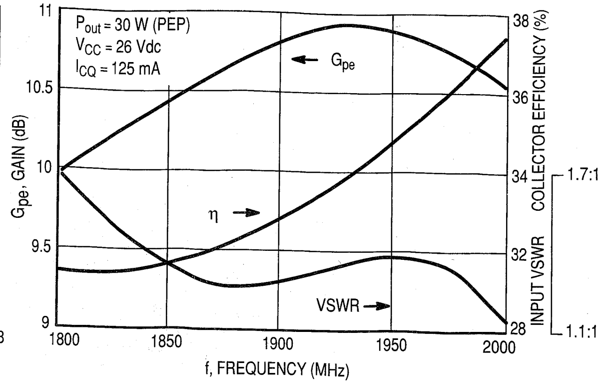


Figure 10. Performance in Broadband Circuit

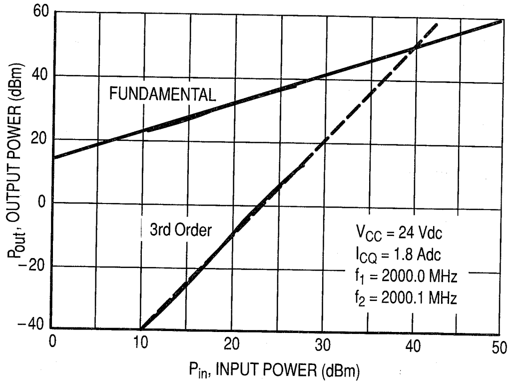
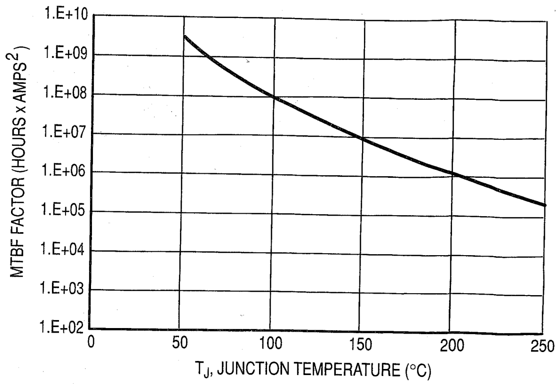
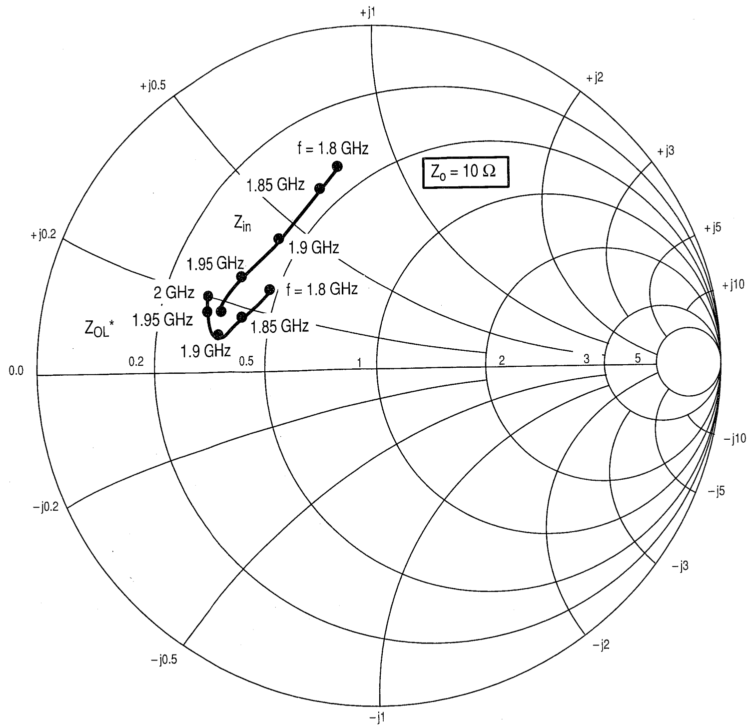


Figure 11. Class A Third Order Intercept Point



This above graph displays calculated MTBF in hours x ampere^2 emitter current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTBF factor by I_C^2 for MTBF in a particular application.

Figure 12. MTBF Factor versus Junction Temperature



V_{CC} = 26 V, I_{CQ} = 125 mA, P_{out} = 30 W (PEP)

f MHz	Z_{in}(1) Ω	Z_{OL}* Ω
1800	4.5 + j7.0	4.7 + j2.4
1850	4.5 + j6.0	4.4 + j1.6
1900	4.5 + j4.6	3.4 + j1.2
1950	3.7 + j2.4	3.3 + j1.6
2000	3.5 + j1.5	3.5 + j2.0

Z_{in}(1) = Conjugate of fixture base impedance.

Z_{OL}* = Conjugate of the optimum load impedance at given output power, voltage, bias current and frequency.

Figure 13. Series Equivalent Input and Output Impedence

Table 1. Common Emitter S–Parameters at V_{CE} = 24 Vdc, I_C = 1.8 Adc

f GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1.5	.964	158	.65	74	.046	60	.859	161
1.55	.960	156	.74	68	.047	56	.841	161
1.6	.952	155	.87	60	.049	53	.815	160
1.65	.933	153	1.05	50	.048	46	.787	161
1.7	.892	149	1.32	35	.047	40	.744	163
1.75	.804	149	1.64	13	.040	29	.719	168
1.8	.727	157	1.78	–18	.026	21	.778	175
1.85	.787	163	1.50	–50	.015	54	.883	174
1.9	.873	163	1.14	–73	.020	81	.937	171
1.95	.921	160	.84	–89	.026	88	.949	168
2	.941	157	.62	–102	.031	93	.950	165
2.05	.943	155	.48	–109	.036	93	.946	164
2.1	.940	153	.38	–118	.040	92	.942	163
2.15	.928	151	.30	–127	.042	97	.939	162
2.2	.917	150	.24	–133	.049	99	.935	161
2.25	.907	150	.20	–140	.056	101	.933	160
2.3	.888	148	.17	–150	.066	100	.926	159
2.35	.861	148	.14	–159	.077	98	.916	157
2.4	.853	149	.11	–167	.087	92	.909	157
2.45	.860	146	.10	–176	.095	89	.900	155
2.5	.880	146	.10	156	.119	84	.880	155

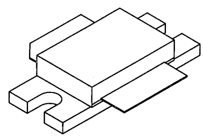
The RF Sub–Micron Bipolar Line
RF Power Bipolar Transistors

MRF20060
MRF20060S

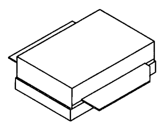
The MRF20060 and MRF20060S are designed for broadband commercial and industrial applications at frequencies from 1800 to 2000 MHz. The high gain, excellent linearity and broadband performance of these devices make them ideal for large–signal, common emitter class A and class AB amplifier applications. These devices are suitable for frequency modulated, amplitude modulated and multi–carrier base station RF power amplifiers.

- Guaranteed Two–tone Performance at 2000 MHz, 26 Volts
  Output Power — 60 Watts (PEP)
  Power Gain — 9 dB
  Efficiency — 33%
  Intermodulation Distortion — –30 dBc
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- Capable of Handling 3:1 VSWR @ 26 Vdc, 2000 MHz, 60 Watts (PEP) Output Power
- Designed for FM, TDMA, CDMA and Multi–Carrier Applications

60 W, 2000 MHz
RF POWER
BROADBAND
NPN BIPOLAR



CASE 451–04, STYLE 1
(MRF20060)



CASE 451A–01, STYLE 1
(MRF20060S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage (I_B = 0 mA)	V_{CEO}	25	Vdc
Collector–Emitter Voltage	V_{CES}	60	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ohm)	V_{CER}	30	Vdc
Base–Emitter Voltage	V_{EB}	– 3	Vdc
Collector Current – Continuous	I_C	8	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	200	°C

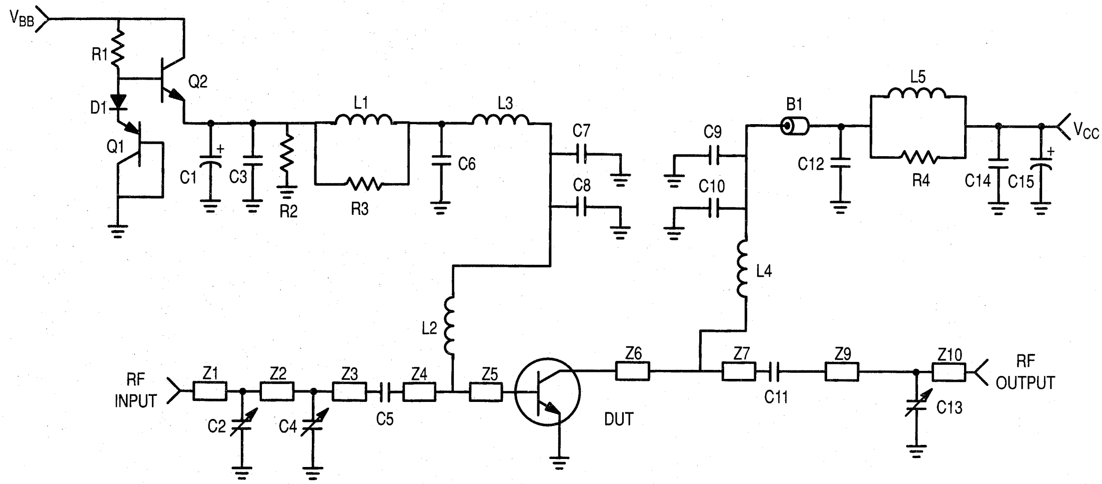
THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

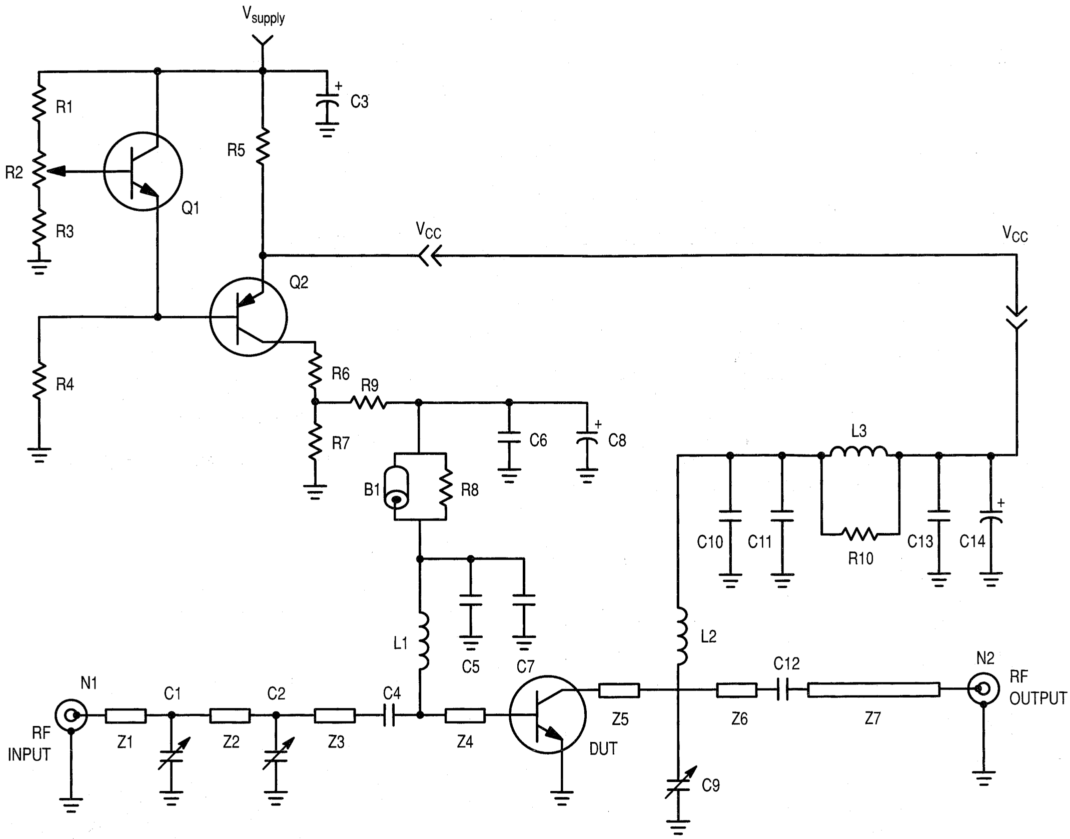
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	25	26	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	69	—	Vdc
Collector–Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	69	—	Vdc
Reverse Base–Emitter Breakdown Voltage (I_B = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3	3.5	—	Vdc
Zero Base Voltage Collector Leakage Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (V_{CE} = 5 Vdc, I_C = 1 Adc)	h_{FE}	20	40	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 26 Vdc, I_E = 0, f = 1.0 MHz) (1)	C_{ob}	—	55	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	G_{pe}	9	9.4	—	dB
Collector Efficiency (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	η	33	35	—	%
Intermodulation Distortion (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	IMD	—	– 33	– 30	dB
Input Return Loss (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz)	IRL	12	19	—	dB
Output Mismatch Stress (V_{CC} = 26 Vdc, P_{out} = 60 Watts (PEP), I_{CQ} = 200 mA, f_1 = 2000.0 MHz, f_2 = 2000.1 MHz, VSWR = 3:1, All Phase Angles at Frequency of Test)	ψ	No Degradation in Output Power			

(1) For Information Only. This Part Is Collector Matched.



B1	Ferrite Bead, P/N 5659065/3B, Ferroxcube	D1	Diode, Motorola (MUR3160T3)
C1	100 µF, 50 V, Electrolytic Capacitor, Mallory	L1, L5	12 Turns, 22 AWG, 0.140″ Choke
C2, C4, C13	0.6–4.0 pF, Variable Capacitor, Gigatrim, Johanson	L2, L4	.5 inch of 20 AWG, ID Choke
C3, C14	0.1 µF, Chip Capacitor, Kemit	L3	12.5 nH Inductor
C5	15 pF, B Case Chip Capacitor, ATC	R1	2 x 130 Ω, 1/8 W Chip Resistor, Rohm
C6, C12	1000 pF, B Case Chip Capacitor, ATC	R2	2 x 100 Ω, 1/8 W Chip Resistor, Rohm
C7, C9	91 pF, B Case Chip Capacitor, ATC	R3, R4	10 Ω, 1/2 W, Resistor
C8, C10	24 pF, B Case Chip Capacitor, ATC	Q1	Transistor, PNP Motorola (BD136)
C11	13 pF, B Case Chip Capacitor, ATC	Q2	Transistor, NPN Motorola (MJD47)
C15	470 µF, 50 V, Electrolytic Capacitor, Mallory	Board	Glass Teflon®, Arlon GX–0300–55–22, ε_r

Figure 1. Class AB, 1.93 – 2 GHz Test Fixture Electrical Schematic



B1	Short Bead, Fair Rite
C1, C2	0.6–4.5 pF, Trimmer, Gigatrim, Johanson
C3, C8	100 μF, 50 V Electrolytic, Mallory
C4, C12	12 pF, Chip Capacitor, ATC
C5, C11	91 pF, Chip Capacitor, ATC
C6	0.01 μF, Chip Capacitor, ATC
C7, C10	24 pF, Chip Capacitor, ATC
C9	0.4–2.5 pF, Trimmer, Gigatrim, Johanson
C13	0.1 μF, Chip Capacitor, ATC
C14	470 μF, 63 V Electrolytic, Mallory
L1	2 Turn, 27 AWG, 0.049″ ID Coil
L2	0.041″ dia., 0.7″ Length Wire
L3	11 Turn, 20 AWG, 0.19″ ID Coil
N1, N2	Type N Flange Mount RF 55–22, Connector, Omni Spectra
Q1	Transistor, NPN, Motorola (BD135)
Q2	Transistor, PNP, Motorola (BD136)
R1	270 Ω, Chip Resistor, 1/8 Watt, Rohm
R2	10 KΩ, 1/4 Watt, Potentiometer
R3	4.7 KΩ, Chip Resistor, 1/8 Watt, Rohm
R4	2 x 4.7 KΩ, Chip Resistor, 1/8 Watt, Rohm
R5	1.0 Ω, 25 Watt, 1% Resistor, DALE
R6	38 Ω, Axial Lead, 1 Watt Resistor
R7	4.2 KΩ, Chip Resistor, 1/8 Watt, Rohm
R8	3 x 39 Ω, Chip Resistors, 1/8 Watt, Rohm
R9	2 x 10 Ω, Chip Resistor, 1/8 Watt, Rohm
R10	10 Ω, Axial Lead, 1 Watt Resistor
Board	Glass Teflon®, Arlon GX–0300–55–22, $\varepsilon_r = 2.55$

Figure 2. Class A, 1.93 – 2 GHz Test Fixture Electrical Schematic

TYPICAL CHARACTERISTICS

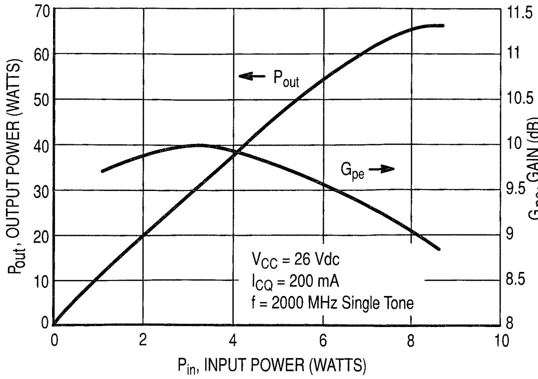


Figure 3. Output Power & Power Gain versus Input Power

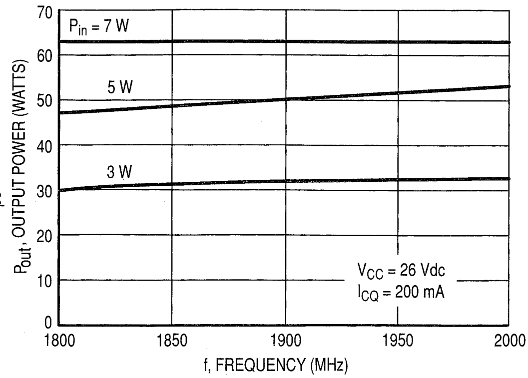


Figure 4. Output Power versus Frequency

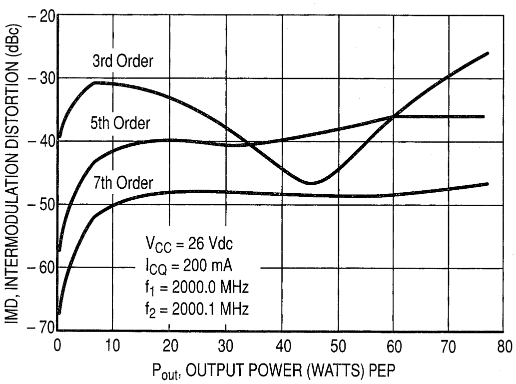


Figure 5. Intermodulation Distortion versus Output Power

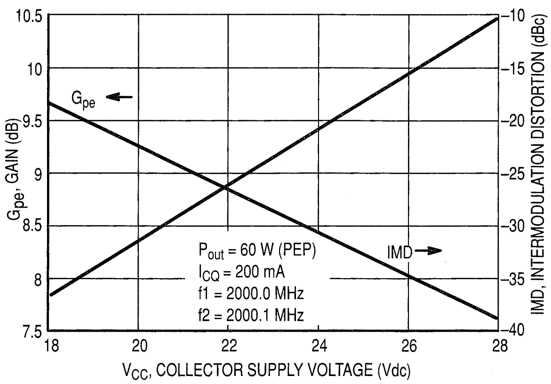


Figure 6. Power Gain and Intermodulation Distortion versus Supply Voltage

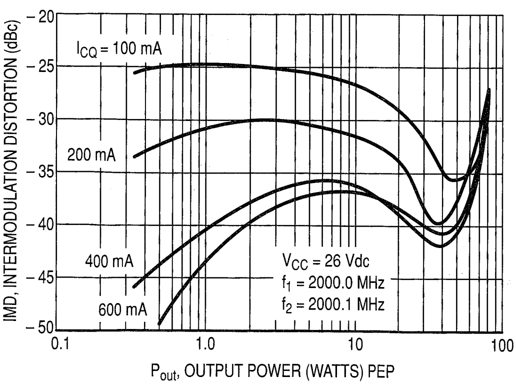


Figure 7. Intermodulation Distortion versus Output Power

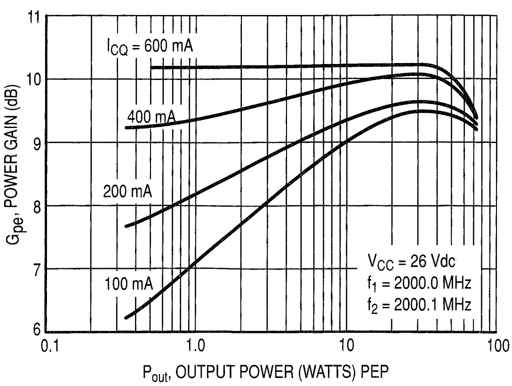


Figure 8. Power Gain versus Output Power

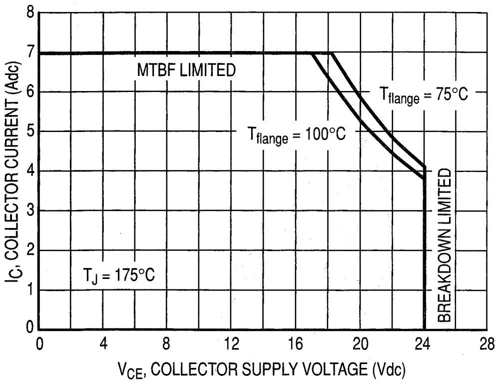


Figure 9. Class A DC Safe Operating Area

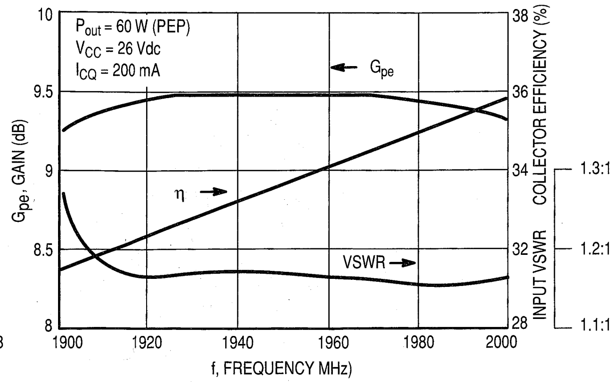


Figure 10. Performance in Broadband Circuit

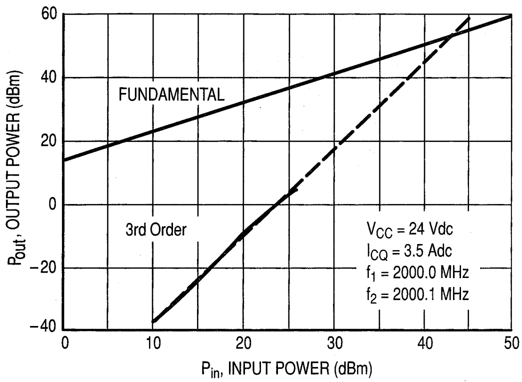
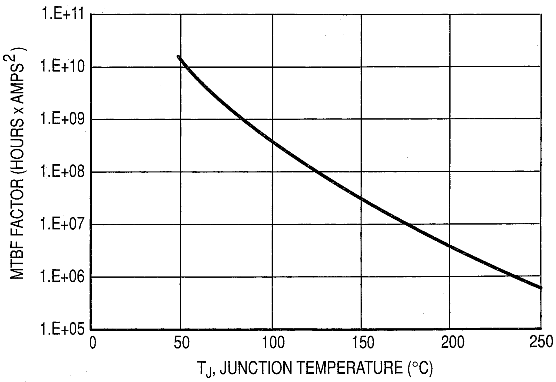
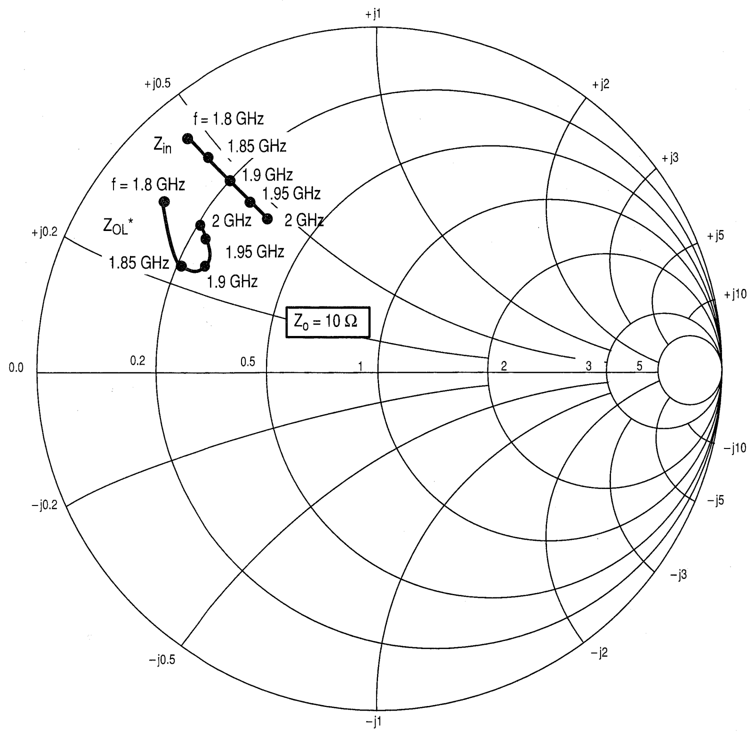


Figure 11. Class A Third Order Intercept Point



This above graph displays calculated MTBF in hours x ampere^2 emitter curent. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTBF factor by I_C^2 for MTBF in a particular application.

Figure 12. MTBF Factor versus Junction Temperature



V_{CC} = 26 V, I_{CQ} = 200 mA, P_{out} = 60 W (PEP)

f MHz	$Z_{in}(1)$ Ω	Z_{OL}^* Ω
1800	1.0 + j4.8	1.7 + j3.3
1850	1.5 + j4.8	2.2 + j2.7
1900	2.0 + j4.7	2.4 + j3.0
1950	2.5 + j4.7	2.3 + j3.2
2000	3.5 + j4.7	2.0 + j3.4

$Z_{in}(1)$ = Conjugate of fixture base terminal impedance.

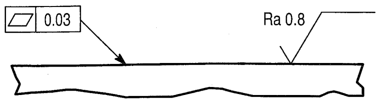
Z_{OL}^* = Conjugate of the optimum load impedance at given output power, voltage, bias current and frequency.

Figure 13. Series Equivalent Input and Output Impedence

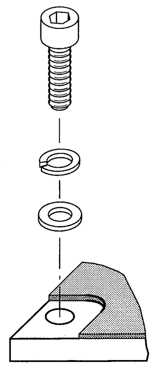
Table 1. Common Emitter S–Parameters at V_{CE} = 24 Vdc, I_C = 3.5 Adc

f GHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1.5	0.986	168	0.32	81	0.031	60	0.923	169
1.55	0.985	167	0.35	76	0.031	63	0.918	169
1.6	0.981	167	0.40	70	0.032	61	0.908	169
1.65	0.973	166	0.45	63	0.030	53	0.897	169
1.7	0.968	165	0.52	56	0.033	50	0.889	168
1.75	0.951	163	0.62	46	0.028	47	0.880	169
1.8	0.914	161	0.76	32	0.027	39	0.871	170
1.85	0.851	161	0.91	12	0.024	26	0.863	171
1.9	0.789	164	1.02	–15	0.015	5	0.888	174
1.95	0.810	170	0.94	–44	0.005	–7	0.931	174
2	0.880	172	0.75	–68	0.006	–151	0.953	172
2.05	0.934	170	0.57	–85	0.010	152	0.967	170
2.1	0.964	168	0.45	–98	0.015	158	0.965	169
2.15	0.977	165	0.36	–109	0.022	164	0.955	168
2.2	0.975	163	0.30	–118	0.033	165	0.950	167
2.25	0.961	161	0.25	–128	0.049	160	0.947	167
2.3	0.942	160	0.22	–139	0.066	149	0.938	166
2.35	0.919	157	0.19	–149	0.077	142	0.931	165
2.4	0.860	156	0.17	–163	0.100	137	0.922	165
2.45	0.821	159	0.15	177	0.128	122	0.914	165
2.5	0.781	161	0.14	157.0	0.156	108	0.907	165

MOUNTING RECOMMENDATIONS



○ 8 Fixing holes M3
Minimum useful depth: — Copper/Aluminum: 6 mm



HEATSINK TOOLING

- Flatness better than 0.03 mm.
- Roughness: Typical value 0.8.

THERMAL COMPOUND

- Paste with silicones: SICERONT KF Ref. 1201 Recommended.
- Thickness: Optimum between 0.06 mm and 0.15 mm, on the whole back surface of the amplifier.
  (Typical volume: 700 mm 3 for 0.1 mm thickness)
  (Equivalent weight: 1.5g for 2.2 density paste).

SCREWS

- Socket head cap screws: — CHC M3 x 10 for Copper/Aluminum Heatsink.
- Material: Nickel plated steel.

WASHERS

- Split lock washers WZ ∅3 + Flat washers ZU ∅3.

CLEANING

- Some components of this amplifier are not qualified for every kind of cleaning solvent.
- Do not clean the amplifier in a solvent bath.
- Local cleaning is recommended.

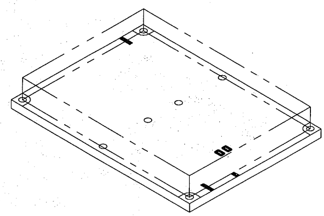
The RF Line
Broadband RF Power Amplifier for TV Transmitter

MRFA2602

The MRFA2602 is a solid state class A amplifier and is specifically designed for TV transposers and transmitters. This amplifier incorporates microstrip technology and reliable Motorola push–pull transistors.

- Specified 25.5 Volts, 470–860 MHz Characteristics
  Output Power — 40 Watts @ −50 dB (3 Tones)
  Output Power — 60 Watts Min @ 1 dB Comp. (CW)
  Gain — 8.5 dB Min (Small Signal)

**60 W, 470–860 MHz
CLASS A
RF POWER AMPLIFIER**



CASE 429C–03, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	26.5	Vdc
Input Power	P_{in}	15	W
Storage Temperature Range	T_{stg}	−40 to +100	°C
Operating Temperature (1)	T_{op}	−20 to +70	°C

NOMINAL OPERATION CONDITION (T_C = 60°C)

Supply	V_{CC} = 25.5 V	I_{sup} = 9.2 A

ELECTRICAL CHARACTERISTICS (T_C = 25°C, Nominal Supply, 470–860 MHz Bandwidth, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain (small signal)	G_p	8.5	—	—	dB
Gain Ripple (small signal)	G_{rple}	—	—	±1	dB
Output Power @ 1 dB Compression	P_{out}	60	—	—	W
Mismatch Tolerance (P_{out} = 60 W)	VSWR	∞:1	—	—	—
Intermodulation (−8 dB/–7 dB/–16 dB, P_{ref} = 40 W)	IMD1	—	—	−50	dB
Intermodulation (−8 dB/–10 dB/–16 dB, P_{ref} = 40 W)	IMD2	—	—	−53	dB
Input Return Loss/Output Return Loss	IRL/ORL	—	—	−15	dB

NOTE:
1. Temperature is measured at temperature test point (on the flange of the transistor).

REV 3

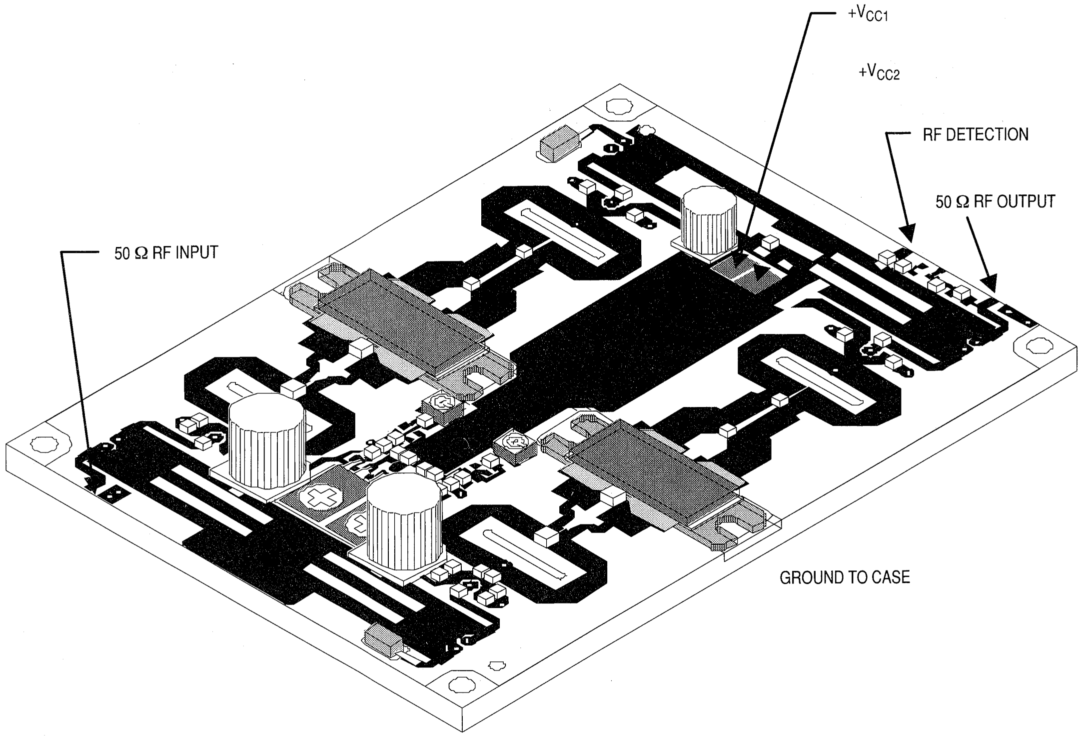


Figure 1. MRFA2602 Connections

TYPICAL CHARACTERISTICS

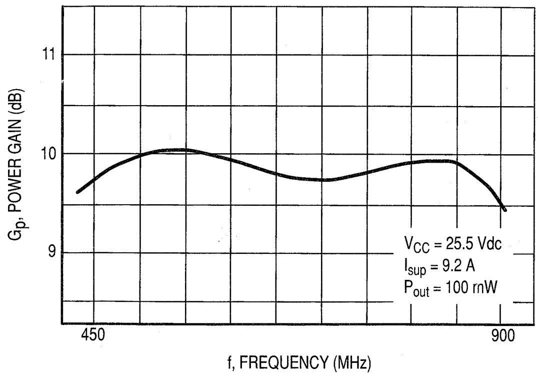


Figure 2. Power Gain versus Frequency

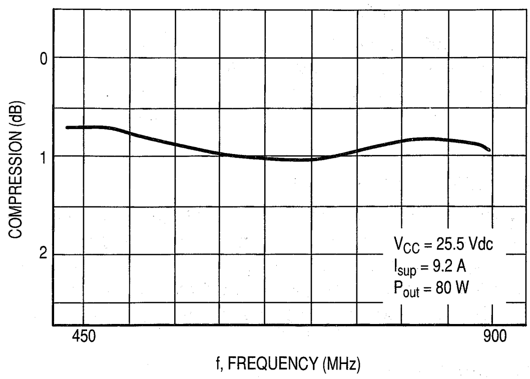


Figure 3. Gain Compression versus Frequency

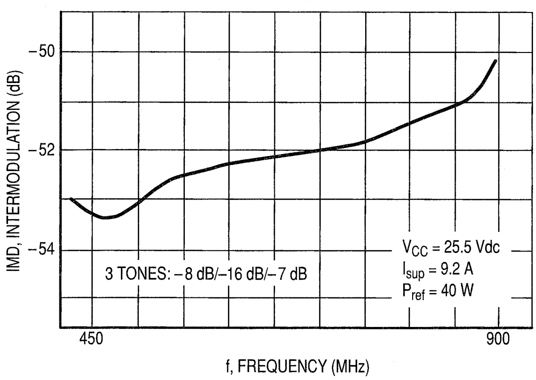


Figure 4. Intermodulation versus Frequency

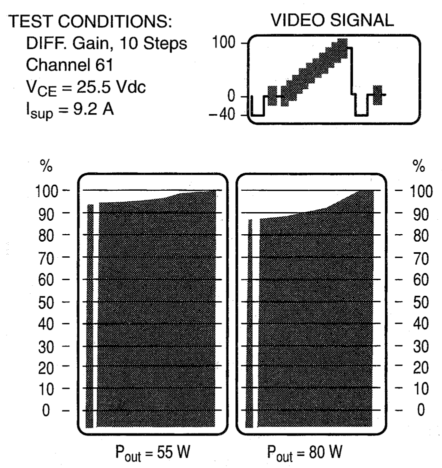


Figure 5. Differential Gain

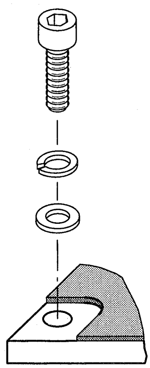
MOUNTING RECOMMENDATIONS

1. HEATSINK TOOLING

- Planarity: Better than 0.03 mm
- Roughness: Typical Value 0.8
- 8 Fixing Holes M3

2. THERMAL COMPOUND

- Paste with silicones: SICERONT KF Ref. 1201 Recommended.
- Thickness: Optimum between 0.06 mm and 0.15 mm, on the whole back surface of the amplifier.
  (Typical volume: 700 mm 3 for 0.1 mm thickness)
  (Equivalent weight: 1.5 g for 2.2 density paste)



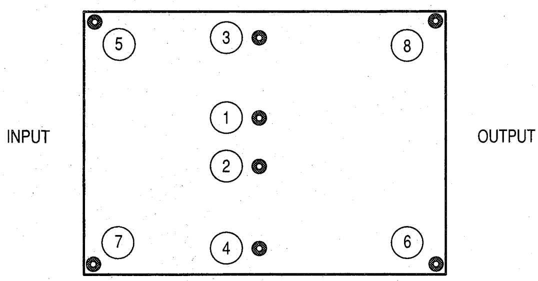
3. SCREWS

- Socket head cap screws: — CHC M3 x 10 for Copper/Aluminum Heatsink.
- Material: Nickel plated steel.

4. WASHERS

- Split lock washers WZ ∅3 + Flat washers ZU ∅3.

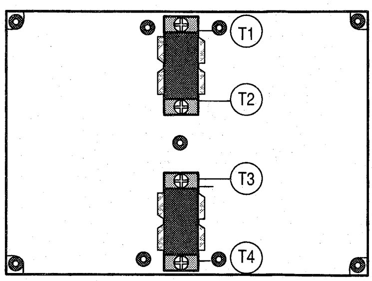
5. TIGHTENING ORDER



Maximum Recommended Torque: 12 Kg.cm
(10.5 in. lbs.)

6. MOUNTING VERIFICATION

Supply the amplifier (25.5 Vdc) without RF signal, and measure temperature on points 1, 2, 3, and 4.



Characteristic	Typ	Max	Unit
T1, T2, T3, T4	—	70	°C
Δ(T1, T2), Δ(T3, T4)	3	5	°C

CLEANING RECOMMENDATIONS

Some components of this amplifier are not qualified for every kind of cleaning solvent, so DO NOT clean the amplifier in a solvent bath. Local cleaning is recommended.

The RF Line
Broadband R.F. Array for TV Transmitter

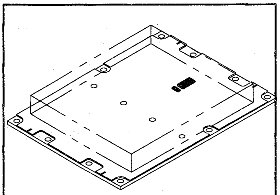
MRFA2604

**230 W PEAK SYNC.
470–860 MHz
CLASS AB
RF POWER AMPLIFIER**

The MRFA2604 is a solid state class AB amplifier specifically designed for TV transposers and transmitters. This amplifier incorporates microstrip technology and reliable Motorola push–pull transistors.

The MRFA2604 includes a thermal compensation (differential gain is constant versus average picture level (APL)) which can be partially disconnected.

- Specified 28 Volts, 470–860 MHz Characteristics
  Output Power = 175 Watts (CW)/230 Watts (Video)
  Minimum Gain = 8.0 dB (@ Nominal Power)
- 50 Ω Input and Output Impedance
- Class AB Operation
- Thermally Compensated



CASE 439–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	32	Vdc
Current	I_{max}	15	Adc
Storage Temperature Range	T_{stg}	−40 to +100	°C
Operating Temperature (1)	T_{op}	−20 to +70	°C

NOMINAL OPERATION CONDITION

Supply Voltage/Quiescent Current (2)	V_{CC} = 28 V	I_Q = 0.9 A

ELECTRICAL CHARACTERISTICS IN CW (T_C = 25°C, V_{CC} = 28 V, I_Q = 0.5 A, without thermal correction)

Characteristic	Symbol	Min	Typ	Max	Unit
Instantaneous Bandwidth	BW	470	—	860	MHz
Power Gain (P_{out} = 175 W)	G_p	8.0	9.0	—	dB
Gain Ripple (P_{out} = 175 W)	G_{rple}	—	±0.5	±1.0	dB
Output Power @ 1.0 dB Compression	P_{out}	175 (3)	190	—	W
Efficiency (P_{out} = 175 W)	η	45 (3)	50	—	%
Input Return Loss	I_{RL}	—	−20	−15	dB

ELECTRICAL CHARACTERISTICS IN VIDEO (T_C = 25°C, I_{sup} = 0.9 A, with thermal compensation)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Power @ 28 V (Peak Sync. B/G standard)	P_{out}	230	240	—	W
Power Gain @ black level (P_{sync} = 230 W, V_{CC} = 28 V)	G_p	8.0	9.0	—	dB

(1) Temperature is measured at temperature test point (on the flange of the transistor).
(2) Tuned in the factory for optimum thermal correction @ 25°C.
(3) Thermal correction cannot be disconnected, and CW performances are slightly affected (−5.0 W, −3% typical), but output power with a video signal remain the same.

REV 1

TYPICAL CHARACTERISTICS

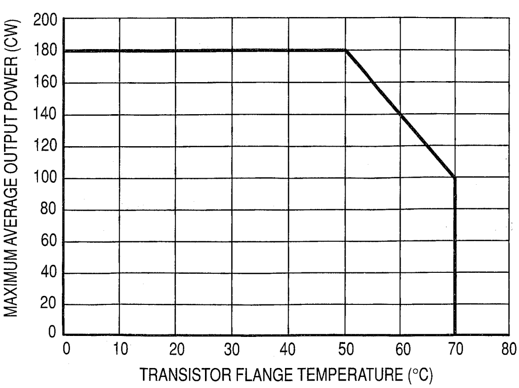


Figure 1. Maximum Average Output Power versus Temperature

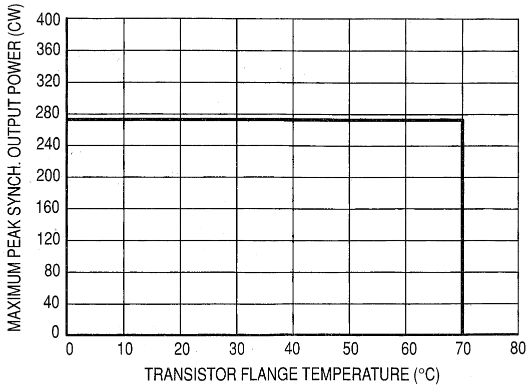


Figure 2. Maximum Peak Synch. Output Power (B/G Standard) versus Temperature

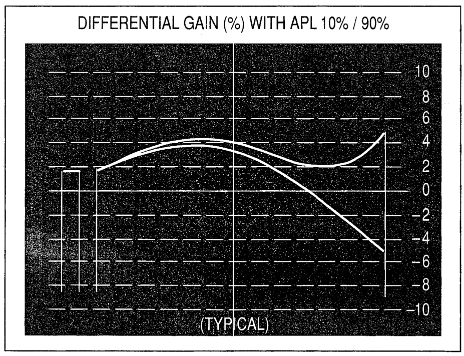


Figure 3. Without Thermal Compensation

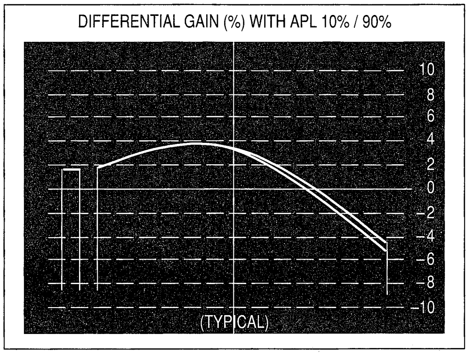
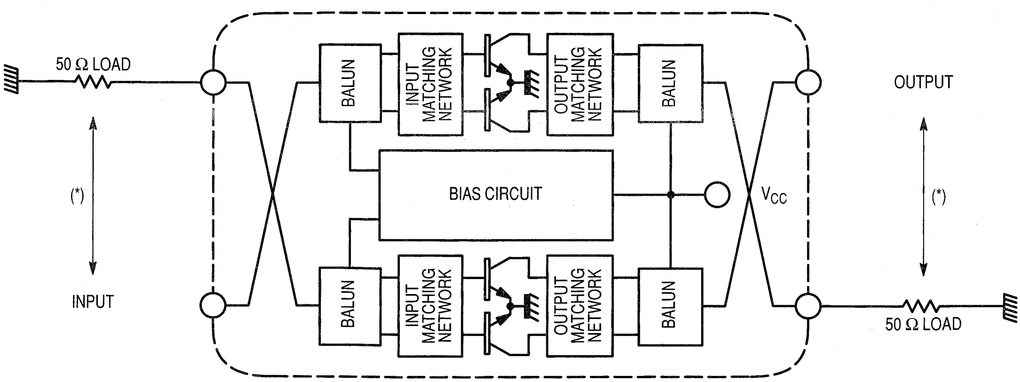


Figure 4. With Thermal Compensation

WARNING: Please read instructions carefully for operating/set–up and mounting recommendations prior to operating this device.



* Loads positions can be inverted if required.

Figure 5. Internal Schematic and External Connections

CW MEASUREMENTS WITHOUT THERMAL COMPENSATION**
(see Figure 23)

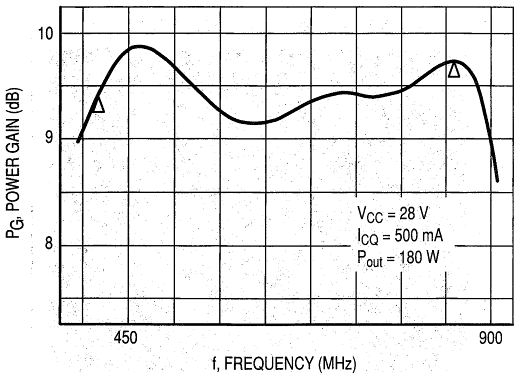


Figure 6. Power Gain versus Frequency

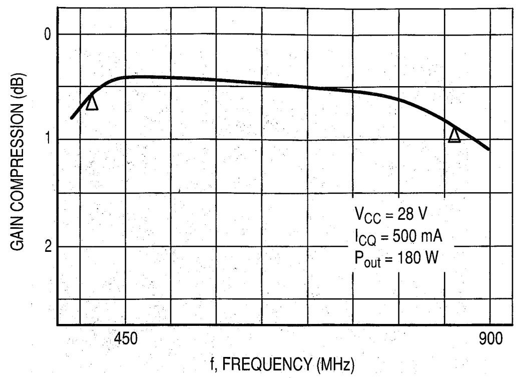


Figure 7. Gain Compression versus Frequency

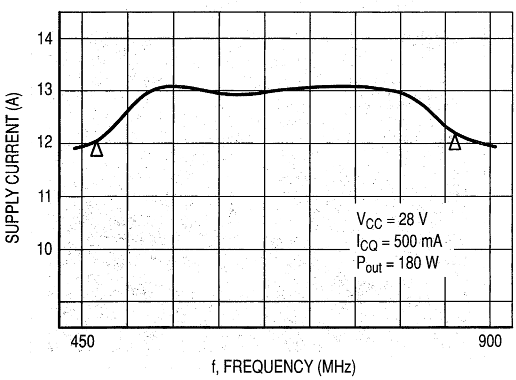


Figure 8. Supply Current versus Frequency

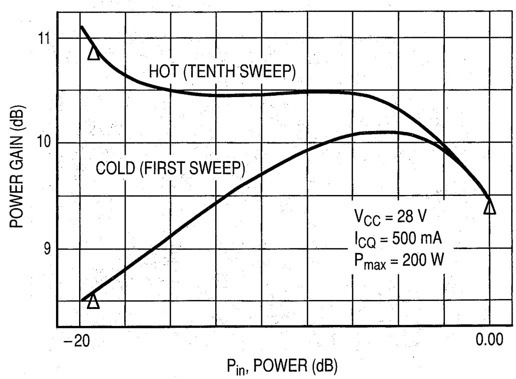


Figure 9. Power Gain versus Input Power

** Measurement results are typical values and are not guaranteed

VIDEO MEASUREMENTS WITH THERMAL COMPENSATION, B/G STANDARD
(Measurement results are typical values and are not guaranteed)

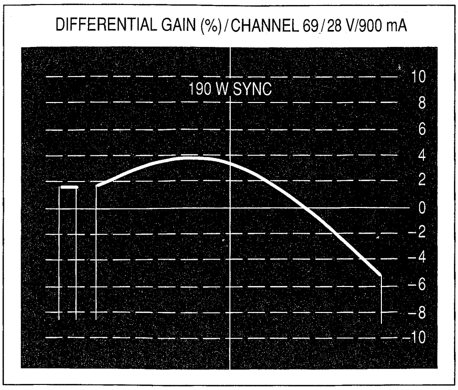


Figure 10. Differential Gain 190 W Sync

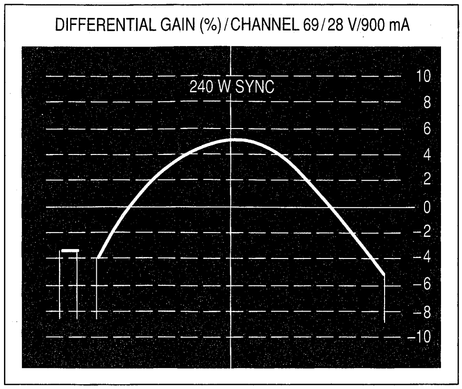


Figure 11. Differential Gain 240 W Sync

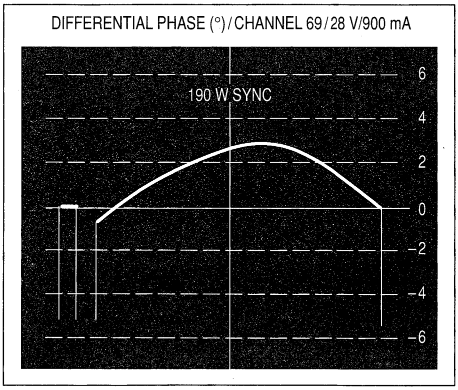


Figure 12. Differential Phase 190 W Sync

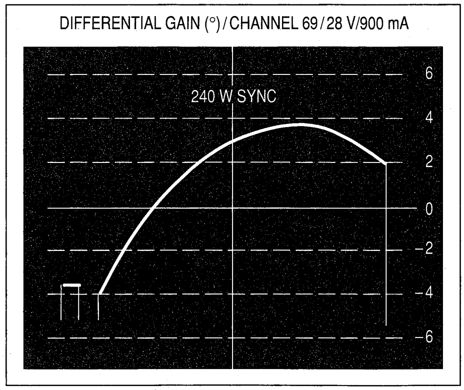
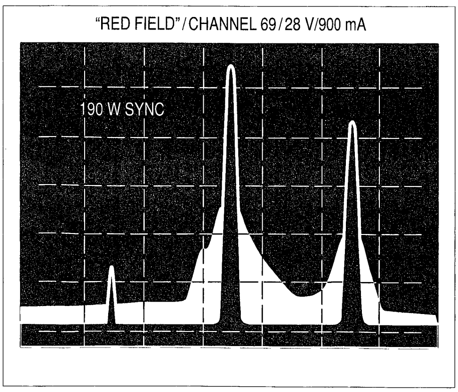
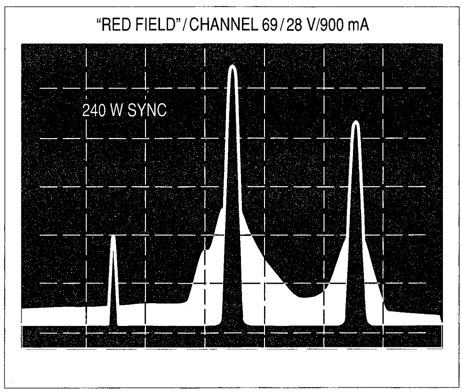


Figure 13. Differential Phase 240 W Sync



SIDE BAND REGENERATION 10 dB/div–2 MHz/div

Figure 14. "Red Field" 190 W Sync



SIDE BAND REGENERATION 10 dB/div–2 MHz/div

Figure 15. "Red Field" 240 W Sync

VIDEO MEASUREMENTS WITH THERMAL COMPENSATION, BG STANDARD
(Measurement results are typical values and are not guaranteed)

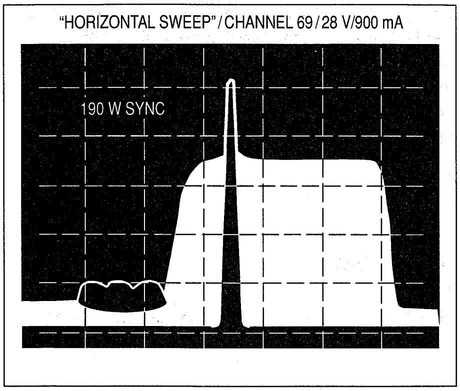


Figure 16. "Horizontal Sweep" 190 W Sync

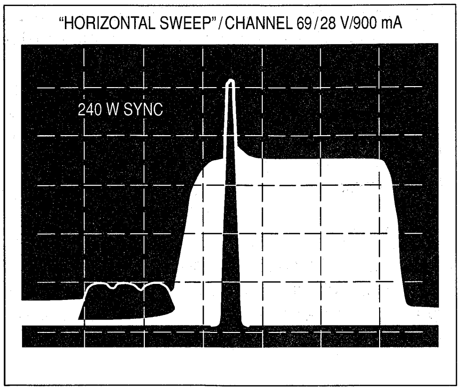


Figure 17. "Horizontal Sweep" 240 W Sync

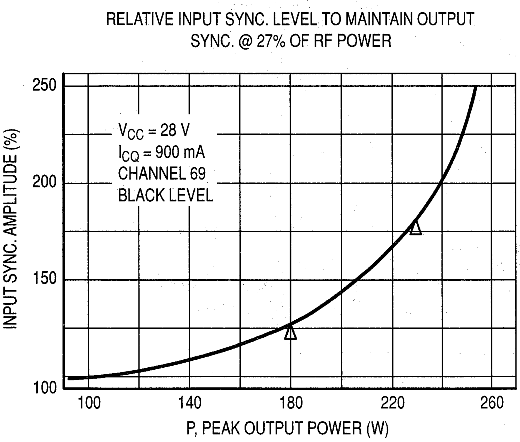


Figure 18. Input Sync. versus Output Power

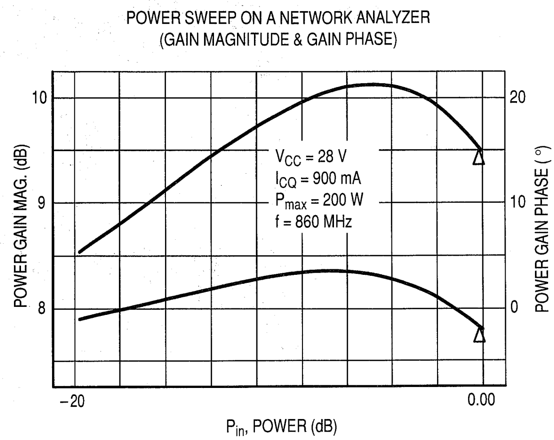


Figure 19. Power Gain versus Input Power

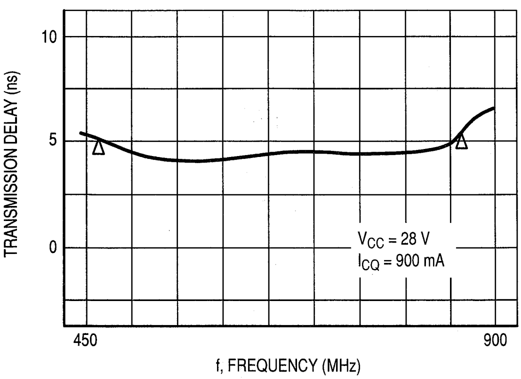


Figure 20. Delay versus Frequency

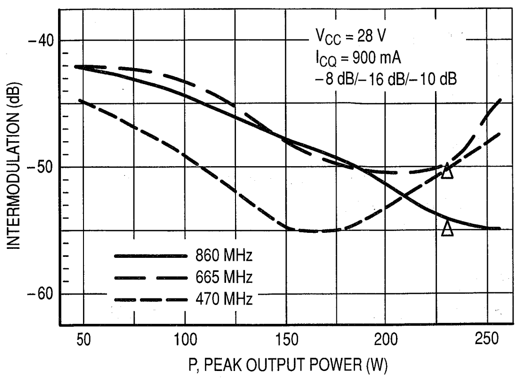


Figure 21. Intermodulation versus Output Power

OPERATING AND SET–UP RECOMMENDATIONS

1. QUIESCENT CURRENT
   - **With Thermal Compensation:** The amplifier is tuned in the factory at 28 V/900 mA (total current) with the compensation "ON." Depending on the temperature of the amplifier and of the RF transistor, this value can be slightly different but it does not affect the overall performances.
   - **Without Thermal Compensation:** If the amplifier has to be used without the compensation, P1 (tuning of quiescent current) has to be set–up in its initial position before applying power supply (see Figure 22). When power supply is applied P1 is tuned to obtain 500 mA.
   - **Max. current:** In any case I_Q **must not exceed 1.2 A.**

2. THERMAL COMPENSATION

   The amplifier is tuned in the factory for optimum compensation at 180 W peak, B/G standard, channel 69. If the amplifier is used at a different level (driver for instance), the compensation may not be optimized and can be retuned by using P2.

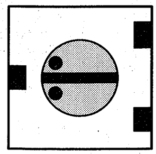


Figure 22. Initial Position of P1

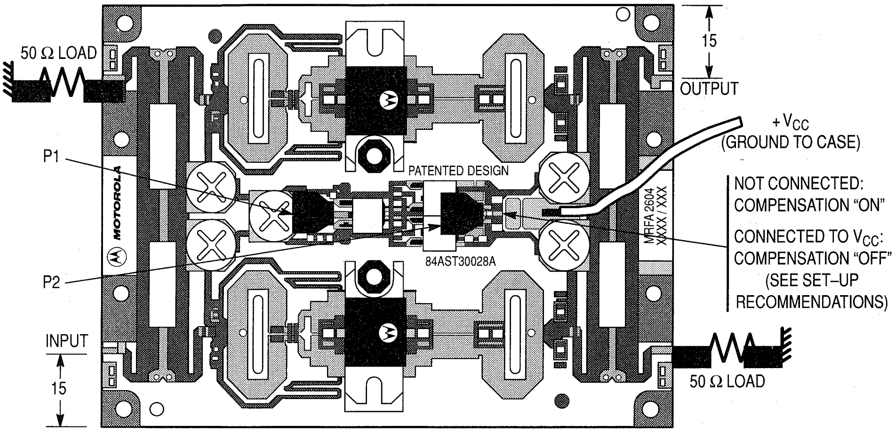
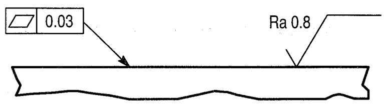


Figure 23. MRFA2604 Connections

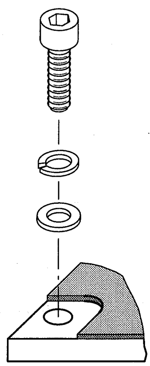
MOUNTING RECOMMENDATIONS



1. HEATSINK TOOLING
   - Flatness: better than 0.03 mm
   - Roughness: Typical value 0.8

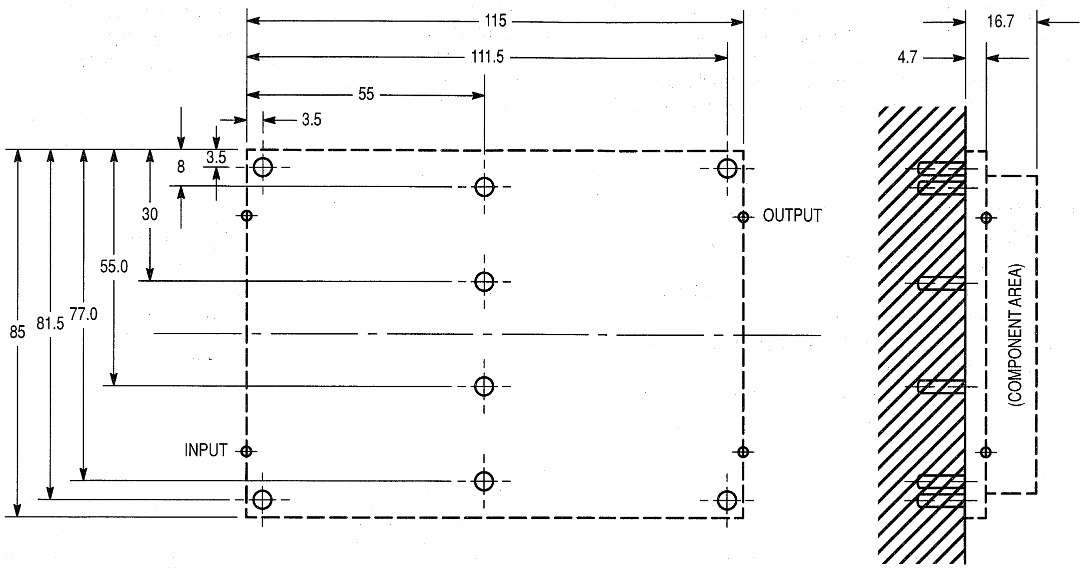
2. SCREWS
   - CHC M3 x 10 for Copper/Aluminum Heatsink
   - Socket head cap screws
   - Material: Nickel plated steel

3. WASHERS
   - Split lock washers WZ ∅3 + Flat washers ZU ∅3



MOUNTING RECOMMENDATIONS (cont')

5. THERMAL COMPOUND:
   - Paste with silicones: SICERONT KF Ref. 1201 Recommended.
   - Thickness: optimum between 0.06 mm and 0.15 mm, on the whole back surface of the amplifier. (Typical volume: 700 mm 3 for 0.1 mm thickness) (Equivalent weight: 1.5 g for 2.2 density paste).

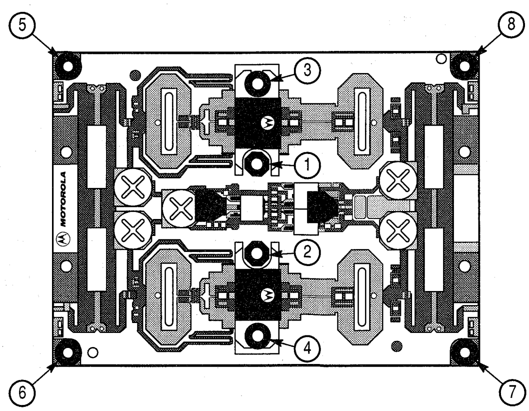


6. TIGHTENING SEQUENCE:

   Engage all screws down to contact, then apply torque **according to given sequence** (see drawing on the right).

7. TORQUE:

   Maximum Recommended Torque: 12 Kg.cm (10.5 in. lbs.)



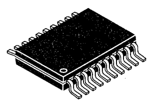
Advance Information

The MRFIC Line Quadrature Modulator

MRFIC0001

QUADRATURE MODULATOR INTEGRATED CIRCUIT

The MRFIC0001 is an integrated Quadrature Modulator designed for operation in the 50 to 260 MHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications include DQPSK for PDC, NADC, and PHS; GMSK for GSM and DCS1800; and QPSK for CATV.

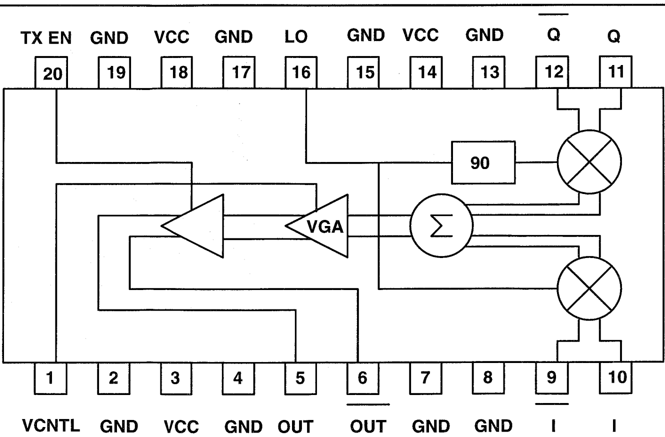


CASE 948D–03
(TSSOP–20)

- Linear I/Q Ports
- On Chip LO Phase Shifter
- I/Q Phase Imbalance = 2 degrees (Typ)
- I/Q Amplitude Imbalance = 0.3 dB (Typ)
- Gain Control = 30 dB (Typ)
- Single Source Low Operating Supply Voltage
- Low Power Consumption
- Low–Cost, Low Profile Plastic TSSOP Package
- Order MRFIC0001R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M001

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.5	Vdc
Control Voltages	TX EN, VCNTL	6.5	Vdc
LO Input Power	P_{LO}	0.0	dBm
Differential I/Q Input Voltage	V_D	2.0	V_{pp}
I, $\bar{I}$, Q, and $\bar{Q}$ DC Bias Voltage	V_B	2.0	Vdc
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C



Pin Connections and Functional Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 4

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.7 to 5.5	Vdc
LO Input Power	P_{LO}	–10	dBm
LO Frequency	f_{LO}	50 to 260	MHz
Differential I/Q Input Voltage	V_D	0 to 1.0	Vdc
I, $\overline{I}$, Q, and $\overline{Q}$ DC Bias Voltage	V_B	1.5 to 1.7	Vdc
Variable Gain Amplifier Control Voltage	V_{cntl}	0 to V_{CC}	Vdc
Transmit Enable Low Voltage	TX EN	0 to 0.2	Vdc
Transmit Enable High Voltage	TX EN	V_{CC} – 0.2 to V_{CC}	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V, TX EN = 3.0 V, V_{cntl} = 0.0 V, V_D = 0.8 V_{PP}, V_B = 1.6 V, P_{LO} = –10 dBm, f_{LO} = 248 MHz, f_D = 100 kHz, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Current	–	10	12	mA
Standby Current (TX EN = 0.0V)	–	40	100	µA
Single Sideband Output Power Level	–15	–13	–	dBm
Single Sideband Output Power 1dB Compression Point	–	–10	–	dBm
LO Leakage(2)	–	–55	–45	dBm
Undesired Sideband Level	–	–35	–30	dBc
Output Level Dynamic Range (V_{cntl} = 0 to 2.2V)(2)	–	30	–	dB
Turn–on/off Time	–	2	–	µs
I/Q Data				
Input 3dB Bandwidth	–	5	–	MHz
Amplitude Imbalance	–	0.3	–	dB
Phase Imbalance	–	2	–	degree

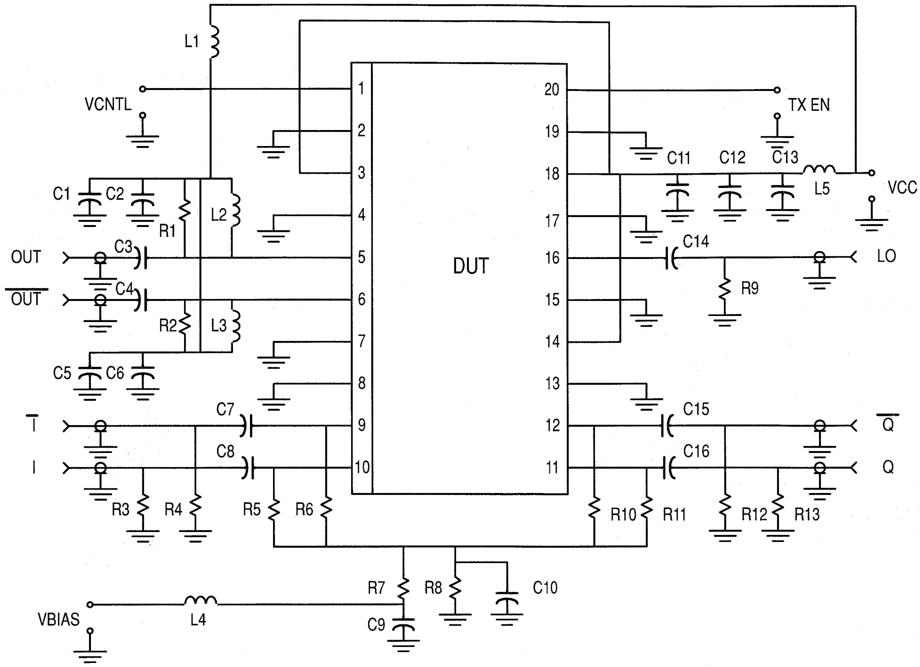
(1) All electrical characteristics measured in test circuit schematic shown in Figure 1.
V_B is the bias voltage on the input data ports.
V_D is the sinusoidal differential voltage on the input data ports when testing the part in a single sideband mode.
Above power levels are the single–ended output power.
(2) LO leakage power is unaffected by V_{cntl} setting.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

f MHz	Impedance Ω					
	LO		IF or –IF		I, –I, Q, –Q	
	R	jX	R	jX	R	jX
50	924	–694	164	–2330	181	–2448
60	825	–716	110	–1913	121	–2003
70	715	–713	83.2	–1661	88.1	–1709
80	635	–690	81.4	–1422	87.0	–1470
90	576	–691	86.8	–1312	93.4	–1361
100	509	–668	69.2	–1172	74.2	–1213
110	453	–651	56.0	–1055	72.2	–1091
120	400	–623	56.9	–969	60.3	–998
130	355	–595	47.3	–884	67.5	–913
140	330	–576	49.4	–835	38.3	–871
150	291	–551	49.8	–784	47.0	–815
160	259	–525	37.7	–730	41.2	–763
170	239	–509	32.5	–678	35.9	–712
180	225	–489	30.0	–651	33.0	–683
190	206	–473	30.4	–613	29.4	–644
200	187	–452	17.0	–579	22.7	–612
210	172	–440	33.1	–544	23.8	–580
220	158	–416	27.7	–521	24.5	–549
230	149	–402	20.5	–503	14.2	–530
240	137	–392	26.1	–482	18.3	–508
250	130	–375	19.5	–461	11.9	–485
260	119	–374	19.5	–437	17.1	–458
270	114	–353	20.1	–423	12.0	–443
280	105	–343	18.7	–408	11.1	–426
290	103	–332	20.7	–394	10.4	–412
300	93.5	–320	19.3	–380	9.65	–397
310	88.0	–312	17.9	–366	8.86	–380
320	84.8	–302	18.0	–354	6.91	–368
330	82.5	–296	19.4	–342	7.71	–354
340	76.1	–288	18.2	–332	6.02	–343
350	72.4	–282	15.0	–322	6.74	–331

Table 1. Selected Port Impedances



C1, C5, C9, C12 – 10000 pF, Chip Capacitor
C2, C6, C11 – 100 pF, Chip Capacitor
C3, C4 – 3.6 pF, Chip Capacitor
C7, C8, C10, C13, C15, C16 – 1 uF, Chip Capacitor
C14 – 10 pF, Chip Capacitor
L1, L4, L5 – 1.2 µH, Chip Inductor
L2, L3 – 68 nH, Chip Inductor

R1, R2 – 1000 Ω, Chip Resistor
R3, R4, R12, R13 – 510 Ω, Chip Resistor
R5, R6, R10, R11 – 2200 Ω, Chip Resistor
R7, R8, – 5100 Ω, Chip Resistor
R9 – 56 Ω, Chip Resistor

Figure 1. Typical Biasing Configuration

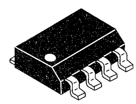
The MRFIC Line
Broadband GaAs Switch

MRFIC0903

ANTENNA SWITCH
GaAs MONOLITHIC
INTEGRATED CIRCUIT

The MRFIC0903 is an integrated GaAs SPDT switch designed for transceivers operating in the 100 MHz to 2.0 GHz frequency range. The design utilizes Motorola's advanced GaAs RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC0903 include Class 4 and 5 GSM, Class 1 and 2 DCS1800, DCS1900, DAMPS, PDC, digital cellular systems as well as analog cellular systems.

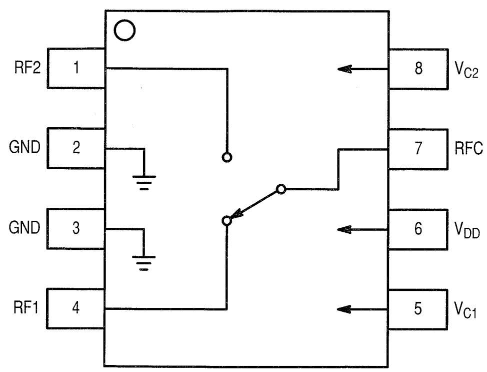
- 2.8 W Transmitting Capability through the Transmit Path with a 5.0 Volt Differential Control Signal
- 1.25 W Transmitting Capability through the Transmit Path with a 3.0 Volt Differential Control Signal
- Single Source Operating Supply Voltage
- Low Power Consumption
- Low–Cost, Low Profile Plastic SOIC Package
- Available in Tape and Reel by Adding R2 Suffix. R2 Suffix = 2,500 Units per Reel.
- Device Marking = M0903



CASE 751–05
(SO–8)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	10	Vdc
Control Voltage	V_{C1}, V_{C2}	V_{DD} + 0.8, V_{DD} – 12	Vdc
Power Dissipation	P_D	1.0	W
Power Input (Non–selected Port)	P_{in}	0.325	W
Ambient Operating Temperature	T_A	–35 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C



Pin Connections and Functional Block Diagram

REV 1

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	0 to 5.0	Vdc
Control Voltage Range	V_{C1}, V_{C2}	V_{DD} – 5.0 to V_{DD} + 0.5	Vdc
RF Frequency Range	f_{RF}	100 to 2000	MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V, P_{in} = 2.5 W (34 dBm), f = 900 MHz, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Current				
I_{DD}	—	100	170	µA
$I_{Control}$	—	150	300	µA
VSWR	—	1.5:1	—	
Insertion Loss (RFC/RF1, RFC/RF2)	—	0.55	0.8	dB
Isolation (RFC/RF2, RFC/RF1)	18	20	—	dB
Output Power at 0.1 dB Compression	—	34.5	—	dBm

Electrical Characteristics at 900 MHz measured in test circuit schematic shown in Figure 1 with board losses removed.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V, P_{in} = 2.0 W (33 dBm), f = 1800 MHz, T_A = 25°C unless otherwise noted)

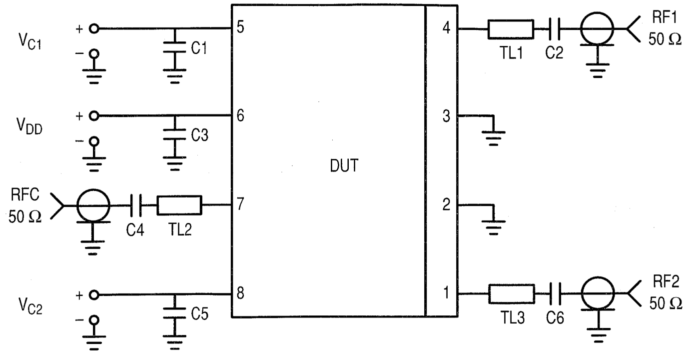
Characteristic	Min	Typ	Max	Unit
Supply Current				
I_{DD}	—	100	170	µA
$I_{Control}$	—	150	300	µA
VSWR	—	1.5:1	—	
Insertion Loss (RFC/RF1, RFC/RF2)	—	0.7	0.85	dB
Isolation (RFC/RF2, RFC/RF1)	18	20	—	dB
Output Power at 0.1 dB Compression	—	34	—	dBm

Electrical Characteristics at 1800 MHz measured in test circuit schematic shown in Figure 2 with board losses removed.

V_{C1} and V_{C2} Input Voltage	Min	Typ	Max	Unit
High	V_{DD}	—	V_{DD} + 0.5	Vdc
Low	V_{DD} – 10	—	V_{DD} – 5	Vdc

V_{C1}	V_{C2}	RFC – RF1	RFC – RF2
High	Low	Insertion Loss	Isolation
Low	High	Isolation	Insertion Loss

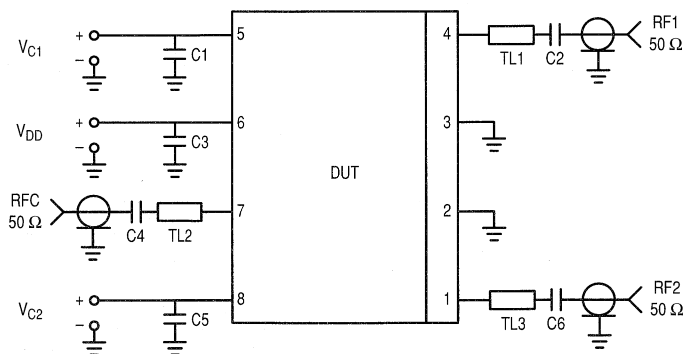
Table 1. Logic Levels



C1, C5 — 2.7 pF, Chip Capacitor
C2, C4, C6 — 100 pF, Chip Capacitor
C3 — 10 pF, Chip Capacitor
TL1, TL3 — 12 degrees of 50 Ω line at 1 GHz
TL2 — 15 degrees of 50 Ω line at 1 GHz

Note: Decoupling capacitors on pins 5, 6 and 8 must be as close as possible to the pins.

Figure 1. 300 MHz to 1600 MHz Test Circuit Configuration



C1, C5 — 1.3 pF, Chip Capacitor
C2, C3, C4, C6 — 8.2 pF, Chip Capacitor
TL1, TL3 — 12 degrees of 50 Ω line at 1 GHz
TL2 — 15 degrees of 50 Ω line at 1 GHz

Note: Decoupling capacitors on pins 5, 6 and 8 must be as close as possible to the pins.

Figure 2. 1600 MHz to 2000 MHz Test Circuit Configuration

TYPICAL CHARACTERISTICS

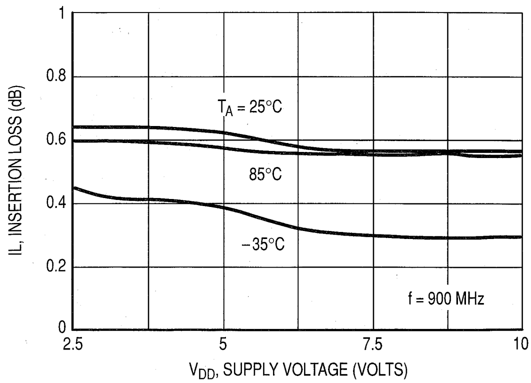


Figure 3. Insertion Loss at 0.1 dB Compression versus Supply Voltage

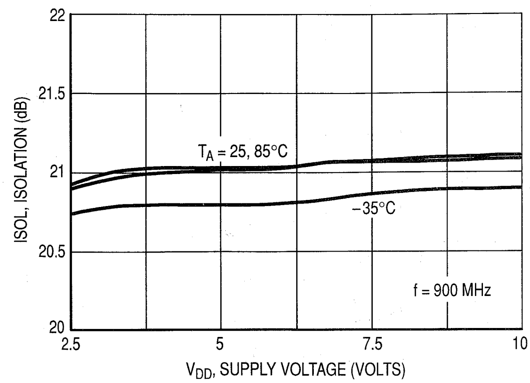


Figure 4. Isolation at 0.1 dB Compression versus Supply Voltage

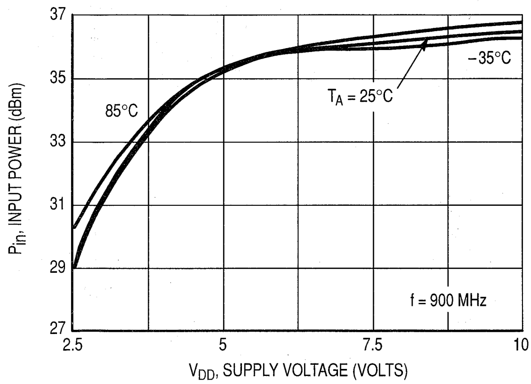


Figure 5. Input Power at 0.1 dB Compression versus Supply Voltage

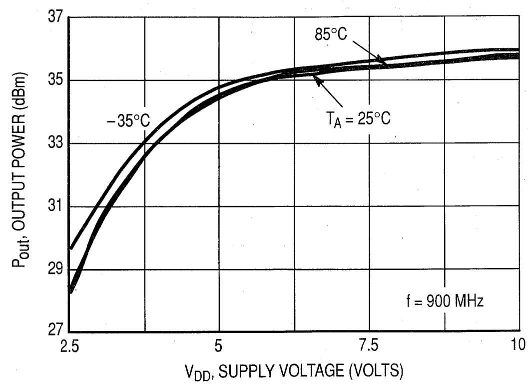


Figure 6. Output Power at 0.1 dB Compression versus Supply Voltage

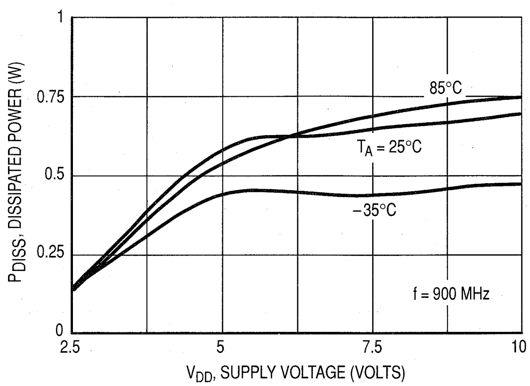


Figure 7. Dissipated Power at 0.1 dB Compression versus Supply Voltage

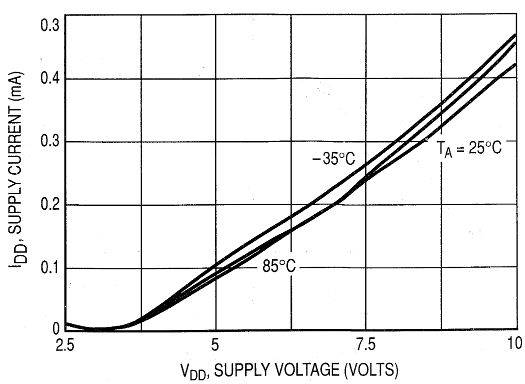


Figure 8. Supply Current at 0.1 dB Compression versus Supply Voltage

TYPICAL CHARACTERISTICS

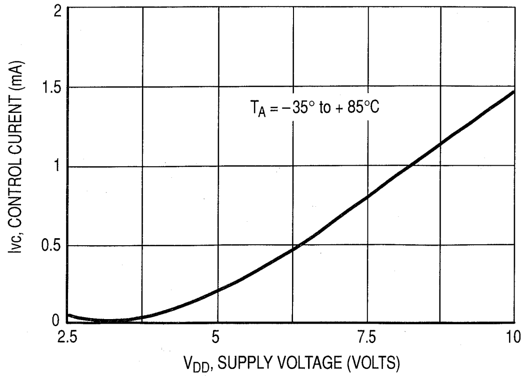


Figure 9. Control Current at Vc Pins at 0.1 dB Compression versus Supply Voltage

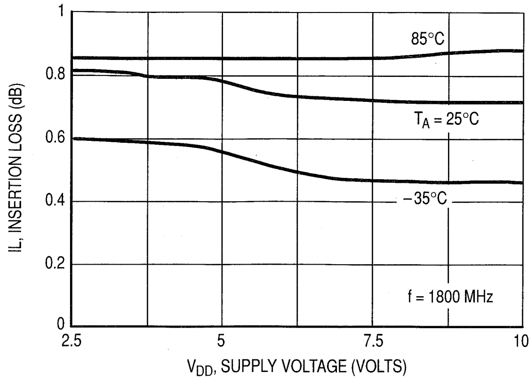


Figure 10. Insertion Loss at 0.1 dB Compression versus Supply Voltage

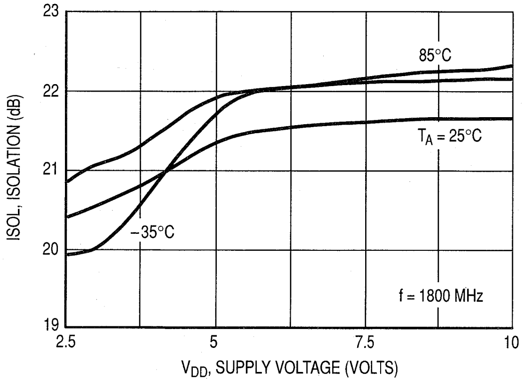


Figure 11. Isolation at 0.1 dB Compression versus Supply Voltage

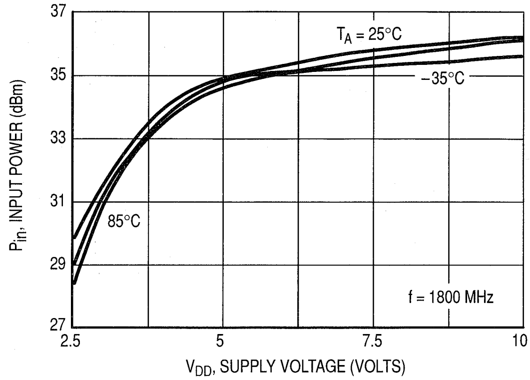


Figure 12. Input Power at 0.1 dB Compression versus Supply Voltage

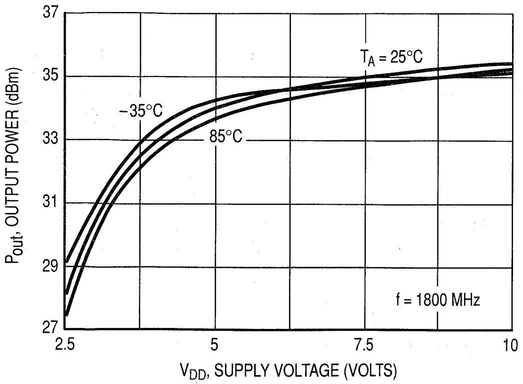


Figure 13. Output Power at 0.1 dB Compression versus Supply Voltage

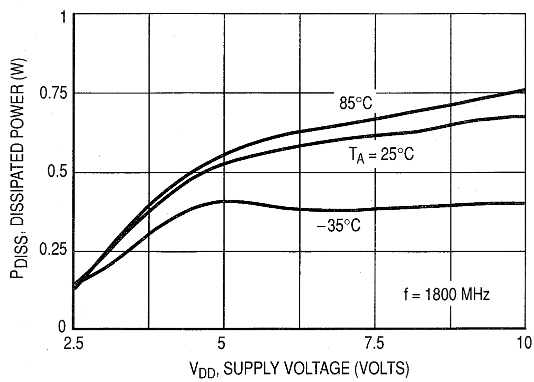


Figure 14. Dissipated Power at 0.1dB Compression versus Supply Voltage

TYPICAL CHARACTERISTICS

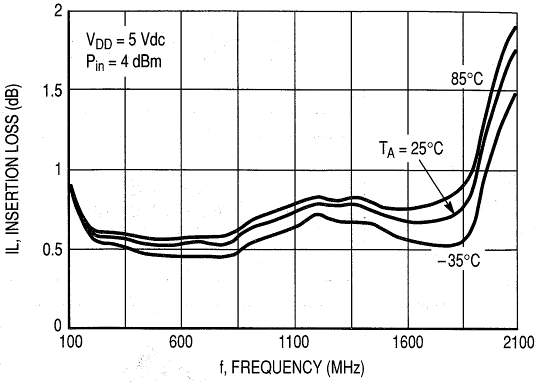


Figure 15. Insertion Loss versus Frequency

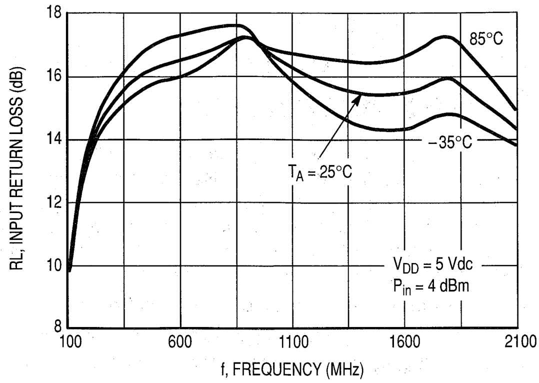


Figure 16. Input Return Loss versus Frequency

APPLICATIONS INFORMATION

DESIGN INFORMATION

The MRFIC0903 SPDT antenna switch was designed for low cost, flexibility and ease of use. This is accomplished by its internal topology that allows control of the switch through its TTL/CMOS compatible (0 to V_{DD}) control pins. Operating on a single positive supply, the switch was designed for a minimum supply voltage, minimum power consumption and low current TTL/CMOS compatible control signals.

THEORY OF OPERATION

The MRFIC0903 can be used as a transmit and receive or antenna diversity switch in the frequency range from 100 MHz to 2 GHz with incident power levels as high as 4 watts.

The frequency behavior can be optimized by resonating the DC blocking capacitor's position and value with the parasitic inductance of the package lead. Operation from 300 MHz to 1.6 GHz can be optimized with a high Q 100 pF blocking capacitor. For the higher frequency band from 1.6 GHz to 2.0 GHz, a 8.2 pF capacitor is suggested. Further improvements can be achieved by resonating the inductance of V_{DD}, V_{C1}, and V_{C2} pins with the appropriate capacitor values.

The power handling capability and linearity of the MRFIC0903 is dependent only on the supply voltage. With a 3 V supply, the device handles 1.25 W (1.6 W PEP) of incident power while maintaining good linearity and low harmonic distortion. The power transmitting capability increases to 3 W of incident power with a 5 V supply and up to 4 W with a 7.5 V supply.

Due to the device's inherently low harmonic distortion, the switch requires little harmonic filtering at its outputs. It also has a high reverse third–order intercept point for use in non–TDMA antenna diversity applications (analog cellular systems).

BIASING CONSIDERATIONS

The MRFIC0903 is based on a floating "cold FET" topology. With this topology, the differential voltage between V_{C1} and V_{C2} dictates the power handling capability. For example, the device's power handling capability is the same with the device biased with 5 V at V_{C1} and 0 V at V_{C2}, with 0 V at V_{C1} and –5 V at V_{C2}, or with 3 V at V_{C1} and −2 V at V_{C2}.

POSSIBLE APPLICATIONS

The MRFIC0903 can be used in a number of cellular and cordless phone applications. The part is applicable for analog cellular phones in systems such as AMPS, TACS, NAMPS, ETACS and NMT900; for digital cellular phones in systems such as GSM, PDC, DAMPS, DCS1800, PCS and NADC; and for cordless phones in systems such as DECT, PHS, ISM, CT1 and CT2. In general it can fit into any application where high power handling capability is required for frequencies ranging from 100 MHz to 2 GHz.

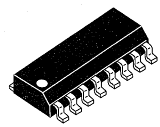
EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line
900 MHz GaAs Two-Stage Driver Amplifier

MRFIC0904

**900 MHz GaAs
TWO STAGE DRIVER AMP
INTEGRATED CIRCUIT**



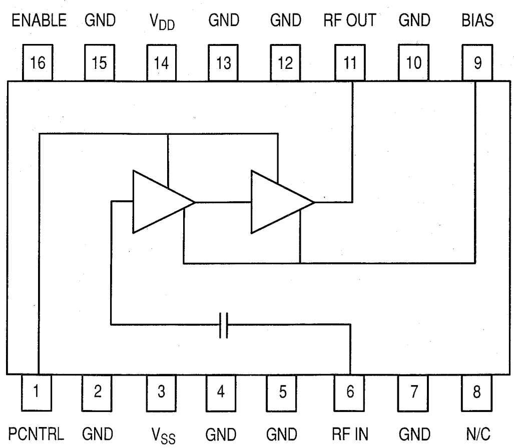
**CASE 751B–05
(SO–16)**

The MRFIC0904 is an integrated driver amplifier designed for class A/B operation in the 800 MHz to 1 GHz frequency range. The design utilizes Motorola's Advanced GaAs FET process to yield superior performance and efficiency in a cost effective monolithic device. Off–chip output matching provides maximum flexibility in design. Applications for the MRFIC0904 include GSM, AMPS, and ISM band transmitters.

- GSM Ramping/Gain Control of 45 dB with Power Control Function (PCNTRL)
- Class 4 P_{out} (1 dB Gain Compression) = 26 dBm @ 4.8 V (Typical)
- Class 4 Supply Current (1 dB) = 120 mA @ 4.8 V (Typical)
- Class 5 P_{out} (1 dB Gain Compression) = 24 dBm 3.6 V (Typical)
- Class 5 Supply Current (1 dB) = 120 mA @ 3.6 V (Typical)
- Low Cost Surface Mount Plastic Package
- Order MRFIC0904R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0904

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD} V_{SS}	6.0 –3	Vdc
Power Control Voltage	PCNTRL	V_{DD}	Vdc
Enable Voltage	ENABLE	V_{DD}	Vdc
Input Power	P_{in}	5	dBm
Operating Ambient Temperature	T_A	– 35 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Thermal Resistance, Junction to Case	θ_{JC}	60	°C/W



Pin Connections and Functional Block Diagram

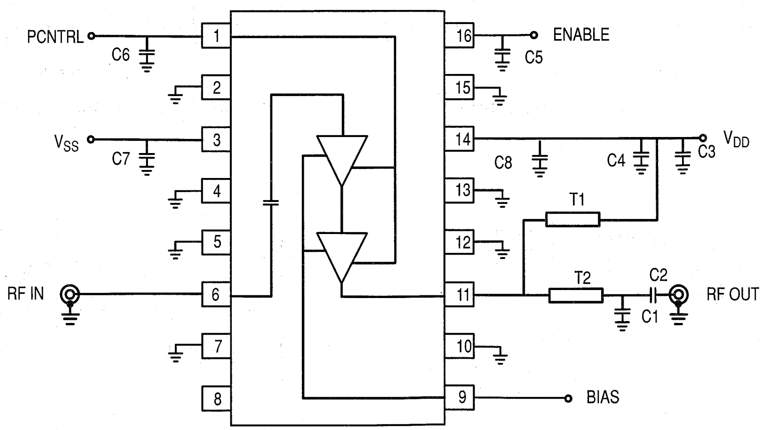
RECOMMENDED OPERATING RANGES (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD} V_{SS}	2.7 to 5.0 −2.75 to −2.25	Vdc
Bias Voltage Range	BIAS	0 to 1.0	Vdc
Power Control Voltage Range	PCNTRL	0 to 3.0	Vdc
Enable Voltage ON State	ENABLE	2.5	Vdc
Enable Voltage OFF State	ENABLE	0.5	Vdc
RF Frequency	f	800 to 1000	MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.6 V, V_{SS} = –2.5 V, BIAS = 0.0 V, PCNTRL = 3.0 V, ENABLE = 3.0 V, P_{in} = –2 dBm, f = 900 MHz, Z_O = 50 Ω, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Current I_{DD} I_{SS}	 — —	 120 1.0	 160 1.75	mA
Standby Current: Off–mode (ENABLE = 0 V) I_{DD} I_{SS}	 — —	 50 60	 130 360	µA
Output Power	22.5	24	—	dBm
Output Power at 1 dB Gain Compression	—	24.5	—	dBm
Input Return Loss	—	14	—	dB
PCNTRL Current	—	200	—	µA
ENABLE Current	—	200	—	µA
Gain Control Range	—	45	—	dB
Enable/Control Input 3 dB Bandwidth	—	1	—	MHz

(1) All electrical Characteristics are measured in test circuit schematic as shown in Figure 1.



C1 – 2.7 pF
C2, C4, C8 – 100 pF
C3 – 1 µF
C5, C6 – 10 pF
C7 – 1000 pF
T1 – 90° @ 900 MHz, Z_0 = 100 Ω
T2 – 9° @ 900 MHz, Z_0 = 50 Ω
BOARD MATERIAL = FR4

Figure 1. Applications Circuit Configuration

TYPICAL CHARACTERISTICS

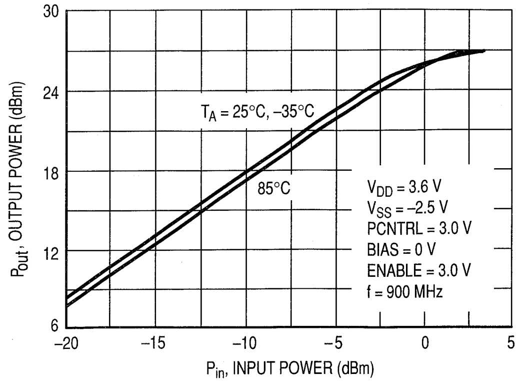


Figure 2. Output Power versus Input Power

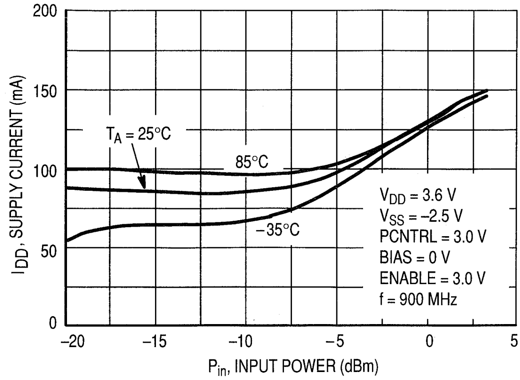


Figure 3. Supply Current versus Input Power

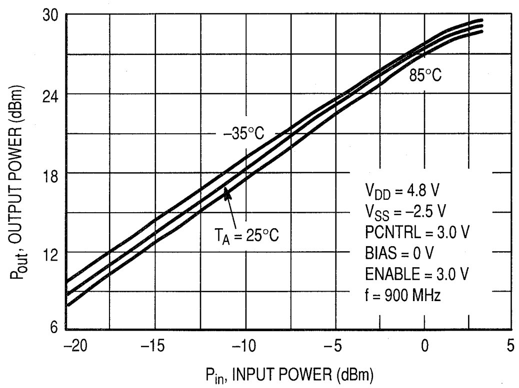


Figure 4. Output Power versus Input Power

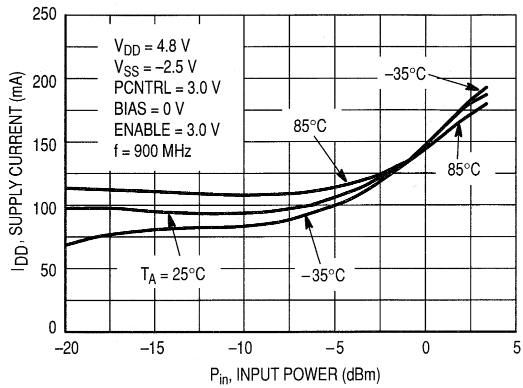


Figure 5. Supply Current versus Input Power

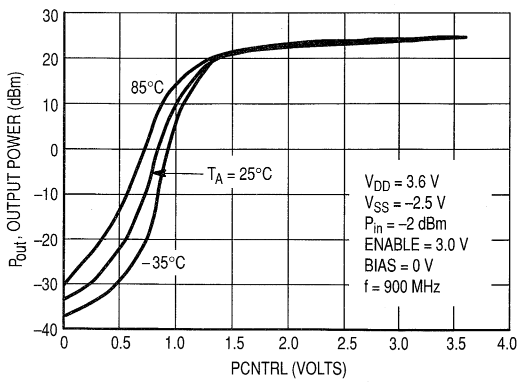


Figure 6. Output Power versus PCNTRL

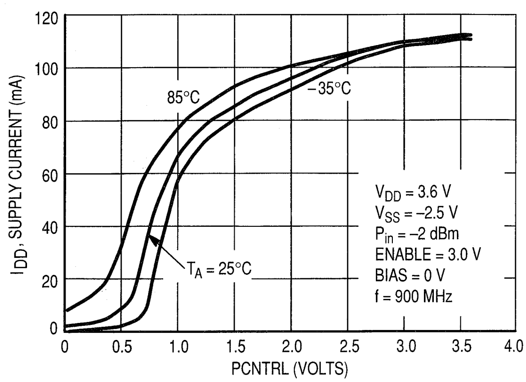


Figure 7. Supply Current versus PCNTRL

TYPICAL CHARACTERISTICS

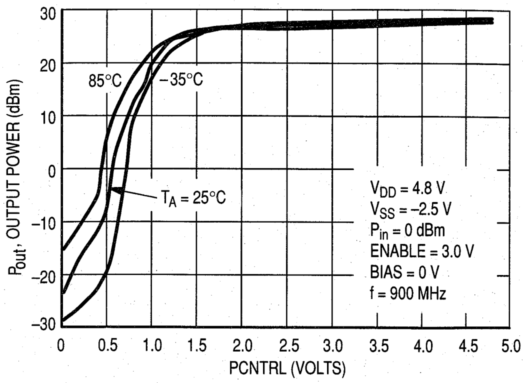


Figure 8. Output Power versus PCNTRL

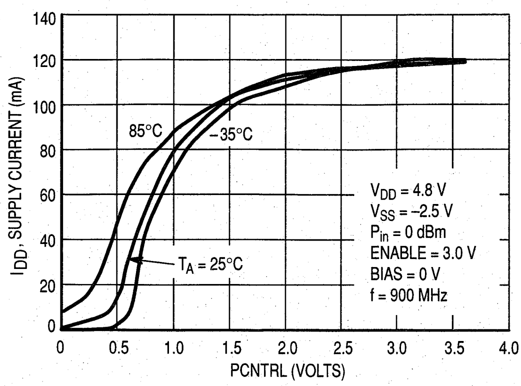


Figure 9. Supply Current versus PCNTRL

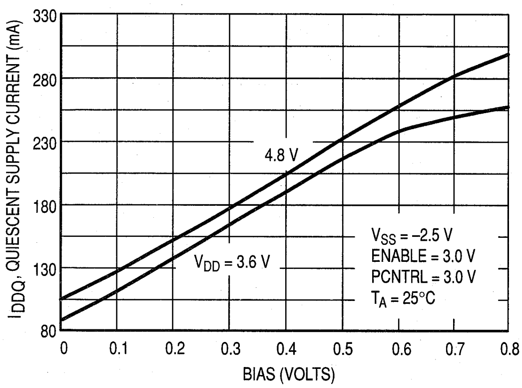


Figure 10. Quiescent Supply Current versus BIAS

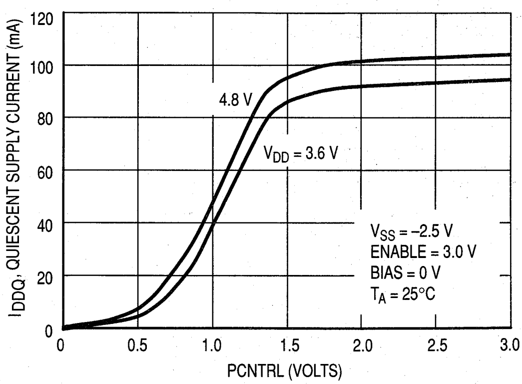


Figure 11. Quiescent Supply Current versus PCNTRL

Table 1. Scattering Parameters
(V_{DD} = 3.6 V, V_{SS} = –2.5 V, BIAS = 0.0 V, PCNTRL, ENABLE = 3 V, 50 Ω System)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
500	0.922	–40.93	12.201	–76.39	0.002	72.64	0.276	166.48
550	0.887	–52.05	16.242	–98.58	0.002	62.03	0.276	169.80
600	0.826	–65.21	21.133	–116.66	0.003	44.52	0.297	175.47
650	0.698	–81.22	28.039	–140.66	0.004	26.65	0.342	173.06
700	0.419	–99.95	33.973	174.46	0.004	6.35	0.360	169.94
750	0.206	–106.43	32.195	145.72	0.006	–9.10	0.393	163.65
800	0.073	–56.19	31.685	121.12	0.006	–31.13	0.392	154.83
850	0.146	–4.45	29.419	85.45	0.006	–47.59	0.351	146.93
900	0.170	–1.59	25.996	64.50	0.006	–61.44	0.305	145.90
950	0.183	10.82	24.115	45.18	0.007	–80.54	0.276	152.91
1000	0.232	27.47	22.091	16.72	0.007	–107.22	0.287	162.87
1050	0.302	34.19	19.995	–5.08	0.007	–116.06	0.310	167.00
1100	0.395	34.85	17.411	–26.64	0.006	–125.77	0.337	170.51
1150	0.522	29.21	14.15	–52.28	0.006	–146.60	0.380	169.57
1200	0.607	23.25	11.961	–71.38	0.005	–154.46	0.403	167.34
1250	0.675	17.30	9.76	–88.04	0.005	–177.16	0.419	163.73
1300	0.743	9.17	7.951	–108.01	0.004	160.61	0.436	159.33

Table 2. Scattering Parameters
(V_{DD} = 4.8 V, V_{SS} = –2.5 V, BIAS = 0.0 V, PCNTRL, ENABLE = 3 V, 50 Ω System)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
500	0.910	–41.17	12.58	–78.69	0.0012	65.66	0.228	168.72
550	0.873	–51.75	17.09	–99.91	0.0024	43.49	0.232	172.87
600	0.807	–64.98	22.33	–118.28	0.0032	48.13	0.252	177.75
650	0.671	–81.03	29.24	–142.97	0.0041	17.29	0.293	174.31
700	0.409	–100.12	35.95	172.30	0.0040	–10.22	0.326	172.83
750	0.200	–104.83	34.04	143.18	0.0055	–14.65	0.349	164.57
800	0.080	–53.72	33.08	118.78	0.0056	–28.05	0.345	156.12
850	0.142	–6.52	30.64	83.58	0.0057	–45.38	0.307	147.87
900	0.165	0.32	27.22	62.36	0.0065	–62.81	0.248	146.40
850	0.187	14.68	24.95	41.95	0.0066	–86.95	0.226	146.72
1000	0.252	28.28	22.30	14.13	0.0062	–100.71	0.257	167.95
1050	0.323	32.92	20.06	–7.52	0.0057	–113.16	0.279	172.05
1100	0.409	32.35	17.37	–28.14	0.0049	–121.71	0.310	173.62
1150	0.527	26.77	14.03	–53.24	0.0051	–152.49	0.349	171.86
1200	0.606	21.18	11.89	–71.66	0.0051	–159.64	0.365	169.36
1250	0.669	15.59	9.74	–87.41	0.0043	–155.55	0.381	163.46
1300	0.735	8.10	7.96	–107.51	0.0039	171.99	0.397	161.81

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC0904 is a versatile driver amplifier designed to operate in the 800 MHz to 1 GHz frequency range for cellular phone and Industrial, Scientific, and Medical (ISM) applications. The amplifier is designed using depletion mode GaAs MESFETs to perform at high efficiency at battery voltages of 3.6 and 4.8 Volts. While designed as a driver amplifier for a discrete transistor final stage, the device can act as a power amplifier for lower power systems such as ISM applications in telemetry and cordless telephones.

THEORY OF OPERATION

The MRFIC0904 has various control features making it versatile and applicable to both linear and saturated applications. The BIAS pin allows the setting of drain quiescent current. For non–linear applications such as GSM cellular, the pin can be grounded. For better gain and linearity, a positive voltage up to about 0.6 Volts can be applied. The PCNTRL pin allows the control of the output power over a wide dynamic range with low AM to AM distortion such as is required in GSM and other cellular systems. As shown in Figures 6 through 9, PCNTRL affects both the output power and the drain current thus maintaining good efficiency over a range of output power. The ENABLE pin is used to control the on–off state of the device and is useful as a reduced current standby control. A logic high signal of more than 2.5 Volts turns the device on. A logic low signal of less than 0.5 Volts reduces total supply current to typically less than 200 μA.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

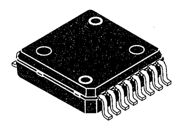
The MRFIC Line
900 MHz GaAs Integrated Power Amplifier

MRFIC0912

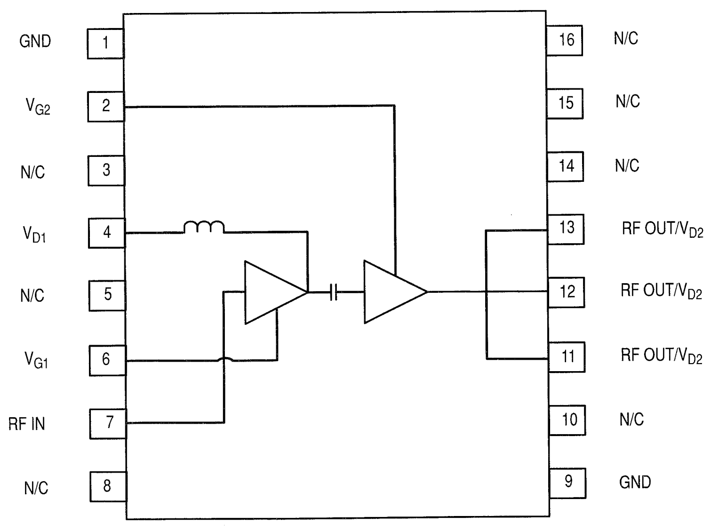
Designed primarily for use in high efficiency Analog Cellular applications, the MRFIC0912 is a two–stage power amplifier in Motorola's proprietary Power Flat Pack 16–lead package. This integrated circuit requires minimal off-chip matching while allowing for the maximum in flexibility in optimizing gain and efficiency. The design employs Motorola's planar, self–aligned GaAs MESFET IC process to give the highest efficiency possible.

- Usable Frequency Range = 800–1000 MHz, Specified for 824–905 MHz
- 30.8 dBm Minimum Output Power
- 470 mA Maximum Supply Current at 30.8 dBm Output
- 23.8 dB Minimum Gain
- Simple Off–chip Matching for Maximum Power/Efficiency Flexibility
- 4.6 Volt Supply
- 45 dB/Volt Typical Power Output Control
- Order MRFIC0912R2 for Tape and Reel Option. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0912

900 MHz
GaAs INTEGRATED
POWER AMPLIFIER



CASE 978–02
(PFP–16)



Pin Connections and Functional Block Diagram

REV 1

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Ratings	Symbol	Limit	Unit
Supply Voltage	V_{D1}, V_{D2}	8	Vdc
RF Input Power	P_{RF}	20	dBm
Gate Voltage	V_{G1}, V_{G2}, V_{GG}	–5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Case Temperature	T_C	– 35 to +100	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	18	°C/W

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	824–905	MHz
Supply Voltage	V_{D1}, V_{D2}	4.0–6.0	Vdc
Gate Voltage	V_{G1}, V_{G2}	–2.3 to –1.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 4.6 V, T_A = 25°C, f_{RF} = 840 MHz, P_{in} = 7 dBm, V_{GG} set for I_{D2Q} = 200 mA, Tested in Circuit Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
RF Output Power	30.8	31.2	—	dBm
Power Slump (V_{D1}, V_{D2} = 4.0 V, T_C = 100°C)	28.5	—	—	dBm
Load Mismatch Survival (V_{D1}, V_{D2} = 7 V, Load VSWR = 10:1, all phases, 10 sec)	No Degradation			
Spurious Output (V_{D1},V_{D2} = 0 to 7 V, P_{in} = 5 to 9 dBm, Load VSWR = 10:1)	—	—	–60	dBc
Input Return Loss	—	10	—	dB
Harmonic Output (P_{out} = 30.8 dBm)				dBc
$2f_0$	—	—	–25	
$3f_0$	—	—	–40	
$4f_0$	—	—	–40	
Noise Power (V_{DD} = 0 to 7 V, 45 MHz Above f_{RF} at 30 kHz BW)	—	—	–93	dBm
Maximum Power Control Voltage Slope (Change in P_{out} for Change on V_{D1})	—	45	—	dB/V
Total Supply Current (V_{D1} set for P_{out} = 30.8 dBm)	—	430	470	mA
V_{GG} Required for I_{D2Q} = 200 mA	–2.3	–2.0	–1.7	Vdc
Gate Current during RF Operation	–2	—	2	mA

DESIGN AND APPLICATIONS INFORMATION

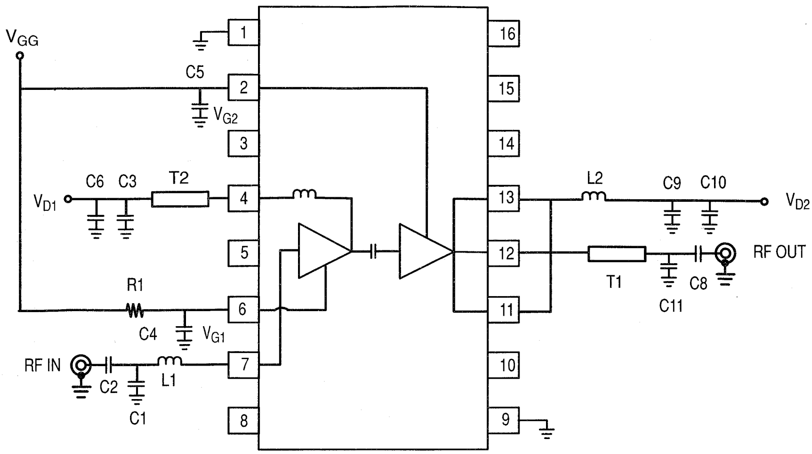
The MRFIC0912 has been designed for high efficiency 900 MHz applications such as analog cellular and Industrial, Medical and Scientific (ISM) equipment. The two stage MESFET design utilizes Motorola's planar refractory gate process to allow high performance GaAs to be applied to consumer applications. The proprietary PFP–16 package assures good grounding and low thermal resistance.

As shown in Figure 1, the gate voltage pins can be ganged together and one voltage applied to both gates to set the quiescent operating current. Alternatively, V_{G1} and V_{G2} can be set separately. V_{D1} can be used as power control with a 45 dB per volt sensitivity. The placement of C3 in the V_{D1} supply line can be varied to optimize RF performance since T2 is part of a shunt L matching section. On the output, pins 11, 12 and 13, the placement of C11 is adjusted for best RF performance.

Layout is important for amplifier stability and RF performance. Ground vias must be located as close to circuit ground connections as possible. Power supply bypassing C3, C6, C9, and C10 must be included to reduce out–of–band gain and prevent spurious output.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.



R1	1 kΩ	C6	0.01 µF	L2	22 nH
C1	3.3 pF	C10	1 µF	T1	50 Ω, 13° @ 840 MHz
C2, C3, C8, C9	100 pF	C4, C5	1000 pF	T2	50 Ω, 8° @ 840 MHz
C11	8.2 pF	L1	10 nH		

BOARD MATERIAL — GLASS/EPOXY, ε_r = 4.45, THICKNESS = 18 MIL

Figure 1. Applications Circuit Configuration

TYPICAL CHARACTERISTICS

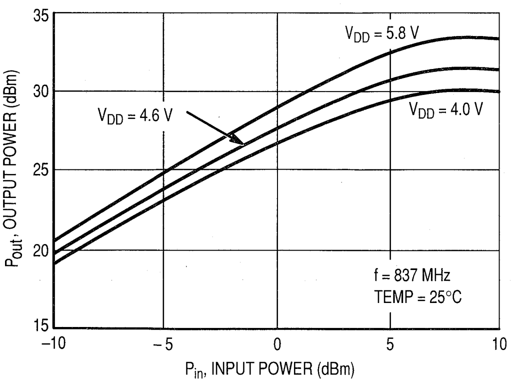


Figure 2. Output Power versus Input Power

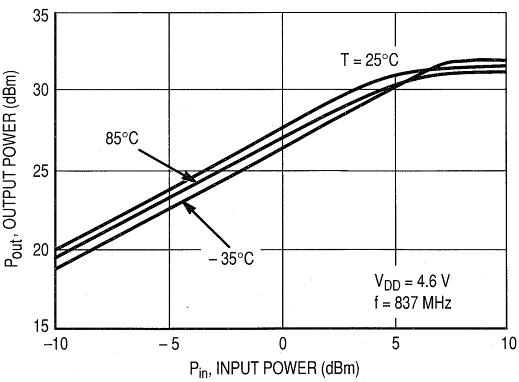


Figure 3. Output Power versus Input Power

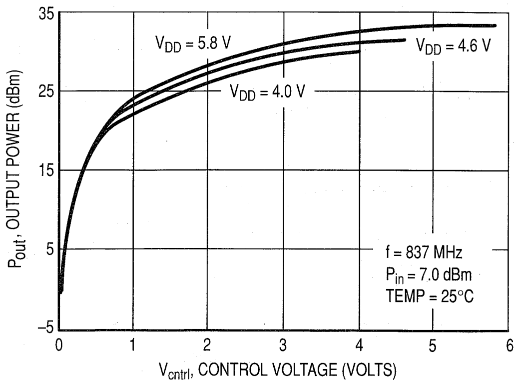


Figure 4. Output Power versus Control Voltage

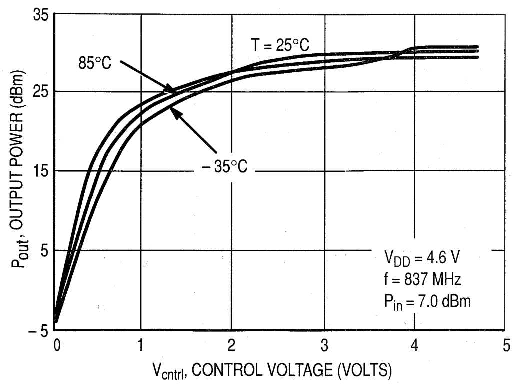


Figure 5. Output Power versus Control Voltage

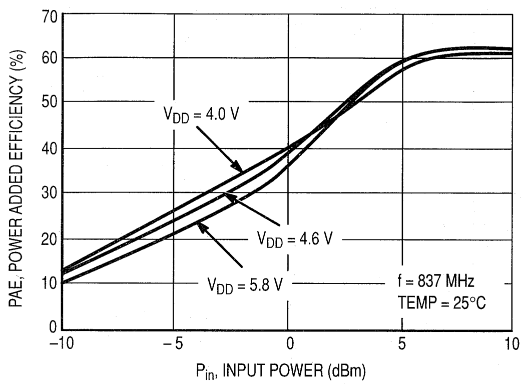


Figure 6. Power Added Efficiency versus Input Power

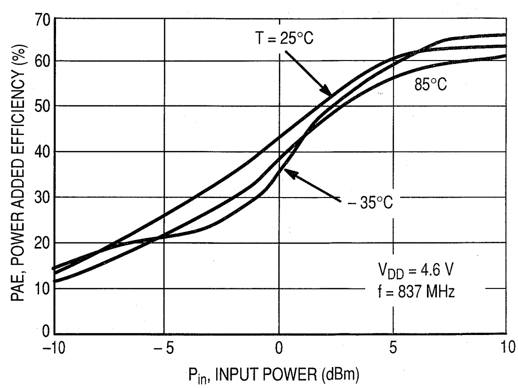


Figure 7. Power Added Efficiency versus Input Power

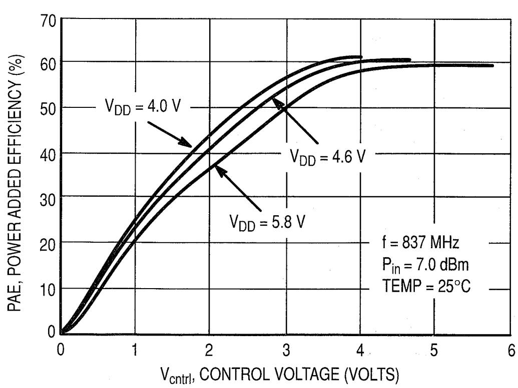


Figure 8. Power Added Efficiency versus Control Voltage

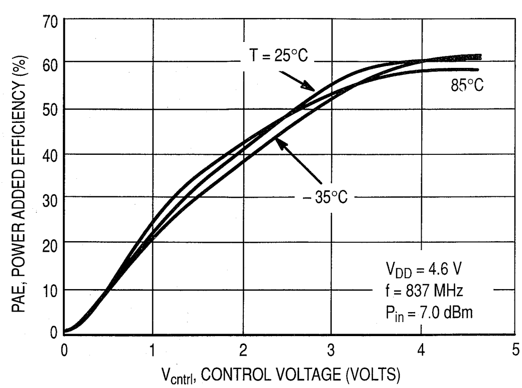


Figure 9. Power Added Efficiency versus Control Voltage

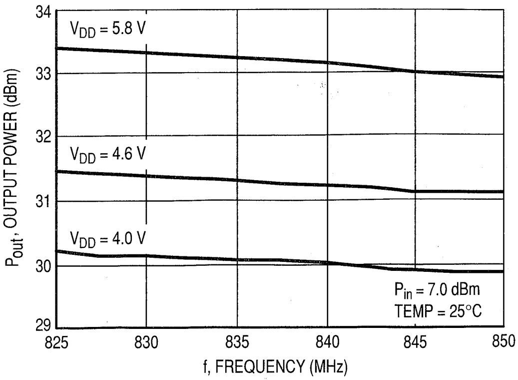


Figure 10. Output Power versus Frequency

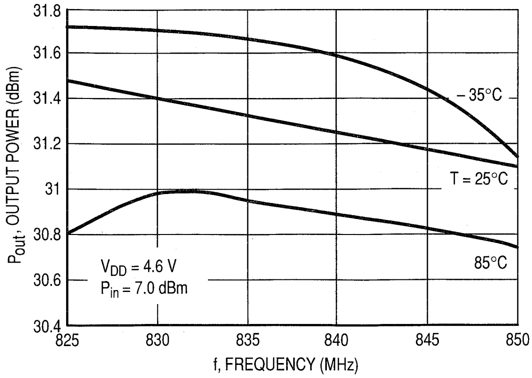


Figure 11. Output Power versus Frequency

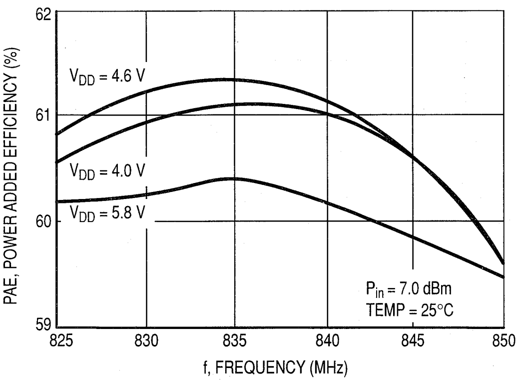


Figure 12. Power Added Efficiency versus Frequency

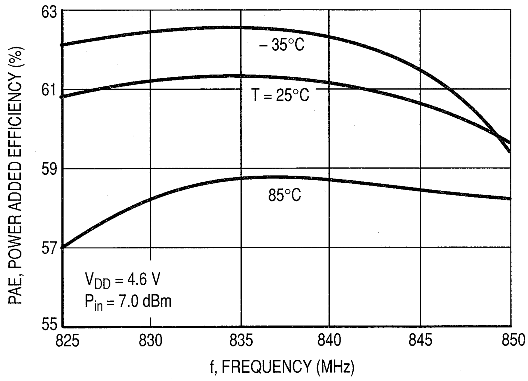


Figure 13. Power Added Efficiency versus Frequency

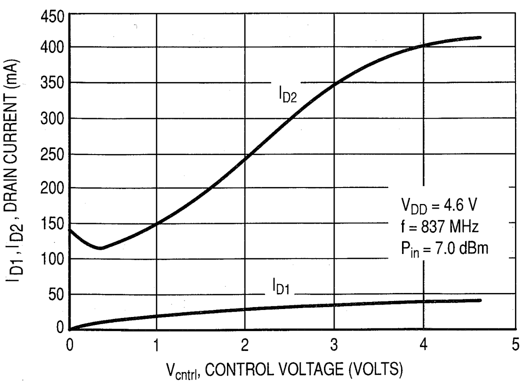


Figure 14. Drain Current versus Control Voltage

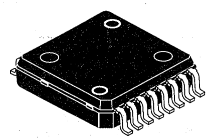
The MRFIC Line
900 MHz GaAs Integrated Power Amplifier

MRFIC0913

**900 MHz
GSM CELLULAR
INTEGRATED POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT**

This integrated circuit is intended for GSM class IV handsets. The device is specified for 2.8 watts output power and 48% minimum power added efficiency under GSM signal conditions at 4.8 Volt supply voltage. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Package which gives excellent thermal performance through a solderable backside contact.

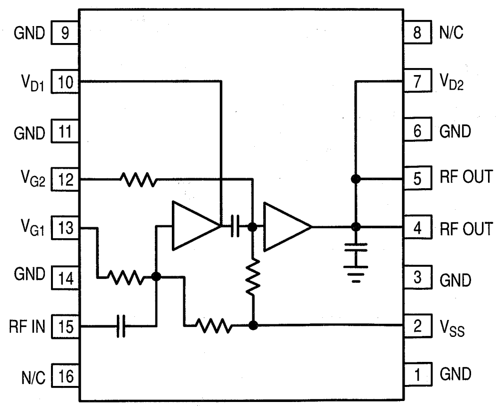
- Usable Frequency Range 800 to 1000 MHz
- Typical Output Power:
  36.0 dBm @ 5.8 Volts
  35.0 dBm @ 4.8 Volts
  31.5 dBm @ 3.6 Volts
- 48% Minimum Power Added Efficiency
- Low Parasitic, High Thermal Dissipation Package
- Order MRFIC0913R2 for Tape and Reel Option.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0913



**CASE 978–02
(PFP–16)**

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}	9	Vdc
RF Input Power	P_{in}	15	dBm
Gate Voltage	V_{SS}	–6	Vdc
Ambient Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W



Pin Connections and Functional Block Diagram

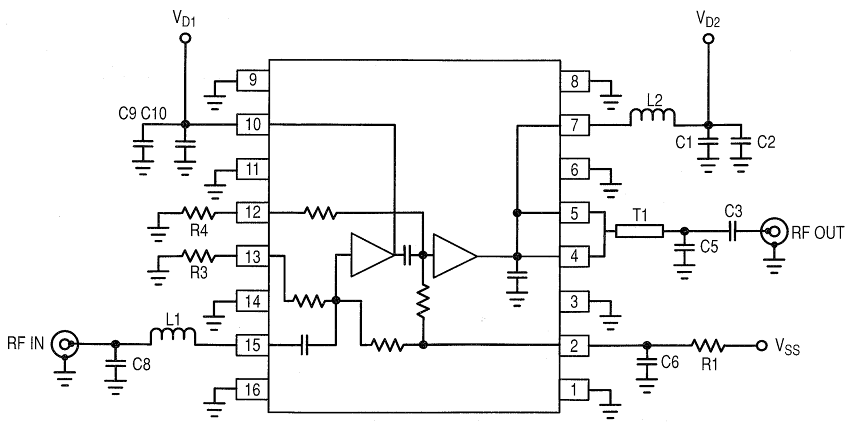
REV 1

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}	2.7 to 7.5	Vdc
Gate Voltage	V_{SS}	–5 to –3	Vdc
RF Frequency Range	f_{RF}	800 to 1000	MHz
RF Input Power	P_{RF}	6 to 13	dBm

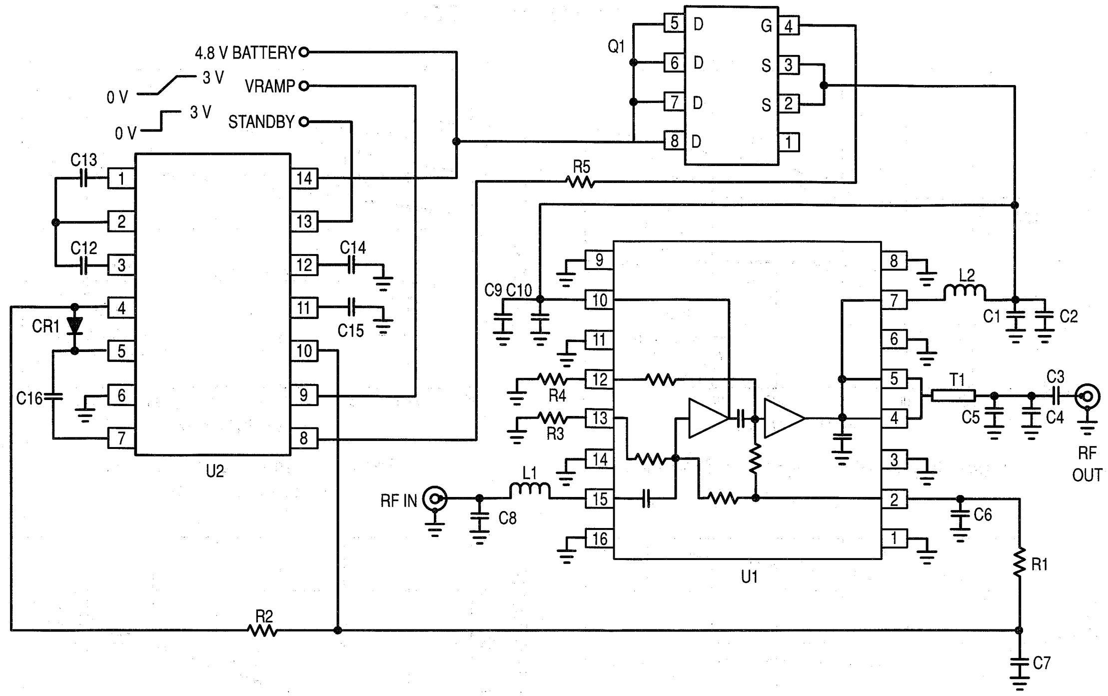
ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 4.8 V, V_{SS} = –4 V, P_{in} = 10 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Reference Circuit Shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Frequency Range	880	—	915	MHz
Output Power	34.5	35	—	dBm
Power Added Efficiency	48	—	—	%
Input VSWR	—	2:1	—	VSWR
Harmonic Output 2nd 3rd	 — —	 — —	 –30 –35	dBc
Output Power at Low voltage (V_{D1}, V_{D2} = 4.0 V)	33.3	33.5	—	dBm
Output Power, Isolation (V_{D1}, V_{D2} = 0 V)	—	–20	–15	dBm
Noise Power in 100 kHz, 925 to 960 MHz	—	—	–90	dBm
Stability – Spurious Output (P_{in} = 10 to 13 dBm, P_{out} = 5 to 35 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle, V_{D1}, V_{D2} adjusted for Specified P_{out})	—	—	–60	dBc
Load Mismatch stress (P_{in} = 10 to 13 dBm, P_{out} = 5 to 35 dBm, Load VSWR = 10:1 at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth (V_{D1}, V_{D2} = 0 to 6 V)	1	—	—	MHz
Negative Supply Current	—	—	1.25	mA



C1, C3, C10	47 pF, ATC	L1	8.2 nH, 0805 Toko	R3	1.8 kΩ
C2, C9	47 nF, Vitramon	L2	10 Turn MicroSpring, Coilcraft 1606–10	R4	2.7 kΩ
C5	10 pF, ATC			T1	5 mm 30 Ω Microstrip Line
C6	22 nF, Vitramon	R1	330 Ω	BOARD MATERIAL	Glass/Epoxy, ε_r = 4.45
C8	6.8 pF, ATC				

Figure 1. 900 MHz Reference Circuit



C1	33 pF, 0603 NPO/COG	CR1	MMBD701LT1	R2	100 Ω
C2, C9	33 nF	L1	8.2 nH, 0805 Toko	R3	1.8 kΩ
C3	47 pF, 0603 NPO/COG	L2	10 Turn MicroSpring,	R4	2.7 kΩ
C4, C5, C8	6.8 pF, 0603 NPO/COG		Coilcraft 1606–10 (for	R5	470 Ω
C6	33 nF		improved harmonic rejection	T1	5 mm 30 Ω Microstrip Line
C7	220 nF		only)	U1	MRFIC0913
C10	33 pF, 0603 NPO/COG	Q1	MMSF4N01HD	U2	MC33169 (–4 V Version)
C12 – C16	1 μF	R1	330 Ω	BOARD MATERIAL	Glass/Epoxy, $\varepsilon_r = 4.45$

Note: Use of a Schottky diode such as MMBD701LT1 for CR1 is mandatory below 3.6 V.
A general purpose silicon diode can be used above 3.6 V.

Figure 2. GSM Application Circuit Configuration with Drain Switch and MC33169 GaAs Power Amplifier Support IC

TYPICAL CHARACTERISTICS

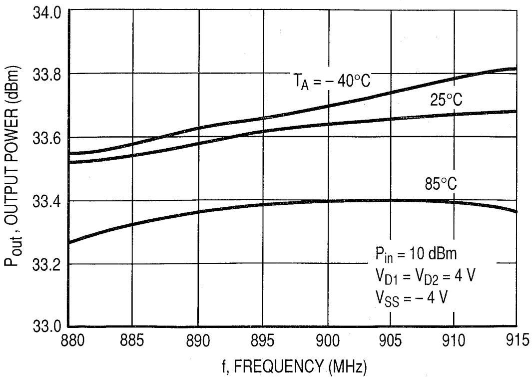


Figure 3. Output Power versus Frequency

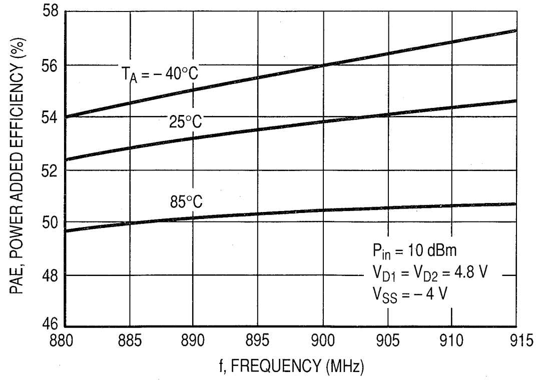


Figure 4. Power Added Efficiency versus Frequency

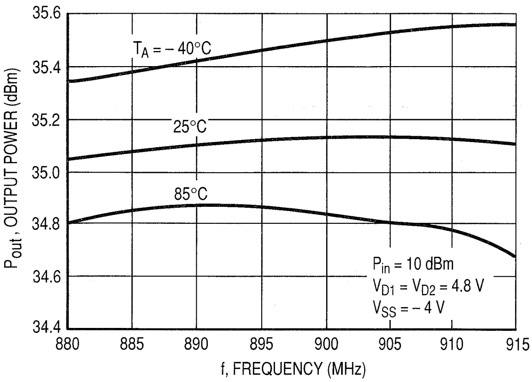


Figure 5. Output Power versus Frequency

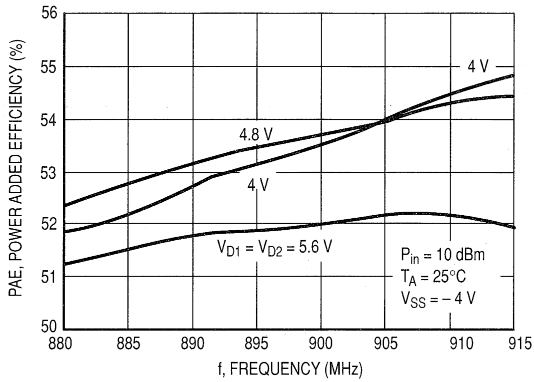


Figure 6. Power Added Efficiency versus Frequency

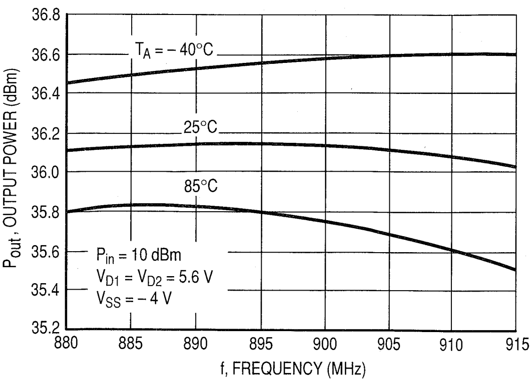


Figure 7. Output Power versus Frequency

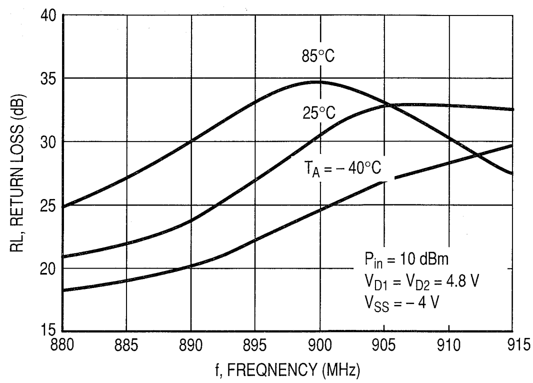


Figure 8. Input Return Loss versus Frequency

TYPICAL CHARACTERISTICS

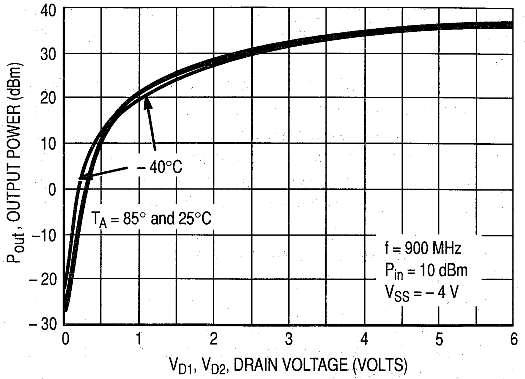


Figure 9. Output Power versus Drain Voltage

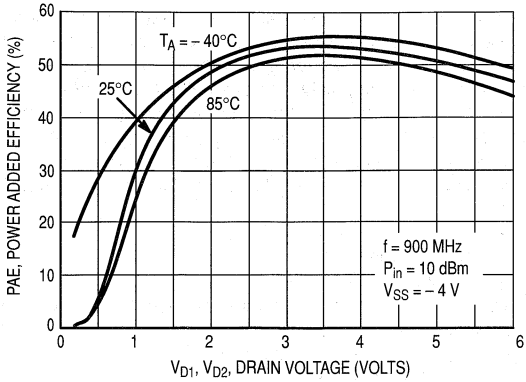


Figure 10. Power Added Efficiency versus Drain Voltage

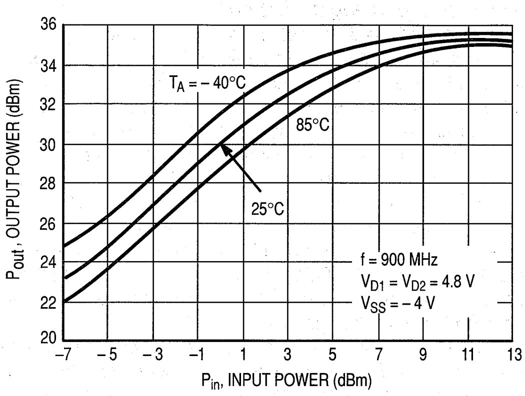


Figure 11. Output Power versus Input Power

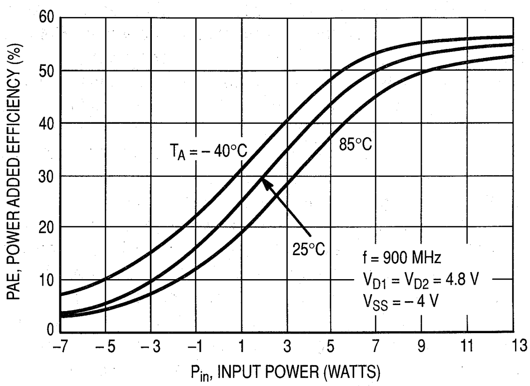


Figure 12. Power Added Efficiency versus Input Power

f	Z_{in} Ohms		Z_{OL}^{*} Ohms	
(MHz)	R	jX	R	jX
880	13.65	–44.05	3.15	5.06
885	13.64	–44.74	3.13	4.97
890	13.65	–45.44	3.10	4.89
895	13.64	–46.14	3.08	4.80
900	13.64	–46.84	3.06	4.71
905	13.65	–47.55	3.04	4.63
910	13.66	–48.27	3.02	4.54
915	13.66	–49.00	3.00	4.45

Table 1. Device Impedances Derived from Circuit Characterization

Design Philosophy

The MRFIC0913 is a two–stage Integrated Power Amplifier designed for use in cellular phones, especially for those used in GSM Class IV, 4.8 V operation. With matching circuit modifications, it is also applicable for use in GSM Class IV 6 V and Class V 3.6 V equipment. Due to the fact that the input, output and some of the interstage matching is accomplished off chip, the device can be tuned to operate anywhere within the 800 to 1000 MHz frequency range. Typical performance at different battery voltages is:

- 36.0 dBm @ 5.8 V
- 35.0 dBm @ 4.8 V
- 31.5 dBm @ 3.6 V

This capability makes the MRFIC0913 suitable for portable cellular applications such as:

- 6 and 4.8 V GSM Class IV
- 3.6 V GSM Class V
- 3.6 V, 1.2 W Analog Cellular

RF Circuit Considerations

The MRFIC0913 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical GSM Class IV applications circuit.

The input match is a shunt–C, series–L, low–pass structure and can be retuned as desired with the only limitation being the on–chip 12 pF blocking capacitor. For saturated applications such as GSM and analog cellular, the input match should be optimized at the rated RF input power.

Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} supply line. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the inductance of the device's wirebonds and leadframe pin.

Output matching is accomplished with a one–stage low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through chip capacitors mounted along a 30 or 50Ω microstrip transmission line. Values and positions are chosen to present a 3Ω loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. When low–Q commercial chip capacitors are used for the shunt capacitors, loss can be reduced by mounting two capacitors in parallel, as shown in Figure 2, to achieve the total value needed.

Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes. The bias supply line which supplies the output should include an RF choke of at least 8 nH, surface mount solenoid inductors or equivalent length of microstrip lines. Discrete inductors will usually give better efficiency and conserve board space.

The DC blocking capacitor required at the output of the device is best mounted at the 50Ω impedance point in the circuit where the RF current is at a minimum and the capacitor loss will have less effect.

Biasing Considerations

Gate bias is supplied to each stage separately through resistive division of the V_{SS} voltage. The top of each divider is brought out through pins 12 and 13 (V_{G2} and V_{G1} respectively) allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of each stage separately.

For applications where the amplifier is operated close to saturation, such as GSM and analog cellular, the gate bias can be set with resistors. Variations in process and temperature will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quiescent currents of 80 to 160 mA for the first stage and 400 to 800 mA for the second stage.

For linear modes of operation which are required for PDC, DAMPS and CDMA, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1.25 mA is required in the divider network so a DAC can be used as the voltage source. Typical settings for 6 V linear operation are 100 mA ±5% for the first stage, and 500 mA ±5% for the second stage.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_D^2. This provides a very linear and repeatable power control transfer function. This technique can be used open–loop to achieve 20–25 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for GSM phase II control where 29 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control.

The transmit waveform ramping function required for systems such as GSM can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for GSM, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power.

For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC0913 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 300 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 μs before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Conclusion

The MRFIC0913 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as GSM where saturated amplifier operation is used.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

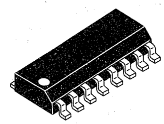
The MRFIC Line
900 MHz LDMOS Integrated Power Amplifier

MRFIC0914

This integrated circuit is intended for two–way paging applications and for other Industrial, Scientific and Medical (ISM) at 900 MHz band applications. The three stage design is implemented in Motorola's low cost, high performance LDMOS process and housed in a low–cost surface mount SOIC package. Input and output matching is implemented off–chip for maximum flexibility while interstage matching is on–chip. A power control pin is included allowing 60 dB dynamic range.

- 30.5 dBm Output Power for 3 dBm Input Power at 900 MHz
- 32 dB Typ Small Signal Gain
- 40% Efficiency Min at 30.5 dBm Output Power
- 4.0 to 5.5 Volt Operation
- Low–Cost, Low Profile Plastic SOIC Package
- Order MRFIC0914R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0914

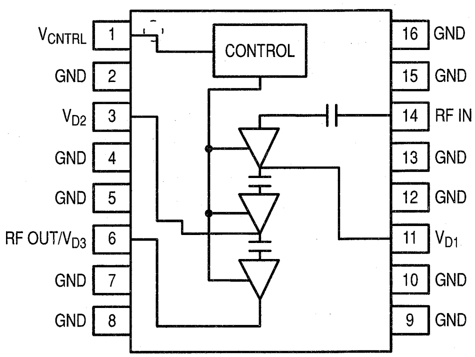
900 MHz PAGING POWER AMPLIFIER Si MONOLITHIC INTEGRATED CIRCUIT



CASE 751B–05 (SOIC–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}, V_{D3}	9	Vdc
Supply Current	I_{Dtotal}	2	Adc
Power Control Voltage	V_{CNTRL}	4.8	Vdc
Input Power	P_{in}	6	dBm
Ambient Operating Temperature	T_A	−30 to +80	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Thermal Resistance, Junction to Case	θ_{JC}	26	°C/W



Pin Connections and Functional Block Diagram

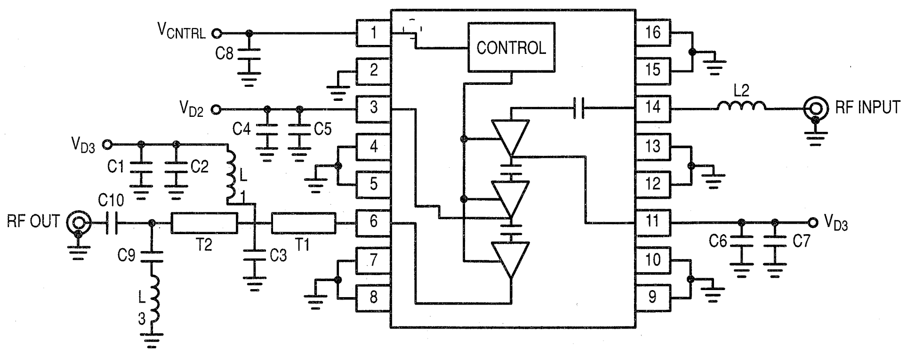
REV 2

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	V_{D1}, V_{D2}, V_{D3}	3.6 to 5.8	Vdc
Power Control Voltage	V_{CNTRL}	0 to 4.8	Vdc
RF Frequency Range	f_{RF}	890 to 928	MHz

ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2}, V_{D3} = 4.8 V, f = 900 MHz, P_{in} = 3 dBm, 1 ms, 10% duty cycle, V_{CNTRL} Adjusted for I_{Dtotal} = 583 mA, T_A = 25°C unless otherwise noted. Measured in Circuit Configuration Shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Output Power	1.12	—	—	W
Efficiency	40	—	—	%
Output Power at 1 dB Gain Compression	—	29	—	dBm
Saturated Output Power	—	31	—	dBm
Output Third Order Intercept Point	—	36	—	dBm
Dynamic Range (V_{CNTRL} = 0 to 4.8 V)	—	60	—	dB
Input Return Loss	7	12	—	dB
Output Power, Low Voltage (V_{D1}, V_{D2}, V_{D3} = 3.84 V)	0.56	—	—	W
Spurious Output (Load VSWR = 20:1, All Phase Angles)	—	–60	–50	dBc
Harmonic Output (With External Matching Circuit)	—	—	–45	dBc



C1, C7 — 0.01 µf
C2, C6, C8 — 33 pF
C3 — 12 pF
C4 — 1.0 µF
C5, C10 — 100 pF
C9 — 2.1 pF
L1 — 33 nH
L2 — 5.6 nH
L3 — 3.3 nH
T1 — 50 Ω MICROSTRIP, 7.5° @ 900 MHz
T2 — 50 Ω MICROSTRIP, 31.6° @ 900 MHz
BOARD MATERIAL — 18 MIL FR4

Figure 1. Application Circuit Configuration

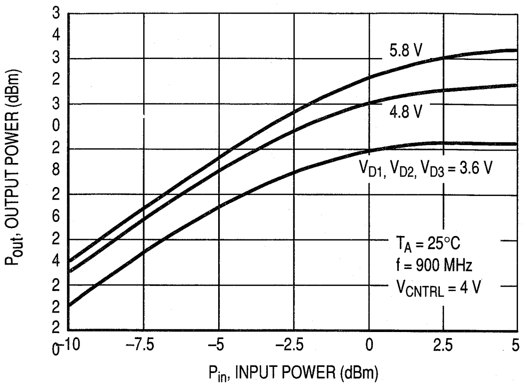


Figure 2. Output Power versus Input Power

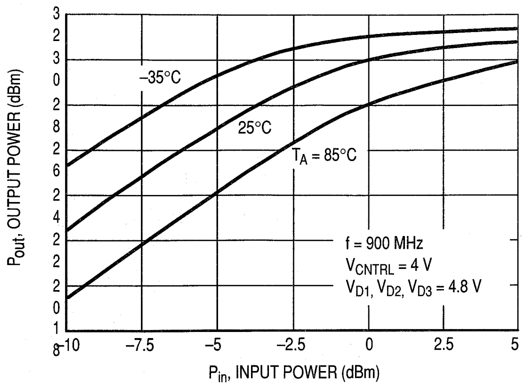


Figure 3. Output Power versus Input Power

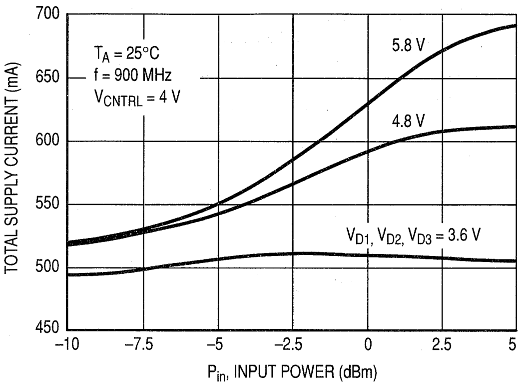


Figure 4. Supply Current versus Input Power

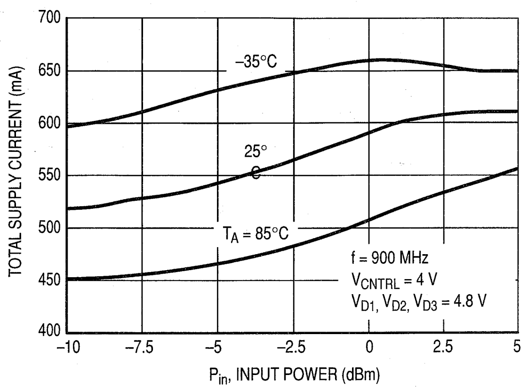


Figure 5. Supply Current versus Input Power

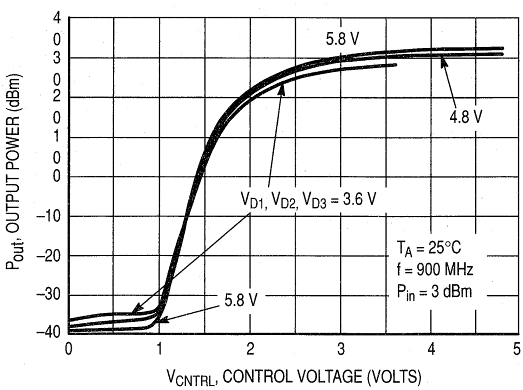


Figure 6. Output Power versus V_{CNTRL}

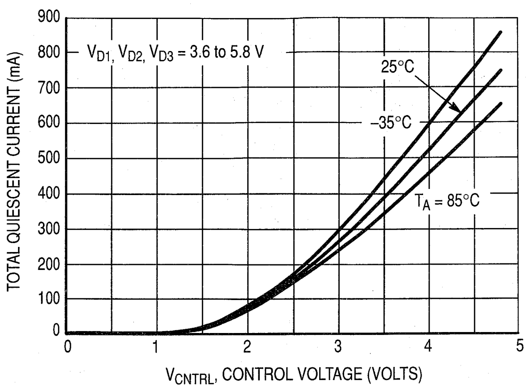


Figure 7. Quiescent Current versus V_{CNTRL}

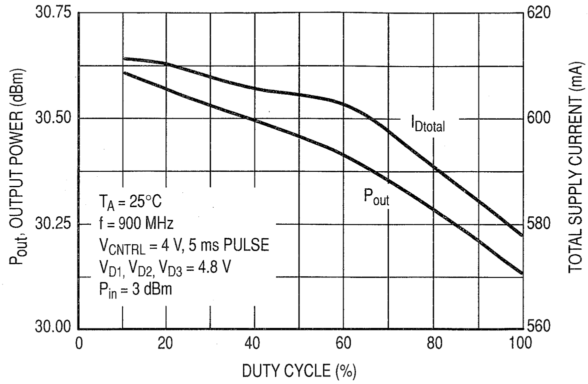


Figure 8. Output Power versus Duty Cycle

f	Z_{in} (Ω)		$Z_{OL}{}^*$ (Ω)	
MHz	R	jX	R	jX
800	48.8	–16.3	2.56	14.3
850	49.0	–17.9	3.30	14.4
900	49.0	–19.6	2.80	13.1
950	49.4	–21.2	3.94	14.0
1000	49.8	–23.1	3.95	12.6

Table 1. Device Impedances Derived from Circuit Characterization

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC0914 three stage LDMOS integrated power amplifier was designed for low cost and flexibility. While the target application was two–way paging, the device can be used in a variety of 800 to 1000 MHz applications and it is particularly suited to burst mode digital transmissions with constant envelope modulation schemes. Only one supply is required. The V_{CNTRL} pin allows the setting of the gate bias of the three stages simultaneoulsy for optimum gain and efficiency and serves as a transmit control with more than 60 dB dynamic range.

CIRCUIT DETAILS

In Figure 1, the 900 MHz applications circuit, note that each stage has a separate supply pin, including the RF Output for the third stage. Care should be taken in bypassing these supply connections to avoid low frequency oscillation. Chip capacitors should be mounted as close to the leads and ground vias as possible. Ground vias should be provided close to the indicated ground leads as well. L1 is a bias choke supplying the third stage and could be replaced with a quarter wave line or air–wound inductor.

RF performance is sensitive to the output matching network. C9 and L3 form a second harmonic trap which enhances efficiency. Placement of C3 along the 50Ω line at the device output is critical to gain and efficiency. L2, the input matching inductor, is optional. Without this inductor, the input match is still typically better than 2:1 VSWR.

It should be note that Figure 1 does not portray the parasitics of the chip components nor their solder mounting pads. The board material is 18 mil dielectric thickness FR4. The impedances shown in Table 1 were derived from circuit characterization and are given as an aid to original designs.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” to the device type. For a complete list of currently available boards and ones in development for newly introduced products, please consult your local Motorola Distributor or Sales Office.

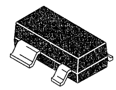
The MRFIC Line
General Purpose RF Cascode Amplifier

MRFIC0916

SILICON GENERAL PURPOSE RF CASCODE AMPLIFIER

The MRFIC0916 is a cost–effective, high isolation cascode silicon monolithic amplifier in the industry standard SOT–143 surface mount package designed for general purpose RF applications. On chip bias circuitry sets the bias point while matching is accomplished off chip affording the maximum in application flexibility.

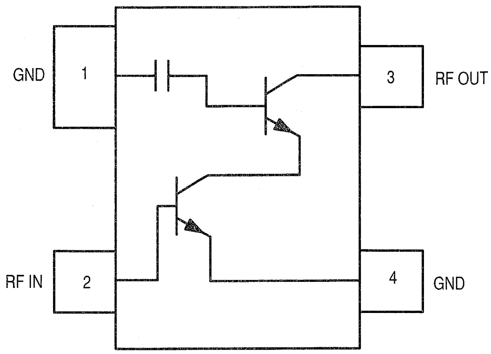
- Usable Frequency Range = 100 to 2500 MHz
- 18.5 dB typical gain at 850 MHz, V_{CC} = 2.7 Volts
- 2.3 dBm typical Output Power at 1 dB Gain Compression at 850 MHz, V_{CC} = 2.7 Volts
- 44 dB Typical Reverse Isolation at 850 MHz
- 5.6 mA Max Bias Current at V_{CC} = 2.7 Volts
- 2.7 to 5 Volt Supply
- Available in Tape and Reel by Adding T1 Suffix to Part Number. T1 Suffix = 3,000 Units per 8 mm, 7 inch Reel.
- Device Marking = 16



CASE 318A–05 (SOT–143)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Limit	Unit
Supply Voltage	V_{CC}	6	Vdc
RF Input Power	P_{RF}	10	dBm
Power Dissipation	P_{DIS}	100	mW
Supply Current	I_{CC}	20	mA
Thermal Resistance, Junction to Case	$R_{\theta JC}$	250	°C/W
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Case Temperature	T_C	– 35 to +100	°C



Pin Connections and Functional Block Diagram

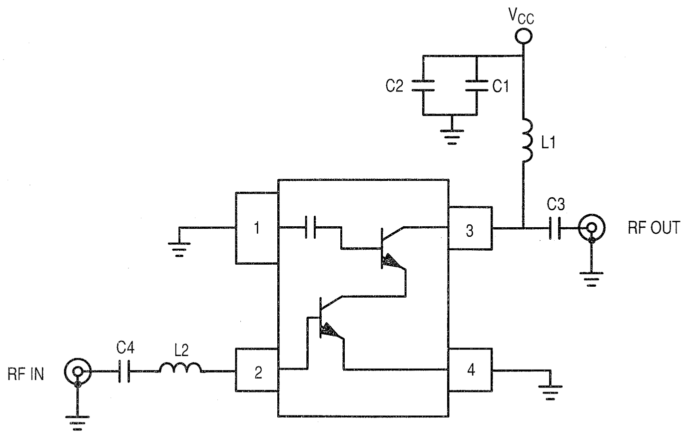
REV 1

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	100 to 2500	MHz
Supply Voltage	V_{CC}	2.7 to 5	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V, T_A = 25°C, f_{RF} = 850 MHz, Tested in Circuit Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain	16.5	18.5	20.5	dB
Noise Figure	—	1.9	—	dB
Power Output at 1dB Gain Compression	0	2.3	—	dBm
Output 3rd Order Intercept Point	—	11	—	dBm
Reverse Isolation	—	44	—	dB
Supply Current	3.8	4.7	5.6	mA



C1 – 100 pF
C2 – 0.01 µF
C3 – 1.4 pF
C4 – 100 pF
L1 – 8.2 nH
L2 – 6.8 nH

Figure 1. 850 MHz Applications Circuit Configuration

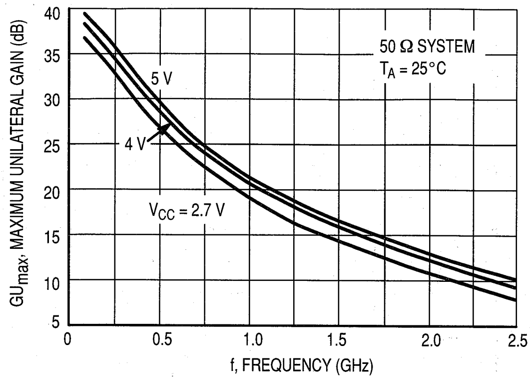


Figure 2. GU_{max} versus Frequency

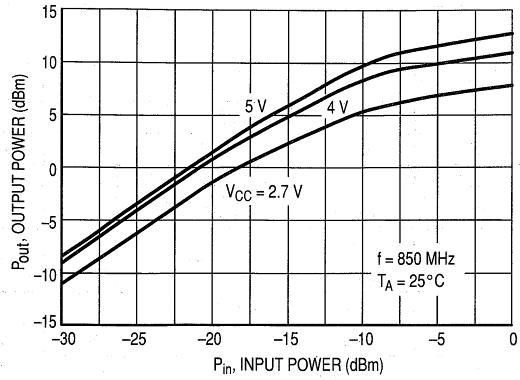


Figure 3. Output Power versus Input Power

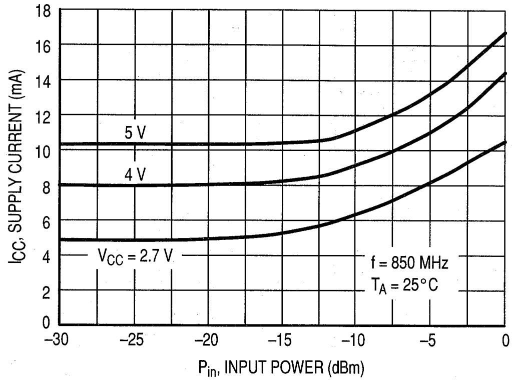


Figure 4. Supply Current versus Input Power

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\lvert S_{11} \rvert$	$\angle \phi$	$\lvert S_{21} \rvert$	$\angle \phi$	$\lvert S_{12} \rvert$	$\angle \phi$	$\lvert S_{22} \rvert$	$\angle \phi$
100	0.806	–17.01	12.03	162.32	0.001	–0.14	0.956	–4.69
200	0.765	–33.28	11.18	145.74	0.001	71.58	0.948	–8.69
300	0.713	–47.99	10.18	130.99	0.002	69.67	0.945	–13.23
400	0.652	–61.35	9.06	118.01	0.003	64.61	0.930	–17.35
500	0.574	–70.94	8.06	106.50	0.003	62.93	0.904	–20.85
600	0.533	–81.00	7.09	96.50	0.003	61.94	0.891	–24.71
700	0.493	–89.33	6.36	87.60	0.003	63.16	0.875	–28.18
800	0.469	–97.65	5.62	79.57	0.003	66.33	0.857	–31.89
900	0.432	–103.64	5.16	72.38	0.002	80.79	0.845	–35.21
1000	0.409	–110.68	4.70	65.39	0.002	100.33	0.831	–38.86
1100	0.396	–116.17	4.29	58.75	0.002	127.72	0.815	–42.52
1200	0.383	–122.20	3.91	52.55	0.003	152.57	0.799	–45.77
1300	0.373	–126.00	3.66	46.34	0.004	164.39	0.789	–49.49
1400	0.369	–131.29	3.38	40.61	0.006	169.63	0.776	–53.23
1500	0.366	–134.46	3.14	35.29	0.008	172.81	0.762	–56.86
1600	0.366	–140.07	2.93	29.63	0.011	172.47	0.751	–60.74
1700	0.364	–143.07	2.75	23.86	0.013	172.79	0.738	–64.66
1800	0.368	–147.48	2.58	18.42	0.016	171.54	0.727	–68.29
1900	0.377	–148.91	2.42	13.15	0.020	170.15	0.719	–72.29
2000	0.381	–153.42	2.27	7.58	0.023	167.89	0.707	–76.58
2100	0.394	–155.23	2.15	2.46	0.027	165.86	0.695	–80.50
2200	0.396	–158.91	2.03	–3.00	0.032	163.46	0.685	–84.85
2300	0.416	–160.43	1.90	–8.32	0.037	161.00	0.672	–88.93
2400	0.424	–162.98	1.81	–13.30	0.042	158.00	0.662	–93.38
2500	0.434	–166.35	1.68	–18.45	0.047	155.58	0.654	–97.89

Table 1. Scattering Parameters (V_{CC} = 2.7 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle \phi$	$\|S_{21}\|$	$\angle \phi$	$\|S_{12}\|$	$\angle \phi$	$\|S_{22}\|$	$\angle \phi$
100	0.744	–17.43	16.979	160.38	0.001	–2.89	0.955	–4.40
200	0.691	–33.58	15.442	142.46	0.001	83.36	0.950	–8.33
300	0.627	–47.53	13.633	127.28	0.002	76.39	0.946	–12.79
400	0.558	–59.50	11.851	114.52	0.002	70.12	0.931	–16.75
500	0.482	–67.02	10.284	103.51	0.002	67.02	0.907	–20.11
600	0.440	–75.50	8.957	94.12	0.002	66.00	0.895	–23.85
700	0.401	–81.87	7.930	85.95	0.002	68.71	0.880	–27.22
800	0.377	–88.89	7.003	78.57	0.002	73.50	0.863	–30.83
900	0.348	–93.11	6.348	71.96	0.002	90.55	0.852	–34.06
1000	0.328	–98.88	5.747	65.59	0.002	113.74	0.838	–37.62
1100	0.317	–103.27	5.223	59.57	0.002	146.45	0.822	–41.18
1200	0.306	–108.54	4.765	53.98	0.003	165.49	0.808	–44.34
1300	0.301	–111.30	4.425	48.39	0.004	175.51	0.798	–47.95
1400	0.297	–116.30	4.082	43.18	0.006	177.46	0.785	–51.59
1500	0.298	–118.89	3.790	38.32	0.008	179.45	0.771	–55.11
1600	0.298	–124.58	3.531	33.13	0.011	178.69	0.760	–58.88
1700	0.301	–127.19	3.300	28.02	0.014	178.02	0.748	–62.66
1800	0.305	–131.73	3.093	23.10	0.016	176.25	0.737	–66.16
1900	0.319	–133.16	2.901	18.34	0.020	174.44	0.729	–70.03
2000	0.324	–137.94	2.724	13.33	0.023	172.03	0.717	–74.16
2100	0.339	–140.09	2.575	8.67	0.027	169.82	0.706	–77.92
2200	0.342	–143.98	2.434	3.79	0.032	166.99	0.696	–82.07
2300	0.367	–146.00	2.278	–0.98	0.036	164.37	0.684	–86.04
2400	0.375	–148.75	2.166	–5.56	0.042	161.35	0.674	–90.25
2500	0.387	–152.75	2.020	–10.12	0.046	158.69	0.666	–94.64

Table 2. Scattering Parameters (V_{CC} = 4 V, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\lvert S_{11} \rvert$	$\angle \phi$	$\lvert S_{21} \rvert$	$\angle \phi$	$\lvert S_{12} \rvert$	$\angle \phi$	$\lvert S_{22} \rvert$	$\angle \phi$
100	0.707	–17.56	20.04	159.03	0.001	–7.95	0.954	–4.25
200	0.648	–33.40	17.93	140.29	0.001	86.24	0.950	–8.15
300	0.579	–46.60	15.53	124.94	0.002	78.79	0.946	–12.54
400	0.509	–57.44	13.31	112.38	0.002	72.27	0.931	–16.42
500	0.438	–63.51	11.40	101.70	0.002	69.34	0.908	–19.68
600	0.397	–70.90	9.87	92.70	0.002	69.55	0.896	–23.35
700	0.363	–76.05	8.69	84.92	0.002	71.59	0.882	–26.64
800	0.340	–82.18	7.67	77.89	0.002	79.44	0.865	–30.20
900	0.316	–85.44	6.91	71.60	0.002	95.59	0.855	–33.36
1000	0.298	–90.52	6.24	65.56	0.001	121.55	0.841	–36.86
1100	0.290	–94.44	5.67	59.82	0.002	152.13	0.826	–40.37
1200	0.280	–99.17	5.17	54.53	0.003	169.84	0.811	–43.48
1300	0.277	–101.65	4.79	49.25	0.005	177.80	0.802	–47.02
1400	0.274	–106.49	4.42	44.27	0.006	–179.84	0.790	–50.59
1500	0.278	–109.07	4.10	39.65	0.008	–179.19	0.776	–54.04
1600	0.276	–114.88	3.82	34.68	0.011	–179.68	0.765	–57.73
1700	0.281	–117.46	3.56	29.88	0.013	179.47	0.753	–61.43
1800	0.285	–122.11	3.34	25.21	0.016	177.73	0.742	–64.85
1900	0.300	–123.94	3.14	20.70	0.019	175.80	0.734	–68.66
2000	0.305	–128.93	2.95	15.91	0.023	173.47	0.723	–72.71
2100	0.322	–131.48	2.78	11.50	0.027	171.04	0.712	–76.37
2200	0.324	–135.50	2.63	6.84	0.031	168.25	0.703	–80.42
2300	0.351	–138.04	2.47	2.33	0.036	165.47	0.691	–84.31
2400	0.358	–140.88	2.34	–2.05	0.041	162.71	0.681	–88.42
2500	0.371	–145.28	2.19	–6.40	0.046	160.19	0.674	–92.74

Table 3. Scattering Parameters (V_{CC} = 5 V, 50 Ω System)

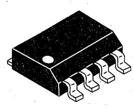
Advance Information

The MRFIC Line

Balanced Transmit Mixer

MRFIC0931

BALANCED TRANSMIT MIXER SILICON MONOLITHIC INTEGRATED CIRCUIT



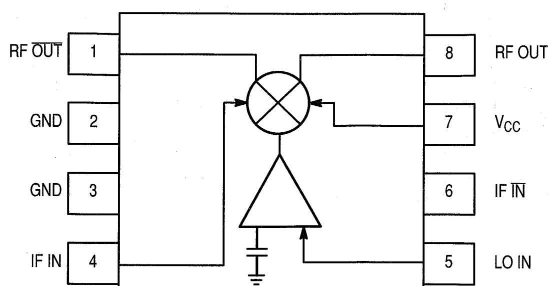
CASE 751-05 (SO-8)

The MRFIC0931 is a balanced Gilbert cell mixer with LO buffer amplifier intended for transmit upmixer application. The device is usable for Industrial, Scientific and Medical (ISM), Cellular and PCS applications and is packaged in a low–cost surface mount package.

- Usable 500–2000 MHz
- High Output Power @ 1 dB Gain Compression, 3.6 Volts
  0.9 dBm (Typ) @ 900 MHz
  –2 dBm (Typ) @ 1800 MHz
- 2.7–4.8 Volts Operation
- Balanced Design for Good LO Rejection
- 47 mA (Max) Current @ 4.5 Volts
  45 mA (Max) Current @ 3.6 Volts
- Low Cost Surface Mount Package
- Order MRFIC0931R2 for Tape and Reel.
  R2 suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M0931

ABSOLUTE MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	5	Vdc
Input Power, IF and LO	P_{IF}, P_{LO}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C



Pin Connections and Functional Block Diagram

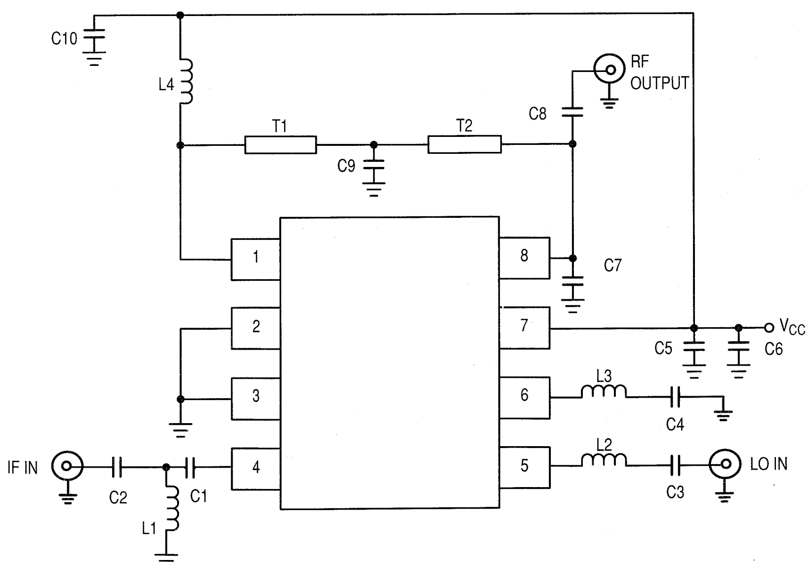
REV 1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltages	V_{CC}	2.7 to 4.5	Vdc
RF Frequency Range	f_{RF}	500 to 2000	MHz
IF Frequency Range	f_{IF}	0 to 250	MHz

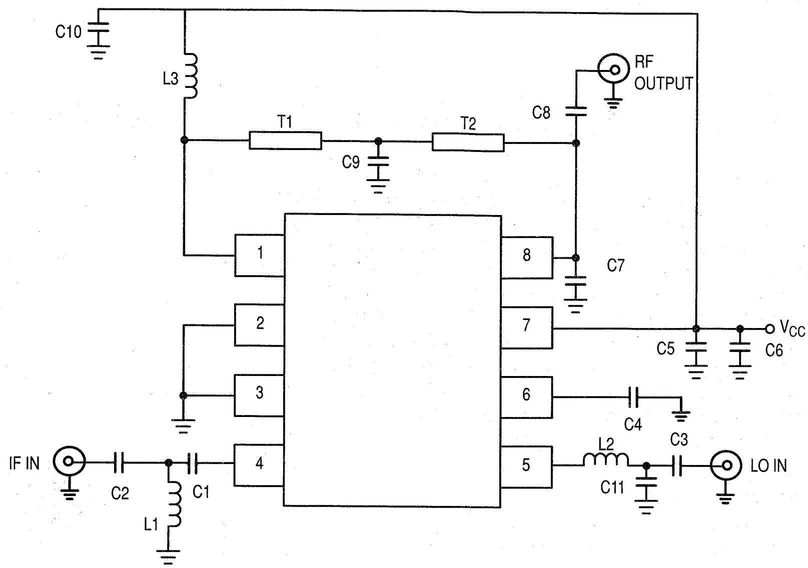
ELECTRICAL CHARACTERISTICS (T_A = 25°C, measured in circuit shown in Figure 1 or 2 as frequency indicates)

Parameter	Min	Typ	Max	Unit
RF Output Power (f_{IF} = 88 MHz, f_{LO} = 815 MHz, P_{LO} = –10 dBm, P_{IF} = –20 dBm, V_{CC} = 4.5 V)	2	4	8	dBm
LO Feed Through (f_{IF} = 88 MHz, f_{LO} = 815 MHz, P_{LO} = –10 dBm, P_{IF} = –20 dBm, V_{CC} = 4.5 V)	—	—	–16	dBc
Undesired Sideband Output (f_{IF} = 88 MHz, f_{LO} = 815 MHz, P_{LO} = –10 dBm, P_{IF} = –20 dBm, V_{CC} = 4.5 V)	—	—	– 25	dBc
Small Sigal Conversion Gain (f_{IF} = 100 MHz, P_{IF} = –25 dBm, V_{CC} = 3.6 V)				
900 MHz (P_{LO} = –10 dBm)	—	25	—	dB
1800 MHz (P_{LO} = –5 dBm)	—	20	—	dB
Power Output at 1 dB Gain Compression (f_{IF} = 100 MHz, P_{IF} = –25 dBm, V_{CC} = 3.6 V)				
900 MHz (P_{LO} = –10 dBm)	—	0.9	—	dBm
1800 MHz (P_{LO} = –5 dBm)	—	–2	—	dBm
Supply Current				
V_{CC} = 4.5 V	—	38	47	mA
V_{CC} = 3.6 V	—	30	45	mA



C1, C4, C6, C10	1000 pF	L1, L3	220 nH
C2	13 pF	L2	3.3 nH
C3, C9	10 pF	L4	12 nH
C5	100 pF	T1, T2	1/8 λ 50 Ω Microstrip
C7	2.4 pF	Board Material	Epoxy/Glass ε_r = 4.45
C8	2 pF		

Figure 1. 903 MHz Configuration Test Circuit



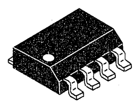
C1, C6, C10	1000 pF
C2	10 pF
C3, C4, C5, C8	100 pF
C7	1.2 pF
C9	2.7 pF
C11	1 pF
L1,	180 nH
L2	3.3 nH
L3	2.7 nH
T1, T2	1/8 λ 50 Ω Microstrip
Board Material	Epoxy/Glass $\varepsilon_r = 4.45$

Figure 2. 1800 MHz Applications Circuit

The MRFIC Line
GPS GaAs Low Noise Amplifier

MRFIC1501

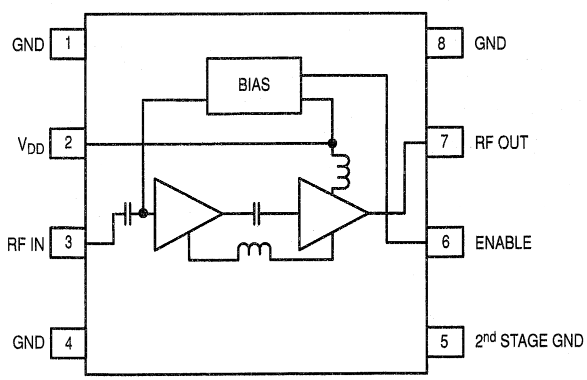
**1.6 GHz GaAs
LOW NOISE
AMPLIFIER**



**CASE 751–05
(SO-8)**

The MRFIC1501 is a low cost yet high performance two–stage, low–noise amplifier designed primarily for use in Global Positioning Satellite System (GPS) and other L–band satellite receivers. The broadband nature of the design makes the device applicable to a variety of L–band applications where high performance at reasonable current and cost are required. Supply current is minimized through a current sharing DC cascode circuit configuration. Supply voltage can be applied to either the V_{DD} pin or the RF output pin for remote antenna applications. The integrated circuit requires minimal off-chip matching while allowing for maximum flexibility in optimizing gain and noise figure. An ENABLE pin is provided to allow for a reduced supply current standby mode. The design employs Motorola's low cost planar self–aligned MESFET process to assure repeatable characteristics at minimal cost.

- Usable Frequency Range = 1 to 2 GHz
- 18 dB Typ Gain at V_{DD} = 5 Volts
- 1.1 dB Typ Noise Figure at V_{DD} = 5 Volts
- Simple Off-chip Matching for Maximum Gain/Noise Figure Flexibility
- Single Bias Supply = 3 to 5 Volts
- Low Power Consumption = 30 mW (Typ) at 5 Volts
- Low Cost Surface Mount Plastic Package
- Order MRFIC1501R2 for Tape and Reel Option.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M1501



Pin Connections and Functional Block Diagram

REV 1

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

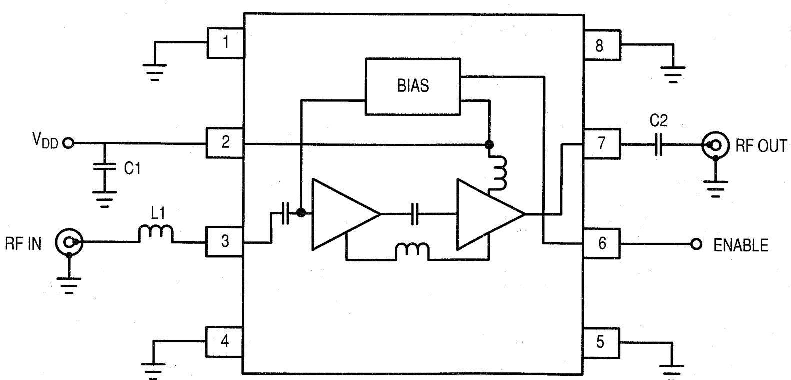
Ratings	Symbol	Limit	Unit
Supply Voltage	V_{DD}	6	Vdc
RF Input Power	P_{RF}	3	dBm
ENABLE Voltage	ENABLE	6	Vdc
V_{DD} Current Sourcing (With Supply Connected to Pin 7)	I_{PIN2}	20	mA
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +100	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	1 to 2	GHz
ENABLE “ON” (Device Operational) Voltage	ENABLE	V_{DD} ± 0.5	Vdc
ENABLE “OFF” (Device in Standby Mode) Voltage	ENABLE	0 to 0.5	Vdc
Supply Voltage	V_{DD}	3 to 5	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, RF = 1.575 GHz, ENABLE = 5 V, Circuit Configuration Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
RF Gain	17	18	—	dB
SSB Noise Figure	—	1.1	—	dB
RF Output 3rd Order Intercept Point	—	10	—	dBm
Output 1 dB Gain Compression	—	0	—	dBm
Reverse Isolation (s_{12})	—	30	—	dB
Input Return Loss	—	10	—	dB
Output Return Loss	—	10	—	dB
Supply Current	—	5.9	7.5	mA



C1, C2 – 22 pF
L1 – 11 nH (Implemented in Microstrip)

Figure 1. Applications Circuit Configuration

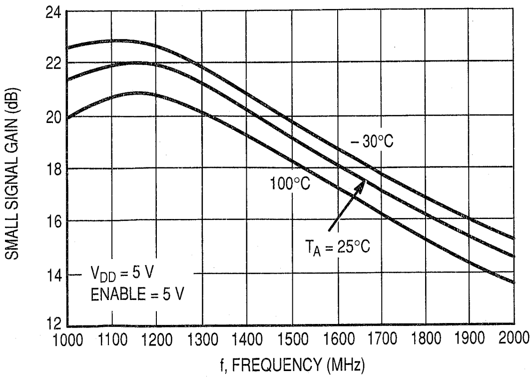


Figure 2. Small Signal Gain versus Frequency

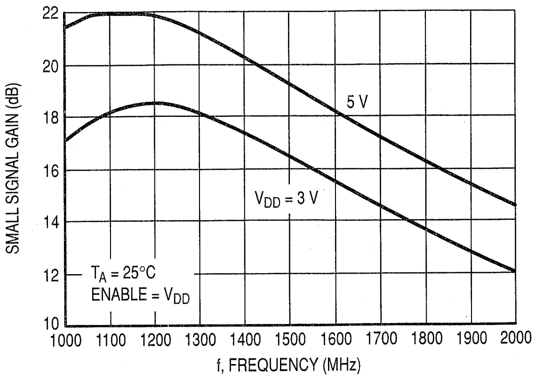


Figure 3. Small Signal Gain versus Frequency

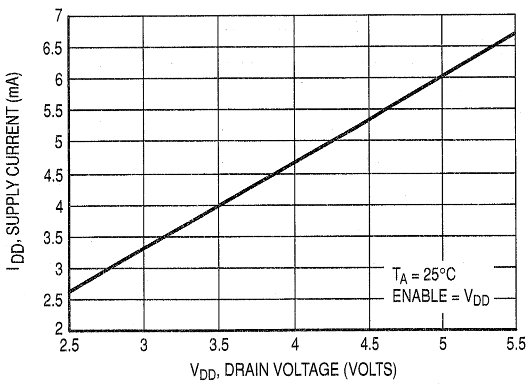


Figure 4. Drain Current versus Drain Voltage

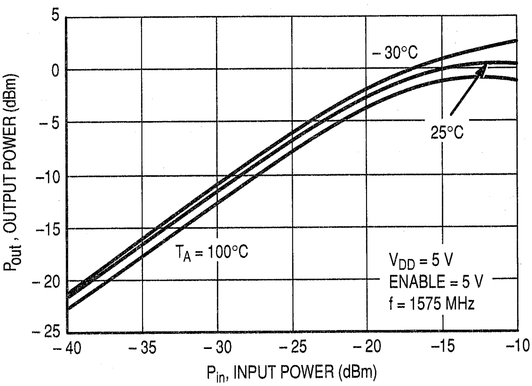


Figure 5. Output Power versus Input Power

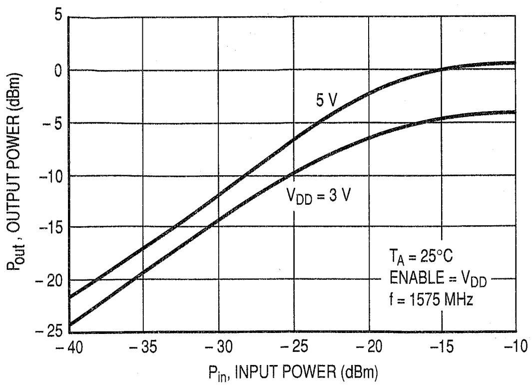


Figure 6. Output Power versus Input Power

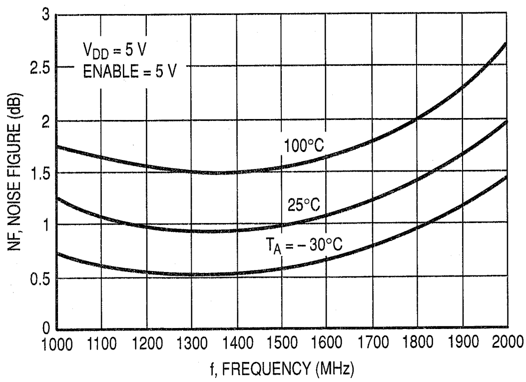


Figure 7. Noise Figure versus Frequency

TYPICAL CHARACTERISTICS

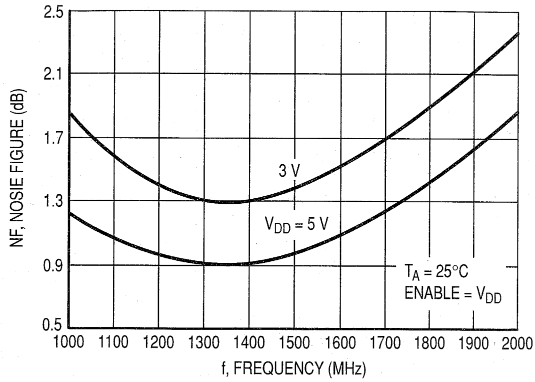


Figure 8. Noise Figure versus Frequency

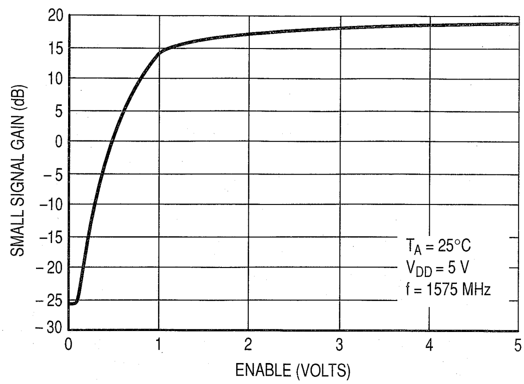


Figure 9. Gain versus ENABLE Voltage

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The circuit configuration employs a DC cascode arrangement which allows current sharing between two FETs. This gives excellent noise figure at reduced supply current. Since GPS applications often require the downconverter to be remotely mounted at the antenna, the output is DC coupled so that the drain voltage can be supplied through the coax feed. The V_{DD} pin can actually supply other components in the equipment at less than 20 mA of current. On–chip bias circuitry tracks changes in device threshold voltage and temperature and is externally controlled through the ENABLE pin. This feature allows for a low current standby mode or for gain reduction. Refer to Figure 9 for control characteristics.

CIRCUIT CONSIDERATIONS

As shown in Figure 1, impedance matching of the MRFIC1501 is quite simple. Through use of an on–chip source inductor in the first stage, Γ_{opt} and and Γ_{in}^* are approximately equal. A single inductor at the input will give good input match and noise figure. This inductor can be implemented with a high impedance microstrip line or a chip inductor.

As with all RF active circuit designs, bypassing the supply pin is recommended. Layout and ground via location is important. Vias should be located as close as possible to ground pins and the ground side of off–chip components.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” to the device type. For a complete list of currently available boards and ones in development for newly introduced products, please consult your local Motorola Distributor or Sales Office.

Table 1. Scattering Parameters (V_{DD} = 3 Volts, ENABLE = 3 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
795	0.958	–28.07	3.218	28.76	0.011	179.98	0.358	21.08
825	0.959	–29.71	3.448	23.95	0.011	176.45	0.336	15.36
855	0.954	–31.16	3.534	18.42	0.012	172.43	0.311	9.65
870	0.951	–32.04	3.535	16.03	0.011	171.06	0.297	6.67
900	0.945	–33.63	3.502	11.26	0.012	166.26	0.273	1.19
930	0.935	–35.48	3.528	6.47	0.013	166.48	0.250	–5.16
960	0.932	–37.28	3.689	2.07	0.014	164.19	0.227	–11.04
990	0.921	–39.03	3.867	–2.41	0.016	163.33	0.203	–18.26
1020	0.912	–40.69	3.954	–7.56	0.018	160.39	0.181	–25.17
1050	0.901	–42.28	3.975	–12.01	0.019	158.58	0.158	–33.18
1080	0.892	–44.16	4.039	–16.73	0.020	154.26	0.138	–40.98
1110	0.879	–46.05	4.154	–21.72	0.021	151.91	0.119	–49.98
1140	0.865	–47.91	4.296	–27.64	0.022	147.91	0.101	–58.85
1170	0.846	–49.35	4.320	–32.73	0.022	147.32	0.086	–71.10
1200	0.825	–51.34	4.224	–36.64	0.022	147.46	0.077	–87.14
1230	0.800	–51.92	4.125	–40.14	0.026	152.91	0.070	–118.39
1260	0.798	–52.57	4.224	–42.75	0.029	141.81	0.053	–155.35
1290	0.782	–53.50	4.371	–47.81	0.030	135.50	0.051	169.35
1320	0.775	–55.70	4.554	–53.11	0.031	132.76	0.049	140.94
1350	0.758	–57.05	4.525	–57.58	0.030	128.85	0.052	126.02
1380	0.742	–58.70	4.501	–61.64	0.031	125.89	0.061	114.60
1410	0.721	–60.03	4.511	–66.70	0.030	123.70	0.073	105.25
1440	0.703	–60.76	4.538	–71.38	0.031	121.40	0.083	97.32
1470	0.686	–61.48	4.553	–75.65	0.030	119.75	0.095	89.55
1500	0.668	–62.72	4.497	–79.44	0.031	116.74	0.107	82.70
1530	0.652	–63.71	4.436	–83.00	0.031	115.52	0.119	77.82
1560	0.633	–63.91	4.437	–87.36	0.030	115.29	0.132	72.37
1575	0.629	–64.01	4.458	–89.76	0.030	114.23	0.139	69.33
1590	0.621	–63.94	4.474	–91.54	0.030	112.50	0.147	66.71
1620	0.604	–64.46	4.477	–95.21	0.031	112.56	0.159	62.76
1650	0.586	–63.98	4.425	–98.51	0.030	111.63	0.172	58.00
1680	0.576	–64.45	4.330	–102.11	0.031	108.93	0.185	54.00
1710	0.559	–64.36	4.264	–105.61	0.030	106.34	0.198	50.85
1740	0.549	–64.02	4.227	–108.90	0.030	106.33	0.208	47.46
1770	0.538	–63.89	4.219	–112.08	0.030	106.56	0.222	43.54
1800	0.527	–63.69	4.172	–114.95	0.029	104.83	0.233	40.56
1830	0.523	–63.58	4.046	–118.53	0.030	104.72	0.244	37.76
1860	0.511	–62.83	3.965	–121.26	0.028	102.55	0.256	34.88
1890	0.503	–62.92	3.925	–124.29	0.029	103.12	0.266	32.47
1920	0.495	–62.26	3.917	–126.71	0.029	102.20	0.275	29.95
1950	0.485	–60.97	3.843	–129.24	0.029	102.70	0.283	27.89
1980	0.479	–60.47	3.759	–132.13	0.029	101.50	0.290	25.95
2010	0.474	–59.93	3.631	–135.13	0.027	98.87	0.300	24.27

Table 2. Scattering Parameters (V_{DD} = 4 Volts, ENABLE = 4 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
900	0.927	–34.45	4.901	4.43	0.011	167.24	0.210	–4.75
930	0.915	–36.30	4.962	–0.21	0.012	166.66	0.185	–12.35
960	0.908	–38.22	5.164	–4.86	0.013	165.06	0.160	–20.80
990	0.895	–39.78	5.383	–9.68	0.015	161.65	0.135	–30.56
1020	0.883	–41.42	5.485	–14.72	0.016	158.86	0.112	–42.22
1050	0.869	–43.05	5.514	–19.31	0.017	158.43	0.092	–55.71
1080	0.858	–44.69	5.573	–24.34	0.018	155.12	0.078	–73.31
1110	0.840	–46.48	5.695	–29.10	0.019	151.63	0.068	–94.03
1140	0.822	–48.23	5.813	–35.10	0.020	149.83	0.063	–115.86
1170	0.804	–49.58	5.817	–40.03	0.020	149.25	0.066	–136.79
1200	0.783	–51.19	5.741	–43.83	0.020	149.99	0.077	–153.70
1230	0.750	–51.37	5.625	–47.36	0.023	155.59	0.102	–172.32
1260	0.753	–51.39	5.762	–49.92	0.026	144.73	0.114	165.51
1290	0.747	–52.29	5.894	–55.24	0.028	137.19	0.122	150.89
1320	0.741	–54.09	6.078	–60.53	0.028	134.63	0.123	139.00
1350	0.727	–55.80	5.998	–65.01	0.028	131.72	0.129	131.12
1380	0.709	–57.17	5.957	–68.70	0.028	128.11	0.137	124.50
1410	0.692	–58.13	5.921	–73.18	0.027	126.13	0.144	117.65
1440	0.676	–59.05	5.928	–77.75	0.027	126.40	0.153	111.32
1470	0.661	–59.68	5.909	–81.80	0.028	122.94	0.162	105.05
1500	0.641	–60.62	5.821	–85.30	0.027	122.00	0.169	98.79
1530	0.628	–61.62	5.715	–88.81	0.028	119.28	0.179	93.52
1560	0.613	–61.52	5.686	–93.11	0.028	119.11	0.190	87.97
1575	0.606	–61.90	5.667	–95.29	0.028	119.48	0.196	85.31
1590	0.599	–61.76	5.667	–97.03	0.029	117.97	0.201	82.57
1620	0.587	–62.04	5.635	–100.45	0.028	117.17	0.209	78.01
1650	0.570	–61.74	5.550	–103.32	0.027	117.04	0.222	73.51
1680	0.560	–62.07	5.423	–106.67	0.028	114.76	0.233	69.07
1710	0.543	–62.20	5.318	–110.16	0.028	112.28	0.243	65.48
1740	0.534	–61.92	5.250	–113.26	0.028	113.29	0.253	61.42
1770	0.527	–61.70	5.212	–116.15	0.028	112.91	0.264	58.10
1800	0.516	–61.84	5.146	–118.66	0.029	113.11	0.274	54.22
1830	0.511	–61.24	4.991	–121.89	0.027	112.07	0.285	50.97
1860	0.501	–60.19	4.848	–124.80	0.027	111.64	0.295	47.95
1890	0.491	–60.35	4.783	–127.80	0.027	110.45	0.304	45.16
1920	0.484	–59.86	4.747	–130.12	0.028	109.45	0.315	42.60
1950	0.474	–58.58	4.697	–132.44	0.028	109.35	0.323	40.11
1980	0.471	–58.40	4.605	–134.97	0.028	111.10	0.329	38.15
2010	0.462	–57.51	4.407	–138.30	0.026	108.25	0.339	35.69

Table 3. Scattering Parameters (V_{DD} = 5 Volts, ENABLE = 5 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\lvert S_{11}\rvert$	∠ φ	$\lvert S_{21}\rvert$	∠ φ	$\lvert S_{12}\rvert$	∠ φ	$\lvert S_{22}\rvert$	∠ φ
900	0.909	–35.17	6.271	–1.16	0.011	168.82	0.163	–11.03
930	0.892	–37.01	6.337	–6.08	0.011	165.10	0.137	–21.39
960	0.882	–38.73	6.583	–10.74	0.012	163.68	0.109	–33.61
990	0.869	–40.38	6.808	–15.88	0.014	161.24	0.088	–49.68
1020	0.855	–41.71	6.927	–21.01	0.015	160.19	0.072	–71.47
1050	0.840	–43.22	6.925	–25.76	0.016	157.93	0.065	–98.66
1080	0.828	–44.84	6.996	–30.74	0.017	156.01	0.067	–124.50
1110	0.807	–46.50	7.081	–35.59	0.018	152.69	0.076	–144.89
1140	0.791	–47.98	7.172	–41.40	0.019	151.04	0.088	–161.86
1170	0.769	–49.03	7.150	–45.93	0.019	150.32	0.103	–174.42
1200	0.745	–50.40	7.082	–49.82	0.018	149.54	0.120	178.54
1230	0.716	–49.79	6.940	–53.44	0.021	156.21	0.149	168.88
1260	0.726	–49.58	7.070	–56.18	0.024	146.99	0.165	154.85
1290	0.724	–50.16	7.183	–61.43	0.025	140.13	0.175	144.80
1320	0.721	–52.48	7.285	–66.39	0.027	136.54	0.177	136.23
1350	0.707	–54.20	7.176	–70.78	0.025	133.27	0.183	130.59
1380	0.690	–55.55	7.102	–74.39	0.026	131.27	0.191	124.77
1410	0.675	–56.53	7.006	–78.73	0.026	129.73	0.198	119.51
1440	0.660	–57.13	6.962	–82.74	0.026	127.44	0.204	113.76
1470	0.646	–57.73	6.936	–86.50	0.026	126.66	0.212	108.23
1500	0.629	–58.40	6.822	–89.92	0.026	124.54	0.219	102.92
1530	0.618	–59.69	6.687	–93.31	0.026	122.48	0.227	98.15
1560	0.601	–59.69	6.606	–97.38	0.026	121.63	0.235	93.28
1575	0.594	–59.80	6.573	–99.55	0.027	122.68	0.243	90.64
1590	0.592	–59.78	6.548	–101.29	0.027	122.13	0.246	88.16
1620	0.577	–60.13	6.477	–104.22	0.027	120.48	0.254	84.10
1650	0.562	–59.69	6.366	–106.82	0.027	119.01	0.263	79.24
1680	0.552	–60.13	6.218	–110.11	0.027	118.15	0.272	75.16
1710	0.543	–60.34	6.094	–113.45	0.026	117.67	0.282	71.64
1740	0.529	–59.65	6.000	–116.40	0.027	118.05	0.291	67.99
1770	0.523	–59.54	5.945	–119.10	0.026	116.25	0.301	64.28
1800	0.515	–59.87	5.845	–121.60	0.027	117.55	0.311	60.73
1830	0.507	–59.61	5.676	–124.69	0.027	116.91	0.320	57.22
1860	0.497	–58.77	5.488	–127.65	0.027	115.88	0.330	54.18
1890	0.491	–58.79	5.414	–130.43	0.027	114.66	0.339	51.39
1920	0.478	–58.39	5.376	–132.53	0.028	117.05	0.348	48.34
1950	0.472	–57.29	5.324	–134.66	0.029	114.84	0.356	45.85
1980	0.466	–56.94	5.193	–137.20	0.028	114.82	0.363	43.87
2010	0.461	–56.18	4.972	–140.40	0.027	114.81	0.372	41.56

Table 4. Noise Parameters (V_{DD} = 5 Volts, ENABLE = 5 Volts, 50 Ω System)

f (MHz)	NF_{min} (dB)	Γ_0		R_N
		MAG	∠ φ	
1.000	0.8	0.859	26.36	0.98
1.575	1.0	0.793	43.87	0.70
2.000	1.3	0.713	55.80	0.56

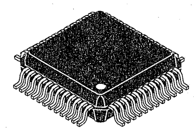
The MRFIC Line
Integrated GPS Downconverter

MRFIC1502

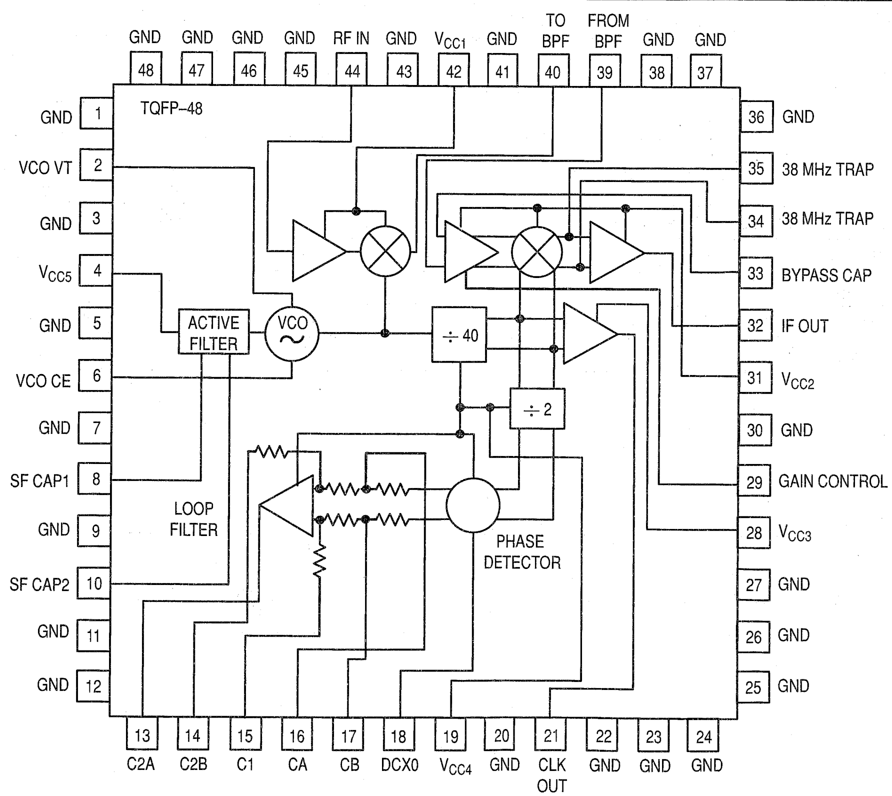
1.575 GHz GPS DOWNCONVERTER

This integrated circuit is intended for GPS receiver applications. The dual conversion design is implemented in Motorola's low–cost high performance MOSAIC 3 silicon bipolar process and is packaged in a low–cost surface mount TQFP–48 package. In addition to the mixers, a VCO, a PLL and a loop filter are integrated on–chip. Output IF is nominally 9.5 MHz.

- 65 dB Minimum Conversion Gain
- 5 Volts Operation
- 50 mA Typical Current Consumption
- Low–Cost, Low Profile Plastic TQFP Package
- Order MRFIC1502R2 for Tape and Reel.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1502



CASE 932–02
(TQFP–48)



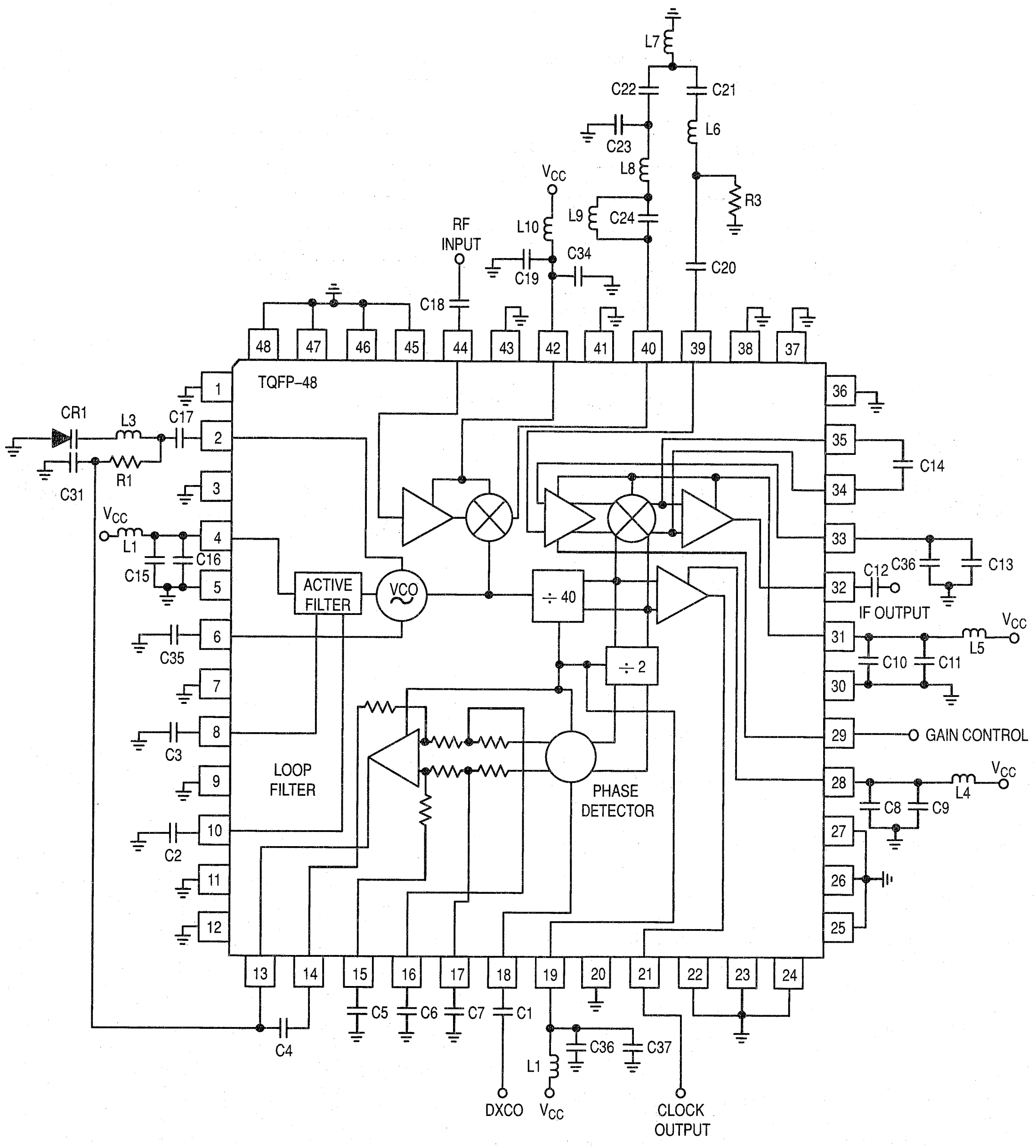
Pin Connections and Functional Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Limit	Unit
DC Supply Voltage	V_{DD}	+6.0	Vdc
DC Supply Current	I_{DD}	60	mA
Operating Ambient Temperature	T_A	– 40 to +100	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Lead Soldering Temperature Range (10 seconds)	—	+260	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, and V_{CC} = 5 V, Tested in Circuit shown in Figure 1 unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Voltage	4.75	—	5.25	Vdc
Supply Current	—	—	60	mA
L–Band Gain (Measured from L–Band Input to 47 MHz Output)	—	20	—	dB
IF Gain (Measured from 47 MHz Input to 9.5 MHz Output with Gain Control at Maximum)	—	45	—	dB
Conversion Gain (Measured from L–Band Input to 9.5 MHz Output with Gain Control at Maximum)	65	—	—	dB
Gain Control (Externally Adjustable 0 to 5.0 V, Maximum at 0 V)	—	40	—	dB
Noise Figure (Double Sideband)	—	9.5	—	dB
L–Band Input VSWR (Measured into 50 Ω; 1575.42 ± 5.0 MHz)	—	2:1	—	—
First IF Output VSWR (Measured into 50 Ω; 47.74 ± 5.0 MHz)	—	2:1	—	—
Second IF Output VSWR (Measured into 50 Ω; 9.5 ± 5.0 MHz)	—	2:1	—	—
Input Impedance @ 1st IF 47.7 ± 5 MHz (For Reference Only)	—	2000	—	Ω
Output 1.0 dB Compression Point	—	–7	—	dBm
First LO (Measured at the First IF Output)	—	–20	—	dBm
All Other Harmonics (Measured at the First IF Output)	—	–45	—	dBm
38.1915 MHz Leakage at First IF Output	—	–50	—	dBm
Second LO (Measured at the Second IF Output)	—	–25	—	dBm
All Other Harmonics (Measured at Second IF Output)	—	–45	—	dBm
Reference Oscillator Input	400	—	4500	mVpp
Clock Output Frequency Amplitude Low High (Clock Amplitude Measured with the Output Loaded in 15 pF and 40 kΩ) Duty Cycle	$2Xf_{ref}$ — 2.0 45	—	$2Xf_{ref}$ 0.8 — 55	 V V %
VCO Lock Voltage	1.2	—	3.0	V
Phase Detector Gain	—	0.16	—	V/Radian
VCO Modulation Sensitivity	—	15	—	MHz/V



C1, C8, C10, C12, C13, C15, C19, C20, C37	10,000 pF	C24	68 pF, ATC
C4, C5	5600 pF	C35	0.4 pF, ATC
C6, C7, C31	1000 pF	CR1	2.7 pF, MA45233–123, MACOM
C2, C3	1.0 μF	L1, L4, L5, L10	2.2 μH, 1008CS–222XKBC, COILCRAFT
C14	3.9 pF, ATC	L3	2.2 nH, LL2012–F2N2S, TOKO
C16, C18, C36	27 pF, ATC	L6	2.2 μH
C17	15 pF, ATC	L7	220 nH
C21	5.6 pF, ATC	L8	0.56 μH
C9, C11, C34, C36	47 pF, ATC	L9	0.27 μH
C22, C23	120 pF, ATC	R1	10 kΩ
		R3	220 Ω

Figure 1. Test Circuit Configuration

Table 1. Port Impedance Derived from Circuit Characterization

Pin Number	Pin Name	f (MHz)	Z_{in} Ohms	
			R	jX
44	RF IN	1575.42	38.3	–16.09
40	TO BPF	47.74	54.45	11.3
39	FROM BPF	47.74	43	1.5
32	IF OUT	9.5	560	–850

Z_{in} represents the input impedance of the pin.

APPLICATION INFORMATION

Design Philosophy

The MRFIC1502 design is a standard dual downconversion configuration with an integrated fixed frequency phase–locked loop to generate the two local oscillators and the buffer to generate the sampling clock for a digital correlator and decimator. The active device for the L–band VCO is also integrated on the chip. This chip is designed in the third generation of Motorola's Oxide Self Aligned Integrated Circuits (MOSAIC 3) silicon bipolar process.

Circuit Considerations

The RF input to the MRFIC1502 is internally matched to 50 ohms. Therefore, only AC coupling is required on the input. The output of the amplifier is fed directly into the first mixer. This mixer is an active Gilbert Cell configuration. The output of the mixer is brought off–chip for filtering of the unwanted mixer products. The amplifier and mixer have their own V_{CC} supply (pin 42) in order to reduce the amount of coupling to the other circuits. There are two bypass capacitors on this pin, one for the high frequency components and one for the lower frequency components. These two capacitors should be placed physically as close to the bias pin as possible to reduce the inductance in the path. The capacitors should also be grounded as close to the ground of the IC as possible, preferably through a ground plane.

The output impedance of the first mixer is 50 ohms, while the input impedance to the first IF amplifier is 1 kΩ. There is a trap (zero) designed in at the second LO frequency to limit the amount of LO leakage into the high gain first IF amplifier.

The first IF amplifier is a variable gain amplifier with 25 dB of gain and 40 dB of gain control. The gain control pin can be grounded to provide the maximum gain out of the amplifier. If the baseband design utilizes a multi–bit A/D converter in the digital signal processing chip, this amplifier could be used to control the input to the A/D converter. The amplifier has an external bypassing capacitor. This capacitor should be on the order of 0.01 µF, and again should be located near the package pin.

The second mixer design is also a Gilbert Cell configuration. The interface between the mixer and the second IF amplifier is differential in order to increase noise immunity. This differential interface is also brought off–chip so that some additional filtering could be added in parallel between the output of the mixer and input to the amplifier. This filtering is primarily to reduce the amount of LO leakage into the final IF amplifier and is achieved using a single 3.9 pF capacitor across the differential ports. The value of the capacitor determines the high frequency of the low pass structure.

The supply pin for the IF circuits is pin 33. This supply pin should be isolated from the other chip supplies in order to reduce the amount of coupling. The recommended capacitors are a 47 pF and a 0.01 µF, in parallel to bypass the supply to ground and should be placed physically as close to the pin as possible.

The output of the second IF amplifier is 50 ohms with a bandwidth of ±5.0 MHz. This signal must be filtered before being digitized in order to limit the noise entering the A/D converter.

VCO Resonator Design

The design and layout of the circuits around the voltage controlled oscillator (VCO) are the most sensitive of the entire layout. The active device and biasing resistors are integrated on the MRFIC1502. The external circuits consist of the power supply decoupling, the capacitors for the integrated supply superfilter, the resonator and frequency adjusting elements, and the bypassing capacitor on the emitter of the active device.

The VCO supply is isolated from the rest of the PLL circuits in order to reduce the amount of noise that could cause frequency/phase noise in the VCO. The supply should be filtered using a 22 µH inductor in series and a 27 pF and 0.01 µF in parallel. The 27 pF capacitor should be series resonant at least as high as the VCO frequency to get the most L–band bypassing as possible. The on–chip supply filter requires two capacitors off–chip to filter the supply. The capacitors on the input (pin 8) and output (pin 10) of the filter are 1.0 µF, and the output also has a high frequency bypass capacitor in parallel. The input capacitor should not be smaller than a 1.0 µF to insure stability of the supply filter.

The VCO design is a standard negative resistance cell with a buffer amplifier. The resonating structure is connected to the base of the active device and consists of a coupling capacitor, a hyper–abrupt varactor diode, and a wire wound chip inductor. With the values shown on the application circuit, the VCO is centered at 1527.7 MHz, and the gain of the VCO is approximately 20 MHz/Volt.

The above performance is heavily dependent on the capacitive structure that is used as the emitter bypass on pin 6. The total capacitance should be approximately 1.0 pF; that can be achieved using either a discrete element or a microstrip open circuited stub. The evaluation circuit shown uses a 0.4 pF capacitor.

Phase–locked Loop Design

The VCO signal at 1527.68 MHz is divided by 40 to get the second LO frequency of 38.19 MHz. In addition to providing the LO to the second mixer, the 38 MHz signal is output through a translator and is used as the sampling clock for the digital correlator and decimator circuits. There is an additional divide by two so the signal used by the phase detector is at 19.096 MHz. The reference input to the phase detector (pin 18) has an input sensitivity of 400 mVpp minimum and 2.5 Vpp maximum.

The loop filter design is the standard op–amp loop filter, resulting in a type 2 second order loop. The layout of the discrete components around the loop filter and VCO is very critical to the performance of the phase–locked loop. Care should be taken in routing the VCO control voltage line from the output of the loop filter to the varactor diode.

The output of the divide by 40 is buffered by a clock translator that converts the low level sine wave into a TTL level square wave. The loading on the buffer is high so the peak currents can reach as high as 50 mA with the maximum load of 1.0 kΩ in parallel with 40 pF on the output. Therefore, the translator has a dedicated V_{CC} supply, pin 28, which requires external bypassing and isolation. The recommended bypassing uses two capacitors in parallel, a 47 pF and a 0.01 µF capacitor.

Conclusion

The MRFIC1502 offers a highly integrated downconverter solution for GPS receivers. For more detailed applications information on GPS system design refer to application note AN1610, "Using Motorola's MRFIC1502 in Global Positioning System Receivers."

The MRFIC Line
1.8 GHz Antenna Switch

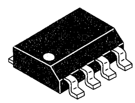
Designed primarily for use in DECT, Japan Personal Handy System (PHS), other wireless Personal Communication Systems (PCS) applications, and 2.4 GHz ISM band applications. The MRFIC1801 is a single pole, double throw reflective antenna switch featuring low insertion loss and high power handling capability in a low-cost SOIC-8 package. The integrated circuit requires no off-chip matching and provides for easy control circuit interface. The high power handling capability allows application in higher power wireless systems than traditional GaAs antenna switches.

Together with the rest of the MRFIC180X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

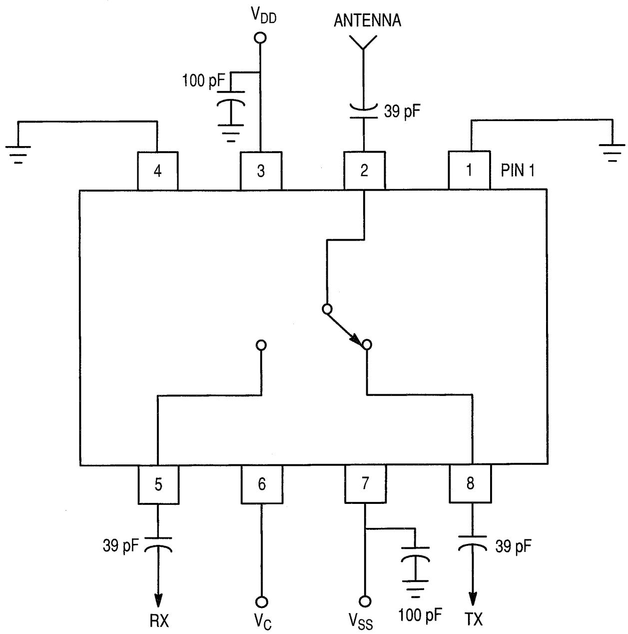
- Usable Frequency Range 1.5 to 2.5 GHz
- High 1.0 dB Compression Point = 29 dBm (Typ)
- Low Transmit Insertion Loss = 0.75 dB (Typ)
- High Transmit to Receive Isolation = 22 dB (Typ)
- Single Control Pin for Easy Switching Signal Interface
- Low Current Drain = 300 μA (Typ) in TX, 45 μA (Typ) in RX
- Low Cost Surface Mount Plastic Package
- Order MRFIC1801R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M1801

MRFIC1801

1.8 GHz
TRANSMIT/RECEIVE
ANTENNA SWITCH
GaAs MONOLITHIC
INTEGRATED CIRCUIT



CASE 751–05
(SO-8)



Functional Block Diagram and Pin Assignment

REV 2

MAXIMUM RATINGS (T_A= 25°C unless otherwise noted)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	10	Vdc
Supply Voltage Difference	$V_{DD} - V_{SS}$	8	Vdc
RF Input Power	P_{in}	33	dBm
Switch Control Voltage	V_C	V_{DD} +1, V_{SS} −1	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to + 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	2.7 to 5.5	Vdc
Supply Voltage Difference	$V_{DD} - V_{SS}$	5.5	Vdc
Switch Control Voltage	V_C	V_{DD} to V_{SS}	Vdc
Operating Frequency	f	1.5 to 2.5	GHz

ELECTRICAL CHARACTERISTICS ($V_{DD} - V_{SS}$ = 5.5 V, T_A = 25°C, f = 1.9 GHz)

Characteristic	Min	Typ	Max	Unit
Antenna to Receive Insertion Loss (RX Mode, P_{IN} = 0 dBm)	—	0.8	1	dB
Transmit to Antenna Insertion Loss (TX Mode, P_{IN} = +27 dBm)	—	0.6	1	dB
Transmit to Receive Isolation in TX Mode (P_{IN} = +27 dBm)	—	22	—	dB
Antenna to Transmit Isolation in RX Mode (P_{IN} = 0 dBm)	—	18	—	dB
Input Return Loss, all ports	—	15	—	dB
Transmit to Antenna Input 1.0 dB Compression	—	29	—	dBm
Leakage Current (RX Mode)	—	45	—	μA
Total Supply Current (TX Mode)	—	300	—	μA

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

APPLICATIONS INFORMATION

The MRFIC1801 is a SPDT switch. A series–shunt pair of FETs are used in each path for improved isolation. The power handling capability of the MRFIC1801 is determined by the difference between V_{DD} and V_{SS}. Typical operating conditions are V_{DD} = 3.0 V and V_{SS} = –2.5 V, but a negative V_{SS} is not required. V_{SS} can be grounded.

Mode	V_C
RX	V_{SS}
TX	V_{DD}

Table 1. Logic Table

TYPICAL CHARACTERISTICS
($V_{DD} - V_{SS}$ = 5.5 V)

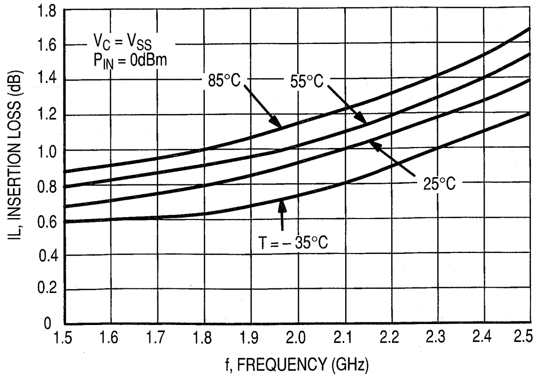


Figure 1. Antenna to Receive Insertion Loss

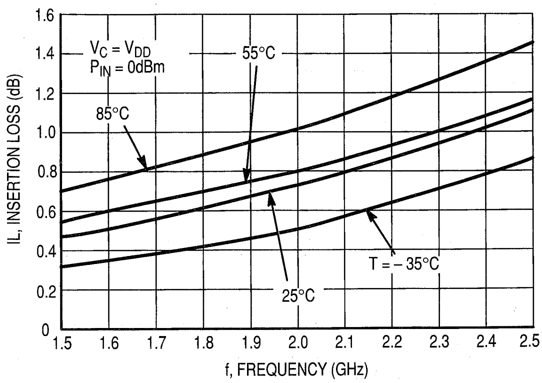


Figure 2. Transmit to Antenna Insertion Loss (Small Signal)

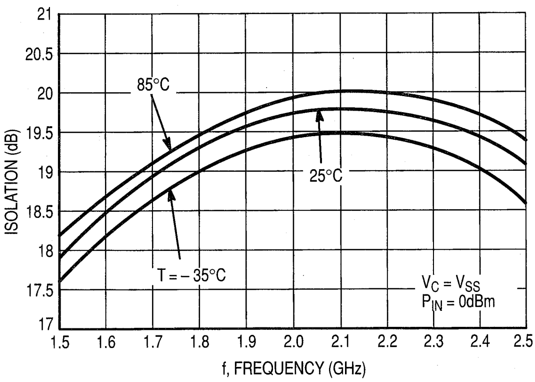


Figure 3. Antenna to Transmit Isolation in RX Mode

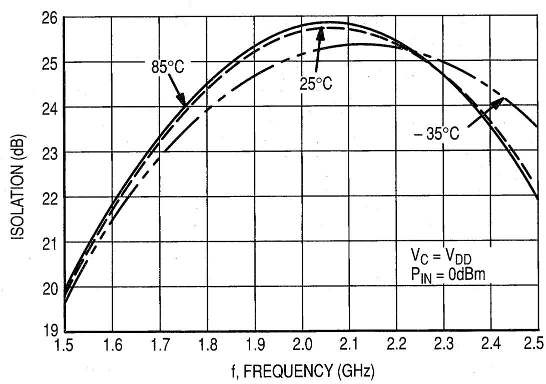


Figure 4. Transmit to Receive Isolation in TX Mode

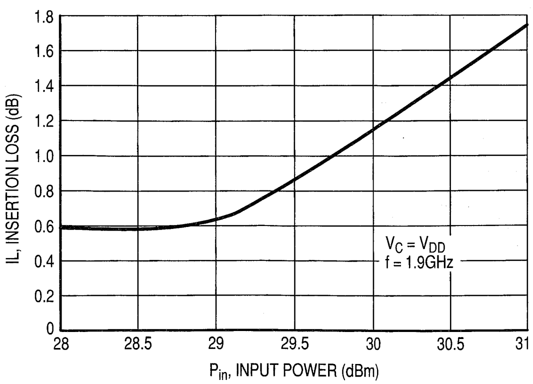


Figure 5. Antenna Switch Insertion Loss versus Input Power (Large Signal)

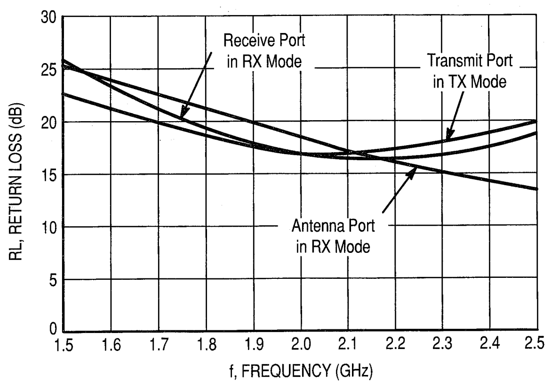
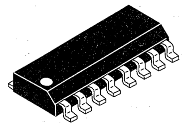


Figure 6. Return Loss

The MRFIC Line
1.8 GHz Upconverter

MRFIC1803

1.8 GHz UPMIXER, EXCITER AND LO AMP GaAs MONOLITHIC INTEGRATED CIRCUIT



CASE 751B-05 (SO–16)

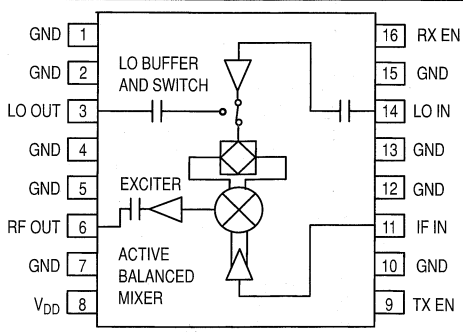
Designed primarily for use in DECT, Japan's Personal Handy System (PHS), and other wireless Personal Communication Systems (PCS) applications at 1.8 GHz, but also applicable to Industrial, Scientific and Medical (ISM) applications at 2.5 GHz. The MRFIC1803 is a complete active upmixer, exciter amplifier, and LO buffer amplifier in a low-cost SOIC-16 package. The low power consumption design includes a single balanced active mixer, CMOS compatible receive and transmit enable inputs, a buffer/exciter amplifier, and a buffered LO output capable of driving the MRFIC1804 downconverter. IF, LO and RF ports are matched to 50 Ω and no off-chip baluns are required. With both TX and RX enable pins low, the device is in standby mode and draws less than 0.3 mA.

Together with the rest of the MRFIC180X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- 10 dB IF to RF Conversion Gain
- Usable Frequency Range = 1.7 to 2.5 GHz
- Low Power Consumption = 80 mW (Typ)
- Single Bias Supply = 2.7 to 3.3 V
- No External Baluns Required
- IF, LO and RF Ports Matched to 50 Ω
- Low LO Power Requirement = –10 dBm (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1803R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1803

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	5.5	Vdc
IF Input Power	P_{IF}	3	dBm
LO Input Power	P_{LO}	3	dBm
Transmit and Receive Enable Voltage	TX EN, RX EN	5.5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to + 85	°C



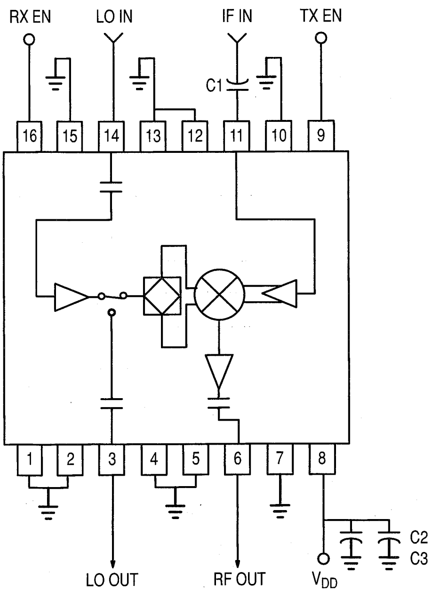
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
LO Input Frequency	f_{LO}	1.5 to 2.4	GHz
LO Input Power	P_{LO}	–10	dBm
IF Input Frequency	f_{IF}	70 to 350	MHz
RF Output Frequency	f_{RF}	1.7 to 2.5	GHz
Transmit and Receive Enable Voltage	TX EN, RX EN	2.7 to V_{DD}	Vdc
Supply Voltage	V_{DD}	2.7 to 5	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3 V, T_A = 25°C, LO = 1790 MHz @ –10 dBm, IF = 110 MHz @ –15 dBm, TX EN = 3.0 V, RX EN = 0 V, unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
IF to RF Conversion Gain	8	10	—	dB
RF Output 1 dB Compression	—	– 2	—	dBm
RF Output 3rd Order Intercept	—	9	—	dBm
LO Feed Through to RF Port	—	–19	—	dBm
Auxiliary LO Output Power (TX EN = 0 V, RX EN = 3 Vdc)	—	– 4	—	dBm
Supply Current, TX Mode	—	28	50	mA
Supply Current, RX Mode (TX EN = 0 V, RX EN = 3 Vdc)	—	3	—	mA
Standby Mode Current (TX EN = 0 V, RX EN = 0 Vdc)	—	0.1	0.3	mA



C1 470 pF
C2 100 pF
C3 0.1 µF (optional)

Figure 1. Applications Circuit Configuration

Typical Characteristics

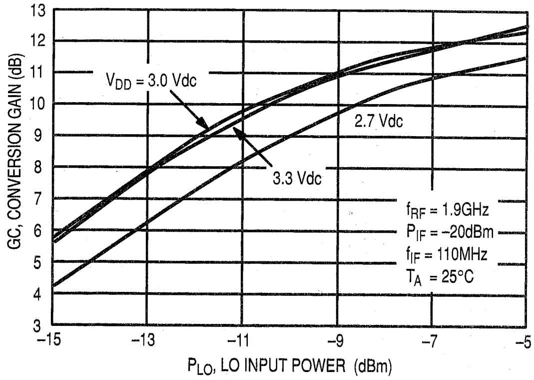


Figure 2. Conversion Gain versus LO Power

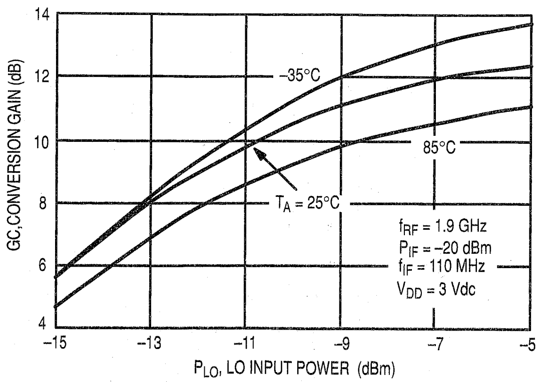


Figure 3. Conversion Gain versus LO Power

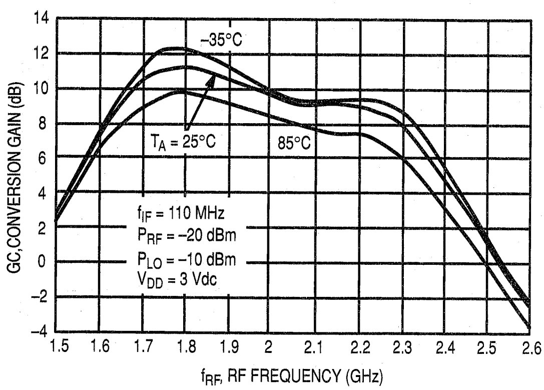


Figure 4. Conversion Gain versus RF Frequency

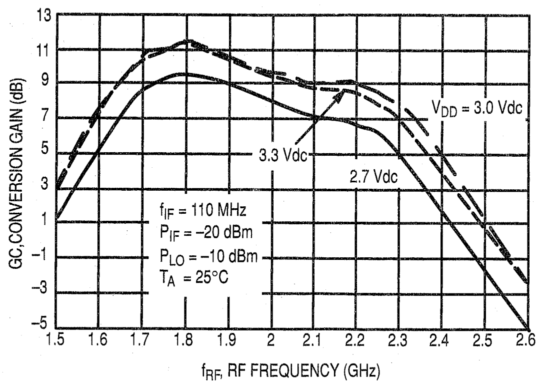


Figure 5. Conversion Gain versus RF Frequency

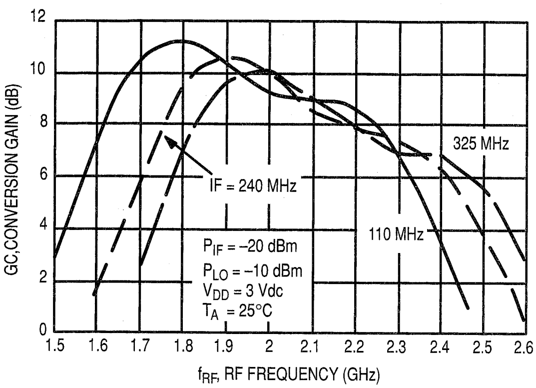


Figure 6. Conversion Gain versus RF Frequency

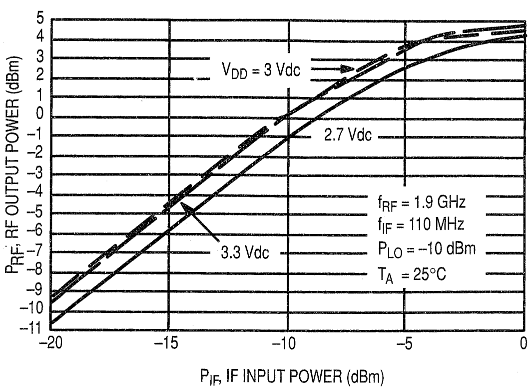


Figure 7. RF Output Power versus IF Input Power

Typical Characteristics

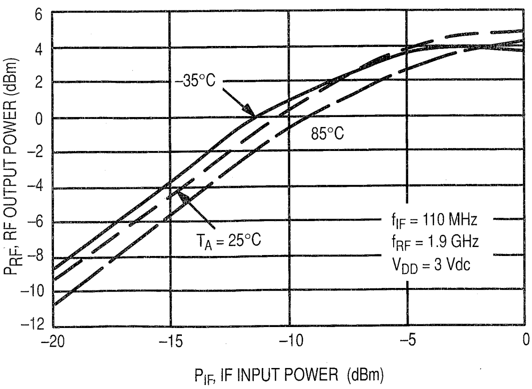


Figure 8. RF Output Power versus IF Input Power

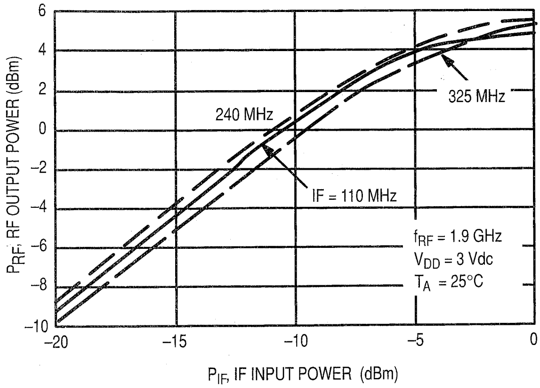


Figure 9. RF Output Pwer versus IF Input Power

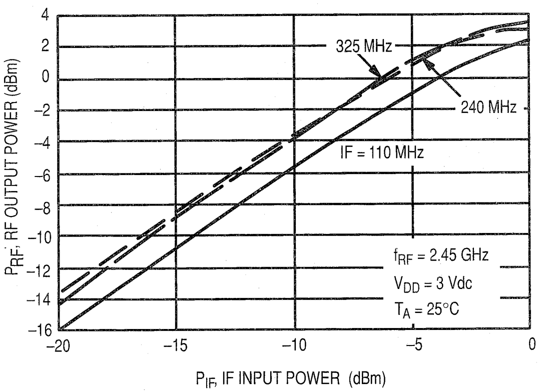


Figure 10. RF Output Power versus IF Input Power at 2.45GHz

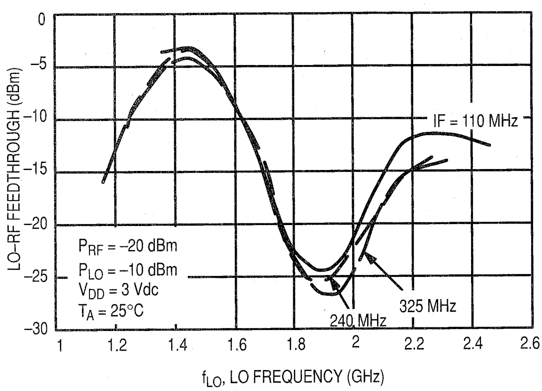


Figure 11. LO to RF Feedthrough versus LO Frequency

Frequency (MHz)	RF Output	LO Input	LO Output
1500	22.07 –j11.36	41.98 +j22.31	20.09 +j31.15
1550	21.74 –j4.69	50.60 +j9.80	26.39 +j40.79
1600	22.28 +j2.16	41.93 –j0.07	37.63 +j52.47
1650	24.01 +j8.25	32.74 +j3.32	56.16 +j63.47
1700	26.64 +J14.13	28.78 +j11.39	87.97 +j67.31
1750	30.83 +j20.11	28.98 +j21.04	131.33 +j40.34
1800	36.39 +j25.30	32.13 +j30.26	137.85 –j16.48
1850	43.92 +j29.26	37.68 +j40.38	103.88 –j50.81
1900	54.37 +j30.98	48.31 +j54.15	69.58 –j53.97
1950	65.34 +j28.57	68.80 +j70.87	50.13 –j46.24
2000	75.30 +j21.12	118.18 +j86.46	38.97 –j36.86
2050	81.19 +j8.43	220.83 +j17.19	32.08 –j27.58
2100	80.22 –j4.24	148.91 –j120.77	28.43 –j19.86
2150	74.20 –j14.00	58.50 –j105.11	26.56 –j12.82
2200	65.50 –j19.72	27.23 –j71.51	26.03 –j5.89
2250	57.40 –j21.38	17.22 –j50.26	26.73 –j0.03
2300	50.59 –j20.61	13.00 –j35.19	28.46 +j5.10
2350	44.53 –j18.16	10.95 –j22.96	30.88 +j9.86
2400	40.24 –j14.78	10.23 –j13.58	33.75 +j13.92
2450	37.73 –j10.54	10.20 –j5.32	37.50 +j17.32
2500	36.38 –j6.72	10.62 +j2.90	42.00 +j20.34

Table 1. Selected Device Impedances

DESIGN AND APPLICATIONS INFORMATION

The MRFIC1803 combines a single–balanced FET mixer with an LO pre–amp and an exciter amplifier to form a self–contained upconverter. The device is usable from RF frequencies of 1.7 to 2.5 GHz and at IF frequencies of 70 to 325 MHz. The design is optimized for low side injection in hetrodyne transmitter applications. In the upconversion process, modulation is imparted to an IF carrier which is converted to the RF transmit frequency by a mixer. By DC coupling the IF input, the device can be used for simple on–off keying (OOK) or bi–phase shift keying (BPSK) applications with no IF.

The MRFIC1803 design minimizes the need for off–chip components. An active balun is employed at the IF input and provides an excellent broadband 50Ω match over the full range of IF frequencies. The LO quadrature divider is passive and internal to the device. The LO buffer amplifier is equipped with a diversity switch which switches the amplified LO signal to the LO output pin during RECEIVE mode. The –5 dBm LO output is the appropriate level to drive the MRFIC1804 for 1.8 GHz applications or the MRFIC2401 for 2.4 GHz applications.

As shown in Figure 1, the device is easy to use with minimal off–chip components. More or less bypassing of the control and supply lines may be required depending on board layout and shielding. Careful layout of the RF frequency portions of the board is critical to successful implementation. Controlled impedance lines must be used and any off–chip components must be mounted as close to the IC as possible. The applications circuit was used to gather the information displayed in the typical characteristics curves. Since the MRFIC1803 design was optimized for the 1.7 to 1.9 GHz frequency range, improved performance can be had with some off–chip matching at frequencies outside this range. In particular, matching of the LO port will supply higher LO drive and improve conversion gain. At the RF output, either better gain or better 1dB compression can be had with external matching.

Filtering is generally required in the upconversion process to reduce image and LO radiation. To minimize pin count, this filtering is accomplished external to the device at the exciter output. For the frequency ranges of application, two and three pole ceramic surface filters are available at reasonable cost and with less than 2 dB of loss.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

1.8 GHz LNA/Downmixer

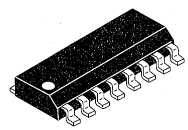
MRFIC1804

1.8 GHz LOW NOISE AMPLIFIER AND DOWNMIXER GaAs MONOLITHIC INTEGRATED CIRCUIT

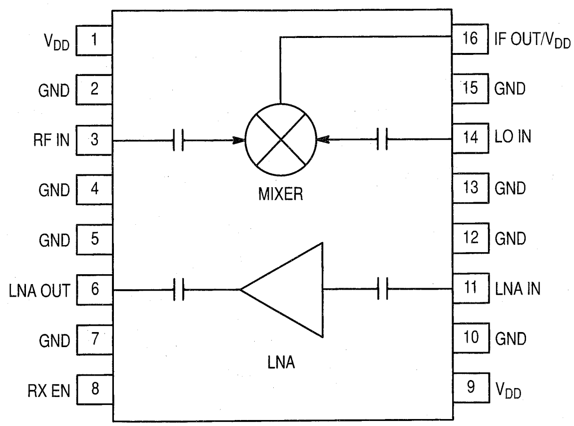
Designed primarily for use in DECT, Japan Personal Handy Phone (JPHP), and other wireless Personal Communication Systems (PCS) applications. The MRFIC1804 includes a low noise amplifier and downmixer in a low-cost SOIC-16 package. The integrated circuit requires minimal off-chip matching while allowing for the maximum in flexibility and efficiency. The mixer is optimized for low side injection and offers reasonable intercept point as well as high efficiency and 4 dB of conversion gain. Image filtering is implemented off-chip to allow maximum flexibility. With both TX and RX enable pins low, the device is in standby mode and draws less than 0.5 mA.

Together with the rest of the MRFIC180X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable Frequency Range = 1.5 to 2.2 GHz
- 14 dB Gain, 2.3 dB Noise Figure LNA
- 4 dB Gain, 13 dB Noise Figure Mixer
- 0.9 dB Mixer Input Intercept Point
- Simple LO/IF Off-Chip Matching for Maximum Flexibility
- Low Power Consumption = 24 mW (Typ)
- Single Bias Supply = 2.7 to 3.3 V
- Low LO Power Requirement = – 5 dBm (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1804R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1804



CASE 751B-05
(SO–16)



Pin Connections and Functional Block Diagram

REV 2

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

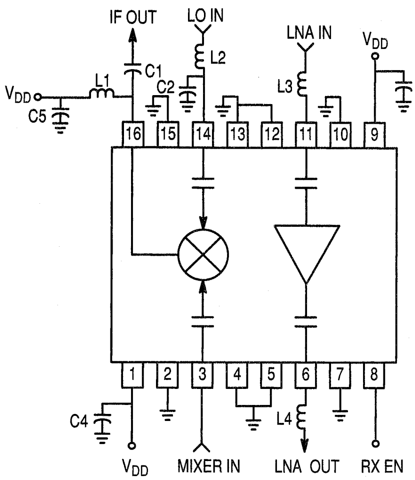
Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD}	5	Vdc
LNA Input Power (Standby Mode)	LNA_{in}	10	dBm
LO Input Power	P_{LO}	0	dBm
Receive Enable Voltage	RX EN	5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Input Frequency	f_{RF}	1.8 to 1.925	GHz
Mixer LO Frequency	f_{LO}	1.5 to 1.9	GHz
IF Output Frequency	f_{IF}	70 to 325	MHz
Supply Voltage	V_{DD}	2.7 to 3.3	Vdc
Receive Enable Voltage	RX EN	2.7 to 3.3	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3 V, T_A = 25°C, LO = 1790 MHz @ – 5 dBm, RF = 1.9 GHz , RX EN = 3 V)

Characteristic	Min	Typ	Max	Unit
LNA Gain	—	14	—	dB
LNA Noise Figure	—	2.3	—	dB
LNA Input 3rd Order Intercept	—	–11	—	dBm
Mixer Conversion Gain (into 50 Ω)	—	4	—	dB
Mixer Noise Figure	—	13	—	dB
Mixer Input 3rd Order Intercept	—	0.9	—	dBm
Downconverter Gain (Less Image Filter Loss)	16	—	—	dB
Supply Current, RX Mode (RX EN = 3 V, LO_{off})	—	7	10	mA
Standby Mode Current (RX EN = 0 V, LO off)	—	—	0.5	mA



C1	12 pF (110 MHz) or 7.5 pF (240 MHz)
C2	0.8 pF
C3, C4	100 pF
C5	1000 pF
L1	82 nH (110 MHz) or 15 nH (240 MHz)
L2	8.2 nH
L3, L4	3.0 nH (Microstrip)

Figure 1. Applications Circuit Configuration (for 110 MHz and 240 MHz IF)

Freq (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
1.5	0.801	–64.71	5.65	–63.77	0.025	139.08	0.685	–62.55
1.6	0.741	–70.03	6.07	–80.96	0.033	128.21	0.622	–74.44
1.7	0.641	–73.54	6.63	–98.00	0.038	123.07	0.622	–83.36
1.8	0.559	–72.72	6.70	–113.87	0.047	113.17	0.560	–92.40
1.82	0.533	–71.10	6.58	–117.42	0.046	111.66	0.543	–93.20
1.84	0.512	–71.20	6.32	–120.25	0.046	109.36	0.530	–94.40
1.86	0.494	–69.93	5.92	–123.27	0.049	107.72	0.513	–95.19
1.88	0.478	–68.86	5.79	–126.51	0.052	106.52	0.498	–95.56
1.9	0.467	–67.50	5.88	–129.49	0.054	104.49	0.486	–96.35
1.92	0.452	–66.18	5.98	–132.33	0.055	103.55	0.476	–97.14
2.0	0.383	–57.10	5.57	–143.54	0.055	97.41	0.412	–96.10
2.1	0.326	–47.69	5.06	–155.69	0.058	92.26	0.344	–90.55
2.2	0.271	–35.10	4.61	–167.78	0.063	86.81	0.276	–83.89
2.3	0.205	–15.07	4.12	175.72	0.072	83.78	0.192	–63.78
2.4	0.708	–12.53	1.84	–155.83	0.073	45.03	0.406	–48.22
2.5	0.462	–34.07	3.18	–178.63	0.055	58.37	0.292	–66.60

Table 1. LNA S–Parameters

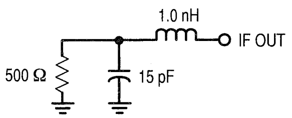


Figure 2. Equivalent IF Output Circuit

TYPICAL CHARACTERISTICS
(V_{DD} = 3 V)

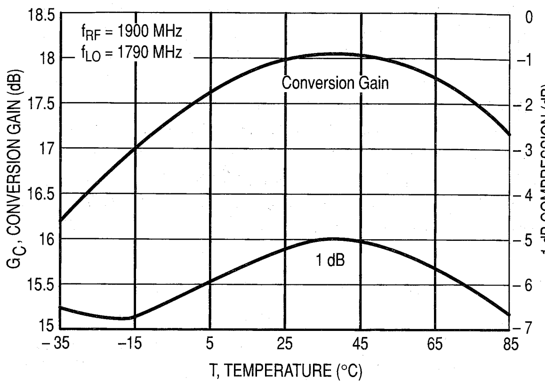


Figure 3. Downconverter Conversion Gain (less Image Filter) and 1 dB Compression versus Temperature

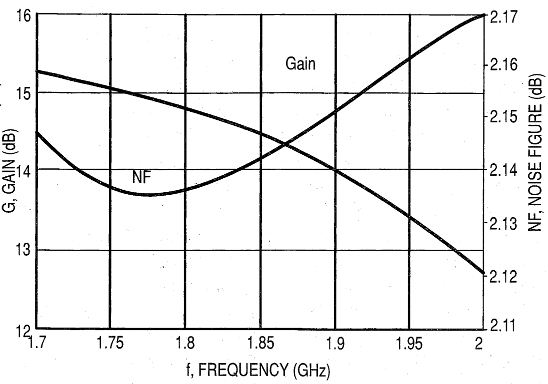


Figure 4. LNA Gain and Noise Figure versus Frequency

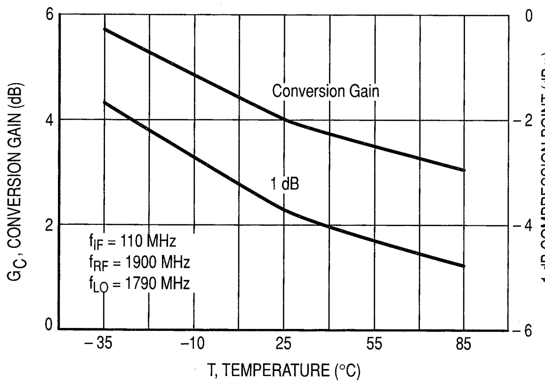


Figure 5. Mixer Conversion Gain and 1 dB Compression versus Temperature

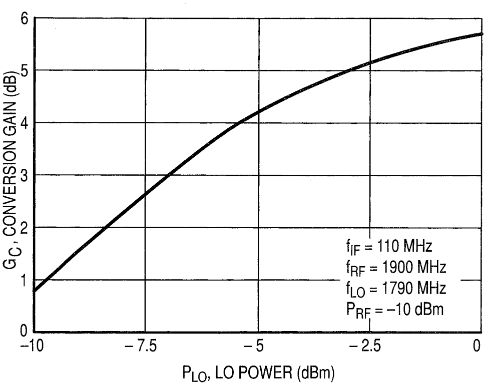


Figure 6. Mixer RF to IF Conversion Gain versus LO Power

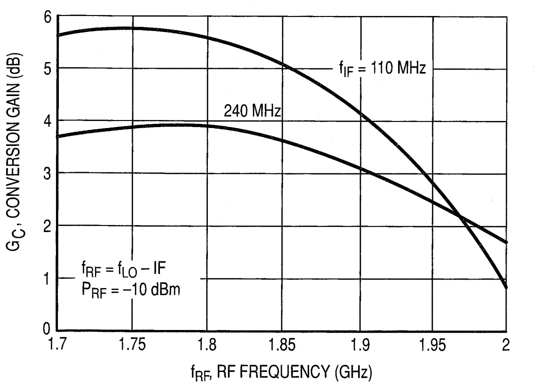


Figure 7. Mixer RF to IF Conversion Gain versus RF Frequency

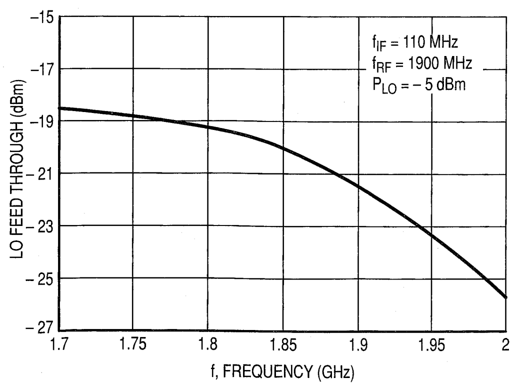


Figure 8. Mixer LO to IF Feed Through versus RF Frequency

DESIGN AND APPLICATIONS INFORMATION

The MRFIC1804 consists of a two–stage GaAs MESFET low noise amplifier and a single ended MESFET mixer. The LNA design conserves bias current through stacking of the two FETs, thus reusing the current. The mixer consists of a common gate stage driving a common source stage with the IF output being the drain of the common source stage shunted with 15 pF. The LNA output and mixer input have been separated to allow the addition of an external image filter. Such a filter, usually ceramic, is useful in improving the mixer noise figure and third order intercept performance. It also provides LO rejection to reduce the amount of LO power which may leak to the antenna. Alternatively, image trapping can be implemented at the LNA input or output with discrete or distributed components.

The design has been optimized for application in the PCS bands around 1.9 GHz but is usable from around 1.5 GHz to 2.2 GHz. For applications at 1.9 GHz and IFs of 110 MHz or 240 MHz, the circuit shown in Figure 1 can be used. This circuit was used to derive the characterization data shown in Figures 3 through 8. For other IF frequencies in the 100 MHz to 350 MHz range, use the IF equivalent circuit shown in Figure 2 for matching network design. As can be seen in the characterization curves, performance appears to degrade above about 1.85 GHz. This is partially a function of the circuit shown in Figure 1 and can be improved, first, by adjusting the LO input match, second, by matching LNA input and and the mixer input off chip.

As with all RF circuits, layout is important. Ground vias must be close to the component or lead to be grounded and vias must be plentiful. RF signal lines should be controlled impedance such as microstrip. Bypassing of power supply leads as shown in Figure 1 is essential to avoid oscillation of the circuits.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

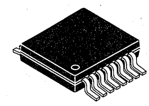
1.9 GHz GaAs Power Amplifier

MRFIC1805

This two–stage class AB monolithic GaAs amplifier in a low–cost 16 lead plastic package is designed for output or driver applications in 1.9 GHz PCS handsets and basestations. The design is optimized for 3.0 Volt operation in systems such as Japan's PHS, Europe's DECT and the emerging North American PCS services. With modifications to the simple off–chip matching, the device can be used in other applications from 1.5 to 2.5 GHz.

- High Output Capability = 27 dBm Typical P_{sat}
  21.5 dBm Typical with PHS Format
- High Gain = 21 dB Typical Small Signal, 20 dB at P_{out} = 22 dBm
- Low Current Drain = 170 mA Typical with PHS Format
  250 mA Typical with DECT Format
- Low–Cost, Low Profile Plastic TSSOP Package
- Order MRFIC1805R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1805

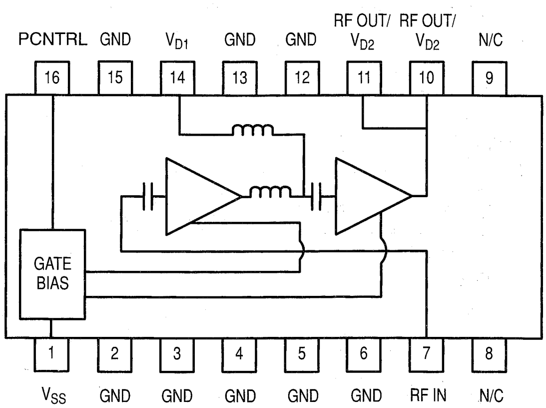
1.9 GHz
POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT



CASE 948C–03
(TSSOP–16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{D1}, V_{D2}	6	Vdc
Supply Voltage	V_{SS}	–4	Vdc
RF Input Power	RF_{in}	+10	dBm
Drain Current	I_{DD}	500	mA
Thermal Resistance, Junction to Air	$R_{\theta JA}$	240	/W
Operating Junction Temperature	T_J	+175	°C
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C



Pin Connections and Functional Block Diagram

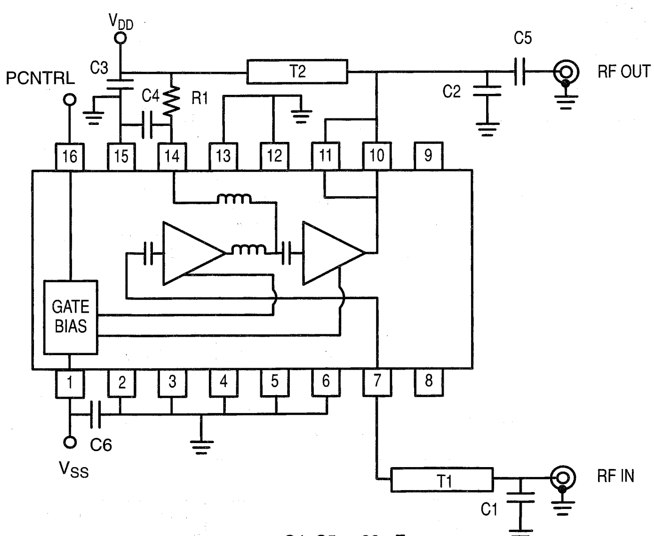
REV 1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{D1}, V_{D2}	2.7 to 5	Vdc
Supply Voltage	V_{SS}	–2.5	Vdc
PA Control Voltage	PCNTRL	0.0 to V_{DD}	Vdc
RF Input Power	P_{in}	–20 to +10	dBm
Operating Frequency Range	f_{OP}	1500 to 2200	MHz

ELECTRICAL CHARACTERISTICS (V_{D1} = V_{D2} = 3 Vdc, V_{ss} = –2.5 Vdc, T_A= 25°C, f = 1.9 GHz, P_{in} = +2 dBm, PCNTRL set for I_{DQ} = 125 mA, circuit configuration as shown in Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Output, Saturation	P_{SAT}	23	25	–	dBm
RF Output Power	P_{out}	20	21.5	–	dBm
Adjacent Channel Power Ratio (384 Kbps π/4 DQPSK Signal, 600 kHz Offset, P_{out} = 21 dBm	P_{ACP}	–	–58	–55	dBc
RF Output 1 dB Compression	P_{1dB}	22	24	–	dBm
2nd Harmonic Output	–	–	–40	–	dBc
3rd Harmonic Output	–	–	–40	–	dBc
Supply Current	I_{DD}	–	170	210	mA
Supply Current	I_{SS}	–	200	300	µA
Supply Current	I_{PCNTRL}	–	220	300	µA
Input Return Loss	–	–	13	–	dB
Reverse Isolation	–	–	31	–	dB
Output Third Intercept	–	–	34	–	dBm
Turn On Time	–	–	1	–	µs



R1 – 22 Ω
C1 – 1.2 pF
C2 – 2.2 pF
C3, C6 – 330 pF
C4, C5, – 22 pF
T1 – 100 Ω Line, 7 mm
T2 – 100 Ω Line, 20 mm
Board Material – 30 MIL FR4
Connectors – SMA Type

Figure 1. Applications Circuit Configuration

TYPICAL CHARACTERISTICS

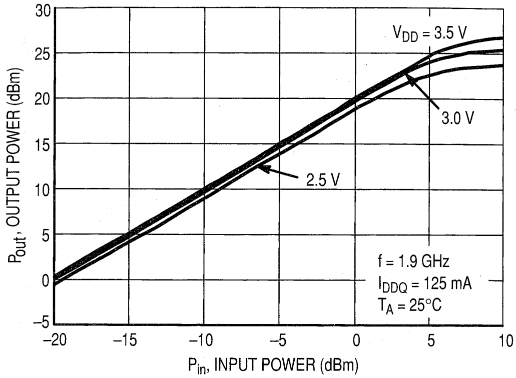


Figure 2. Output Power versus Input Power

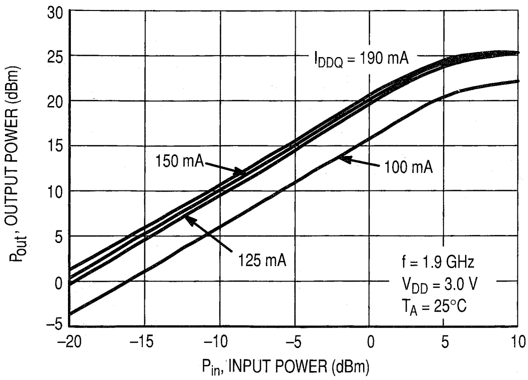


Figure 3. Output Power versus Input Power

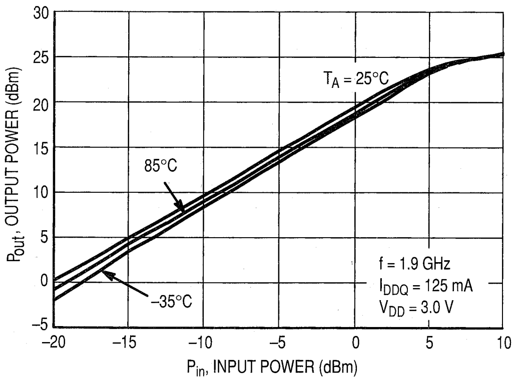


Figure 4. Output Power versus Input Power

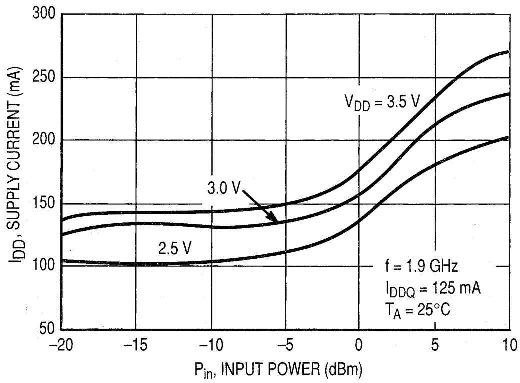


Figure 5. Supply Current versus Input Power

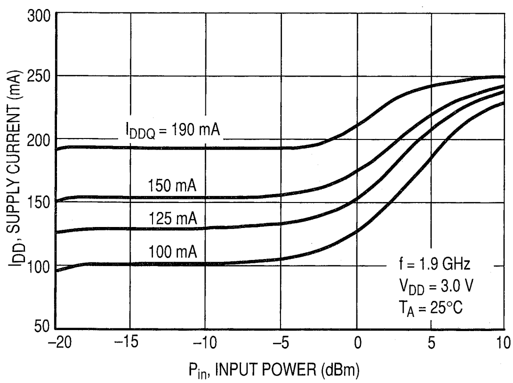


Figure 6. Supply Current versus Input Power

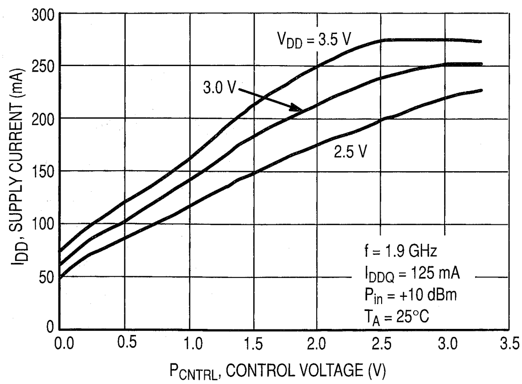


Figure 7. Supply Current versus Control Voltage

TYPICAL CHARACTERISTICS

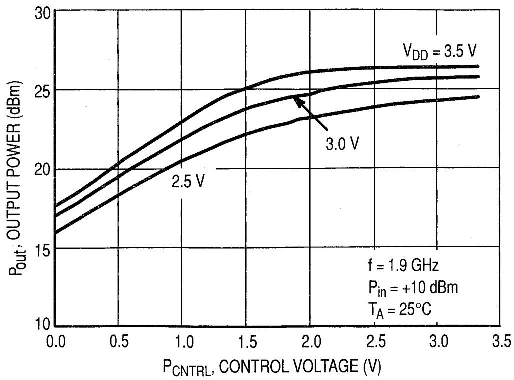


Figure 8. Output Power versus Control Voltage

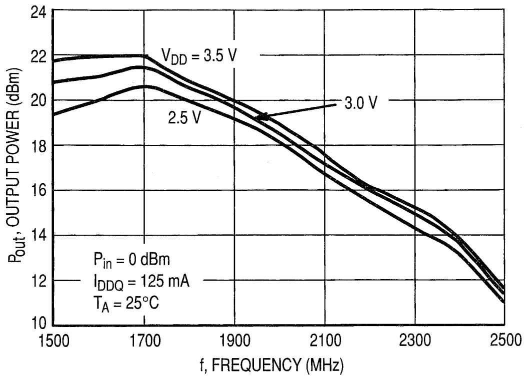


Figure 9. Output Power versus Frequency

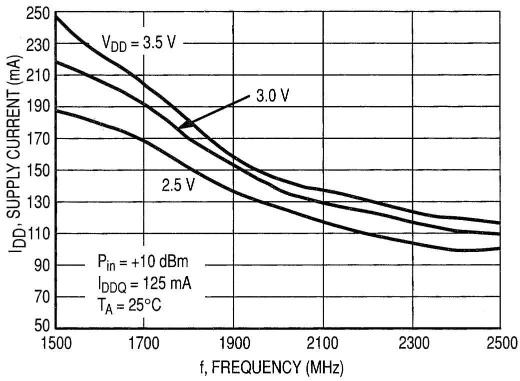


Figure 10. Supply Current versus Frequency

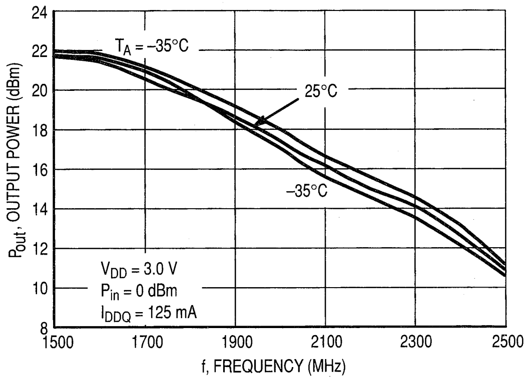


Figure 11. Output Power versus Freqency

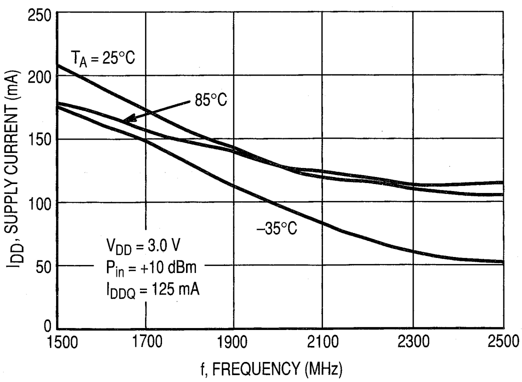


Figure 12. Supply Current versus Frequency

Table 1. Small Signal S–Parameters
($V_{D1} = V_{D2}$ = 3 Vdc, T_A = 25°C, f = 1.9 GHz, PCNTRL set for I_{DQ} = 125 mA, no matching circuit)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$|S_{11}|$	∠ φ	$|S_{21}|$	∠ φ	$|S_{12}|$	∠ φ	$|S_{22}|$	∠ φ
1.50	0.744	–76	10.99	–104	0.013	167	0.494	–177
1.55	0.697	–76	11.01	–114	0.014	164	0.520	179
1.60	0.662	–75	10.39	–124	0.015	163	0.533	174
1.65	0.645	–75	9.22	–132	0.015	160	0.528	170
1.70	0.636	–75	8.93	–135	0.016	157	0.522	167
1.75	0.623	–75	8.90	–141	0.017	157	0.515	164
1.80	0.617	–75	8.24	–148	0.018	158	0.506	161
1.85	0.612	–76	7.70	–152	0.018	155	0.497	159
1.90	0.602	–76	7.06	–158	0.019	154	0.489	156
1.95	0.599	–78	6.41	–160	0.019	154	0.481	154
2.00	0.590	–79	6.16	–160	0.021	154	0.475	152
2.05	0.581	–80	6.12	–165	0.022	152	0.469	150
2.10	0.570	–81	5.83	–170	0.022	150.	0.461	148
2.15	0.562	–83	5.57	–174	0.023	151.	0.458	146
2.20	0.548	–84	5.27	–178	0.024	152	0.455	144
2.25	0.538	–86	5.00	–179	0.025	152	0.450	142
2.30	0.527	–88	4.81	–179	0.027	151	0.448	141
2.35	0.512	–90	4.60	175	0.027	149	0.447	139
2.40	0.499	–92	4.43	171	0.027	146	0.447	137
2.45	0.485	–94	4.27	169	0.028	149	0.449	136
2.50	0.471	–97	4.00	163	0.030	150	0.449	134

Table 2. Small Signal S–Parameters
($V_{D1} = V_{D2} = 3$ Vdc, $T_A = 25°C$, f = 1.9 GHz, PCNTRL set for $I_{DQ} = 150$ mA, no matching circuit)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1.50	0.752	–75	11.90	–104	0.012	169	0.480	–178
1.55	0.699	–75	11.90	–114	0.013	167	0.509	178
1.60	0.662	–75	11.19	–124	0.014	165	0.520	174
1.65	0.643	–74	9.94	–132	0.015	162	0.519	170
1.70	0.628	–74	9.60	–135	0.016	160	0.514	167
1.75	0.616	–74	9.55	–141	0.017	159	0.507	163
1.80	0.607	–74	8.81	–148	0.018	158	0.498	160
1.85	0.598	–75	8.23	–152	0.018	156	0.490	158
1.90	0.590	–75	7.54	–157	0.019	156	0.483	156
1.95	0.584	–77	6.82	–159	0.020	156	0.476	154
2.00	0.573	–78	6.55	–159	0.021	156	0.471	152
2.05	0.564	–79	6.50	–164	0.022	153	0.463	149
2.10	0.550	–81	6.17	–170	0.022	152	0.458	147
2.15	0.541	–82	5.88	–173	0.023	154	0.453	146
2.20	0.529	–84	5.56	–178	0.024	153	0.448	143
2.25	0.518	–86	5.26	–179	0.026	154	0.447	141
2.30	0.507	–88	5.04	–179	0.027	153	0.444	140
2.35	0.492	–90	4.82	176	0.028	150	0.443	138
2.40	0.481	–93	4.62	172	0.028	149	0.442	136
2.45	0.468	–95	4.45	170	0.028	152	0.444	135
2.50	0.454	–97	4.17	165	0.030	152	0.445	133

Table 3. Small Signal S–Parameters
($V_{D1} = V_{D2}$ = 3.3 Vdc, T_A = 25°C, f = 1.9 GHz, PCNTRL set for I_{DQ} = 125 mA, no matching circuit)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1.50	0.764	–73	11.50	–104	0.013	169	0.492	–177
1.55	0.711	–74	11.49	–114	0.014	166	0.518	179
1.60	0.674	–73	10.82	–124	0.014	164	0.528	174
1.65	0.652	–73	9.60	–132	0.016	162	0.524	170
1.70	0.641	–73	9.27	–135	0.016	158	0.519	167
1.75	0.628	–73	9.24	–141	0.017	158	0.507	164
1.80	0.616	–73	8.54	–148	0.017	158	0.495	161
1.85	0.607	–74	7.99	–152	0.019	155	0.489	159
1.90	0.598	–75	7.33	–157	0.019	155	0.480	157
1.95	0.590	–76	6.63	–160	0.020	156	0.471	154
2.00	0.580	–77	6.35	–160	0.021	154	0.461	153
2.05	0.569	–79	6.30	–165	0.021	152	0.454	150
2.10	0.556	–80	5.98	–170	0.023	151	0.445	148
2.15	0.546	–82	5.70	–174	0.022	154	0.439	147
2.20	0.534	–84	5.39	–178	0.024	152	0.436	144
2.25	0.523	–86	5.11	–179	0.025	153	0.430	142
2.30	0.510	–88	4.90	–179	0.026	150	0.427	141
2.35	0.499	–90	4.70	175	0.027	149	0.424	139
2.40	0.486	–93	4.48	171	0.027	148	0.422	137
2.45	0.473	–95	4.31	169	0.027	150	0.422	135
2.50	0.463	–98	4.05	164	0.029	151	0.420	133

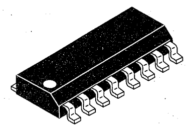
Table 4. Small Signal S–Parameters
($V_{D1} = V_{D2}$ = 3.3 Vdc, T_A = 25°C, f = 1.9 GHz, PCNTRL set for I_{DQ} = 150 mA, no matching circuit)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1.50	0.756	–74	12.03	–105	0.012	168	0.483	–178
1.55	0.702	–75	12.02	–115	0.013	168	0.509	178
1.60	0.663	–74	11.33	–125	0.014	162	0.519	174
1.65	0.644	–73	10.03	–133	0.015	161	0.518	170
1.70	0.628	–73	9.69	–136	0.016	160	0.514	167
1.75	0.614	–73	9.62	–142	0.016	160	0.502	164
1.80	0.603	–74	8.88	–149	0.018	159	0.494	161
1.85	0.596	–74	8.30	–153	0.018	157	0.485	159
1.90	0.584	–75	7.59	–158	0.019	156	0.476	157
1.95	0.577	–76	6.87	–160	0.020	156	0.466	154
2.00	0.567	–77	6.58	–160	0.021	155	0.458	152
2.05	0.559	–79	6.50	–165	0.022	152	0.450	150
2.10	0.545	–80	6.17	–171	0.022	152	0.443	148
2.15	0.536	–82	5.87	–175	0.022	152	0.436	147
2.20	0.524	–84	5.54	–179	0.024	153	0.429	145
2.25	0.512	–86	5.25	–180	0.025	153	0.424	143
2.30	0.500	–88	5.03	180	0.026	152	0.422	141
2.35	0.486	–90	4.78	174	0.027	149	0.418	139
2.40	0.477	–93	4.58	170	0.027	149	0.414	137
2.45	0.462	–95	4.40	168	0.027	150	0.413	136
2.50	0.452	–98	4.13	163	0.029	151	0.412	134

The MRFIC Line
1.8 GHz PA Driver/Ramp

MRFIC1806

1.8 GHz DRIVER AMPLIFIER AND RAMP CIRCUIT GaAs MONOLITHIC INTEGRATED CIRCUIT



CASE 751B–05 (SO–16)

Designed primarily for use in DECT, Japan Personal Handy System (PHS), and other wireless Personal Communication Systems (PCS) applications. The MRFIC1806 includes a two stage driver amplifier and transmit waveform shaping circuitry in a low–cost SOIC–16 package. The amplifier portion employs depletion mode power GaAs MESFETs to produce +21 dBm output with 0 dBm input. The ramping circuit controls the burst–mode transmit rise and fall time and is adjustable through external components. This circuitry also places the amplifier in standby during TDMA receive mode. The MRFIC1806 is sized to drive the MRFIC1807 PA/Switch.

Together with the rest of the MRFIC1800 GaAs ICs, this family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable 1500–2500 MHz
- 23 dB Typical Gain
- +21 dBm Typical 1.0 dB Compression
- Simple Off–Chip Matching for Maximum Flexibility
- 3.0 to 5.0 Volt Supply
- Low Cost Surface Mount Plastic Package
- Order MRFIC1806R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1806

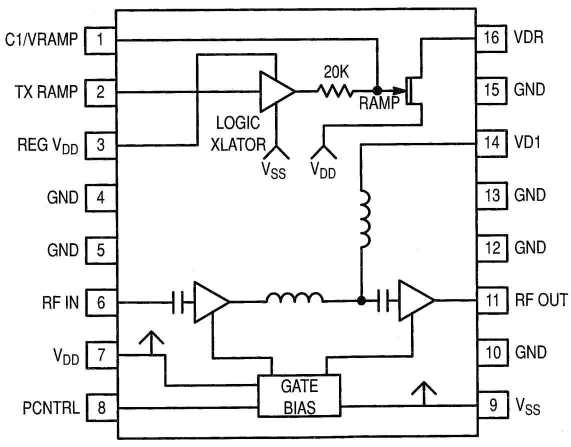


Figure 1. Pin Connections and Functional Block Diagram

REV 2

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD}	6.0	Vdc
Supply Voltage	V_{SS}	−4.0	Vdc
Supply Voltage	REG V_{DD}	4.5	Vdc
Bias Control Voltage	PCNTRL	3.0	Vdc
RF Input Power	P_{IN}	10	dBm
Ramp Circuit Input Voltage (High)	TX RAMP	6.0	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Ambient Operating Temperature	T_A	−10 to +70	°C
Thermal Resistance, Junction to Case	θ_{JC}	100	°C/W

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Input Frequency	f_{RF}	1.5−2.5	GHz
Supply Voltage	V_{DD}	3.0 to 5.0	Vdc
Supply Voltage	V_{SS}	−2.75 to −2.25	Vdc
Supply Voltage	REG V_{DD}	2.9 to 3.1	Vdc
Bias Control Voltage	PCNTRL	0.5 to 1.5	Vdc
RF Input Power	P_{IN}	−20 to +5	dBm
Transmit Burst Enable Voltage (High)	TX RAMP	2.8 to 3.5	Vdc
Transmit Burst Enable Voltage (Low)	TX RAMP	−0.2 to +0.2	Vdc

ELECTRICAL CHARACTERISTICS

DECT Application with Internal Logic Translator (See Figure 2. V_{DD} = 3.5 V, REG V_{DD} = 3.0 V, T_A = 25°C, V_{SS} = −2.5 V, TX RAMP = 3.0 V, PCNTRL set for Quiescent I_{DD} = 120 mA, P_{IN} = −3.0 dBm @ 1.9 GHz unless otherwise stated.)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain (P_{IN} = −7.0 dBm)	21	23	—	dB
Input Return Loss	—	12	—	dB
Reverse Isolation	—	36	—	dB
Output Power	18	19.5	—	dBm
Harmonic Output	—	−36	—	dBc
Output Third Order Intercept	—	33	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.35	0.6	mA
Supply Current, I_{DD} (Pin 7)	—	115	135	mA
Supply Current, REG I_{DD} (Pin 3)	—	0.6	0.9	mA
Ramp Circuit Dynamic Range	40	44	—	dB

STANDBY MODE (TX RAMP = 0 V)

Characteristic	Min	Typ	Max	Unit
Output Power	—	−25	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.4	0.6	mA
Supply Current, REG I_{DD} (Pin 3)	—	0.25	0.4	mA

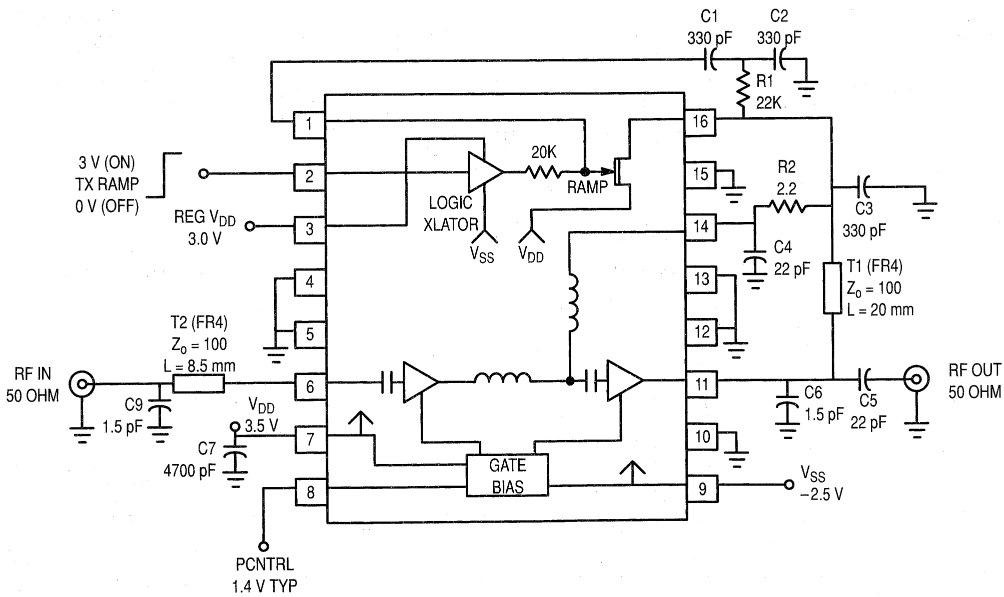


Figure 2. Applications Circuit Details for DECT using Internal Logic Translator

ELECTRICAL CHARACTERISTICS

General Application without Internal Logic Translator (See Figure 3. V_{DD} = 3.5 V, REG V_{DD} (Pin 2) open, V_{SS} = −2.5 V, TX RAMP (Pin 2) grounded, V_{RAMP} = 3.0 V, PCNTRL set for Quiescent I_{DD} = 120 mA, P_{IN} = 0 dBm @ 1.9 GHz, T_A = 25°C unless otherwise stated.)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain (P_{IN} = −7.0 dBm)	21	23	—	dB
Output Power (P_{IN} = 0 dBm)	20	22	—	dBm
Output Power (P_{IN} = +4.0 dBm)	—	23	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.3	0.5	mA
Supply Current, I_{DD} (Pin 7)	—	130	145	mA

STANDBY MODE (V_{RAMP} = −2.4 V)

Characteristic	Min	Typ	Max	Unit
Output Power	—	−25	—	dBm
Supply Current, I_{SS} (Pin 9)	—	0.4	0.6	mA

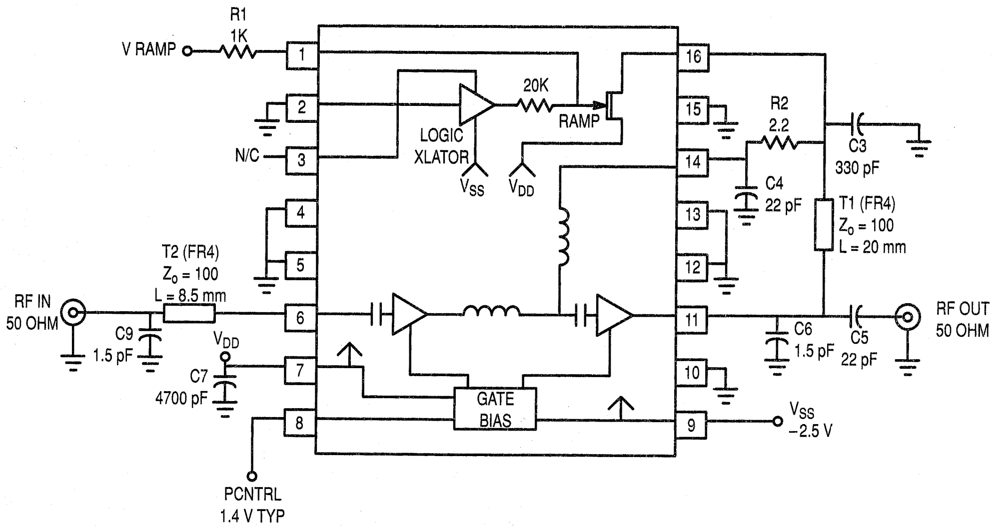


Figure 3. 1.9 GHz General Application Circuit Details (Internal Translator Disabled)

Table 1. Small Signal S−Parameters

(V_{DD} = 3.5 V, I_{DQ} = 120 mA, T_A = 25°C, no matching circuit, reference plane at pins 6 and 11.)

Freq (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
1.5	0.734	−76.8	13.11	−87.9	0.009	−176	0.278	−98.9
1.6	0.654	−82.4	13.01	−109.4	0.012	178	0.326	−116.4
1.7	0.620	−72.6	11.17	−117.4	0.011	152	0.344	−109.8
1.8	0.636	−79.8	12.25	−137.0	0.014	170	0.423	−134.1
1.9	0.607	−80.6	10.77	−151.3	0.017	169	0.421	−147.7
2.0	0.592	−79.4	10.88	−165.1	0.019	163	0.427	−161.8
2.1	0.581	−79.4	9.64	−174.9	0.024	163	0.432	−172.3
2.2	0.571	−78.9	9.30	174.1	0.026	158	0.429	178.8
2.3	0.560	−79.1	7.95	166.9	0.029	157	0.432	171.1
2.4	0.541	−79.8	7.80	155.7	0.033	153	0.442	164.6
2.5	0.521	−80.1	6.90	147.2	0.042	154	0.445	161.7

DESIGN AND APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC1806 is designed to drive the MRFIC1807 Power Amplifier and Transmit/Receive Switch IC in Personal Communications System (PCS) applications such as Europe's DECT and Japan's Personal Handy System (PHS). The design incorporates not only a two–stage GaAs MESFET driver/exciter amplifier, but also externally controllable bias and ramping circuitry. The IC is designed to drive the MRFIC1807 with about +19 dBm which will, in turn, produce +26 dBm output, suitable for DECT. To reduce chip size (and cost) and to allow for flexibility of application, the amplifier has limited on–chip matching. The ramp circuitry is used to shape the drain voltage to the FETs for Time Domain Multiple Access (TDMA) applications and is comprised of a depletion mode pass device driven by a logic translator. Attack and release times are controllable through the use of external components. The IC is configured such that all, part or none of the ramping circuitry can be used, depending on the application.

AMPLIFIER CIRCUIT APPLICATION

As can be seen in Figures 2 and 3, the off–chip matching is straight forward. At frequencies near 1.9 GHz, the input requires 4.7 nH in series and 1.5 pF in shunt. The 4.7 nH series inductance may be implemented with a high–impedance transmission line as shown. The output, being close to 25 Ω, requires only a shunt 1.5 pF capacitor. Drain voltage for stage 1 is supplied through pin 14 and for stage 2 through pin 11, the RF output. Pin 8, PCNTRL is used to set the quiescent bias point for both stages. While nominal I_{DDQ} is 120 mA, it can be set as high as 180 mA for better linearity or lower for better efficiency. 120 mA is a good compromise for DECT and PHS. DECT, which employs GMSK constant envelope modulation can use RF amplifiers close to or in saturation without experiencing spectral regrowth of the signal. PHS, on the other hand, employs $\pi/4$ DQPSK modulation which has some residual AM associated with the encoding. With AM present, RF amplifiers must be backed off from saturation so as not to regrow the filtered sidebands. The MRFIC1806 has plenty of backoff capability for PHS where the MRFIC1807 PA/switch must only produce about +21 dBm. With the 8.0 dB gain of the MRFIC1807, the MRFIC1806 need only produce +13 dBm output so the bias point can be reduced below the 120 mA suggested for DECT. As with all RF circuits, board layout and grounding are important. All RF signal paths must be controlled impedance structures. RF chip components must be high quality. Bypassing capacitors must be close to the IC and to ground vias. Pins which are designated as ground connections must be as close as possible to ground vias.

RAMPING CIRCUIT OPTIONS

The on–chip ramp circuit can be used to control the amplifier attack and release time for DECT applications through the use of a few external components as shown in Figure 2. This ramping is required to control the burst signal rise and fall time to avoid adjacent channel interference. At the same time, system specifications require the transmitter to reach full power in a minimum time. For DECT, it has been shown that a rise time of not greater than 2 microseconds will produce acceptable adjacent channel performance. The system requires full power in not greater than 10 microseconds. A good compromise, and the timing implemented in Figure 2, is 7 microseconds.

The on–chip logic translator can be bypassed as shown in Figure 3 by applying a ramp voltage to Pin 1 through a 1.0 kΩ resistor. This configuration allows flexibility in ramping the amplifier. The regulated V_{DD} voltage is not required so current consumption can be reduced. −2.3 V at Pin 1 turns the pass transistor, and the amplifier, off while a positive voltage will turn the pass transistor on. For full on state it is recommended that V_{RAMP} be close to V_{DD}. V_{RAMP} can also be used to on–off key the amplifier for simple telemetry applications or as transmit/receive control.

For more complex modulation schemes such as $\pi/4$ DQPSK used in PHS, burst ramping can be implemented with the burst mode logic. Referring to Figure 3, the V_{RAMP} voltage should be set to V_{DD} to leave the pass transistor on. The on–chip pass transistor can also be bypassed and V_{DD} applied to Pins 11 and 14.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

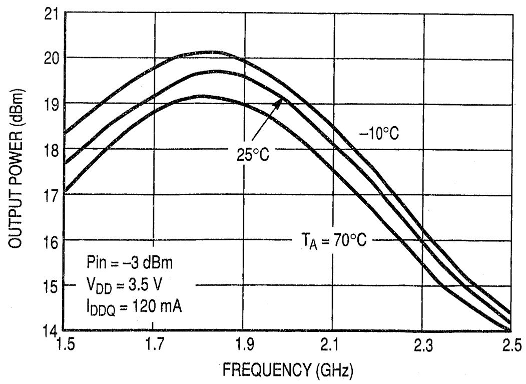


Figure 4. Output Power versus Frequency With Internal Logic Translator

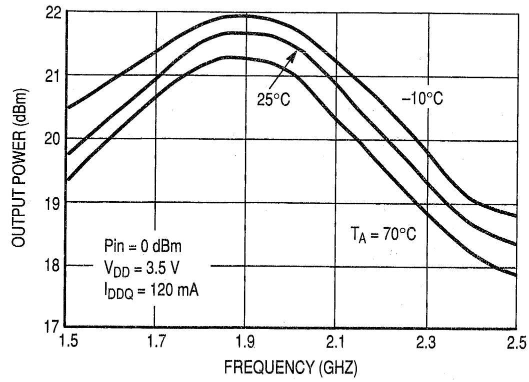


Figure 5. Output Power versus Frequency Without Internal Logic Translator

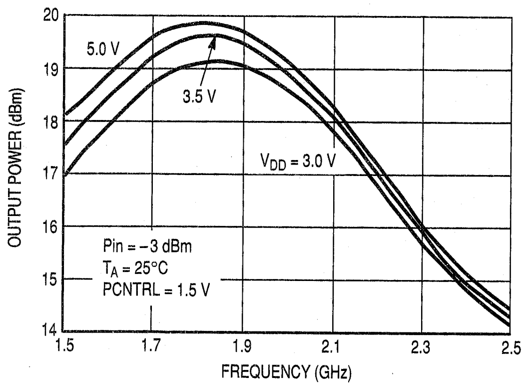


Figure 6. Output Power versus Frequency With Internal Logic Translator

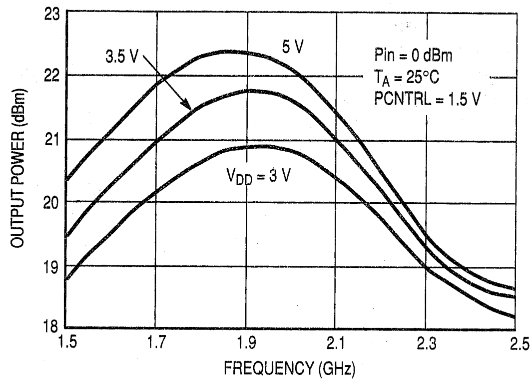


Figure 7. Output Power versus Frequency Without Internal Translator

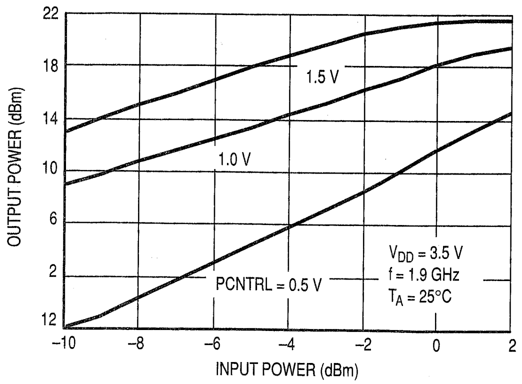


Figure 8. Output Power versus Input Power With Internal Logic Translator

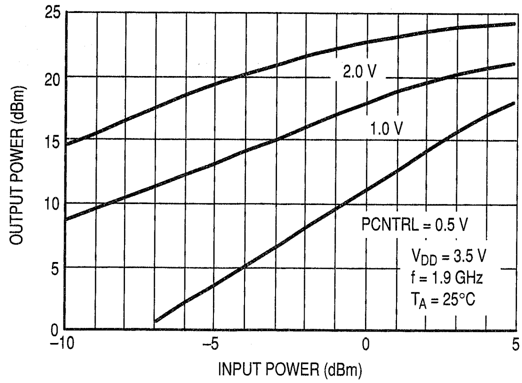


Figure 9. Output Power versus Input Power Without Internal Logic Translator

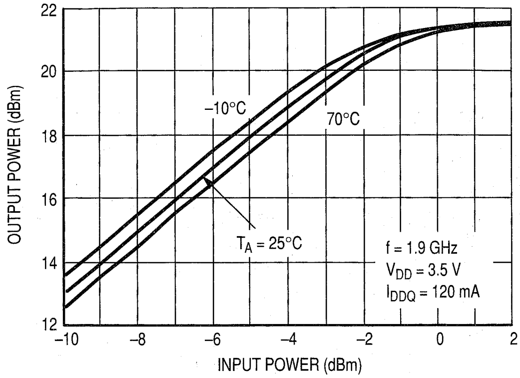


Figure 10. Output Power versus Input Power With Internal Logic Translator

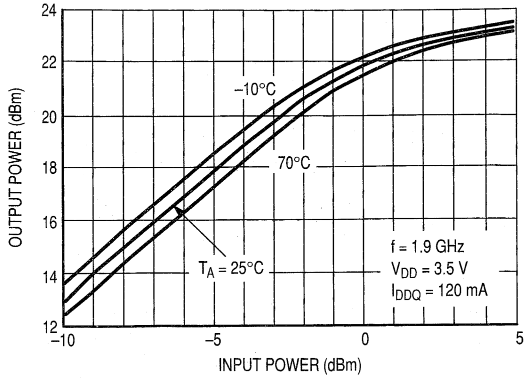


Figure 11. Output Power versus Input Power Without Internal Logic Translator

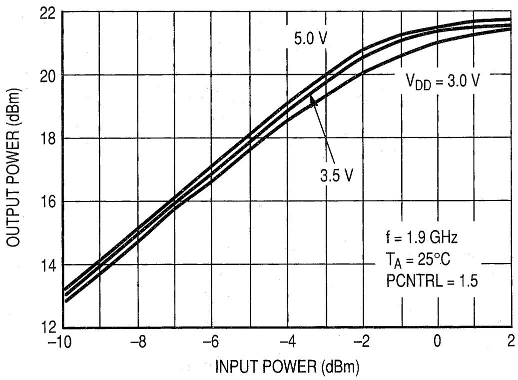


Figure 12. Output Power versus Input Power With Internal Logic Translator

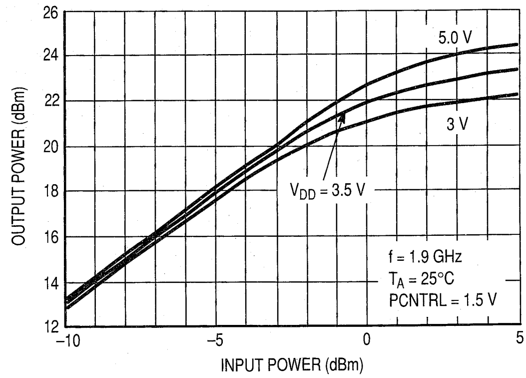


Figure 13. Output Power versus Input Power Without Internal Logic Translator

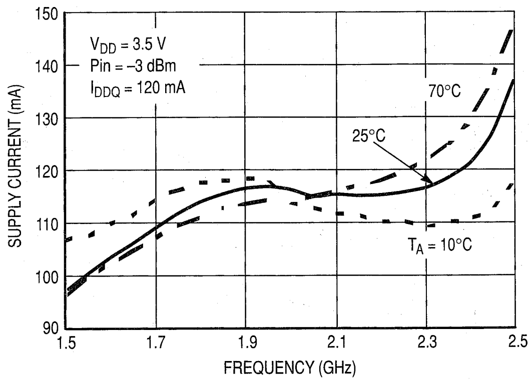


Figure 14. Supply Current versus Frequency With Internal Logic Translator

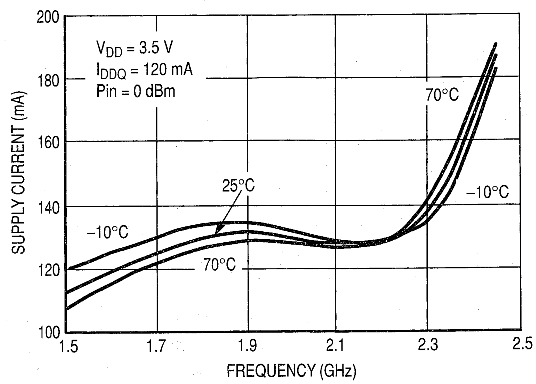


Figure 15. Supply Current versus Frequency Without Internal Logic Translator

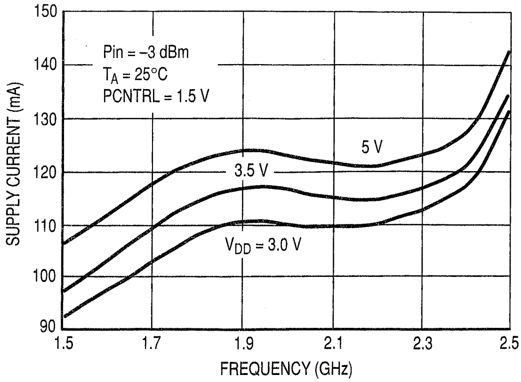


Figure 16. Supply Current versus Frequency With Internal Logic Translator

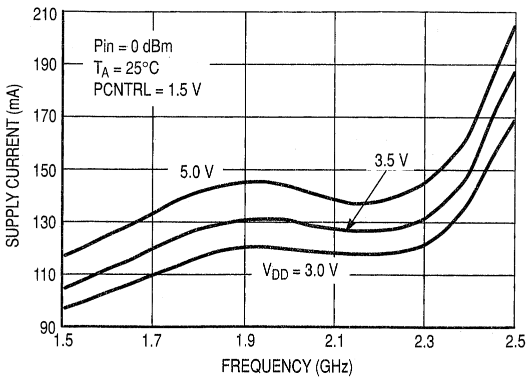


Figure 17. Supply Current versus Frequency Without Internal Logic Translator

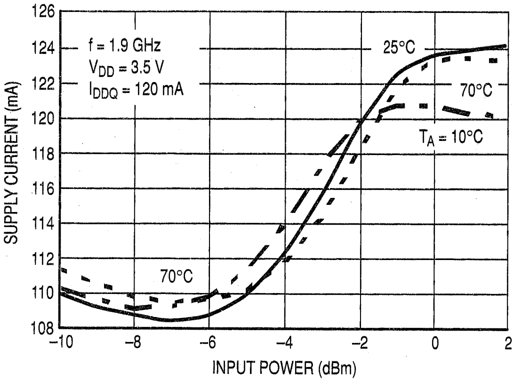


Figure 18. Supply Current versus Input Power With Internal Translator

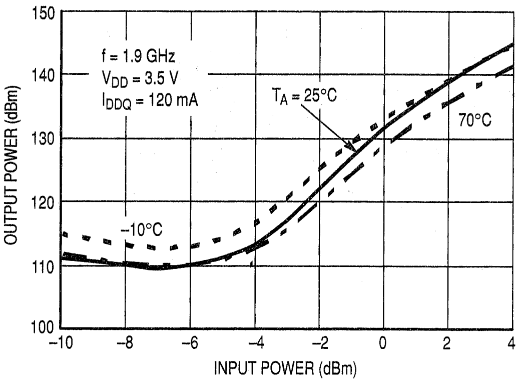


Figure 19. Supply Current versus Input Power Without Internal Translator

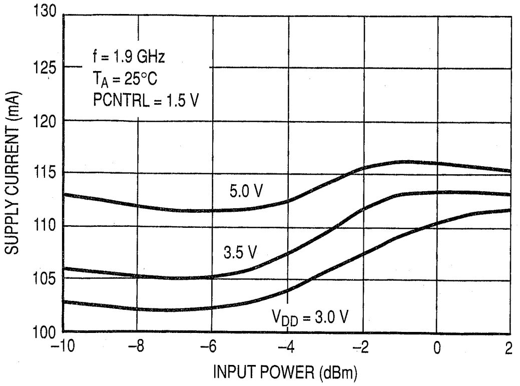


Figure 20. Supply Current versus Input Power With Internal Translator

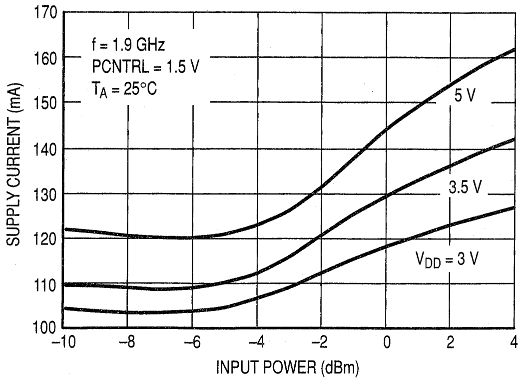


Figure 21. Supply Current versus Input Power Without Internal Logic Translator

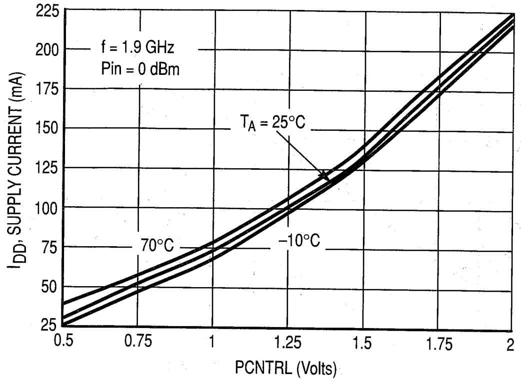


Figure 22. Supply Current versus PCNTRL Without Internal Logic Translator

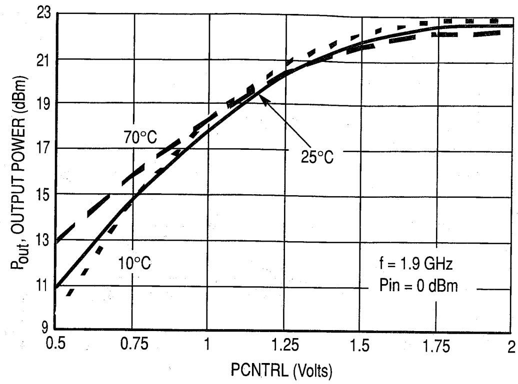


Figure 23. P_{out} versus PCNTRL Without Internal Logic Translator

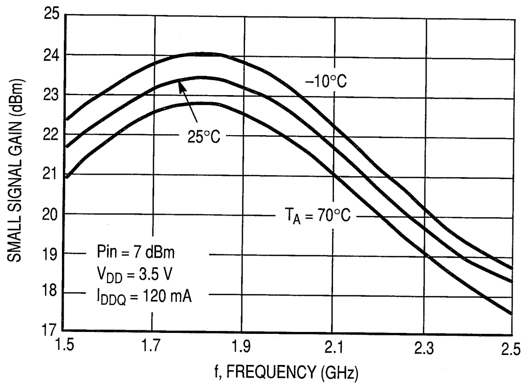


Figure 24. Small Signal Gain versus Frequency With Internal Logic Translator

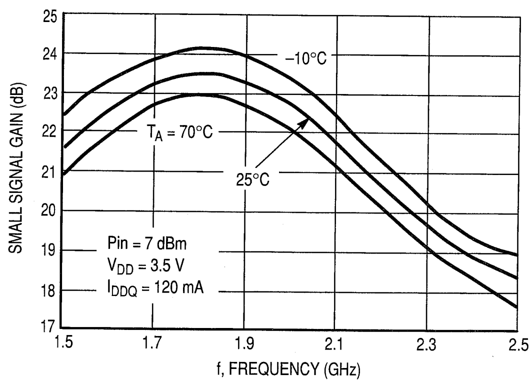


Figure 25. Small signal Gain versus Frequency Without Internal Logic Translator

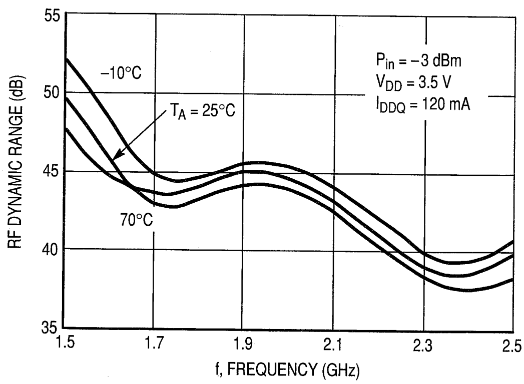


Figure 26. Dynamic Range versus Frequency With Internal Logic Translator

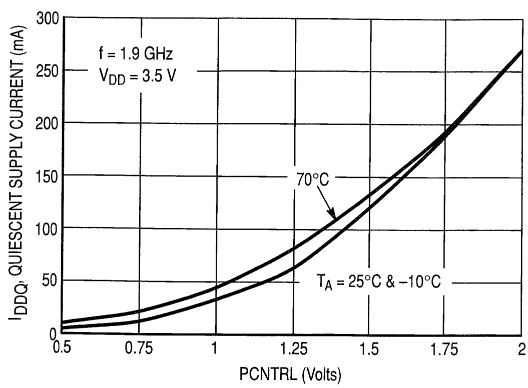


Figure 27. Quiescent Supply Current versus PCNTRL With Internal Logic Translator

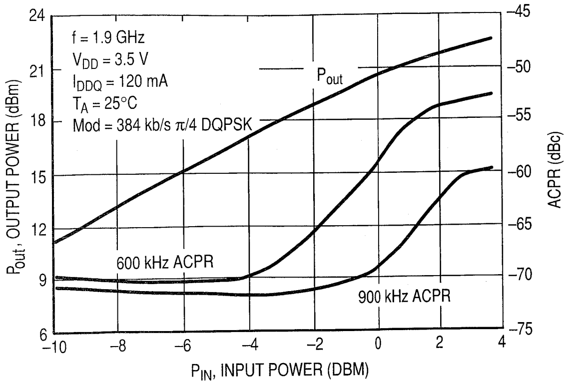


Figure 28. Output Power and Adjacent Channel Power Ratio versus Input Power Without Internal Logic Translator

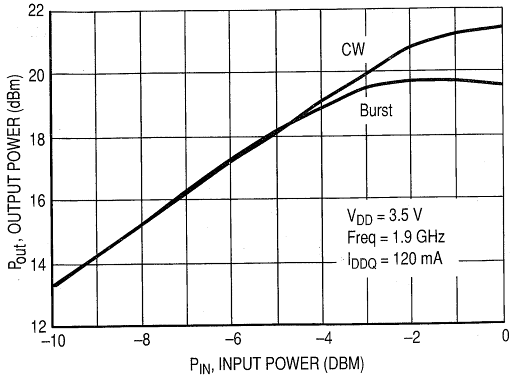


Figure 29. Continuous and Burst Mode Output Power versus Input Power With Internal Logic Translator

MRFIC1807

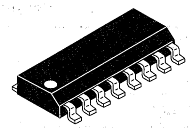
The MRFIC Line
1.8 GHz Power Amp/Switch

Designed primarily for use in DECT, Japan Personal Handy System (PHS) and other wireless Personal Communication Systems (PCS) applications. The MRFIC1807 includes a single–stage power amplifier and transmit/receive switch in a low–cost SOIC–16 package. The amplifier portion employs a depletion mode power GaAs MESFET and produces up to +27 dBm output with +19 dBm input. On–chip power control circuitry allows bias adjustment for optimum performance. The T/R switch is capable of handling up to +28 dBm through the transmit path without significant increase in insertion loss. The switch is controlled by CMOS logic level signals — no negative control voltage required. The MRFIC1807 is sized to be driven by the MRFIC1806 Driver/Ramp IC.

Together with the rest of the MRFIC1800 GaAs ICs, this family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable 1500–2200 MHz
- 8.0 dB Gain Including Switch
- +26 dBm Minimum Output Power at Antenna Port
- 1.0 dB Typ RX Path Insertion Loss
- Simple Off–Chip Matching for Maximum Flexibility
- 3.0 to 5.0 V Supply
- No Spurious Outputs for Load VSWR up to 8:1
- CMOS Level Switching Signal for T/R Switch
- Order MRFIC1807R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1807

1.8 GHz POWER AMPLIFIER AND TRANSMIT/RECEIVE SWITCH
GaAs MONOLITHIC INTEGRATED CIRCUIT



CASE 751B–05
(SO–16)

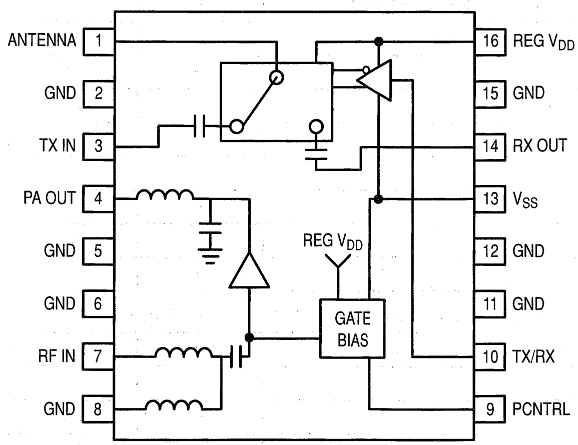


Figure 1. Pin Connection and Functional Block Diagram

REV 2

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise noted)

Rating	Symbol	Limit	Unit
PA Supply Voltage	V_{DD}	6.0	Vdc
Supply Voltage	REG V_{DD}	4.5	Vdc
Supply Voltage	V_{SS}	−4.0	Vdc
RF Input Power	P_{in}	+25	dBm
Switch Control Voltage	TX/RX	6.0	Vdc
PA Control Voltage	PCNTRL	3.0	Vdc
Ambient Operating Temperature	T_A	−10 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Thermal Resistance, Junction to Case	θ_{JC}	24	°C/W

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Input Frequency	f_{RF}	1.5 to 2.2	GHz
PA Supply Voltage	V_{DD}	3.0 to 5.0	Vdc
Supply Voltage	REG V_{DD}	2.9 to 3.1	Vdc
Supply Voltage	V_{SS}	−2.75 to −2.25	Vdc
RF Input Power	P_{IN}	+5.0 to +23	dBm
Switch Control Voltage, High (TX Mode)	TX/RX	2.8 to 3.5	Vdc
Switch Control Voltage, Low (RX Mode)	TX/RX	−0.2 to 0.2	Vdc
PA Control Voltage	PCNTRL	0.0 to 2.5	Vdc

ELECTRICAL CHARACTERISTICS (1)

Transmit Mode (V_{DD} = 3.5 V, REG V_{DD} = 3.0 V, T_A = 25°C, V_{SS} = −2.5 V, PCNTRL 0 V to 2.5 V, P_{IN} = 20 dBm @ 1.9 GHz, TX/RX = 3 V, P_{OUT} Measured at ANT Port)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain (P_{IN} = 0 dBm, PCNTRL set for I_{DDQ} = 180 mA)	7.0	8.0	—	dB
Output Power (PCNTRL adjusted for efficiency ≥ 35%)	26	26.8	—	dBm
Output 1.0 dB Compression (PCNTRL set for I_{DDQ} = 180 mA)	—	25	—	dBm
Harmonic Output (PCNTRL set for P_{OUT} = 26 dBm)	—	−40	—	dBc
Switch RX to TX Switching Time	—	0.1	—	μsec
TX/RX Control Input Current, Pin 10	—	0.2	—	mA
Drain Efficiency (P_{out} = 26 dBm) (2)	—	40	—	%
Supply Current, I_{SS}	—	0.8	1.2	mA
Supply Current, REG I_{DD}	—	0.8	1.2	mA
PCNTRL Control Input Current (Pin 9)	—	15	—	μA
Leakage Power at RX Port	—	−1	+ 6	dBm

Receive Mode (V_{DD} = 0 V, REG V_{DD} = 3.0 V, V_{SS} = −2.5 V, TX/RX = 0 V, T_A = 25°C, Freq = 1.9 GHz)

Characteristic	Min	Typ	Max	Unit
ANT to RX Insertion Loss	—	1.0	1.3	dB
Switch TX to RX Switching Time	—	1.0	—	μsec
Supply Current, REG I_{DD}	—	60	250	μA
Supply Current, I_{SS}	—	60	250	μA

NOTES:
1. Measured with circuit configuration shown in Figure 2.
2. Includes switch loss.

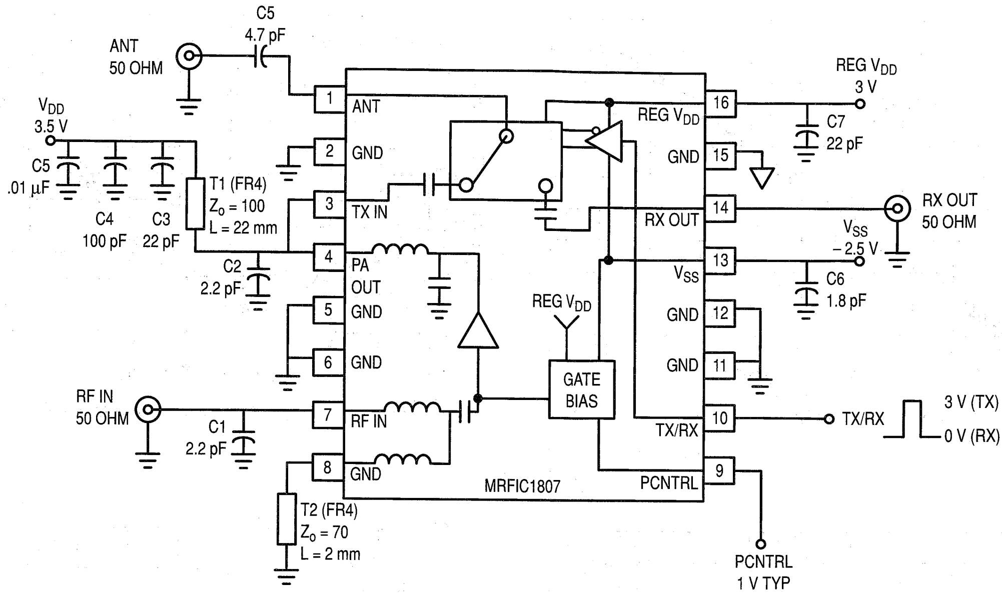


Figure 2. 1.9 GHz Applications Circuit Configuration

Table 1. Small Signal S–Parameters

(V_{DD} = 3.5 V, I_{DDQ} = 180 mA, T_A = 25°C, no input or output matching)

Freq (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
1.5	0.614	–171.5	2.203	82.6	0.104	74.5	0.741	175.4
1.6	0.695	175.7	1.871	71.7	0.110	69.2	0.746	171.5
1.7	0.747	167.3	1.647	63.4	0.108	64.0	0.745	167.4
1.8	0.777	160.3	1.473	56.2	0.106	58.7	0.746	163.0
1.9	0.799	154.2	1.341	49.2	0.120	54.0	0.753	158.9
2.0	0.814	148.3	1.230	43.0	0.118	49.6	0.758	154.8
2.1	0.826	142.5	1.128	36.8	0.114	45.2	0.764	150.6
2.2	0.835	137.0	1.041	31.2	0.120	40.6	0.767	146.7
2.3	0.842	131.4	0.959	26.4	0.127	37.0	0.780	143.4
2.4	0.856	126.6	0.895	21.1	0.124	33.8	0.796	139.8
2.5	0.870	121.7	0.840	16.0	0.126	30.4	0.808	136.4

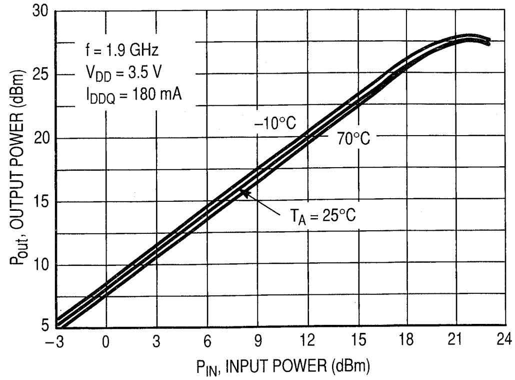


Figure 3. Output Power versus Input Power

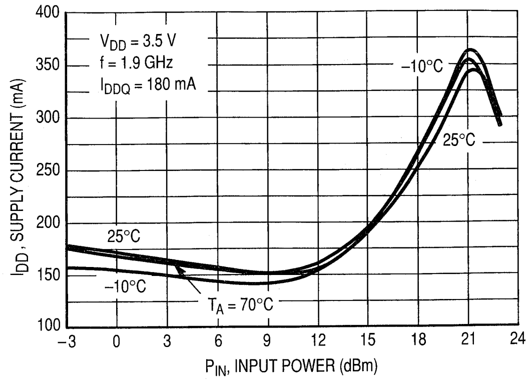


Figure 4. Supply Current versus Input Power

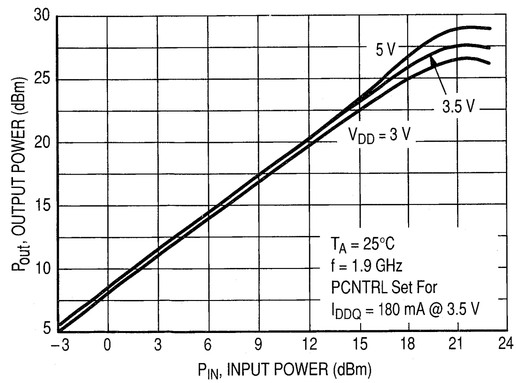


Figure 5. Output Power versus Input Power

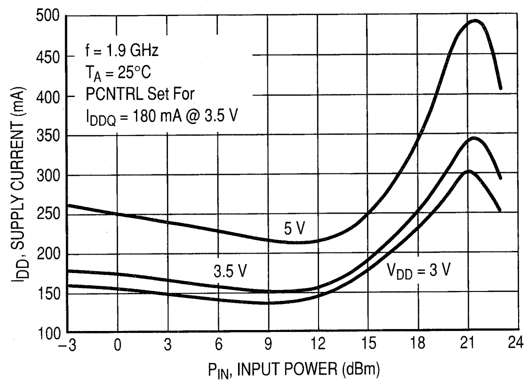


Figure 6. Supply Current versus Input Power

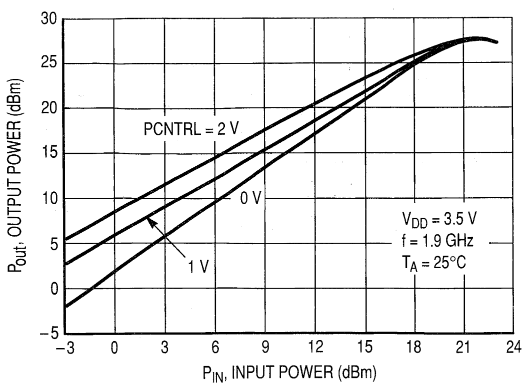


Figure 7. Output Power versus Input Power

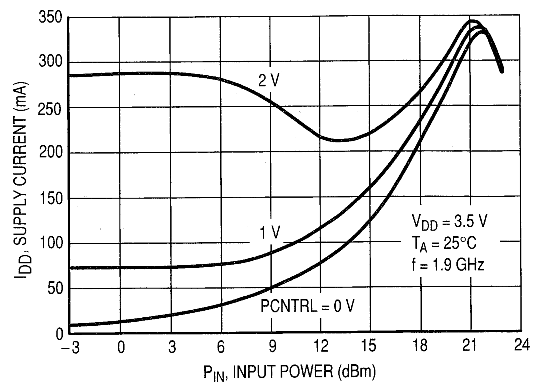


Figure 8. Supply Current versus Input Power

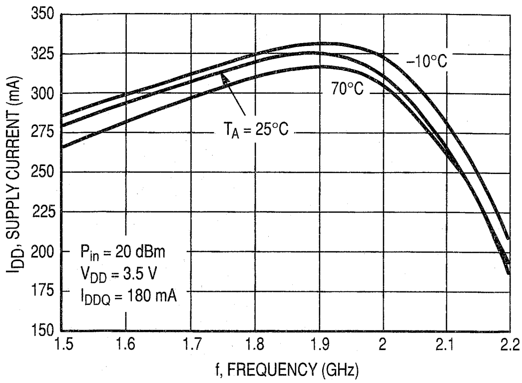


Figure 9. Supply Current versus Frequency

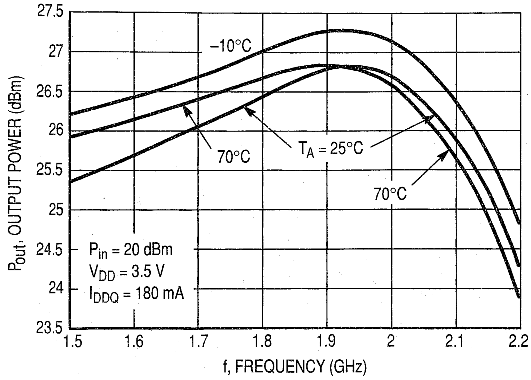


Figure 10. Output Power versus Frequency

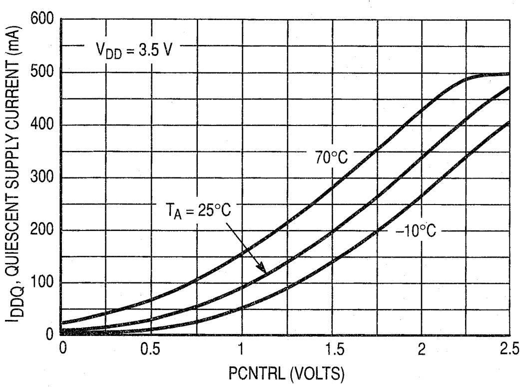


Figure 11. Quiescent Supply Current versus PCNTRL

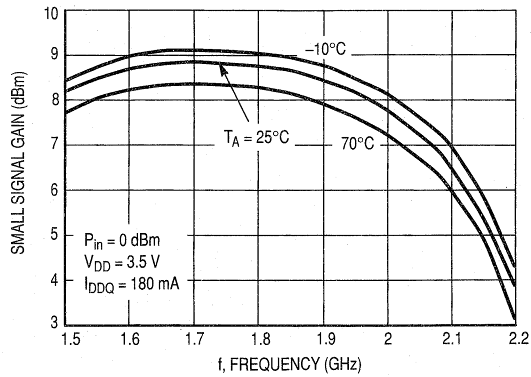


Figure 12. Small Signal Gain versus Frequency

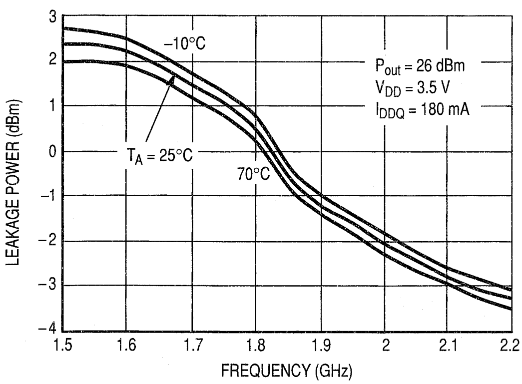


Figure 13. Leakage Power at RX Port in TX Mode versus Frequency

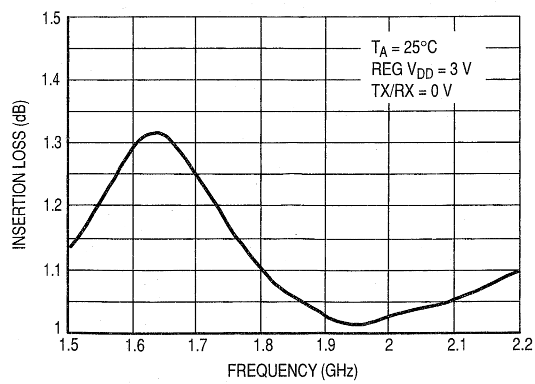


Figure 14. RX Path Insertion Loss in RX Mode versus Frequency

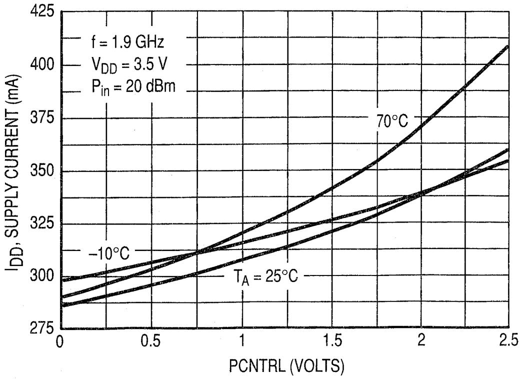


Figure 15. Supply Current versus PCNTRL

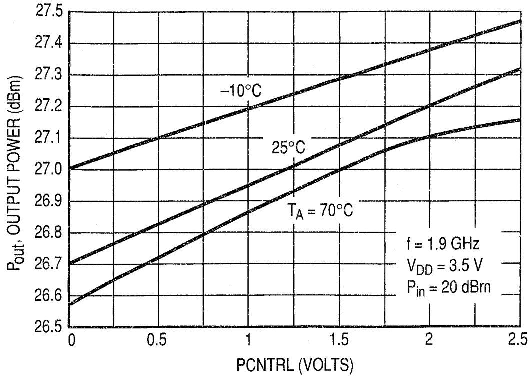


Figure 16. Output Power versus PCNTRL

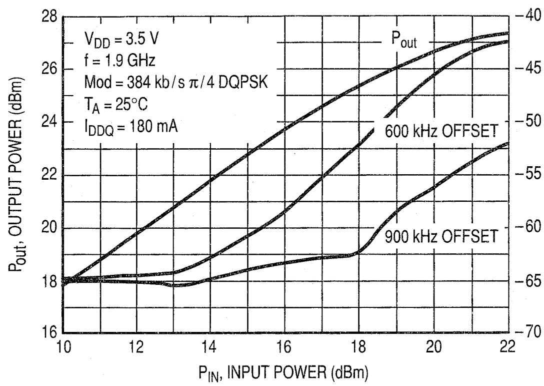


Figure 17. Output Power and Adjacent Channel Power Ratio versus Input Power

DESIGN AND APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC1807 is designed to operate with the MRFIC1806 Driver/Ramp IC in 1.9 GHz Personal Communication System (PCS) applications such as Europe's DECT and Japan's PHS. The design incorporates a depletion mode GaAs power MESFET with a high–power transmit/receive switch and associated bias circuitry in one low–cost SOIC–16 package.

The power MESFET is sized to produce at least 27 dBm saturated output power, including switch loss, from a 3.5 V supply, but the output power can be controlled using the PCNTRL input. This control voltage also allows setting of the quiescent current of the FET. PCNTRL can be set to give best efficiency or linearity for the particular system application. The TX/RX control pin allows fast switching of the T/R switch for TDMA applications. When switching from transmit to receive, the battery supply voltage should be removed from the PA (Pin 4), to avoid excessive current drain. This is usually accomplished using an external pass transistor controlled by the TX/RX signal. Alternatively, if PCNTRL is reduced to 0 V during RX mode, the bias current is reduced to nearly zero.

The Transmit/Receive switch is a reflective MESFET design which is optimized for low loss and power handling in transmit mode. The design can handle 28 dBm of transmit power without significant increase in insertion loss. A regulated 3.0 Volt supply is required at pin 16 for the T/R switch and the bias and control circuitry.

DECT APPLICATIONS

Figure 2 shows the component values for a DECT implementation of the MRFIC1807. For use in equipment designed for DECT, the power amplifier is operated close to saturation to improve device efficiency. Maximum power output at the antenna connector is 24 dBm during a burst. The constant envelope characteristics of the GMSK modulation allow non–linear amplification without spectral regrowth. The transmit signal must be shaped or "ramped" to meet system transmit turn on time requirements of 10 μsec minimum while not splattering into adjacent channels. A turn on time on greater than 2.0 μsec has been shown to give adequate adjacent channel power performance. Most DECT realizations have the modulation applied to the transmit VCO so the most straight forward way of implementing this ramping function is at the power amplifier. The MRFIC1806 Driver/Ramp IC has an on–chip ramping circuit specifically designed for DECT. When ramped in this manner, the MRFIC1806 will supply the appropriately ramped RF signal to the MRFIC1807 which only has to be turned on and off with TX/RX. Alternate off–chip ramping can be implemented either with external components or at baseband. Consult the MRFIC1806 datasheet for more information.

PHS APPLICATIONS

For Japan's Personal Handy System applications, the modulation is π/4 DQPSK. When amplified with a non–linear amplifier, the signal will regrow the sidebands which have been carefully filtered at baseband, resulting in adjacent channel interference. To avoid this spectral regrowth, the amplifier must be operated "backed off" from saturation. The amount of backoff required has been shown to be a function of amplifier saturated output capability and may be as high as 5.0 dB. The PHS specification calls for a maximum average power during a burst to be 19 dBm. This is consistent with 5.0 dB backoff from the DECT operating point so the same DECT operating condition could be used. Alternatively, PCNTRL can be adjusted for a lower bias point to improve efficiency or higher bias for better linearity. With π/4 DQPSK modulation, ramping can be accomplished in the encoder so no external ramp circuit is needed. See the MRFIC1806 data sheet for further details.

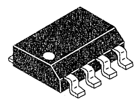
EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line
1.9 GHz GaAs Low Noise Amplifier

MRFIC1808

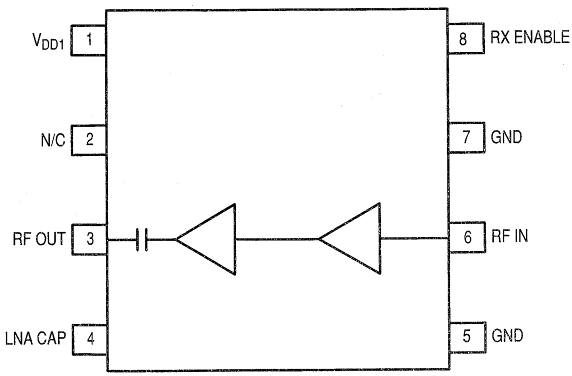
1.9 GHz GaAs LOW NOISE AMPLIFIER



CASE 751–05 (SO–8)

Designed primarily for use in wireless Personal Communication Systems (PCS) applications such as Digital European Cordless Telephone (DECT), Japan's Personal Handy System (PHS) and the emerging North American systems as a preamp for discrete or integrated downmixers. The MRFIC1808 is a two–stage low noise amplifier in a low–cost SO–8 package. The amplifier can be matched to optimize gain or noise figure with simple off–chip input matching. The design employs a novel stacked MESFET design which reuses bias current for the highest gain at minimal current. A CMOS compatible RECEIVE ENABLE pin allows for very low standby current while the system is in transmit mode.

- Usable Frequency Range = 1.7 to 2.1 GHz
- 19 dB Typ Gain
- 1.6 dB Typ Noise Figure
- Simple Off–chip Matching for Maximum Gain/Noise Figure Flexibility
- High Reverse Isolation = –34 dB (Typ)
- Low Power Consumption = 13 mW (Typ)
- Single Bias Supply = 2.7 to 4.5 Volts
- Low Standby Current = 8 µA (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1808R2 forTape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1808



Pin Connections and Functional Block Diagram

REV 1

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

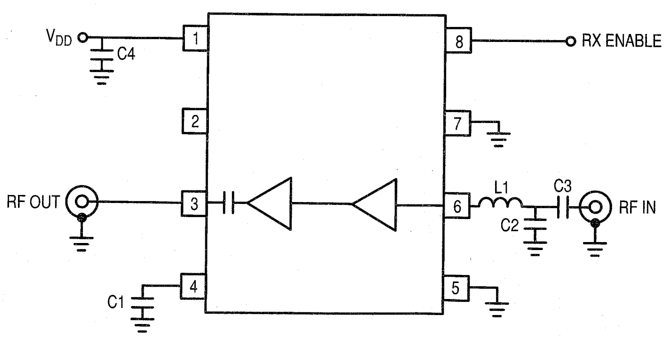
Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD}	5.5	Vdc
RF Input Power	P_{RF}	3	dBm
Enable Voltage	RX ENABLE	5.5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	1.7 to 2.1	GHz
Supply Voltage	V_{DD}	2.7 to 4.5	Vdc
RX Enable Voltage, ON	RX ENABLE	2.7 to V_{DD}	Vdc
RX Enable Voltage, OFF	RX ENABLE	0 to 0.2	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3 V, T_A = 25°C, RF = 1.9 GHz, RX ENABLE = 3 V, Tested in Circuit Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
RF Gain	16.0	19	—	dB
SSB Noise Figure	—	1.6	—	dB
RF Output 3rd Order Intercept Point	—	13	—	dBm
Output 1 dB Gain Compression	–3.0	1	—	dBm
Reverse Isolation (s_{12})	—	–34	—	dB
Input Return Loss	—	–12	—	dB
Output Return Loss	—	–15	—	dB
Supply Current RX Mode	—	4.2	6.5	mA
Supply Current Standby Mode (RX ENABLE = 0 V)	—	8	25	µA



C1 2 pF
C2 1.8 pF
C3, C4 22 pF
L1 5.6 nH

Figure 1. Applications Circuit Configuration

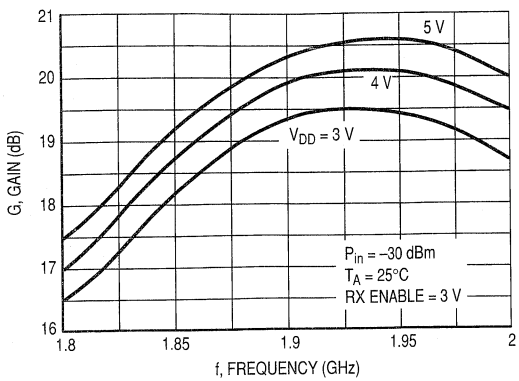


Figure 2. Gain versus Frequency

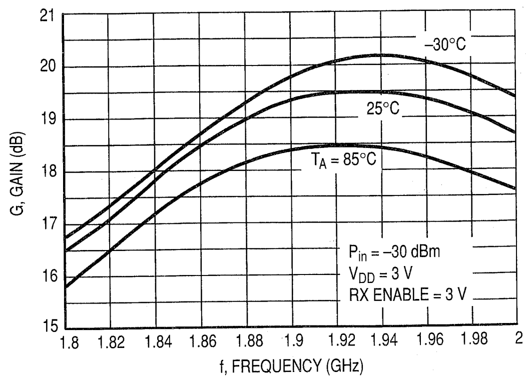


Figure 3. Gain versus Frequency

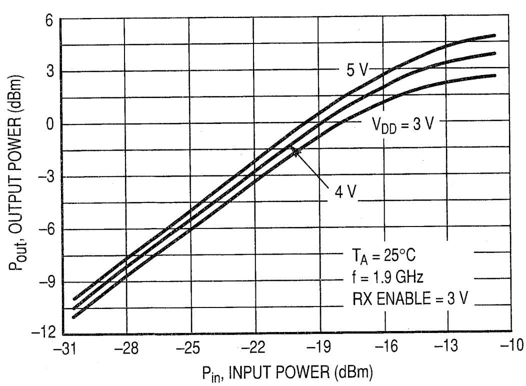


Figure 4. Output Power versus Input Power

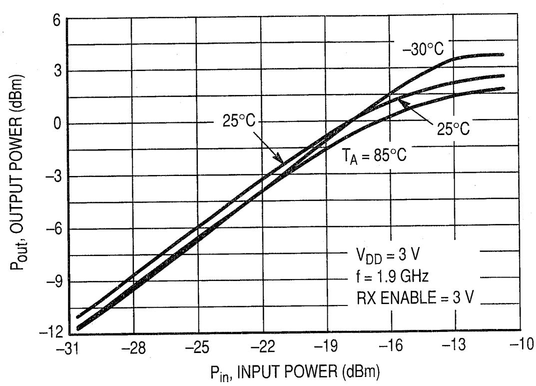


Figure 5. Output Power versus Input Power

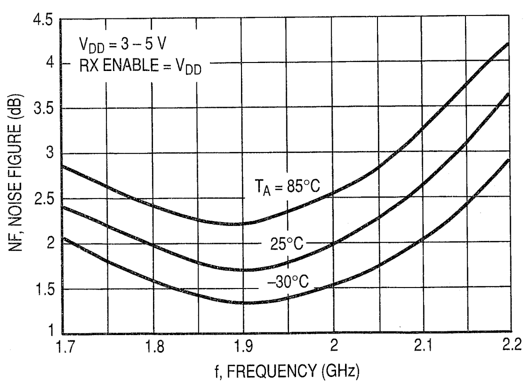


Figure 6. Noise Figure versus Frequency

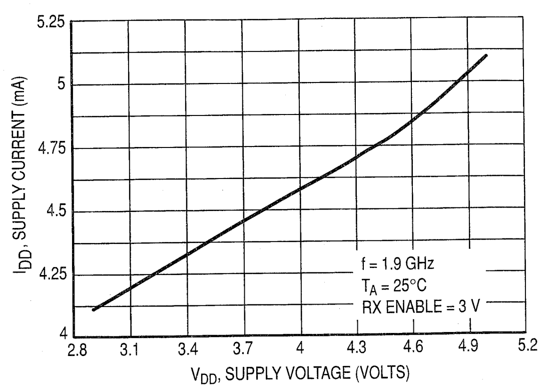


Figure 7. Supply Current versus Voltage

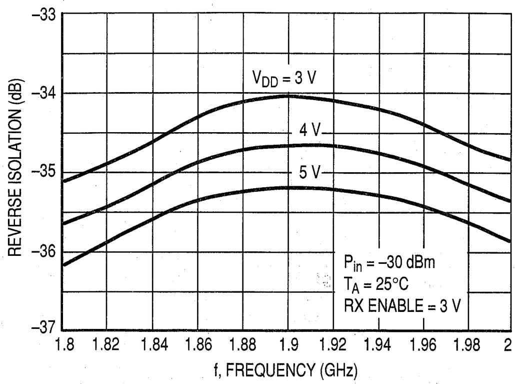


Figure 8. Reverse Isolation versus Frequency

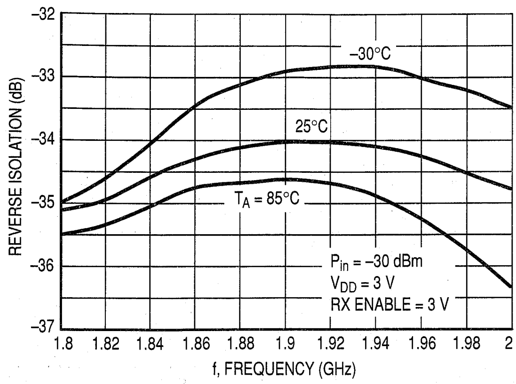


Figure 9. Reverse Isolation versus Frequency

Table 1. Scattering Parameters (V_{DD} = 3 Volts, T_A = 25°C, RX ENABLE = 3 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1500	0.859	–40.95	2.58	139.07	0.013	103.72	0.583	–79.05
1530	0.870	–41.50	2.79	134.79	0.013	105.63	0.530	–80.94
1560	0.866	–42.06	3.01	130.60	0.013	99.14	0.474	–82.85
1590	0.871	–42.92	3.18	125.11	0.014	98.40	0.412	–83.57
1620	0.873	–43.47	3.30	118.70	0.012	98.00	0.348	–83.11
1650	0.876	–43.60	3.37	112.85	0.012	97.39	0.285	–80.54
1680	0.877	–44.86	3.52	106.23	0.012	92.68	0.229	–73.01
1710	0.880	–45.35	3.68	100.77	0.011	93.90	0.186	–60.35
1740	0.876	–46.03	3.80	94.40	0.012	93.12	0.168	–40.74
1770	0.876	–47.22	3.87	88.75	0.011	88.55	0.182	–20.50
1800	0.885	–48.69	3.98	82.96	0.010	88.40	0.221	–6.82
1830	0.879	–48.55	3.98	76.83	0.010	89.46	0.272	–0.29
1860	0.881	–49.87	3.98	71.11	0.009	94.75	0.324	3.05
1890	0.885	–50.71	4.00	66.38	0.009	97.00	0.376	4.39
1920	0.878	–51.81	4.09	61.64	0.009	88.22	0.425	4.25
1950	0.873	–52.42	4.19	56.66	0.008	87.57	0.474	3.79
1980	0.860	–52.98	4.15	51.32	0.007	88.75	0.522	2.22
2010	0.866	–54.24	3.98	44.93	0.006	100.17	0.564	0.85
2040	0.859	–56.12	3.85	40.93	0.005	87.86	0.599	–0.87
2070	0.861	–56.69	3.89	37.99	0.004	99.30	0.634	–3.01
2100	0.850	–57.79	4.04	35.71	0.004	98.94	0.661	–4.59
2130	0.844	–58.53	4.18	31.89	0.004	118.15	0.691	–6.96
2160	0.834	–60.21	4.21	26.88	0.003	137.84	0.714	–8.94
2190	0.834	–61.26	4.15	22.38	0.003	141.53	0.734	–11.49
2220	0.830	–62.53	4.17	18.75	0.004	–164.13	0.760	–13.48
2250	0.817	–63.84	4.22	14.85	0.004	–172.30	0.776	–15.27
2280	0.812	–64.69	4.21	9.17	0.005	–165.76	0.787	–17.20
2310	0.811	–66.64	4.14	4.09	0.006	–148.57	0.805	–19.42
2340	0.800	–67.89	3.95	1.20	0.007	–153.96	0.808	–21.63
2370	0.794	–69.40	3.83	0.29	0.008	–144.49	0.819	–23.38
2400	0.791	–72.05	3.88	0.33	0.009	–133.12	0.822	–26.10
2430	0.784	–73.59	4.09	–2.06	0.012	–138.06	0.826	–28.21
2460	0.774	–75.60	4.30	–8.63	0.014	–138.55	0.824	–30.43
2490	0.769	–78.81	4.33	–16.94	0.015	–146.05	0.821	–32.72
2520	0.751	–80.46	4.31	–23.37	0.018	–148.25	0.815	–35.42
2550	0.737	–83.20	4.23	–27.46	0.021	–149.08	0.798	–37.56
2580	0.707	–86.12	4.08	–32.67	0.024	–155.44	0.767	–39.31

Table 2. Scattering Parameters (V_{DD} = 4 Volts, T_A = 25°C, RX ENABLE = 3 Volts, 50 Ω System)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\lvert S_{11}\rvert$	∠ φ	$\lvert S_{21}\rvert$	∠ φ	$\lvert S_{12}\rvert$	∠ φ	$\lvert S_{22}\rvert$	∠ φ
1500	0.849	–40.63	2.83	138.31	0.013	101.12	0.592	–78.76
1530	0.854	–41.00	3.07	134.02	0.012	99.54	0.537	–80.92
1560	0.852	–41.65	3.30	129.90	0.012	97.89	0.482	–82.91
1590	0.855	–42.76	3.50	124.44	0.013	103.09	0.421	–84.04
1620	0.861	–43.15	3.63	118.09	0.013	104.42	0.357	–84.20
1650	0.862	–43.22	3.73	112.01	0.012	95.75	0.293	–82.14
1680	0.861	–44.49	3.89	106.04	0.012	95.43	0.233	–75.91
1710	0.861	–44.93	4.07	100.17	0.011	99.73	0.187	–63.54
1740	0.869	–45.60	4.19	94.14	0.011	94.00	0.164	–43.94
1770	0.864	–46.48	4.30	87.75	0.011	95.67	0.173	–22.19
1800	0.870	–48.17	4.41	82.13	0.011	88.56	0.210	–7.42
1830	0.860	–48.09	4.41	75.97	0.010	88.92	0.258	0.31
1860	0.866	–49.28	4.41	70.37	0.010	96.31	0.313	3.91
1890	0.870	–50.19	4.46	65.24	0.009	93.39	0.367	5.28
1920	0.861	–50.75	4.54	60.65	0.008	90.74	0.417	5.60
1950	0.852	–51.77	4.66	55.96	0.008	89.58	0.468	4.75
1980	0.849	–52.40	4.56	50.46	0.007	84.42	0.518	3.22
2010	0.847	–53.50	4.40	44.25	0.006	94.48	0.561	1.68
2040	0.847	–55.19	4.25	39.96	0.005	88.62	0.597	–0.03
2070	0.847	–55.75	4.29	37.08	0.004	109.85	0.633	–2.25
2100	0.842	–56.92	4.47	34.67	0.005	103.26	0.664	–3.78
2130	0.830	–57.36	4.61	30.80	0.004	125.77	0.694	–6.23
2160	0.823	–59.26	4.66	26.03	0.004	122.00	0.717	–8.30
2190	0.820	–60.09	4.57	21.27	0.004	152.31	0.742	–10.87
2220	0.820	–61.37	4.57	17.70	0.002	160.02	0.762	–13.04
2250	0.812	–63.01	4.63	13.81	0.003	176.88	0.778	–14.80
2280	0.801	–63.88	4.61	8.47	0.004	–165.16	0.792	–17.00
2310	0.802	–65.68	4.54	2.90	0.005	–156.21	0.807	–19.20
2340	0.789	–67.07	4.32	0.38	0.007	–141.83	0.815	–21.21
2370	0.781	–68.28	4.21	–1.24	0.008	–144.89	0.821	–23.34
2400	0.775	–70.61	4.23	–0.61	0.010	–143.18	0.826	–25.75
2430	0.771	–72.01	4.47	–2.85	0.012	–140.04	0.829	–28.07
2460	0.764	–74.59	4.70	–9.44	0.012	–144.28	0.829	–30.56
2490	0.759	–77.25	4.72	–17.93	0.015	–149.63	0.826	–32.63
2520	0.743	–78.88	4.69	–24.28	0.017	–148.60	0.820	–35.12
2550	0.730	–81.98	4.58	–28.44	0.021	–148.70	0.802	–37.38
2580	0.700	–85.55	4.45	–33.64	0.022	–157.99	0.772	–39.29

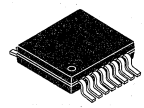
Table 3. Scattering Parameters (V_{DD} = 5 Volts, T_A = 25°C, RX ENABLE = 3 Volts, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1500	0.830	–40.58	3.12	137.17	0.011	98.73	0.600	–78.51
1530	0.839	–41.24	3.39	132.69	0.011	101.93	0.548	–80.73
1560	0.836	–41.75	3.64	128.74	0.012	96.66	0.492	–82.85
1590	0.842	–42.35	3.85	123.33	0.013	99.33	0.433	–84.11
1620	0.848	–42.88	4.02	116.83	0.012	101.06	0.370	–84.63
1650	0.843	–43.41	4.11	110.95	0.012	95.15	0.306	–82.83
1680	0.844	–44.37	4.30	104.87	0.012	96.02	0.243	–77.32
1710	0.849	–45.07	4.49	99.42	0.012	96.86	0.193	–66.79
1740	0.852	–45.25	4.64	93.23	0.010	99.66	0.163	–48.45
1770	0.848	–46.18	4.75	87.02	0.012	88.90	0.164	–26.11
1800	0.856	–47.76	4.88	81.25	0.011	93.18	0.200	–9.04
1830	0.850	–47.99	4.87	75.09	0.010	90.25	0.247	–0.08
1860	0.850	–48.93	4.90	69.14	0.009	88.62	0.301	3.73
1890	0.849	–49.88	4.96	64.08	0.009	93.94	0.355	5.69
1920	0.846	–50.72	5.02	59.31	0.009	93.67	0.407	6.01
1950	0.837	–51.45	5.15	54.55	0.007	90.89	0.459	5.70
1980	0.830	–52.33	5.07	48.85	0.008	98.84	0.511	4.17
2010	0.831	–52.97	4.89	42.81	0.006	90.07	0.557	2.40
2040	0.831	–55.08	4.72	38.38	0.004	100.73	0.593	0.51
2070	0.829	–55.58	4.74	35.43	0.005	96.39	0.631	–1.55
2100	0.823	–56.53	4.95	32.95	0.004	122.68	0.661	–3.57
2130	0.815	–57.23	5.10	29.26	0.004	112.15	0.691	–5.96
2160	0.805	–58.81	5.14	24.21	0.004	132.80	0.718	–7.96
2190	0.802	–59.57	5.04	19.45	0.004	136.20	0.739	–10.56
2220	0.801	–60.70	5.05	15.80	0.003	178.25	0.762	–12.60
2250	0.791	–62.24	5.11	12.01	0.004	170.40	0.780	–14.52
2280	0.781	–62.95	5.08	6.42	0.005	–172.19	0.793	–16.63
2310	0.786	–64.98	4.97	1.09	0.006	–169.11	0.811	–18.96
2340	0.773	–66.05	4.74	–1.76	0.006	–150.31	0.818	–21.10
2370	0.766	–67.23	4.60	–2.91	0.008	–143.53	0.821	–23.29
2400	0.763	–69.83	4.64	–2.54	0.009	–146.46	0.827	–25.81
2430	0.757	–71.49	4.89	–4.89	0.011	–141.36	0.832	–27.88
2460	0.750	–73.61	5.12	–11.49	0.012	–147.16	0.832	–30.37
2490	0.742	–76.17	5.17	–19.88	0.014	–145.27	0.827	–32.68
2520	0.726	–78.01	5.10	–26.09	0.016	–145.14	0.820	–35.26
2550	0.712	–81.26	5.01	–30.13	0.018	–150.98	0.805	–37.48
2580	0.686	–84.54	4.81	–35.31	0.022	–155.55	0.771	–39.32

The MRFIC Line
1.9 GHz GaAs Upconverter

MRFIC1813

1.9 GHz UPMIXER AND EXCITER AMPLIFIER

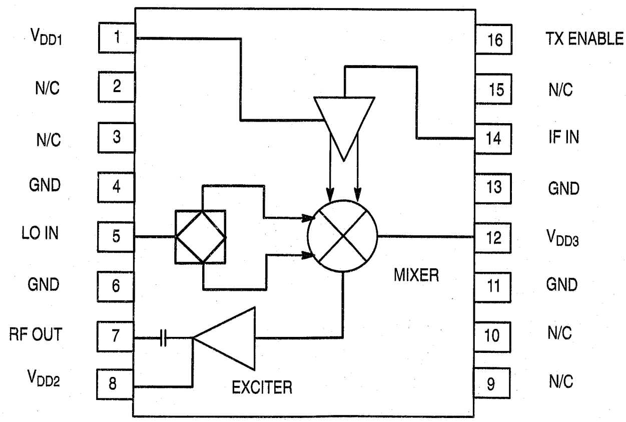


CASE 948C–03 (TSSOP–16)

Designed primarily for use in wireless Personal Communication Systems (PCS) applications such as Digital European Cordless Telephone (DECT), Japan's Personal Handy System (PHS) and the emerging North American systems. The MRFIC1813 is also applicable to 2.4 GHz ISM equipment. The device combines a balanced upmixer and a transmit exciter amplifier in a low-cost TSSOP–16 package. Minimal off-chip matching is required while allowing for maximum flexibility and efficiency. The mixer is optimized for low–side injection and provides more than 12 dB of conversion gain with over 0 dBm output at 1 dB gain compression. Image filtering is implemented off-chip to allow maximum flexibility. A CMOS compatible ENABLE pin allows standby operation where the current drain is less than 250 μA.

Together with other devices from the MRFIC180X or the MRFIC240X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone or 2.4 GHz ISM band equipment.

- Usable Frequency Range = 1.7 to 2.5 GHz
- 15 dB Typ IF to RF Conversion Gain
- 3 dBm Power Output Typ, 0 dBm Minimum at 1 dB Gain Compression
- Simple Off-chip Matching for Maximum Flexibility
- Low Power Consumption = 75 mW (Typ)
- Single Bias Supply = 2.7 to 4.5 Volts
- Low LO Power Requirement = – 5 dBm (Typ)
- Low Cost Surface Mount Plastic Package
- Order MRFIC1813R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1813



Pin Connections and Functional Block Diagram

REV 2

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

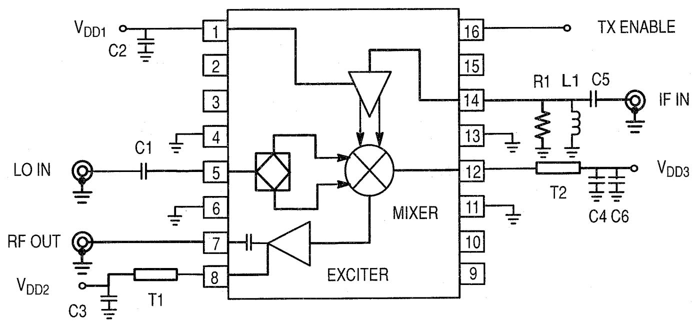
Ratings	Symbol	Limit	Unit
Supply Voltage	V_{DD1}, V_{DD2}, V_{DD3}	5.5	Vdc
IF Input Power	P_{IF}	3	dBm
LO Input Power	P_{LO}	3	dBm
Enable Voltage	TX ENABLE	5.5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Output Frequency	f_{RF}	1.7 to 2.5	GHz
LO Input Frequency	f_{LO}	1.5 to 2.4	GHz
IF Input Frequency	f_{IF}	70 to 350	MHz
Supply Voltage	V_{DD}	2.7 to 4.5	Vdc
TX Enable Voltage, ON	TX ENABLE	2.7 to V_{DD}	Vdc
TX Enable Voltage, OFF	TX ENABLE	0 to 0.2	Vdc

ELECTRICAL CHARACTERISTICS ($V_{DD1,2,3}$, TX ENABLE= 3 V, T_A = 25°C, f_{LO} = 1.65 GHz @ – 5 dBm, f_{IF} = 250 MHz @ –15 dBm)

Characteristic	Min	Typ	Max	Unit
IF to RF Small Signal Conversion Gain (P_{RF} = –35 dBm)	12	15	—	dB
RF Output 1 dB Gain Compression	0	3	—	dBm
RF Output 3rd Order Intercept	—	11	—	dBm
LO Feedthrough to RF Port	—	–15	–10	dBm
Noise Figure	—	11	—	dB
Lower Sideband Output Power at RF Port	—	–10	–6	dBm
Supply Current TX Mode	—	25	35	mA
Supply Current Standby Mode (TX ENABLE = 0 V, LO Off)	—	100	250	µA
TX Enable Current	—	3	—	µA



C1, C2, C3, C4   15 pF
C6   1 µF
R1   300 Ω
T1, T2   MICROSTRIP, Z_0 = 73 Ω, θ = 29° @ 1.9 GHz
BOARD MATERIAL – GLASS/EPOXY, ε_r = 4.45,
DIELECTRIC THICKNESS = 0.018 INCH

IF Frequency	L1	C5
110 MHz	180 nH	12 pF
250 MHz	68 nH	5.6 pF
350 MHz	39 nH	3.9 pF

Figure 1. Applications Circuit Configuration

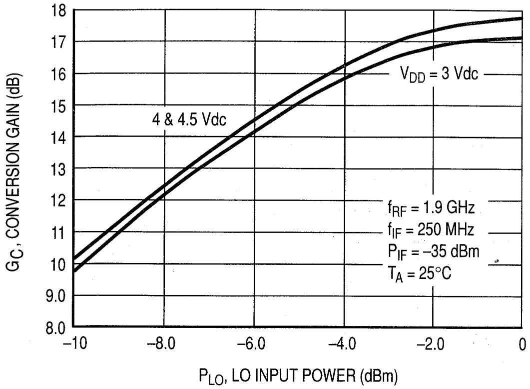


Figure 2. Conversion Gain versus LO Power

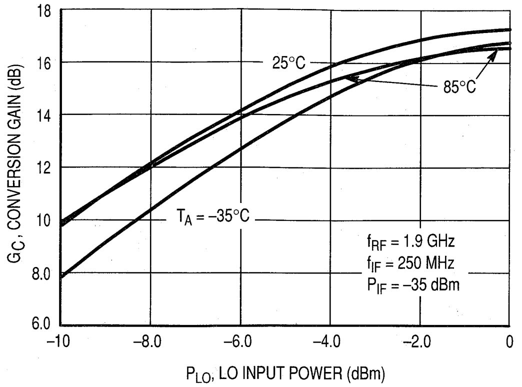


Figure 3. Conversion Gain versus LO Power

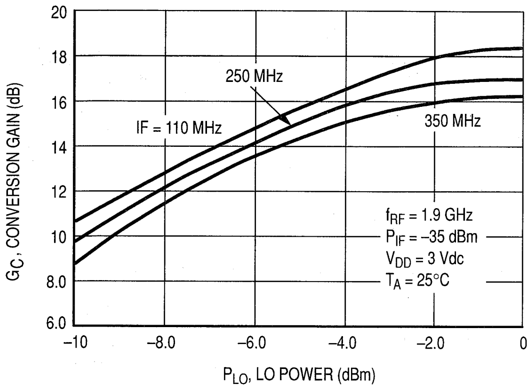


Figure 4. Conversion Gain versus LO Power

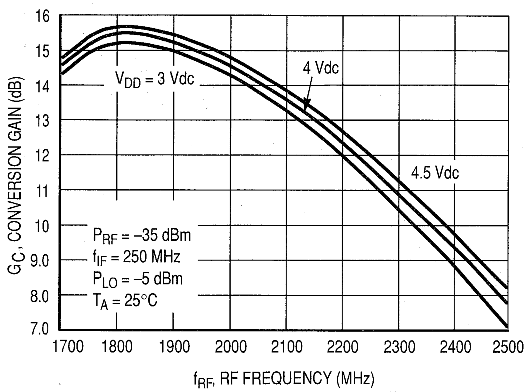


Figure 5. Conversion Gain versus RF Frequency

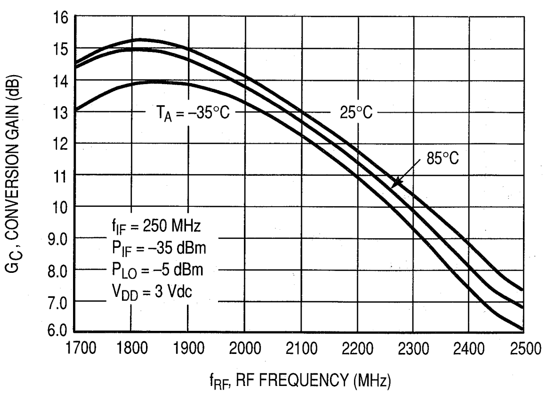


Figure 6. Conversion Gain versus RF Frequency

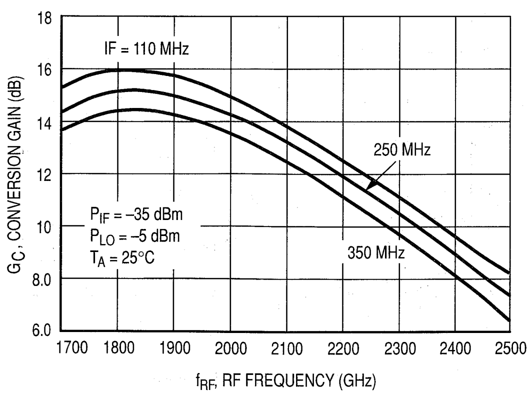


Figure 7. Conversion Gain versus RF Frequency

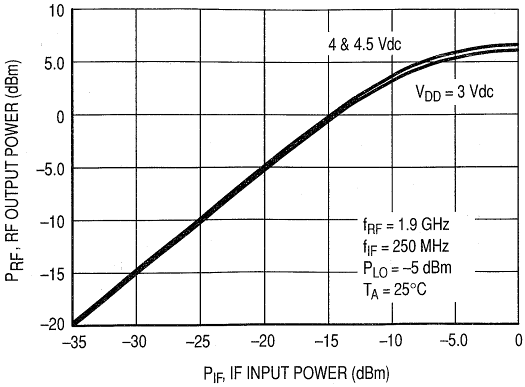


Figure 8. RF Output versus Input Power

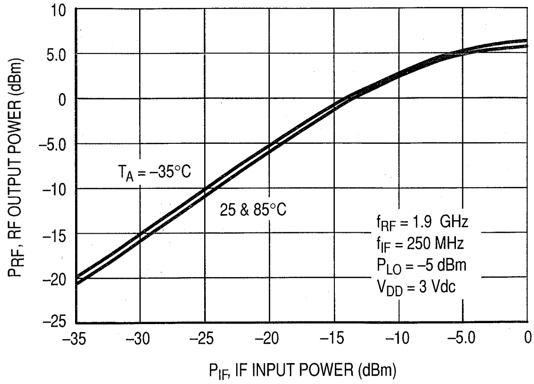


Figure 9. RF Output Power versus IF Input Power

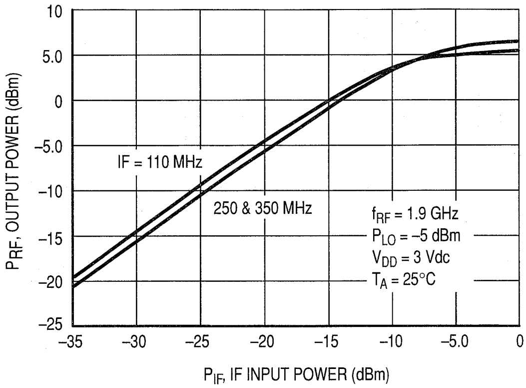


Figure 10. RF Output versus IF Input Power

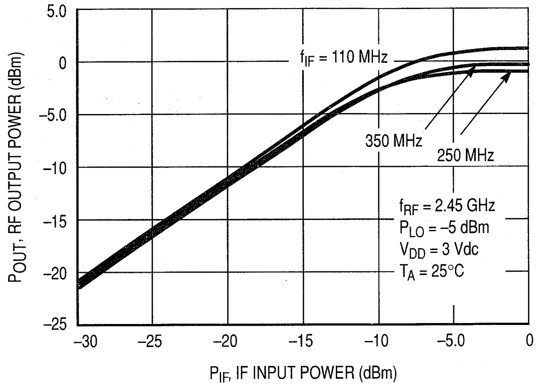


Figure 11. Output Power versus IF Input Power

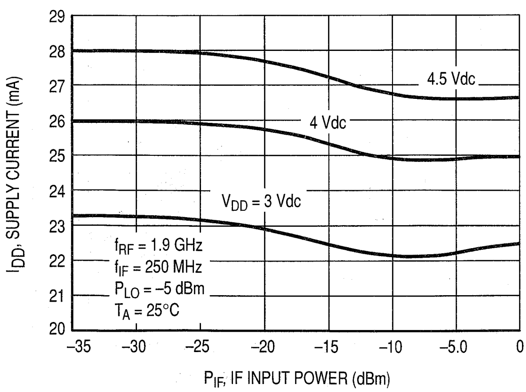


Figure 12. Supply Current versus IF Input Power

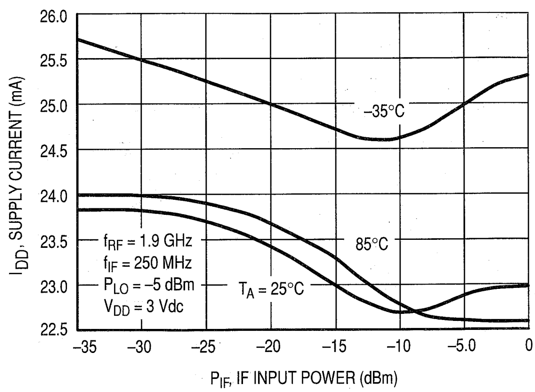


Figure 13. Supply Current versus IF Input Power

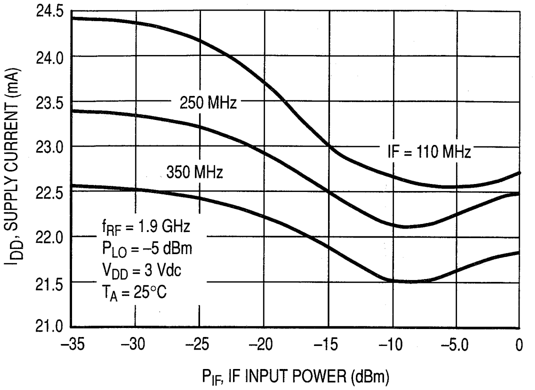


Figure 14. Supply Current versus IF Input Power

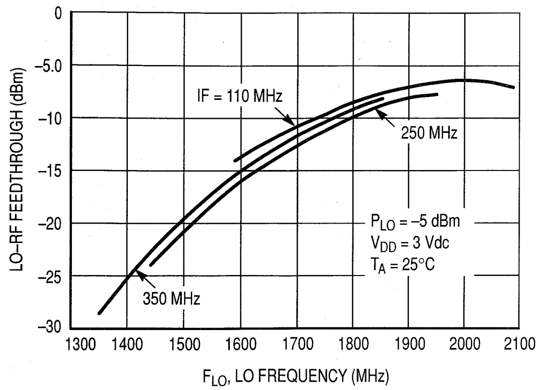


Figure 15. LO to RF Feedthrough versus LO Frequency

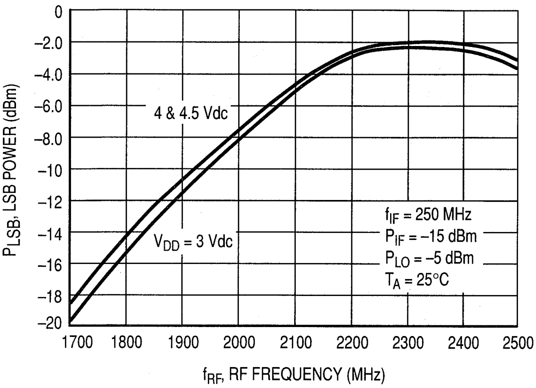


Figure 16. Lower Side Band Power versus RF Frequency

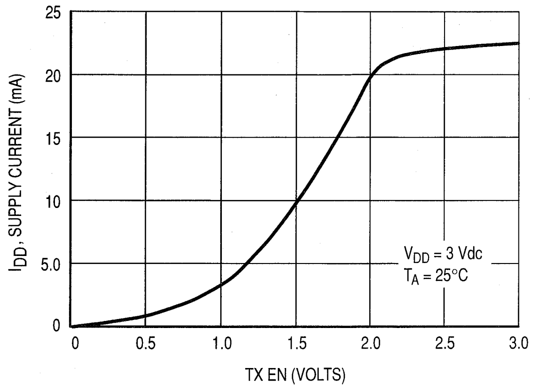


Figure 17. Supply Current versus Transmit Enable Voltage

f	IF Input		LO Input		RF Output (1)	
(MHz)	R	jX	R	jX	R	jX
70	8.3	–452.4				
100	7.3	–318.5				
150	7.1	–211.3				
200	6.6	–156.4				
250	6.5	–123.1				
300	6.1	–100.7				
350	5.7	–84.2				
1100			62.5	3.1		
1200			58.1	4.3		
1300			53.7	4.7		
1400			50.2	4.2		
1500			47.3	3.9		
1600			44.4	3.2		
1700			42.0	1.6	30.4	33.6
1800			40.6	0.5	42.6	16.9
1900			39.6	–0.7	49.1	2.3
2000			38.7	–2.2	40.6	14.2
2100			38.2	–3.6	33.8	17.7
2200			38.4	–5.1	33.3	15.7
2300			38.9	–6.5	32.9	13.7
2400			39.5	–7.8	29.6	13.2
2500					27.4	11.9

(1) Includes T1 shown in Figure 1.

Table 1. Port Impedances versus Frequency
(V_{D1}, V_{D2}, V_{D3}, TX EN = 3 Vdc)

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The MRFIC1813 combines a single–balanced MESFET mixer with an exciter amplifier. It is usable for transmit frequencies from 1.7 to 2.5 GHz and IF frequencies from 70 to 350 MHz. The design is optimized for low–side local oscillator injection in hetrodyne transmit applications.

Minimal off–chip matching is required while allowing for flexibility and performance optimization. An active balun is employed at the IF port which gives good balance down to at least 70 MHz. A passive splitter is used at the LO input to complete the single–balanced configuration.

CIRCUIT CONSIDERATIONS

Figure 1 shows the application circuit used to gather the data presented in the characterization curves. As shown in Table 1, the IF port impedance is very high. Three hundred ohms was chosen for R1 to shunt the IF port as a compromise of gain and bandwidth. A 50 Ω resistor can be used and L1 and C5 eliminated to provide a broadband match. The conversion gain is reduced to about 8 dB. Microstrip inductors T1 and T2 combine with inductance internal to the device to form RF chokes. Some tuning of the RF output can be achieved with T1.

As with all RF devices, circuit layout is important. Controlled impedance lines should be used for all RF and IF interconnects. As shown in Figure 1, power supply by–passing should be used to avoid device instability. Ground vias should be included near all ground connections indicated in the schematic. Off–chip components should be mounted as close to the IC leads as possible.

EVALUATION BOARDS

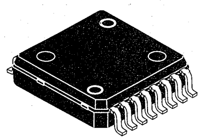
Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” to the device type. For a complete list of currently available boards and one in development for newly introduced products, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line

1800 MHz GaAs Integrated Power Amplifier

MRFIC1818

**1700–1900 MHz MMIC
DCS1800/PCS1900
INTEGRATED POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT**



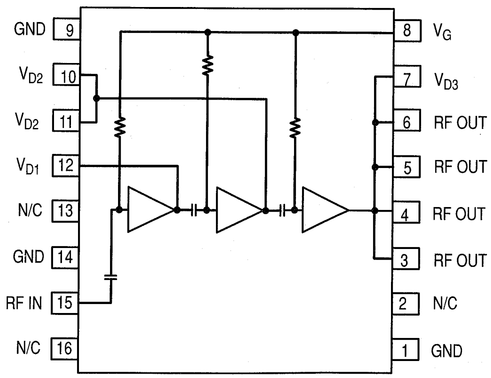
**CASE 978–02
(PFP–16)**

Designed specifically for application in Pan European digital 1.0 watt DCS1800 handheld radios, the MRFIC1818 is specified for 33 dBm output power with power gain over 30 dB from a 4.8 volt supply. With minor tuning changes, the MRFIC1818 can be used for PCS1900 as well as PCS CDMA. To achieve this superior performance, Motorola's planar GaAs MESFET process is employed. The device is packaged in the PFP–16 Power Flat Package which gives excellent thermal and electrical performance through a solderable backside contact while allowing the convenience and cost benefits of reflow soldering.

- Minimum Output Power Capabilities
  33 dBm @ 4.8 Volts
  32 dBm @ 4.0 Volts
- Specified 4.8 Volt Characteristics
  RF Input Power = 3.0 dBm
  RF Output Power = 33 dBm
  Minimum PAE = 35%
- Low Current required from Negative Supply – 2 mA max
- Guaranteed Stability and Ruggedness
- Order MRFIC1818R2 for Tape and Reel.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1818

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Z_O = 50 Ω, unless otherwise noted)

Rating	Symbol	Value	Unit
DC Positive Supply Voltage	$V_{D1, 2, 3}$	7.5	Vdc
DC Negative Supply Voltage	V_{SS}	–5	Vdc
RF Input Power	P_{in}	10	dBm
RF Output Power	P_{out}	36	dBm
Operating Case Temperature Range	T_C	–35 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W



Pin Connections and Functional Block Diagram

REV 2

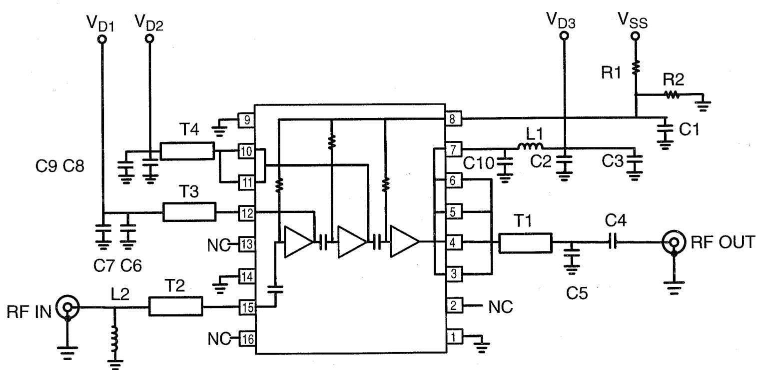
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{D1,2,3}$	2.7 to 6	Vdc
Gate Voltage	V_{SS}	–3.5 to –4.5	Vdc
RF Frequency Range	f_{RF}	1700 to 1900	MHz
RF Input Power	P_{RF}	0 to 6	dBm

ELECTRICAL CHARACTERISTICS ($V_{D1,2,3}$ = 4.8 V, V_{SS} = –4 V, P_{in} = 3 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted. Measured in Reference Circuit Shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Frequency Range	1710	—	1785	MHz
Output Power	33	34.5	—	dBm
Power Added Efficiency	35	42	—	%
Output Power (Tuned for PCS Band, 1850 to 1910 MHz)	—	34.5	—	dBm
Power Added Efficiency (Tuned for PCS Band, 1850 to 1910 MHz)	—	42	—	%
Input VSWR	—	2:1	—	VSWR
Harmonic Output (2nd and 3rd)	—	–35	–30	dBc
Output Power at Low voltage (V_{D1}, V_{D2}, V_{D3}= 4.0 V)	32	33	—	dBm
Output Power, Isolation (V_{D1}, V_{D2}, V_{D3} = 0 V)	—	–40	–35	dBm
Noise Power (In 100 kHz, 1805 to 1880 MHz)	—	–85	–80	dBm
Stability – Spurious Output (P_{in} = 5 dBm, P_{out} = 0 to 33 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle) (1)	—	—	–60	dBc
Load Mismatch stress (P_{out} = 33 dBm, Load VSWR = 10:1 at any Phase Angle) (1)	No Degradation in Output Power after Returning to Standard Conditions			
3 dB V_{DD} Bandwidth	—	2	—	MHz
Negative Supply Current	—	0.7	2	mA

(1) Adjust $V_{D1,2,3}$ (0 to 4.8 V) for specified P_{out}; Duty Cycle = 12.5%, Period = 4.6 ms.

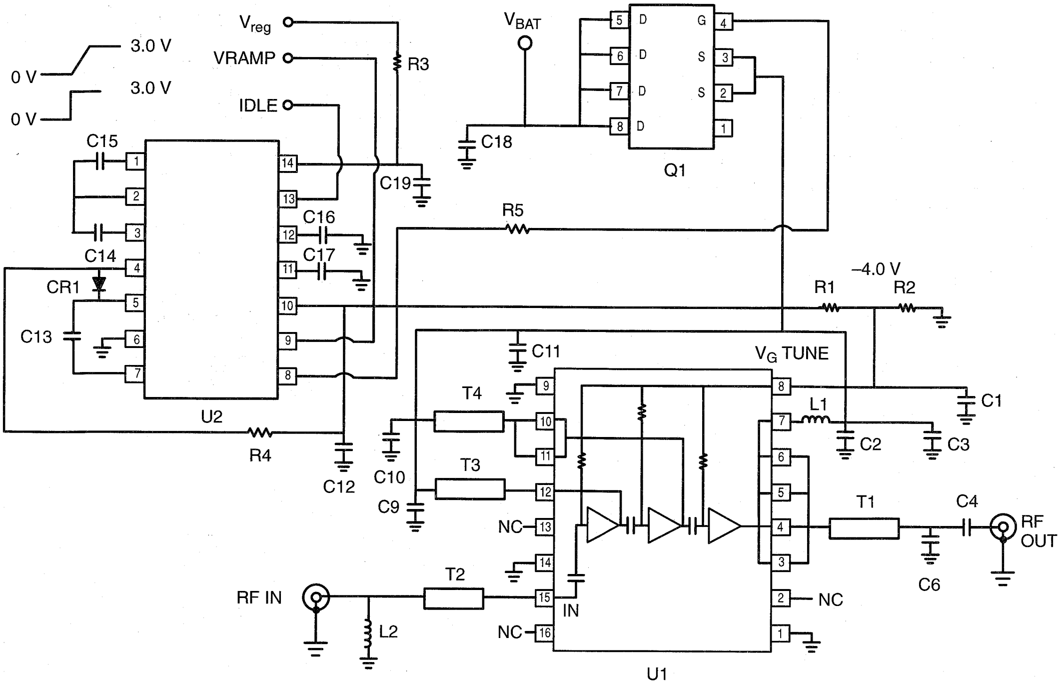


C1	6.8 nF	C5	3.9 pF, NPO/COG	T1	1.4 mm 25 Ω Microstrip Line
C2, C6, C8	22 pF, NPO/COG	L1	18 nH, Coilcraft	T2	5 mm 50 Ω Microstrip Line
C3, C7, C9	47 nF	L2	1.8 nH, Toko 2012	T3	4 mm 50 Ω Microstrip Line
C4	27 pF, NPO/COG	R1, R2 = 2.7 KΩ		T4	0.5 mm 50 Ω Microstrip Line
C10	0.5 pF				

Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm

NOTE: For PCS/DCS1900 applications, the following components are used.
C5 = 2.7 pF, 0603 NPO/COG
L2 = 1.5 nH, Toko 2012
T3 = 1 mm 50 Ω Microstrip Line

Figure 1. Reference Circuit Configuration



C1	6.8 nF	C14, C15	1 μF	R3, R4	100 Ω
C2, C9, C10	22 pF, 0603 NPO/COG	C18	1 μF	R5	470 Ω
C3, C11	47 nF	CR1	MMBD701LT1	T1	2 mm 25 Ω Microstrip Line
C4	27 pF, 0603 NPO/COG	L1	18 nH, Coilcraft or 20 mm 50 Ω Microstrip Line	T2	5 mm 50 Ω Microstrip Line
C6	3.9 pF, 0603 NPO/COG	L2	1.8 nH, Toko 2012 or 5 mm 50 Ω Line	T3	8 mm 40 Ω Microstrip Line
C12	220 nF	Q1	MMSF4N01HD	T4	1 mm 40 Ω Microstrip Line
C13, C16, C17, C19	1 μF	R1, R2	2.7 kΩ	U1	MRFIC1818
				U2	MC33169 (–4 V Version)

Board Material: Glass/Epoxy, ε_r = 4.45, Thickness = 0.5 mm

NOTE: For PCS/DCS1900 applications, the following component values are changed.

C6 = 2.7 pF, 0603 NPO/COG
L2 = 1.5 nH, Toko 2012
T3 = 1 mm 50 Ω Microstrip Line

Figure 2. DCS1800 Applications Circuit Configuration

Typical Characteristics

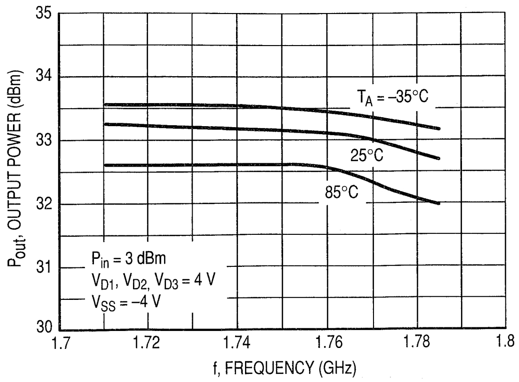


Figure 3. Output Power versus Frequency

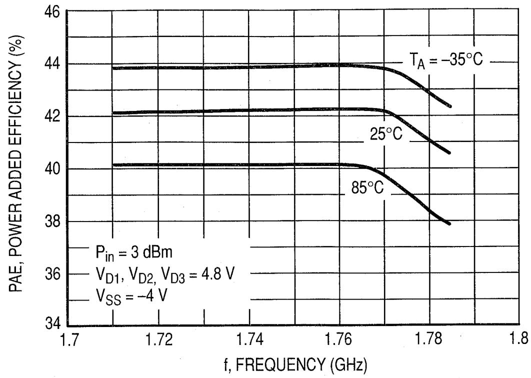


Figure 4. Power Added Efficiency versus Frequency

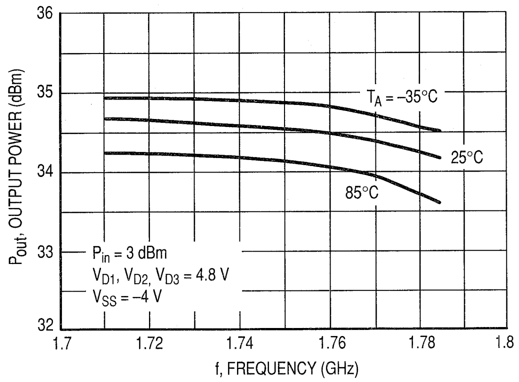


Figure 5. Output Power versus Frequency

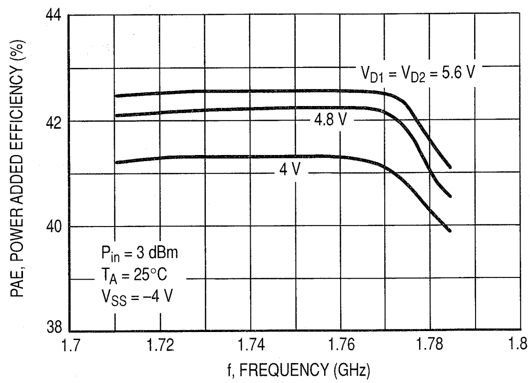


Figure 6. Power Added Efficiency versus Frequency

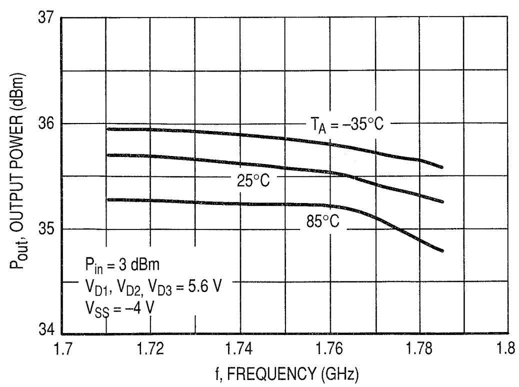


Figure 7. Output Power versus Frequency

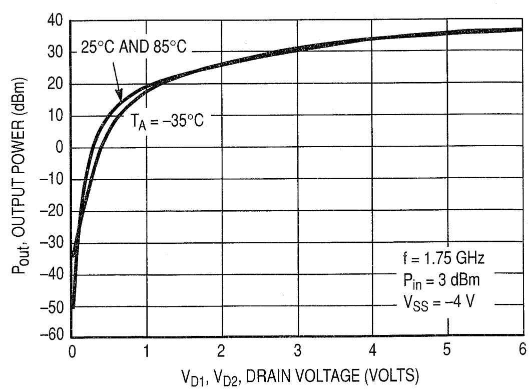


Figure 8. Output Power versus Drain Voltage

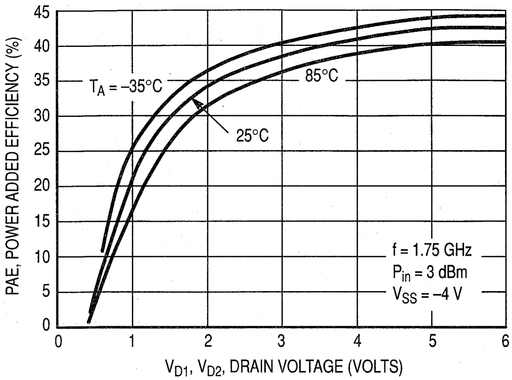


Figure 9. Power Added Efficiency versus Drain Voltage

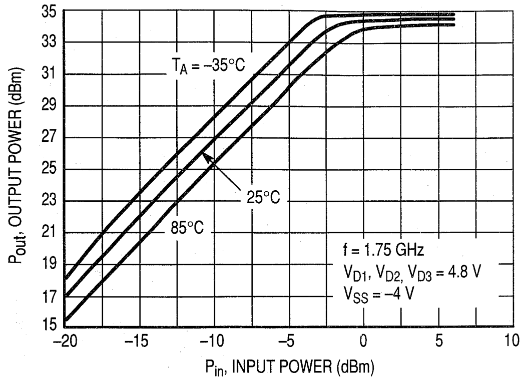


Figure 10. Output Power versus Input Power

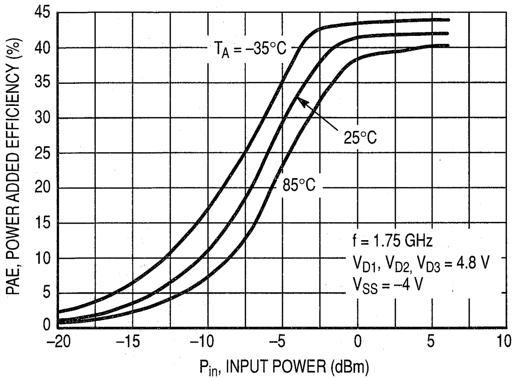


Figure 11. Power Added Efficiency versus Input Power

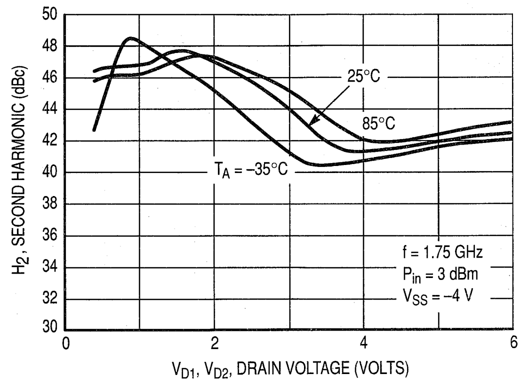


Figure 12. Second Harmonic versus Drain Voltage

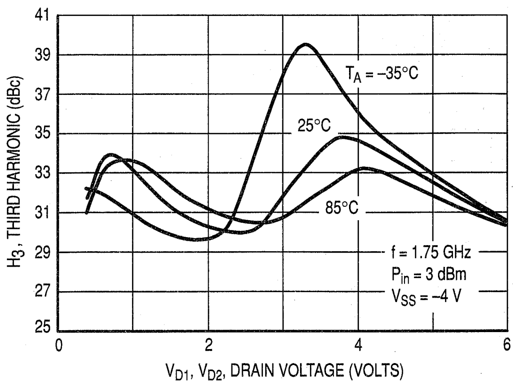


Figure 13. Third Harmonic versus Drain Voltage

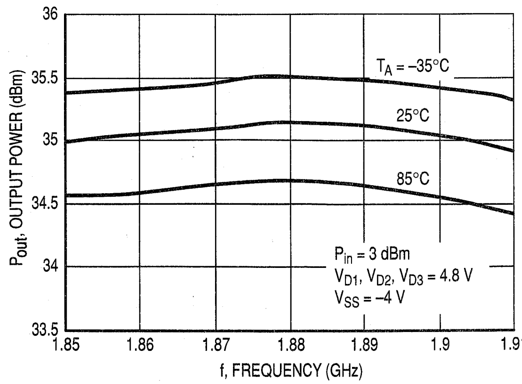


Figure 14. Output Power Versus Frequency – PCS Band

Typical Characteristics

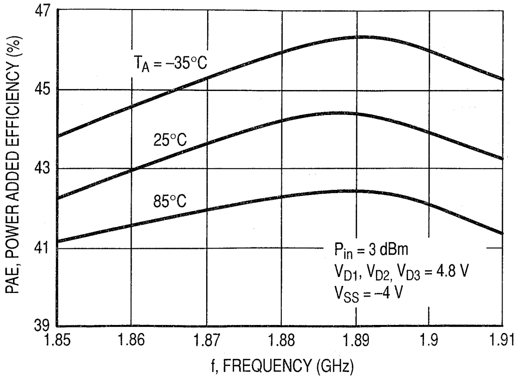


Figure 15. Power Added Efficiency versus Frequency – PCS Band

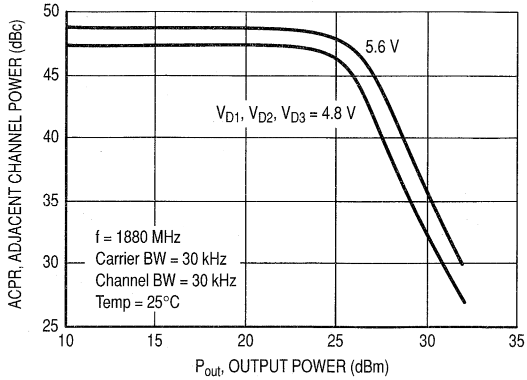


Figure 16. CDMA ACPR at 885 kHz Offset versus Output Power

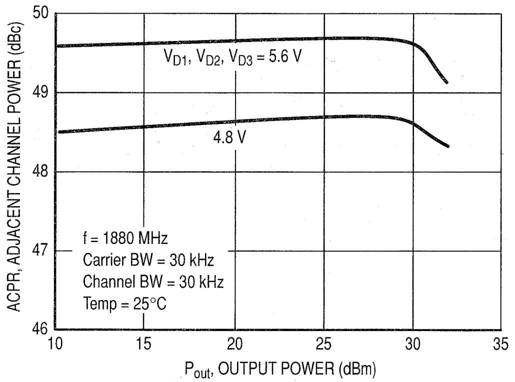


Figure 17. CDMA ACPR at 1980 kHz Offset versus Output Power

Table 1. Optimum Loads Derived from Circuit Characterization

f	Z_{in} OHMS		Z_{OL}* OHMS	
MHz	R	jX	R	jX
1710	9.19	–30.10	6.00	3.80
1720	9.35	–29.60	5.96	3.71
1730	9.50	–29.30	5.88	3.60
1740	9.65	–29.10	5.80	3.46
1750	9.60	–29.00	5.75	3.33
1760	9.42	–28.79	5.67	3.20
1770	9.11	–28.60	5.60	3.07
1780	8.77	–28.30	5.51	2.93
1785	8.54	–28.15	5.45	2.79

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

Table 2. Optimum Loads Derived from Circuit Characterization – PCS Board

f	Z_{in} OHMS		Z_{OL}* OHMS	
MHz	R	jX	R	jX
1850	3.92	–43.30	7.70	0.39
1860	4.01	–43.56	7.64	0.23
1870	4.08	–43.78	7.57	0.15
1880	4.19	–44.00	7.51	0.07
1890	4.29	–44.29	7.50	–0.04
1900	4.31	–44.49	7.44	–0.06
1910	4.37	–44.81	7.35	–0.19

Z_{in} represents the input impedance of the device.
Z_{OL}* represents the conjugate of the optimum output load to present to the device.

APPLICATIONS INFORMATION

Design Philosophy

The MRFIC1818 is a 3–stage Integrated Power Amplifier designed for use in cellular phones, especially for those used in DCS1800 (PCN) 4.8 V operation. With matching circuit modifications, it is also applicable for use in DCS1900 (PCS) equipment. Due to the fact that the input, output and some of the interstage matching is accomplished off chip, the device can be tuned to operate anywhere within the 1500 to 2000 MHz frequency range. Typical performance at different battery voltages is:

- 36 dBm @ 6.0 V
- 34.5 dBm @ 4.8 V
- 32.0 dBm @ 3.6 V

This capability makes the MRFIC1818 suitable for portable cellular applications such as:

- 6V and 4.8 V DCS1800 Class I
- 6V and 4.8 V PCS tag5
- 3.6 V DCS1800 Class II

RF Circuit Considerations

The MRFIC1818 can be tuned by changing the values and/or positions of the appropriate external components. Refer to Figure 2, a typical DCS1800 Class I applications circuit. The input match is a shunt–L, series–C, High–pass structure and can be retuned as desired with the only limitation being the on–chip 6 pF blocking capacitor. For saturated applications such as DCS1800 and DCS1900, the input match should be optimized at the rated RF input power. Interstage matching can be optimized by changing the value and/or position of the decoupling capacitor on the V_{D1} and V_{D2} supply lines. Moving the capacitor closer to the device or reducing the value increases the frequency of resonance with the in–ductance of the device's wirebonds and leadframe pin. Output matching is accomplished with a one–stage low–pass network as a compromise between bandwidth and harmonic rejection. Implementation is through chip capacitors mounted along a 30 or 50 Ω microstrip transmission line. Values and positions are chosen to present a 2.5 W loadline to the device while conjugating the device output parasitics. The network must also properly terminate the second and third harmonics to optimize efficiency and reduce harmonic output. Low–Q commercial chip capacitors are used for the shunt capacitors, as shown in Figure 2. Loss in circuit traces must also be considered. The output transmission line and the bias supply lines should be at least 0.6 mm in width to accommodate the peak circulating currents which can be as high as 2 amperes under worst case conditions. The bias supply line which supplies the output should include an RF choke of at least 18 nH, surface mount solenoid inductors or quarter wave microstrip lines. Discrete inductors will usually give better efficiency and conserve board space. The DC blocking capacitor required at the output of the device is best mounted at the 50 Ω impedance point in the circuit where the RF current is at a minimum and the capacitor loss will have less effect.

Biasing Considerations

Gate bias lines are tied together and connected to the V_{SS} voltage, allowing gate biasing through use of external resistors or positive voltages. This allows setting the quiescent current of all stage in the same time while saving some board space. For applications where the amplifier is operated close to saturation, such as TDMA amplifiers, the gate bias can be set with resistors. Variations in process and tempera–ture will not affect amplifier performance significantly in these applications. The values shown in the Figure 1 will set quies–cent currents of 20 to 40 mA for the first stage, 150 to 300 for the second stage and 400 to 800 mA for the final stage. For linear modes of operation which are required for CDMA amplifiers, the quiescent current must be more carefully controlled. For these applications, the V_G pins can be referenced to some tunable voltage which is set at the time of radio manufacturing. Less than 1 mA is required in the divider network so a DAC can be used as the voltage source.

Power Control Using the MC33169

The MC33169 is a dedicated GaAs power amplifier support IC which provides the –4 V required for V_{SS}, an N–MOS drain switch interface and driver and power supply sequencing. The MC33169 can be used for power control in applications where the amplifier is operated in saturation since the output power in non–linear operation is proportional to V_{D2}. This provides a very linear and repeatable power control transfer function. This technique can be used open loop to achieve 40–45 dB dynamic range over process and temperature variation. With careful design and selection of calibration points, this technique can be used for DCS1800 control where 30 dB dynamic range is required, eliminating the need for the complexity and cost of closed–loop control. The transmit waveform ramping function required for systems such as DCS1800 can be implemented with a simple Sallen and Key filter on the MC33169 control loop. The amplifier is then ramped on as the V_{RAMP} pin is taken from 0 V to 3 V. To implement the different power steps required for DCS1800, the V_{RAMP} pin is ramped between 0 V and the appropriate voltage between 0 V and 3 V for the desired output power. For closed–loop configurations using the MC33169, MMSF4N01HD N–MOS switch and the MRFIC1818 provide a typical 1 MHz 3 dB loop bandwidth. The STANDBY pin must be enabled (3 V) at least 800 μs before the V_{RAMP} pin goes high and disabled (0 V) at least 20 μs before the V_{RAMP} pin goes low. This STANDBY function allows for the enabling of the MC33169 one burst before the active burst thus reducing power consumption.

Conclusion

The MRFIC1818 offers the flexibility in matching circuitry and gate biasing required for portable cellular applications. Together with the MC33169 support IC, the device offers an efficient system solution for TDMA applications such as DCS1800 where saturated amplifier operation is used.

For more information about the power control using the MC33169, refer to application note AN1599, "Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC."

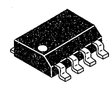
Evaluation Boards

Two versions of the MRFIC1818 evaluation board are available. Order MRFIC1818DCSTF for the 1.8 GHz version and order MRFIC1818PCSTF for the 1.9 GHz version. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line
900 MHz Downconverter (LNA/Mixer)

MRFIC2001

900 MHz DOWNCONVERTER LNA/MIXER SILICON MONOLITHIC INTEGRATED CIRCUIT



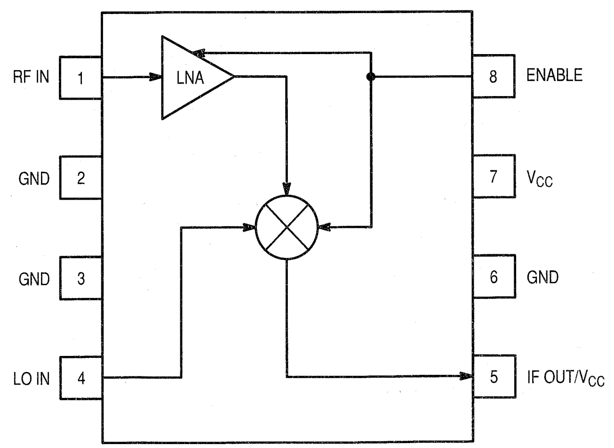
CASE 751-05 (SO-8)

The MRFIC2001 is an integrated downconverter designed for receivers operating in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2001 include CT-1 and CT-2 cordless telephones, remote controls, video and audio short range links, low cost cellular radios, and ISM band receivers. A power down control is provided to minimize current drain with minimum recovery/turn-on time.

- Conversion Gain = 23 dB (Typ)
- Supply Current = 4.7 mA (Typ)
- Power Down Supply Current = 2.0 µA (Max)
- Low LO Drive = –10 dBm (Typ)
- LO Impedance Insensitive to Power Down
- No Image Filtering Required
- No Matching Required for RF IN Port
- All Ports are Single Ended
- Order MRFIC2001R2 for Tape and Reel.
  R2 suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2001

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.5	Vdc
Control Voltage	ENABLE	5.0	Vdc
Input Power, RF and LO Ports	P_{RF}, P_{LO}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C



Pin Connections and Functional Block Diagram

REV 2

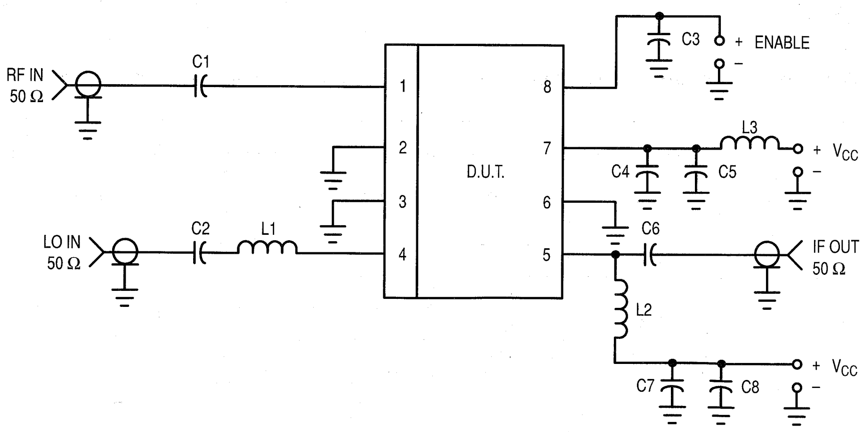
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	2.7 to 5.0	Vdc
Control Voltage Range	ENABLE	0 to 5.0	Vdc
RF Port Frequency Range	f_{RF}	500 to 1000	MHz
IF Port Frequency Range	f_{IF}	0 (dc) to 250	MHz

ELECTRICAL CHARACTERISTICS (V_{CC}, ENABLE = 3.0 V, T_A = 25°C, RF @ 900 MHz, LO @ 1.0 GHz, P_{LO} = –7.0 dBm, IF @ 100 MHz unless otherwise noted)

Characteristic (1)	Min	Typ	Max	Unit
Supply Current: On-Mode	—	4.7	5.5	mA
Supply Current: Off-Mode (ENABLE < 1.0 Volts)	—	0.1	2.0	μA
ENABLE Response Time	—	1.0	—	μs
Conversion Gain	20	23	26	dB
Input Return Loss (RF IN Port)	—	13	—	dB
Single Sideband Noise Figure	—	5.5	—	dB
Input 3rd Order Intercept Point	– 26	– 22.5	—	dBm
Output Power at 1.0 dB Gain Compression	—	–10	—	dBm
LO – RF Isolation (1.0 GHz)	—	37	—	dB
LO – IF Isolation (1.0 GHz)	—	33	—	dB
RF – IF Isolation (900 MHz)	—	4.0	—	dB
RF – LO Isolation (900 MHz)	—	19	—	dB

NOTE:
1. All Electrical Characteristics measured in test circuit schematic shown in Figure 1 below:



C1, C2, C4, C7 — 100 pF Chip Capacitor
C3, C5, C8 — 1000 pF Chip Capacitor
C6 — 6.8 pF Chip Capacitor
L1 — 8.2 nH Chip Inductor
L2 — 270 nH Chip Inductor

L3 — 150 nH Chip Inductor
RF Connectors — SMA Type
Board Material — Epoxy/Glass ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Test Circuit Configuration

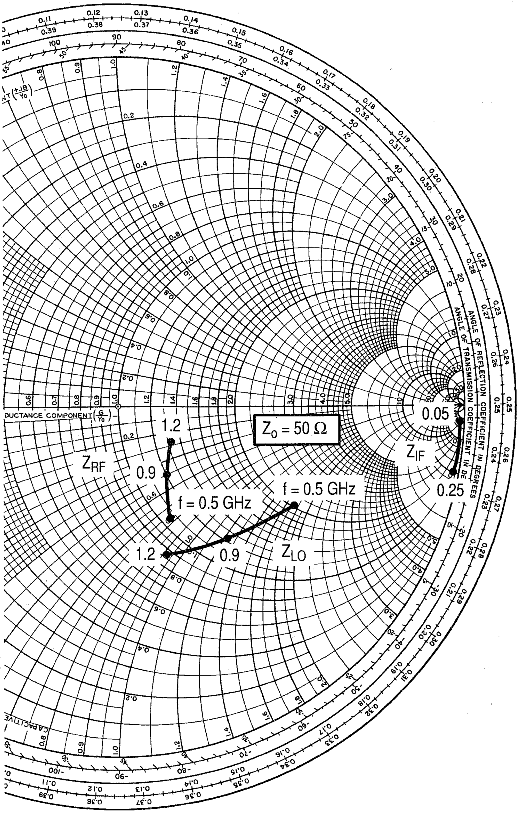


Figure 2. Port Impedances versus Frequency (GHz)

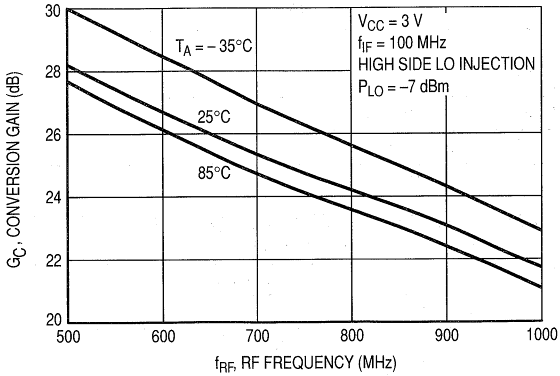


Figure 3. Conversion Gain versus RF Frequency

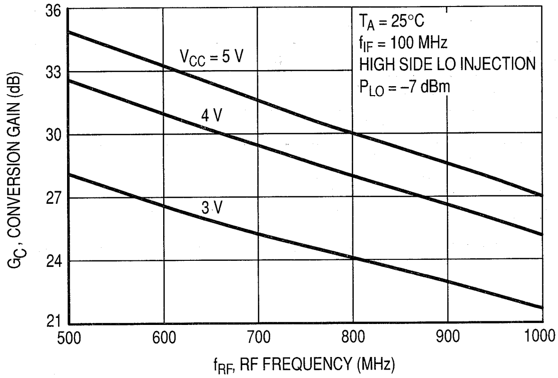


Figure 4. Conversion Gain versus RF Frequency

V_{CC} (Volts)	f (MHz)	Γ_{IF}		Γ_{RF}		Γ_{LO}	
		Mag	∠φ Degrees	Mag	∠φ Degrees	Mag	∠φ Degrees
3.0	50	0.998	– 2.5	—	—	—	—
	100	0.996	– 4.9	—	—	—	—
	150	0.993	– 7.2	—	—	—	—
	200	0.990	–10	—	—	—	—
	250	0.987	–12	—	—	—	—
	500	—	—	0.36	–70	0.58	– 31
	600	—	—	0.32	–70	0.55	– 36
	700	—	—	0.29	– 69	0.53	– 42
	800	—	—	0.26	– 68	0.51	– 48
	900	—	—	0.23	– 63	0.50	– 54
	1000	—	—	0.20	– 58	0.49	– 61
	1100	—	—	0.18	– 51	0.47	– 68
	1200	—	—	0.17	– 44	0.45	– 76

Table 1. Port Reflection Coefficients
(ENABLE = 3.0 V, Z_o = 50 Ω, T_A = 25°C)

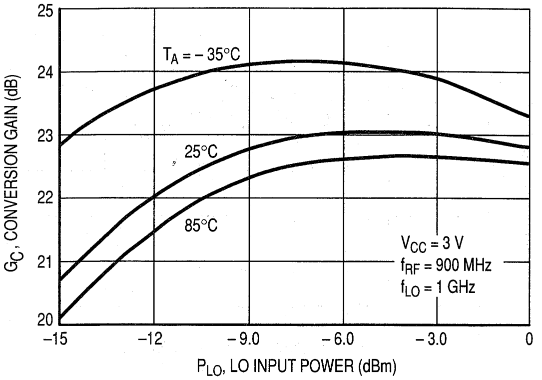


Figure 5. Conversion Gain versus LO Input Power

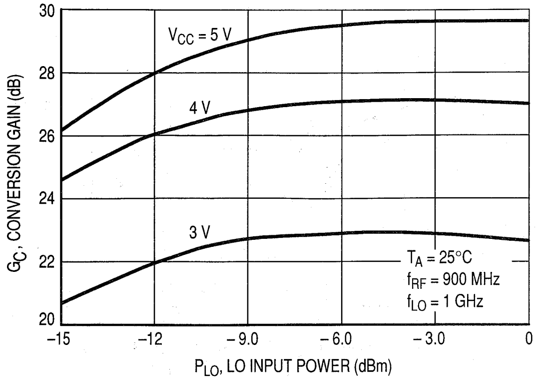


Figure 6. Conversion Gain versus LO Input Power

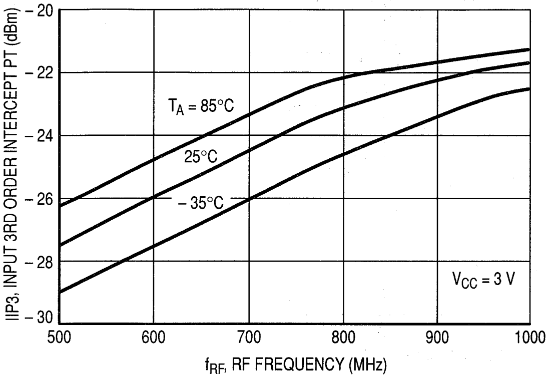


Figure 7. Input Third Order Intercept Point versus RF Frequency

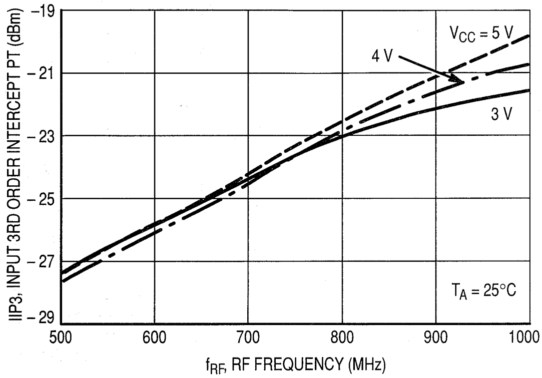


Figure 8. Input Third Order Intercept Point versus RF Frequency

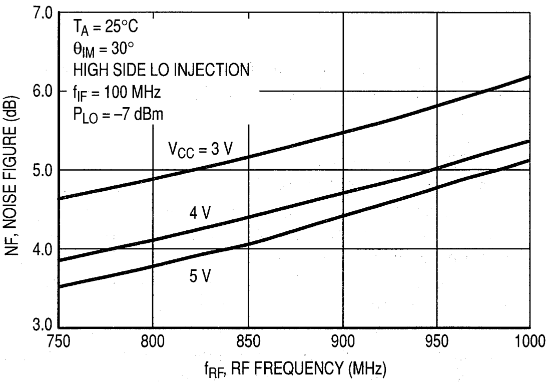


Figure 9. Noise Figure versus RF Frequency

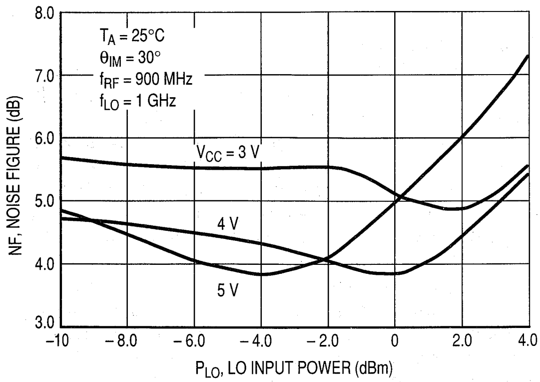


Figure 10. Noise Figure versus LO Input Power

TYPICAL CHARACTERISTICS

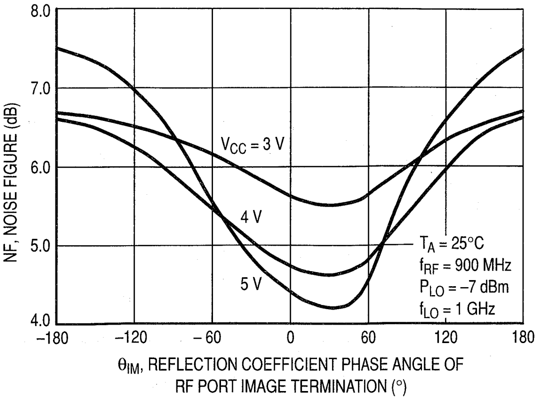


Figure 11. Noise Figure versus Reflection Coefficient Phase Angle of RF Port Image Termination

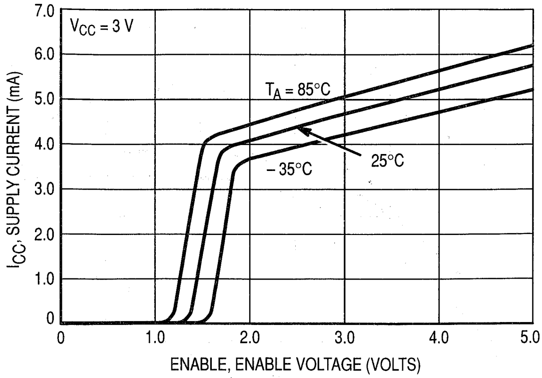


Figure 12. Supply Current versus Enable Voltage

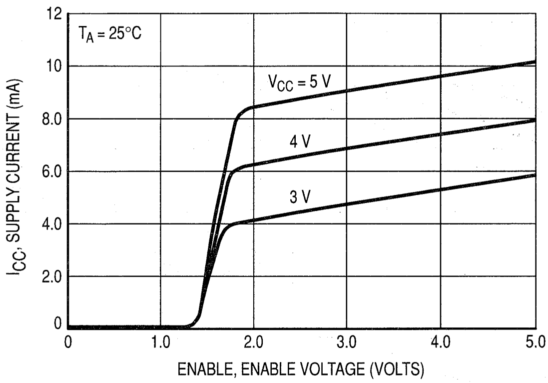


Figure 13. Supply Current versus Enable Voltage

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2001 was designed for low cost, small size, and ease of use. This is accomplished by minimizing the number of necessary external components.

The most significant external component eliminated was an image filter between the LNA and mixer. It was found the ensuing image noise entering the mixer from the LNA could be minimized by optimizing the LNA input termination at the image frequency. Also, a double-balanced mixer was used to reject the IF noise from the LNA. This results in excellent LO and spurious rejection.

To eliminate the need for external baluns or decoupling elements, the unused LO and RF ports of the mixer are decoupled internally. Only one of the IF outputs is used, eliminating the need for an external balun on the IF port as well. Also, the LNA input is matched to 50 ohms internally. External matching is required for the LO and IF ports.

To minimize current drain in various TDD/TDMA systems, the MRFIC2001 has a TTL/CMOS compatible enable pin.

THEORY OF OPERATION

Optimizing the LNA input termination to minimize image noise is quite simple. The optimum LNA input (RF IN pin) termination is $1\angle 30°$ at the image frequency (regardless of what the image frequency is). A reflection coefficient magnitude close to 1 is automatically obtained from a front-end filter, since the image frequency would be in the stop-band. The 30° phase angle can be obtained by rotating the phase angle of the front-end filter with a series 50 ohm transmission line. The dependance of single-sideband noise figure on the image phase angle is shown in Figure 11. As the plot indicates, there is a little over 1.0 dB of variation across all possible phase angles for a 3.0 V supply. Therefore, setting the phase angle is not critical. At higher supply voltages setting the phase angle is more critical (and more rewarding).

Matching the LO port to 50 ohms can be done several ways. The recommended approach is a series inductor as close to the IC as possible. The inductor value is small enough (~8–15 nH depending on LO frequency) to be printed on the board. A DC block is required and should not be placed between the inductor and IC since this will prevent the inductor from being close enough to the IC to provide a good match.

The IF port is an open collector resulting in a very high output impedance. For optimum linearity (IP3), the IF port should be loaded with a 1000 ohm load-line. Since the output requires a bias inductor and blocking capacitor, the IF filter impedance can be transformed to 1000 ohms with these two elements. If a low output VSWR is desired (to reduce IF filter ripple), a 2.0–4.0 K ohm resistor can be placed in parallel with the bias inductor. This will reduce the conversion gain by 1.0–2.0 dB.

The RF port is nearly 55 ohms resistive in series with a small amount of capacitive reactance, which results in a 12–13 dB return loss. If a higher return loss is desired, a 3.0–4.0 nH series inductor printed on the board as close to the IC as possible will improve it to over 20 dB. A DC block is also required.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. An additional 100 pF capacitor and an RF choke are recommended to keep the LO signal off the supply line.

Enabling/Disabling the MRFIC2001 can be done with its TTL/CMOS compatible Enable pin. The trip point is between 1.0 and 2.0 volts.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

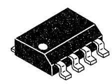
The MRFIC Line
900 MHz Transmit Mixer

MRFIC2002

The MRFIC2002 is a double-balanced, active mixer designed for transmitters operating in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2002 include CT1 and CT2 cordless telephones, GSM, remote controls, video and audio short range links, low cost cellular radios, and ISM band transmitters. A power down control is provided to minimize current drain with minimum recovery/turn-on time.

- Conversion Gain = 10 dB (Typ)
- Supply Current = 5.5 mA (Typ)
- Power Down Supply Current = 2.0 μA (Max)
- LO-RF Isolation = 25 dB (Typ)
- Low LO Drive Required = –10 dBm (Typ)
- LO Impedance Insensitive to Power Down
- No Matching Required for RF OUT Port
- All Ports are Single Ended
- Order MRFIC2002R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2002

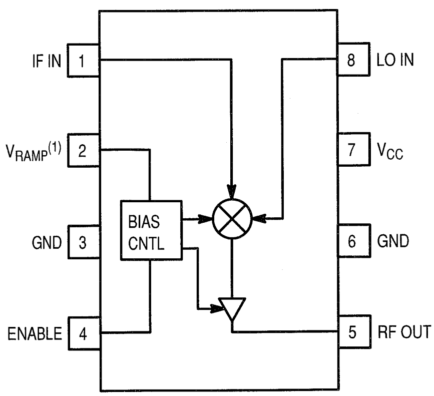
900 MHz TX-MIXER
SILICON MONOLITHIC
INTEGRATED CIRCUIT



CASE 751-05
(SO-8)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.5	Vdc
Control Voltages	ENABLE, V_{RAMP}	5.0	Vdc
Input Power, LO and IF Ports	P_{LO}, P_{IF}	+10	dBm
Operating Ambient Temperature	T_A	–35 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C



(1) For CT2 applications, apply ramp voltage provided in MRFIC2004. For non-CT2, leave open circuited.

Pin Connections and Functional Block Diagram

REV 2

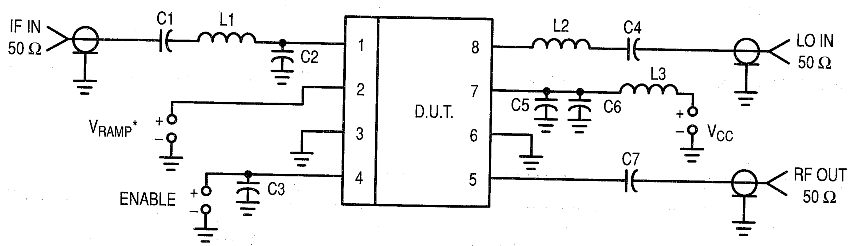
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	2.7 to 5.0	Vdc
Control Voltage Ranges	ENABLE, V_{RAMP}	0 to 5.0	Vdc
RF Port Frequency Range	f_{RF}	500 to 1000	MHz
IF Port Frequency Range	f_{IF}	0 (dc) to 250	MHz

ELECTRICAL CHARACTERISTICS (V_{CC}, Enable = 3.0 V and V_{Ramp}(1) Open Circuited, P_{LO} = –7.0 dBm, IF @ 100 MHz, LO @ 1.0 GHz, RF @ 900 MHz, T_A = 25°C unless otherwise noted)

Characteristic (2)	Min	Typ	Max	Unit
Supply Current: On-Mode Supply Current: Off-Mode (Enable < 1.0 V)	— —	5.5 0.1	7.0 2.0	mA µA
Enable Response Time	—	1.0	—	µs
Conversion Gain	8.0	10	12	dB
Single Sideband Noise Figure	—	10	—	dB
Output Power at 1.0 dB Gain Compression	—	–18	—	dBm
Output Power at Saturation	–16	–14	—	dBm
LO-RF Isolation (1.0 GHz)	—	25	—	dB
LO-IF Isolation (1.0 GHz)	—	65	—	dB
IF-RF Isolation (100 MHz)	—	18	—	dB
IF-LO Isolation (100 MHz)	—	50	—	dB

NOTES:
1. For CT2 applications, apply ramp voltage provided in MRFIC2004. For non-CT2, leave open circuited.
2. All Electrical Characteristics are measured in test circuit schematic as shown in Figure 1.



C1, C3, C6 — 1000 pF Chip Capacitor
C2 — 6.8 pF Chip Capacitor
C4 — 3.9 pF Chip Capacitor
C5 — 100 pF Chip Capacitor
C7 — 5.6 pF Chip Capacitor
L1 — 270 nH Chip Inductor
L2 — 10 nH Chip Inductor
L3 — 390 nH Chip Inductor
RF Connectors — SMA Type
Board Material — Glass/Epoxy ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Test Circuit Configuration

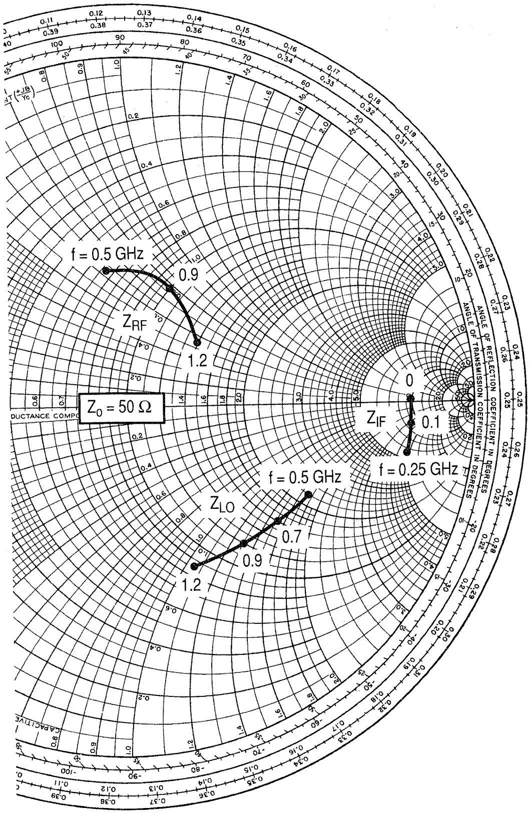


Figure 2. Port Impedances versus Frequency

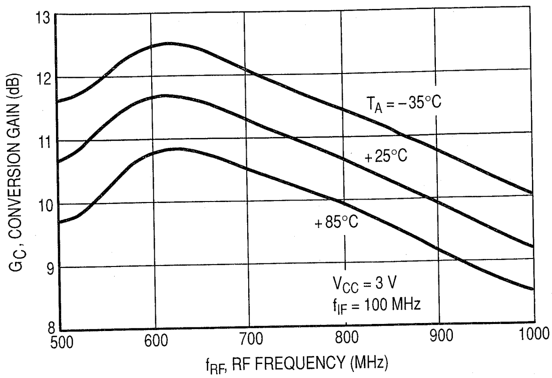


Figure 3. Gain versus RF Frequency

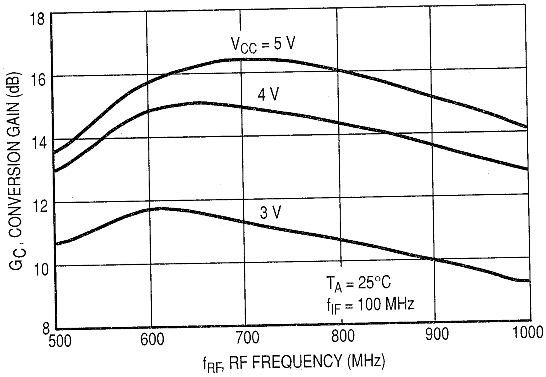


Figure 4. Gain versus RF Frequency

V_{CC} (Volts)	f (MHz)	Γ_{IF}		Γ_{RF}		Γ_{LO}	
		Mag	∠φ Degrees	Mag	∠φ Degrees	Mag	∠φ Degrees
3.0	50	0.83	−2.4	—	—	—	—
	100	0.82	−4.7	—	—	—	—
	150	0.82	−7.1	—	—	—	—
	200	0.81	−9.6	—	—	—	—
	250	0.81	−11.7	—	—	—	—
	500	—	—	0.42	100	0.57	−29
	600	—	—	0.41	94	0.55	−35
	700	—	—	0.40	88	0.54	−41
	800	—	—	0.39	80	0.52	−48
	900	—	—	0.36	71	0.51	−54
	1000	—	—	0.33	63	0.50	−60
	1100	—	—	0.31	55	0.49	−65
	1200	—	—	0.28	45	0.49	−70

Table 1. Deembedded Port Reflection Coefficients
(Enable = 3.0 V, Z_o = 50 Ω, T_A = 25°C)

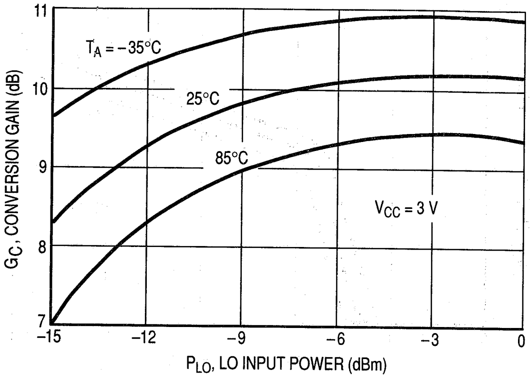


Figure 5. Gain versus LO Input Power

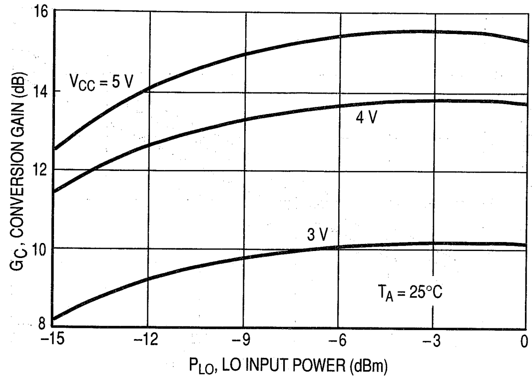


Figure 6. Gain versus LO Input Power

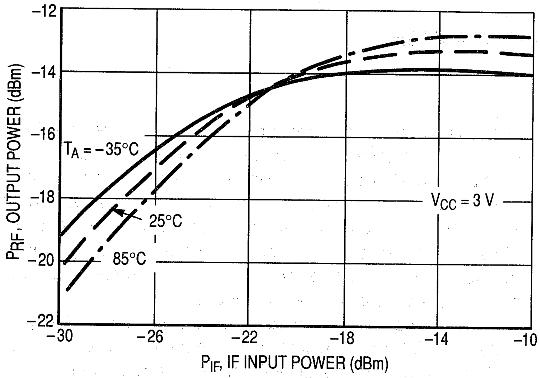


Figure 7. Output Power versus IF Input Power

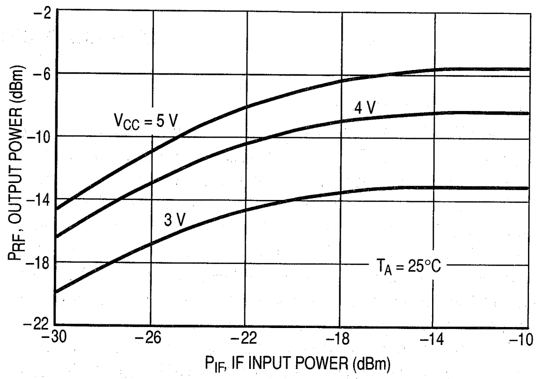


Figure 8. Output Power versus IF Input Power

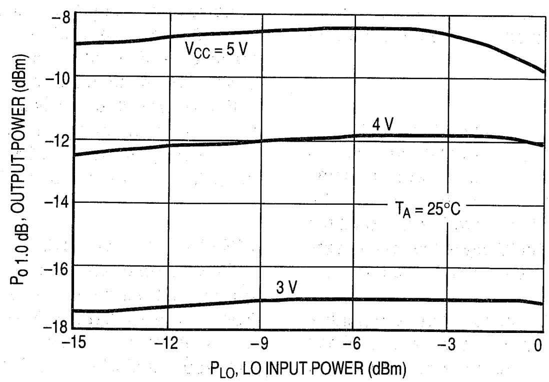


Figure 9. Output Power at 1.0 dB Gain Compression versus LO Input Power

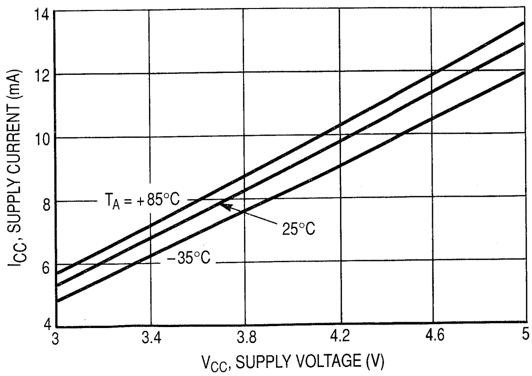


Figure 10. I_{CC} versus V_{CC}

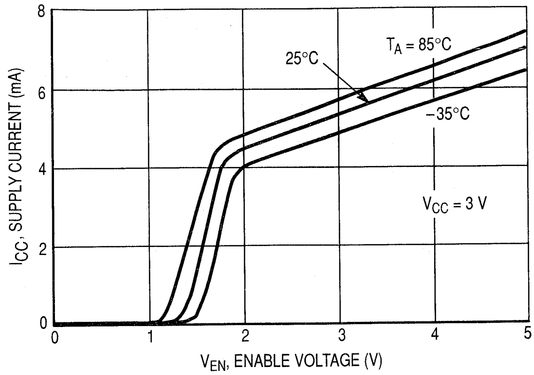


Figure 11. I_{CC} versus Enable Voltage

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2002 was designed to have excellent LO and spurious rejection. This is accomplished by using a double-balanced configuration and using a symmetrical die layout.

To eliminate the need for external baluns or decoupling elements, the unused LO and IF ports are decoupled internally. Only one of the RF outputs is used, eliminating the need for an external balun on the RF port as well. Also, the RF port is buffered to provide a 50 ohm output impedance. External matching is required for the LO and IF ports.

To minimize current drain in various TDD/TDMA systems, two methods of enabling/disabling the MRFIC2002 are provided: one that is TTL/CMOS compatible and one that is triggered from a ramp, such as the one provided in the MRFIC2004. The former method must be used if a ramp is not available. The latter method is more desirable since the MRFIC2002 can remain off during guard times and while in idle mode.

THEORY OF OPERATION

Matching the LO port to 50 ohms can be done several ways. The recommended approach is a series inductor as close to the IC as possible. The inductor value is small enough (~8–15 nH depending on LO frequency) to be printed on the board. A DC block is required and should not be placed between the inductor and IC since this will prevent the inductor from being placed close enough to the IC to provide a good match.

The IF port is approximately 500 ohms resistive in parallel with 1.3 pF of capacitance. If 50 ohms is the desired IF port impedance, a shunt capacitor followed by a series inductor will provide the transformation. A DC block is required and can be placed on either side of the matching network.

The RF port is nearly 50 ohms resistive in series with a small amount of inductive reactance, which results in an 8–11 dB return loss. However, a series 5.6 pF capacitor placed as close to the IC as possible will typically provide greater than a 15 dB return loss. The series capacitor also serves as a DC block which is required.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. An additional 100 pF capacitor and an RF choke are recommended to keep the RF and LO signals off the supply line.

For systems that use a ramp, like the one provided in the MRFIC2004, enabling/disabling can be done by applying the ramp voltage to the V_{RAMP} pin which trips the IC between 0.6 and 1.0 volts. The Enable pin must either be tied high or to the inverse of the receiver enable control line, $\overline{RXEN}$. An inverter is provided in the MRFIC2004 to invert RXEN.

For systems that do not use a ramp, the V_{RAMP} pin can be left open circuited and enabling/disabling the MRFIC2002 can be done with its TTL/CMOS compatible Enable pin. The trip point is between 1.0 and 2.0 volts.

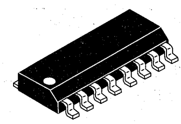
EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line
900 MHz Driver and Ramp

MRFIC2004

900 MHz DRIVER & RAMP SILICON MONOLITHIC INTEGRATED CIRCUIT



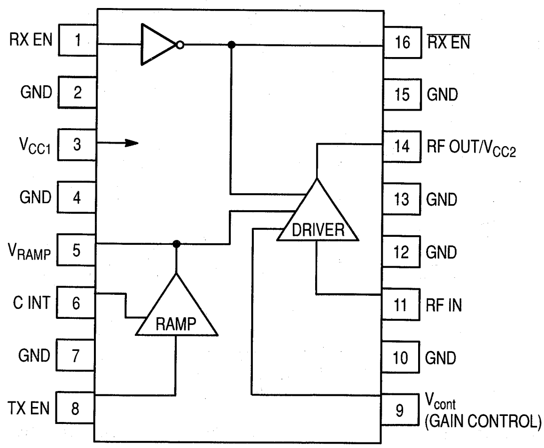
CASE 751B-05 (SO-16)

The MRFIC2004 is an integrated Driver and Ramp designed for transmitters operating in the 800 MHz to 1.0 GHz frequency range. The Ramp is an integrator which can be used for burst control for TDD/TDMA systems. The Driver uses a cascode configuration for high gain and reverse isolation. A power down control is provided to minimize current drain with minimum recovery/turn-on time. Also, an on-board inverter is included to provide complementary control for an antenna switch, such as the MRFIC2003. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2004 include CT1 and CT2 cordless telephones, GSM, remote controls, video and audio short range links, low cost cellular radios, and ISM band transmitters.

- Small Signal Gain = 21.5 dB (Typ)
- Small Signal Gain Control = 34 dB (Typ)
- $P_{o\ 1.0\ dB}$ = −1.0 dBm (Typ)
- On Board Ramp for Burst Control
- Power Down Supply Current = 0.7 mA (Typ)
- Low Operating Supply Voltage (2.7 to 4.0 Volts)
- Input/Output VSWR Insensitive to Gain Control
- Order MRFIC2004R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2004

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC1} V_{CC2}	4.5 6.0	Vdc
Control Voltages	RXEN, TXEN, V_{cont}	6.0	Vdc
Input Power, RF IN Port	P_{RF}	+10	dBm
Operating Ambient Temperature	T_A	−35 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C



Pin Connections and Functional Block Diagram

REV 2

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Ranges	V_{CC1}, V_{CC2}	2.7 to 4.0	Vdc
Control Voltage Ranges	TX EN, RX EN, V_{cont}	0 to V_{CC1}	Vdc
Frequency Range	f	800 to 1000	MHz

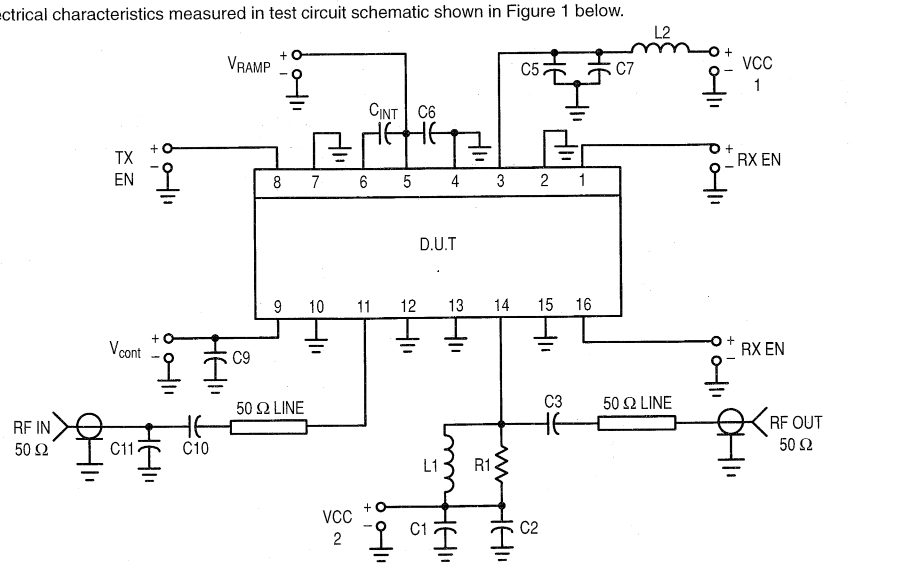
ELECTRICAL CHARACTERISTICS (V_{CC1}, V_{CC2} = 3.0 V, C_{INT} = 2.0 nF, T_A = 25°C, f = 900 MHz, V_{CONT} = 1.3 V)

Characteristics (1)	Min	Typ	Max	Unit
Supply Current, TX EN High, RX EN Low	—	11	13	mA
Supply Current, TX EN Low, RX EN High	—	0.7	1.5	mA
Driver Characteristics (1)				
Gain (Small Signal)	19	21.5	24	dB
Gain Control (Small Signal)	—	34	—	dB
Power Out @ 1.0 dB Gain Compression	−4.0	−1.0	—	dBm
Third Order Intercept Point (out)	—	+7.5	—	dBm
Reverse Isolation	—	32	—	dB
Ramp Characteristics (1)				
Ramp Up Delay Time Rise Time Total Time	— — —	4.0 18 22	— — —	µs
Ramp Down Delay Time Fall Time Total Time	— — —	4.0 18 22	— — —	µs

LOGIC LEVELS (V_{CC1} = 2.7 to 4.0 V, T_A = 25°C)

RX EN & TX EN Input Voltage	Min	Typ	Max	Unit
High Low	V_{CC1} − 0.8 —	— —	— 0.8	V
$\overline{\text{RX EN}}$ Output Voltage				
High Low	V_{CC1} − 0.2 —	— —	— 0.2	V

NOTE:
1. All electrical characteristics measured in test circuit schematic shown in Figure 1 below.



C1, C7, C9 — 1000 pF Chip Capacitor
C2, C5, C6, C10 — 100 pF Chip Capacitor
C3 — 1.6 pF Chip Capacitor
C_{INT} — 2000 pF Chip Capacitor
C11 — 6.2 pF Chip Capacitor
L1 — 4.7 nH Chip Inductor
L2 — 150 nH Chip Inductor
R1 — 330 Ω Chip Resistor
RF Connectors — SMA Type
Board Material — Epoxy/Glass ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Typical Biasing Configuration

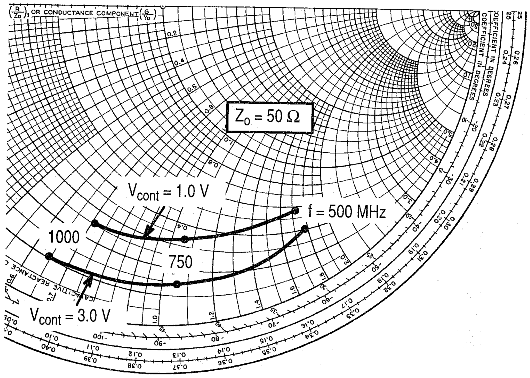


Figure 2. S_{11} versus Frequency versus V_{cont}

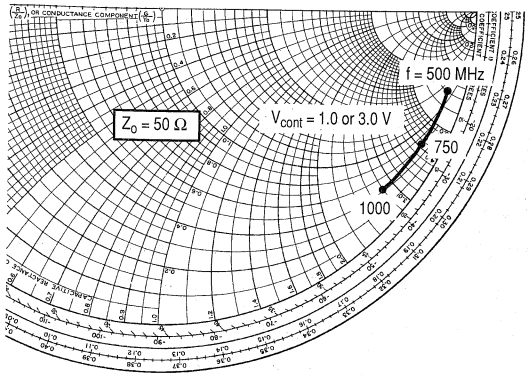


Figure 3. S_{22} versus Frequency

	f	S_{11}		S_{21}		S_{12}		S_{22}	
V_{cont}	(MHz)	$\lvert S_{11} \rvert$	∠φ	$\lvert S_{21} \rvert$	∠φ	$\lvert S_{12} \rvert$	∠φ	$\lvert S_{22} \rvert$	∠φ
1.0	100	0.85	−11.3	10.48	171.5	0.0002	142.7	0.99	−2.9
	300	0.83	−32.8	10.33	156.3	0.0020	129.0	0.99	−7.3
	500	0.79	−56.9	10.15	140.5	0.0030	130.6	0.98	−15.9
	550	0.79	−62.5	10.04	135.9	0.0030	132.6	0.98	−17.9
	600	0.78	−68.5	9.85	130.2	0.0040	133.3	0.98	−20.0
	650	0.77	−74	9.47	126.9	0.0040	135.9	0.98	−22.3
	700	0.76	−79	9.23	123.6	0.0050	137.2	0.98	−24.7
	750	0.76	−84.4	9.02	119.4	0.0050	138.1	0.97	−27.0
	800	0.75	−89.6	8.69	113.8	0.0060	139.7	0.97	−29.3
	850	0.74	−94.5	8.33	110.8	0.0070	140.3	0.97	−31.4
	900	0.73	−99.1	8.13	108.9	0.0080	141.2	0.96	−33.2
	950	0.73	−102	7.98	105.4	0.0090	138.3	0.96	−36.3
	1000	0.72	−106.9	7.70	101.0	0.0100	133.7	0.95	−38.4
1.9	100	0.85	−11.3	0.53	−173.5	0.0002	104.3	0.99	−2.9
	300	0.86	−33.5	0.69	−169.7	0.0009	118.7	0.98	−8.7
	500	0.87	−59.3	0.89	−179.5	0.0010	134.3	0.98	−15.5
	550	0.87	−65.7	0.96	175.1	0.0020	136.3	0.98	−17.5
	600	0.88	−73.1	1.02	169.9	0.0020	138.9	0.97	−19.6
	650	0.88	−78.7	1.04	167.3	0.0020	142.6	0.97	−21.8
	700	0.88	−84.7	1.07	165.0	0.0030	147.8	0.97	−24.1
	750	0.89	−90.7	1.14	161.5	0.0030	153.4	0.96	−26.4
	800	0.89	−98.2	1.17	155.8	0.0040	161.0	0.96	−28.8
	850	0.88	−104.6	1.22	151.2	0.0050	161.8	0.96	−30.7
	900	0.87	−110.1	1.24	144.6	0.0060	162.7	0.95	32.8
	950	0.86	−114.6	1.26	139.9	0.0070	160.3	0.95	−35.1
	1000	0.85	−118.8	1.27	134.1	0.0080	158.2	0.94	−37.2
3.0	100	0.85	−10.9	0.003	−85.9	0.0001	115.0	0.99	−2.8
	300	0.86	−31.9	0.014	−78.8	0.0006	121.0	0.99	−8.5
	500	0.87	−56.9	0.032	−61.1	0.0010	128.0	0.98	−15.1
	550	0.88	−62.4	0.038	−65.8	0.0010	136.2	0.98	−17.0
	600	0.89	−69.4	0.048	−68.3	0.0010	140.0	0.98	−19.2
	650	0.90	−75.1	0.058	−75.1	0.0020	145.1	0.98	−21.3
	700	0.90	−81.3	0.069	−82.4	0.0020	150.8	0.97	−23.6
	750	0.91	−87.3	0.081	−89.4	0.0020	156.8	0.97	−25.8
	800	0.91	−93.8	0.092	−113.4	0.0030	160.3	0.97	−28.1
	850	0.92	−100.7	0.092	−121.8	0.0040	163.3	0.96	−30.1
	900	0.91	−106.8	0.089	−128.2	0.0050	163.3	0.96	−32.3
	950	0.90	−111.4	0.083	−137.1	0.0060	155.2	0.95	−34.5
	1000	0.89	−115.2	0.077	−151.9	0.0060	150.0	0.95	−36.6

Table 1. Small Signal Deembedded S Parameters

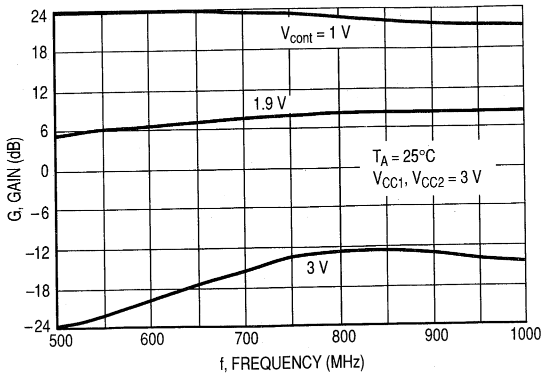


Figure 4. Small Signal Gain versus Frequency

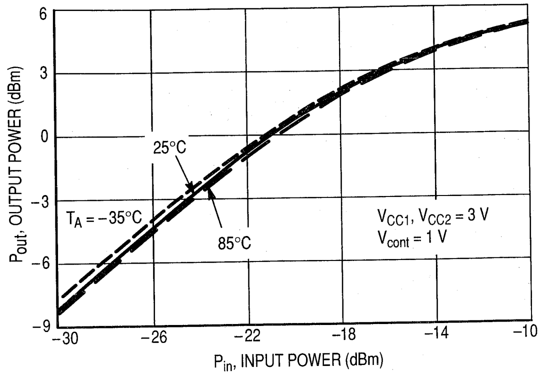


Figure 5. Output Power versus Input Power

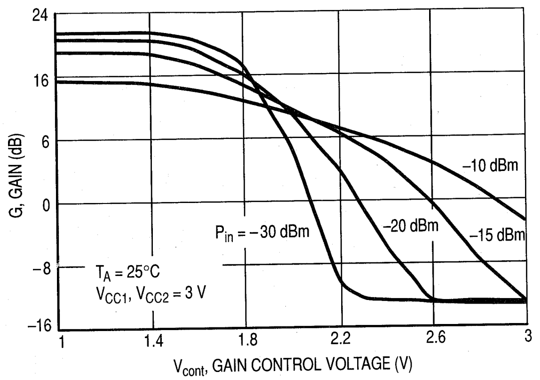


Figure 6. Driver Gain versus Gain Control Voltage

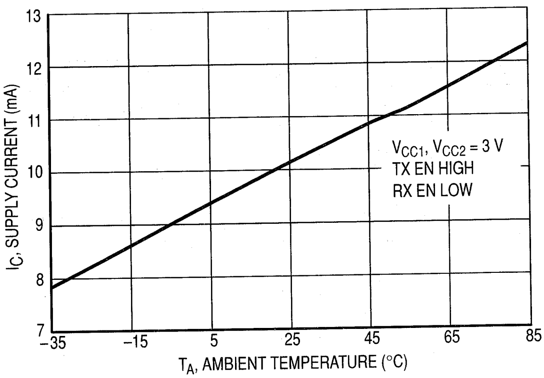


Figure 7. Supply Current versus Ambient Temperature

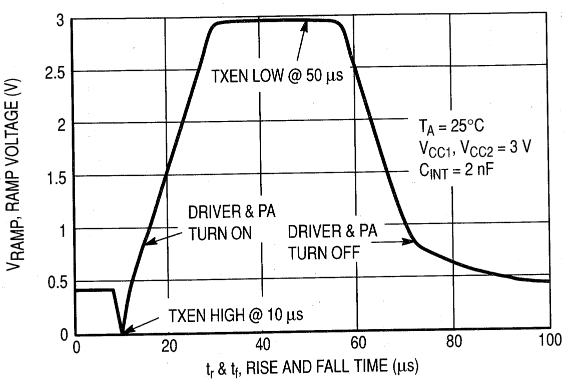


Figure 8. Ramp Voltage versus Rise & Fall Time

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2004 was designed as a support IC for a CT2 chip-set. The other chips making up the chip-set are the MRFIC2001 downconverter, the MRFIC2002 transmit mixer, the MRFIC2003 antenna switch and the MRFIC2006 PA. A complete CT2 front-end solution requires a ramp for burst control, an inverter for complementary antenna switch control and gain control (or an attenuator) for the transmitter low power mode. In order to keep the other chips in the chip-set relatively general purpose, yet provide the system designer with an easily controlled solution, these functions were combined with a driver amplifier into one IC, the MRFIC2004.

THEORY OF OPERATION

The driver is a cascode design that exits the IC open-collector. Impedance matching must be done externally. Since the output requires a bias inductor and DC blocking capacitor, the output can be matched with these two elements. To keep the driver unconditionally stable, it is recommended that a 300–400 ohm resistor be placed in parallel with the bias inductor as close to the IC as possible. Since the output impedance of the driver by itself is very high, the resistor sets the output impedance. The input can be matched with a series inductor followed by a shunt capacitor. Alternatively, a series transmission line followed by a shunt capacitor can be used. A DC block is also required on the input.

Gain control is provided to meet the CT2 low power mode requirement. The CT2 Common Air Interface specification requires the transmitter to be capable of dropping the output power by 16 ± 4.0 dB. Although the driver has 34 dB of small signal gain control, it can be reduced by adding a resistor in series with the gain control pin. The value of the resistor depends on the logic levels being used and the amount of gain compression after the driver. Also, the amount of gain control is a function of the driver input power level. The input power should be kept less than –10 dBm to allow for sufficient gain control to achieve the low power mode. The gain control can also be used for PA output power trimming. However, this is not an efficient method.

The ramp is an integrator which is used to slow down the driver and PA turn-on and turn-off times to reduce AM splatter. By applying a pulse waveform to the input, a linear ramp waveform is created at the output which is then applied to the current mirrors of the driver and PA. An external integrating capacitor is used so that the rise/fall time can be programmed externally. A minimum value of 2.0–2.4 nF is needed to meet the CT2 Common Air Interface splatter specification. For non-TDD/TDMA systems the ramp reverts to an enable/disable function.

The inverter is CMOS/TTL compatible and was included to provide complementary control for an antenna switch such as the MRFIC2003. By applying the receiver enable control line, RXEN, to the inverter the inverse $\overline{RXEN}$ will be created. RXEN and $\overline{RXEN}$ can then be used to control the MRFIC2003 antenna switch.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

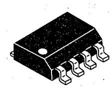
The MRFIC Line
900 MHz 2 Stage PA

MRFIC2006

The MRFIC2006 is an Integrated PA designed for linear operation in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2006 include CT-1 and CT-2 cordless telephones, remote controls, video and audio short range links, low cost cellular radios, and ISM band transmitters.

- 50 Ω Input and Output Impedance
- Typical Gain = 23 dB @ 900 MHz
- Bias Current Externally Adjustable
- Bias Pin can be used to Ramp or Disable
- Class A or AB Linear Operation
- Unconditionally Stable
- SO-8 Leaded Plastic Package
- Order MRFIC2006R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2006

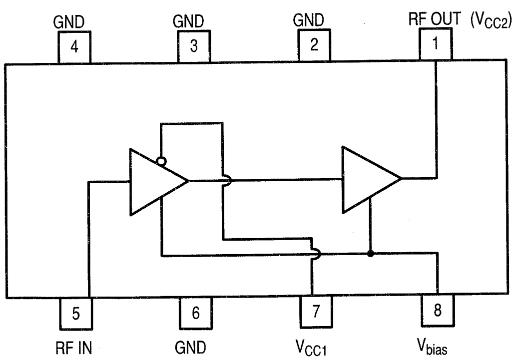
900 MHz 2 STAGE PA
SILICON MONOLITHIC
INTEGRATED CIRCUIT



CASE 751-05
(SO-8)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Z_o = 50 Ω unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC1}, V_{CC2}	5.0	Vdc
Bias Voltage	V_{bias}	6.0	Vdc
Total Supply Current	I_{CC1}, I_{CC2}	100	mA
RF Output Power (V_{CC2} < 4.0 V)	P_{out}	+21	dBm
RF Output Power (4.0 V < V_{CC2} ≤ 5.0 V)	P_{out}	53 – 8 V_{CC2}	dBm
RF Input Power	P_{in}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage and Junction Temperature	T_{stg}	– 65 to +150	°C
Thermal Resistance, Junction to Case	$R_{θJC}$	63	°C/W



Pin Connections and Functional Block Diagram

REV 2

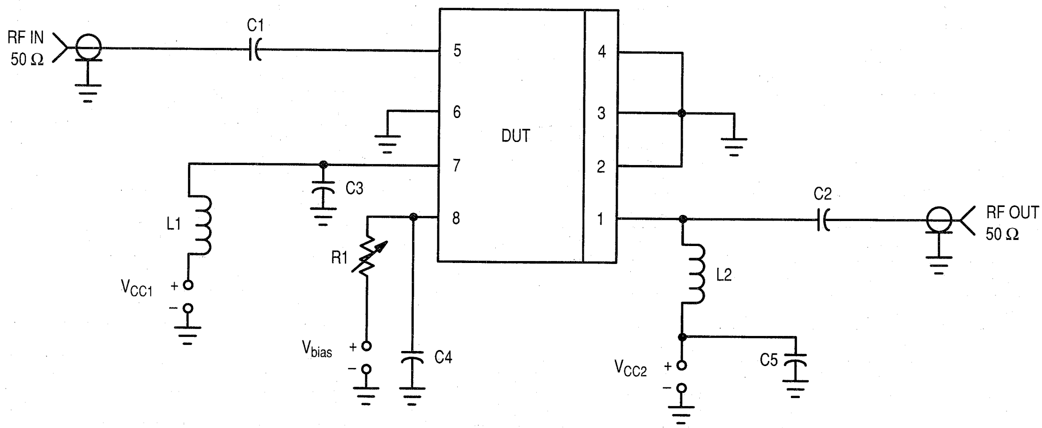
RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Ranges	V_{CC1}, V_{CC2}	1.8 to 4.0	Vdc
Bias Voltage Range	V_{bias}	0 to 5.0	Vdc
RF Frequency Range	f	500 to 1000	MHz

ELECTRICAL CHARACTERISTICS (V_{CC1}, V_{CC2}, V_{bias} = 3.0 V, T_A = 25°C, f = 900 MHz, Z_o = 50 Ω unless otherwise noted)

Characteristics (1)	Min	Typ	Max	Unit
Supply Current — Total I_{CC1} I_{CC2} I Bias	— — — —	46 14 29 3.0	55 — — —	mA mA mA mA
Small Signal Gain	19	23	26	dB
Input Return Loss, RF IN Port	—	15	—	dB
Output Return Loss, RF OUT Port	—	15	—	dB
Reverse Isolation	—	35	—	dB
Output Power at 1.0 dB Gain Compression	+12	+15.5	—	dBm
3rd Order Intercept Point (Out)	—	+ 25	—	dBm
5th Order Intercept Point (Out)	—	+ 21	—	dBm

NOTE:
1. All electrical characteristics measured in test circuit schematic shown in Figure 1 below.



C1, C2 — 100 pF Chip Capacitor
C3, C5 — 1.0 nF Chip Capacitor
C4 — 10 nF Chip Capacitor
L1 — 150 nH Chip Inductor
L2 — 10 nH Chip Inductor

R1 — Resistor Optional
RF Connectors — SMA Type
Board Material — Epoxy/Glass ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Typical Biasing Configuration

Table 1. Scattering Parameters for 900 MHz Two-Stage PA

(V_{CC1}, V_{CC2}, V_{BIAS} = 3 V, I = 49 mA, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
50	0.739	–16.67	3.785	51.56	0.003	–163.12	0.461	–89.23
100	0.702	–24.53	5.772	46.52	0.001	15.96	0.354	–117.30
150	0.671	–33.09	7.901	40.16	0.001	84.34	0.263	–144.77
200	0.649	–41.55	10.065	32.12	0.001	–165.89	0.208	–167.08
250	0.630	–49.79	12.287	23.06	0.002	–159.68	0.169	170.65
300	0.610	–58.60	14.576	12.25	0.002	171.75	0.136	145.40
350	0.592	–67.09	16.834	1.32	0.003	–160.23	0.113	113.52
400	0.567	–75.32	19.009	–10.72	0.005	–167.93	0.105	73.18
450	0.537	–83.69	20.901	–23.88	0.005	167.71	0.122	33.86
500	0.495	–91.79	22.237	–37.89	0.007	159.88	0.157	2.30
525	0.470	–95.35	22.626	–45.02	0.007	168.37	0.178	–10.93
550	0.448	–98.65	22.821	–52.22	0.010	162.65	0.196	–22.73
575	0.421	–101.69	22.834	–59.20	0.009	159.52	0.216	–32.62
600	0.397	–104.40	22.647	–66.13	0.010	155.15	0.233	–42.62
625	0.371	–106.50	22.299	–73.01	0.011	151.24	0.246	–50.98
650	0.349	–108.28	21.813	–79.43	0.011	148.14	0.258	–59.21
675	0.329	–109.85	21.204	–85.70	0.012	145.35	0.269	–66.61
700	0.310	–111.02	20.538	–91.62	0.012	140.66	0.273	–73.29
725	0.293	–111.65	19.824	–97.20	0.014	136.88	0.280	–79.97
750	0.278	–112.24	19.094	–102.54	0.014	136.98	0.281	–85.86
775	0.265	–112.60	18.334	–107.76	0.014	134.67	0.285	–91.50
800	0.252	–112.81	17.594	–112.54	0.016	133.71	0.284	–96.72
825	0.242	–113.50	16.880	–117.13	0.015	129.16	0.282	–102.24
850	0.233	–114.93	16.127	–122.44	0.017	131.80	0.281	–107.68
875	0.224	–115.32	15.438	–126.92	0.017	126.66	0.279	–112.88
900	0.216	–116.04	14.796	–130.89	0.017	127.06	0.275	–117.56
925	0.210	–116.66	14.165	–134.57	0.018	121.77	0.273	–120.85
950	0.203	–117.91	13.555	–138.19	0.019	122.40	0.269	–125.53
975	0.195	–118.87	13.009	–141.73	0.019	120.80	0.265	–129.73
1000	0.191	–120.47	12.515	–145.08	0.019	122.53	0.265	–132.68
1025	0.186	–122.39	12.004	–148.23	0.020	119.56	0.259	–137.22
1050	0.179	–124.03	11.517	–151.36	0.022	115.24	0.254	–140.85
1075	0.175	–126.22	11.063	–154.40	0.022	117.88	0.251	–144.69
1100	0.168	–128.77	10.634	–157.40	0.024	112.04	0.248	–148.25
1125	0.163	–131.41	10.228	–160.15	0.023	112.42	0.246	–151.75
1150	0.161	–133.93	9.841	–163.04	0.023	115.77	0.245	–155.28
1175	0.155	–136.68	9.479	–165.88	0.025	110.34	0.241	–158.69
1200	0.152	–140.85	9.125	–168.50	0.025	109.94	0.241	–161.95

TYPICAL CHARACTERISTICS

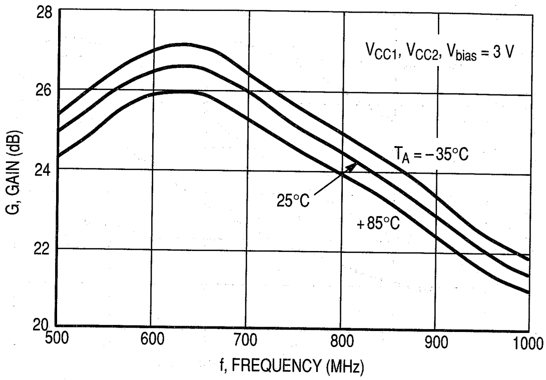


Figure 2. Gain versus Frequency

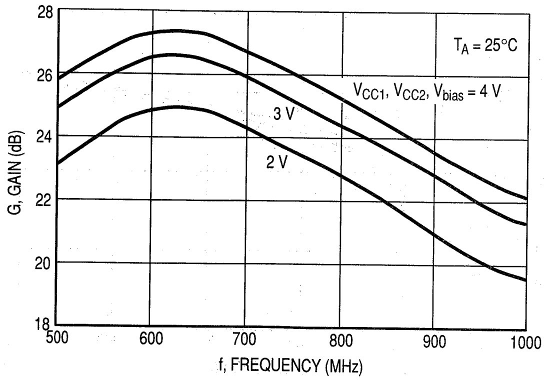


Figure 3. Gain versus Frequency

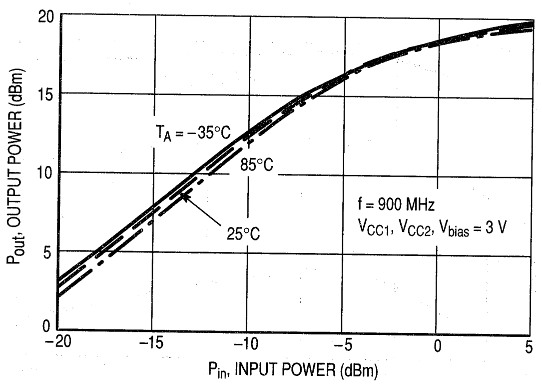


Figure 4. Output Power versus Input Power

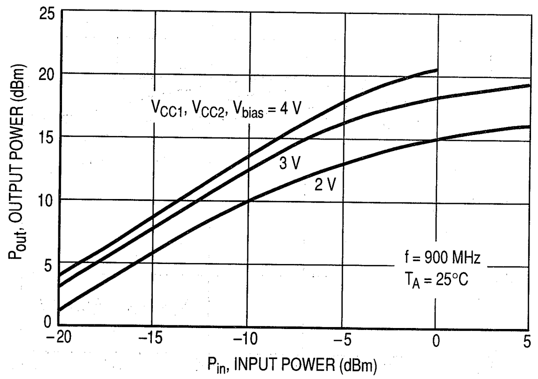


Figure 5. Output Power versus Input Power

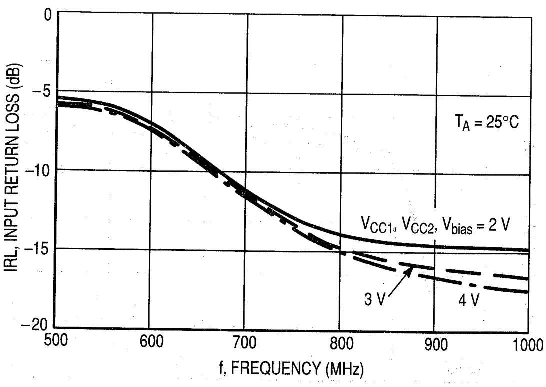


Figure 6. Input Return Loss versus Frequency

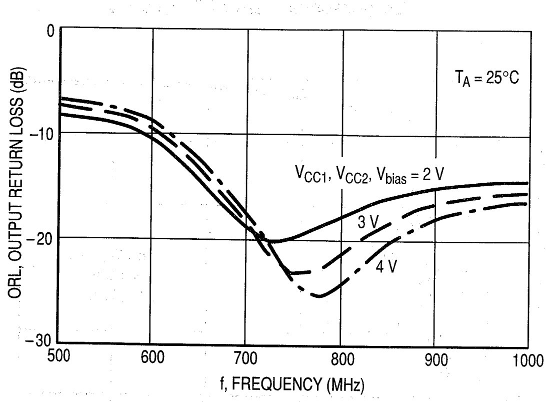


Figure 7. Output Return Loss versus Frequency

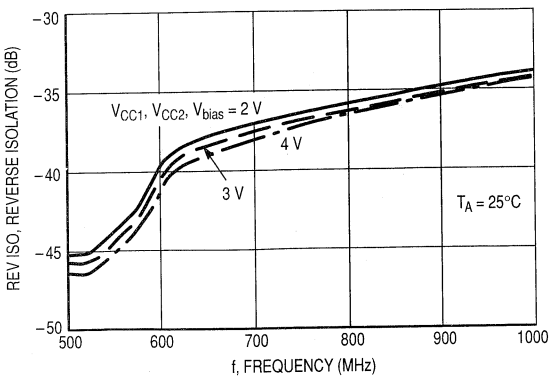


Figure 8. Reverse Isolation versus Frequency

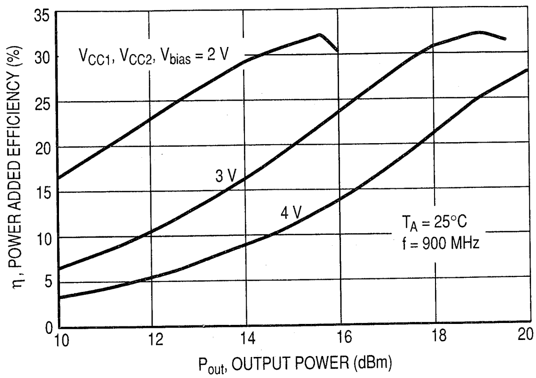


Figure 9. Power Added Efficiency versus Output Power

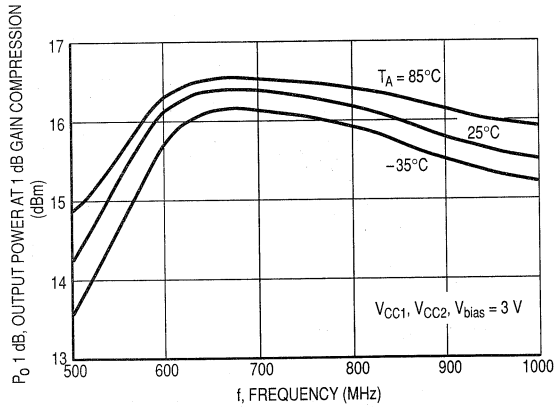


Figure 10. Output Power at 1 dB Gain Compression versus Frequency

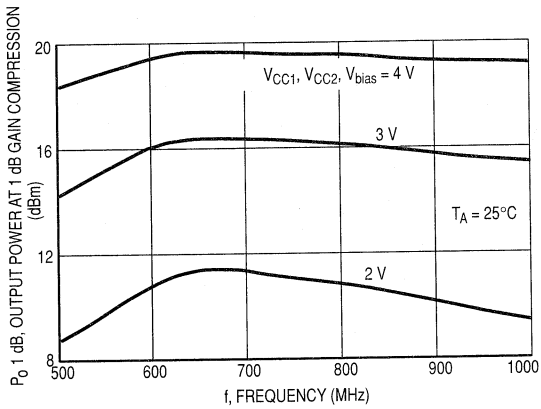


Figure 11. Output Power at 1 dB Gain Compression versus Frequency

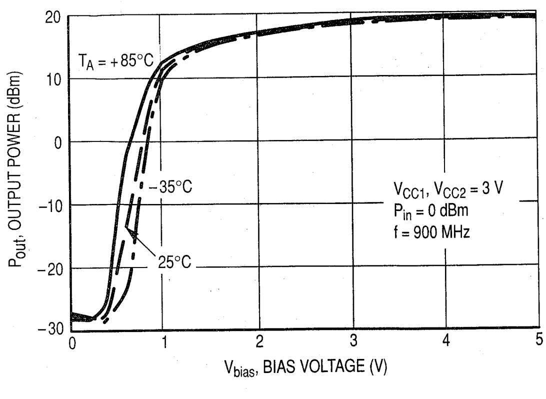


Figure 12. Output Power versus Bias Voltage

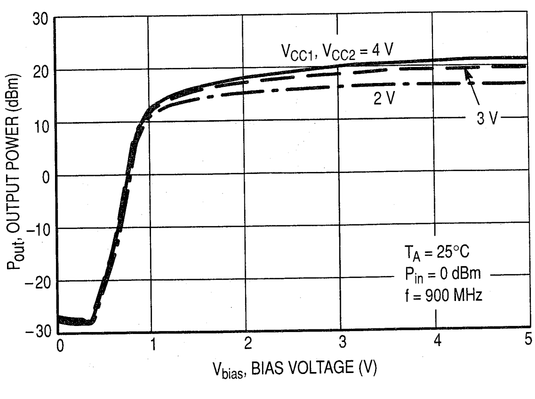


Figure 13. Output Power versus Bias Voltage

TYPICAL CHARACTERISTICS

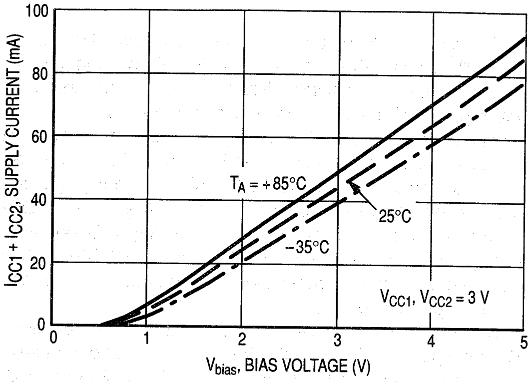


Figure 14. Supply Current versus Bias Voltage

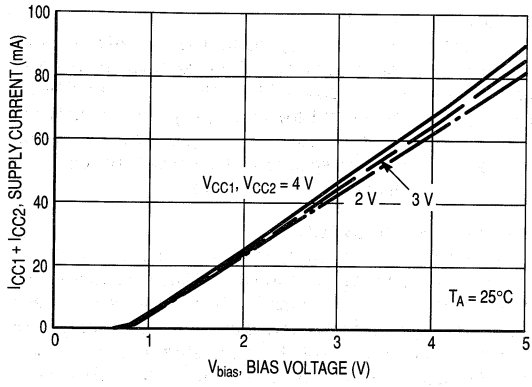


Figure 15. Supply Current versus Bias Voltage

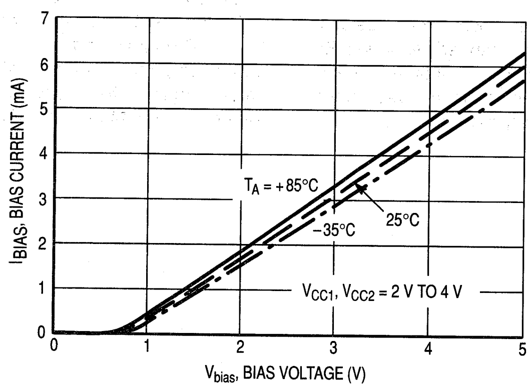


Figure 16. Bias Current versus Bias Voltage

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2006 was designed for low cost and flexibility. Low cost was achieved by minimizing external components and using an SOIC package. Flexibility was achieved by allowing the bias current to be externally adjustable resulting in a broad range of output power capability. The bias pin can be ramped to reduce AM splatter in TDD/TDMA systems and can be used to trim the RF output power.

THEORY OF OPERATION

The input port is internally matched to 50 ohms. Return loss is typically 15–16 dB in the 800–1000 MHz range. The output port is nearly 50 ohms but is an open collector and therefore requires an external bias inductor. Using an RF choke will result in a 11–12 dB output return loss. However, a 10 nH inductor will improve it to 15–20 dB. A 10 nH inductor is small enough in value to be printed on the board. DC blocks are required on the input and output. Values of 100 pF are recommended.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. A series RF choke is recommended to keep the RF signal off the supply line. A 10 nF decoupling capacitor is recommended on the V_{bias} line but does not need to be very close to the IC.

The V_{bias} pin can be used several ways. Tying it directly to V_{CC} will maximize the bias current which will maximize linearity. Adding a series resistor will reduce the bias current which will improve efficiency. Figure 9 shows the efficiency versus output power with V_{bias} tied to V_{CC}. The series resistor will cause these curves to shift to the left. The RF output power can be trimmed by using a variable resistor. The V_{bias} pin can also be used to power down the IC or, in the case of TDD/TDMA systems, to ramp the IC. By applying a linear ramp voltage, such as the one provided by the MRFIC2004, it has been demonstrated to meet the CT2 Common Air Interface splatter specifications.

The MRFIC2006 is internally temperature compensated. For input powers of –5.0 to 0 dBm the output power temperature variation is typically less than 0.2 dB from –35 to +85°C.

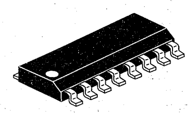
EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line
900 MHz TX-Mixer/Exciter

MRFIC2101

**900 MHz
TX-MIXER/EXCITER
SILICON MONOLITHIC
INTEGRATED CIRCUIT**



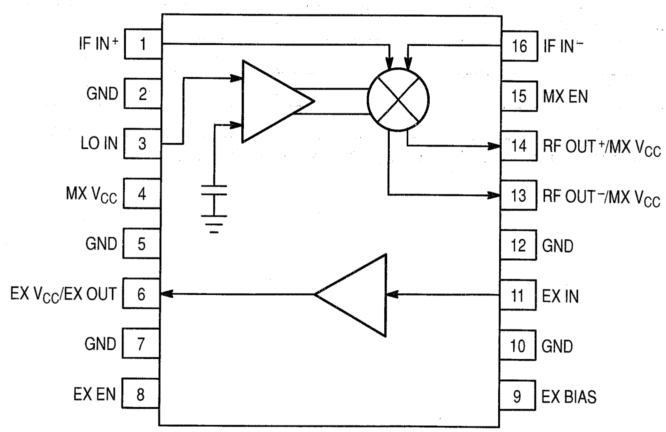
**CASE 751B-05
(SO-16)**

The MRFIC2101 is a high linearity transmit mixer and exciter designed primarily for Digital Cellular radio systems. The mixer is double-balanced for excellent LO and spurious rejection. An on-board LO buffer is provided to reduce LO power requirements and eliminate the need for an external LO balun. A power down control is provided to minimize current drain with minimum recovery/turn-on time. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device.

- High Linearity $IP3_0$ = 23 dBm (Typ)
- Low LO Drive Required = –15 dBm (Typ)
- Externally Adjustable Exciter Bias Current
- Power Down Supply Current = 2.0 μA (Typ)
- SO-16 Narrow Body Plastic Package
- Order MRFIC2101R2 for Tape and Reel.
  R2 suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2101

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Ratings	Symbol	Value	Unit
Supply Voltage	EX V_{CC}, MX V_{CC}, EX BIAS	5	Vdc
Enable Voltages	MX EN, EX EN	6	Vdc
Input Power, LO and IF Ports	P_{LO}, P_{IF}	+10	dBm
Operating Ambient Temperature	T_A	– 35 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C
RF Output Power (EX V_{CC} < 4 V)	P_{out}	18	dBm
RF Output Power (4 V< EX V_{CC} ≤ 5 V)	P_{out}	38 – 5 EX V_{CC}	dBm



Pin Connections and Functional Block Diagram

REV 3

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltages	EX V_{CC}, MX V_{CC}, EX BIAS	4.75	Vdc
Enable Voltages	MX EN, EX EN	0, 4.75	Vdc
RF Port Frequency Range	RF	800 to 1000	MHz
IF Port Frequency Range	IF	0 to 250	MHz

LOGIC LEVELS (T_A = 25°C)

Input Voltage (MX EN, EX EN)	Min	Max	Unit
High	MX V_{CC} –0.8, EX V_{CC} –0.8	—	Volts
Low	—	0.8	Volts

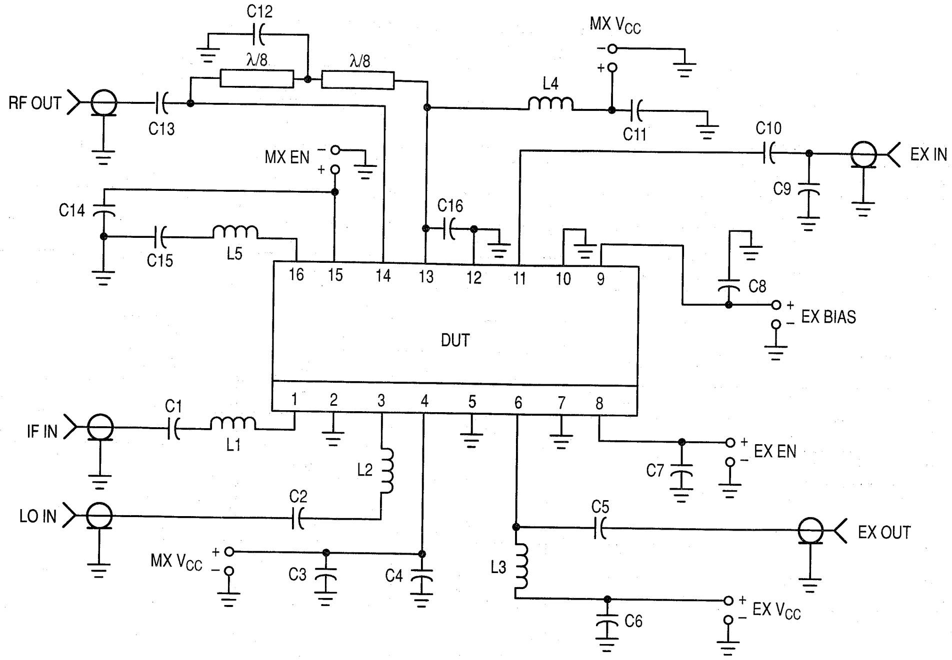
MIXER ELECTRICAL CHARACTERISTICS (MX V_{CC}, MX EN = 4.75 V, T_A = 25°C, RF @ 900 MHz, LO @ 800 MHz, IF @ 100 MHz, P_{LO} = –15 dBm unless otherwise noted)

Characteristic (1)	Min	Typ	Max	Unit
Conversion Gain (Small Signal)	24	26.5	29	dB
Output Power at 1 dB Gain Compression	2.5	4.5	—	dBm
Output Third Order Intercept Point (– 5 dBm out/tone)	—	14	—	dBm
Output Fifth Order Intercept Point (– 5 dBm out/tone)	—	11	—	dBm
LO Leakage	—	– 30	—	dBm
Supply Current (Enabled)	—	45	54	mA
Supply Current (Disabled)	—	1	—	µA
Noise Figure (Single Sideband)	—	5	—	dB

EXCITER ELECTRICAL CHARACTERISTICS (EX V_{CC}, EX EN, EX BIAS = 4.75 V, T_A = 25°C, RF @ 900 MHz unless otherwise noted)

Characteristic (1)	Min	Typ	Max	Unit
Gain (Small Signal)	14	16	18	dB
Output Power at 1 dB Gain Compression	16	18	—	dBm
Output Third Order Intercept Point (+ 3 dBm out/tone)	—	30	—	dBm
Output Fifth Order Intercept Point (+ 3 dBm out/tone)	—	22	—	dBm
LO Leakage (P_{LO} = –15 dBm into Mixer)	—	– 30	—	dBm
Supply Current (Enabled)	—	38	46	mA
Supply Current (Disabled)	—	1	—	µA
Noise Figure	—	5	—	dB

(1) All electrical characteristics are measured in test circuit schematic as shown in Figure 1.



C1, C2, C3,	1000 pF, Chip Capacitor	L1, L5	82 nH, Chip Inductor
C4	100 pF, Chip Capacitor	L2	15 nH, Chip Inductor
C5, C6, C7	1000 pF, Chip Capacitor	L3	8.2 nH, Chip Inductor
C8, C10, C11	1000 pF, Chip Capacitor	L4	12 nH, Chip Inductor
C9, C12	5.6 pF, Chip Capacitor	RF Connectors	SMA Type
C13, C16	2.7 pF, Chip Capacitor	Board Material	0.031″ Thick FR4, 0.5 oz. Copper, ε_r = 4.45, Coplanar Waveguide
C14, C15	1000 pF, Chip Capacitor		

Figure 1. Test Circuit Configuration

Table 1. Mixer Deembedded Port Reflection Coefficients
(Z_O = 50 Ω, T_A = 25°C)

f (MHz)	Γ_{IF}		Γ_{RF}		Γ_{LO}	
	Mag	∠φ Degrees	Mag	∠φ Degrees	Mag	∠φ Degrees
50	0.68	– 9.4	—	—	—	—
100	0.68	– 18	—	—	—	—
150	0.67	– 26	—	—	—	—
200	0.66	– 33	—	—	—	—
250	0.65	– 40	—	—	—	—
500	—	—	0.93	– 28	0.79	– 30
600	—	—	0.92	– 33	0.79	– 32
700	—	—	0.91	– 37	0.79	– 33
800	—	—	0.89	– 41	0.77	– 34
900	—	—	0.87	– 45	0.75	– 34
1000	—	—	0.85	– 48	0.73	– 35
1100	—	—	0.82	– 50	0.69	– 36
1200	—	—	0.79	– 53	0.65	– 37
1300	—	—	0.75	– 56	0.61	– 41
1400	—	—	0.71	– 61	0.56	– 47
1500	—	—	0.66	– 66	0.52	– 55

Table 2. Exciter Small Signal Deembedded S Parameters
(Z_O = 50 Ω, T_A = 25°C)

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\lvert S_{11}\rvert$	∠φ	$\lvert S_{21}\rvert$	∠φ	$\lvert S_{12}\rvert$	∠φ	$\lvert S_{22}\rvert$	∠φ
100	0.51	–121	35.51	131	0.02	50	0.65	–67
200	0.62	–149	22.61	109	0.03	42	0.49	–103
300	0.65	–162	16.05	96	0.03	41	0.43	–122
400	0.65	–170	12.16	87	0.04	41	0.40	–134
500	0.63	–177	9.75	81	0.04	42	0.38	–141
600	0.61	176	8.18	75	0.05	41	0.37	–146
700	0.59	169	7.06	70	0.05	40	0.36	–149
800	0.58	161	6.18	65	0.06	38	0.35	–153
900	0.58	154	5.44	60	0.07	33	0.35	–156
1000	0.59	145	4.91	55	0.07	30	0.35	–163
1100	0.61	139	4.39	51	0.08	27	0.35	–170
1200	0.65	134	3.94	47	0.08	22	0.35	–177
1300	0.67	131	3.56	43	0.08	20	0.37	174
1400	0.69	129	3.22	39	0.09	16	0.40	166
1500	0.71	127	2.92	36	0.09	13	0.43	160

TYPICAL CHARACTERISTICS

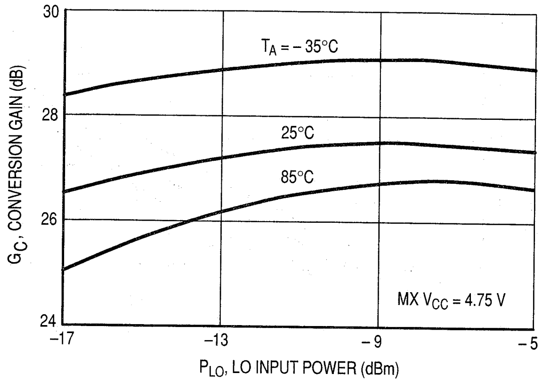


Figure 2. Mixer Gain versus LO Input Power

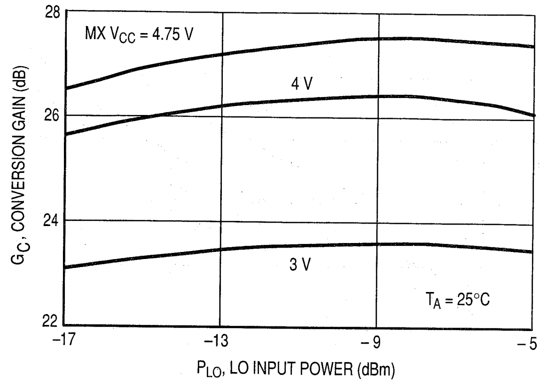


Figure 3. Mixer Gain versus LO Input Power

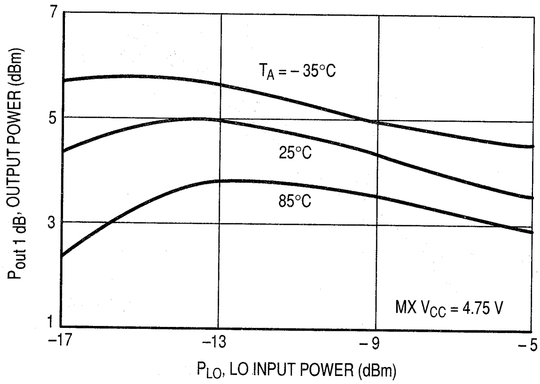


Figure 4. Mixer Output Power at 1 dB Gain Compression versus LO Input Power

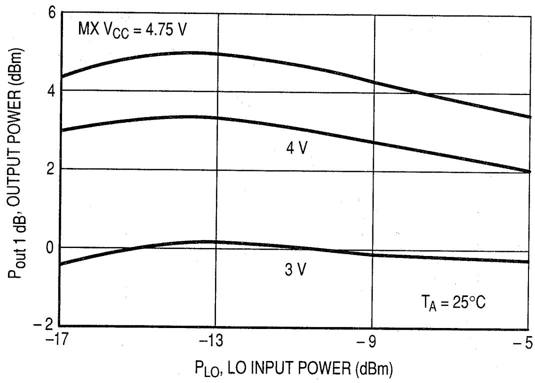


Figure 5. Mixer Output Power at 1 dB Gain Compression versus LO Input Power

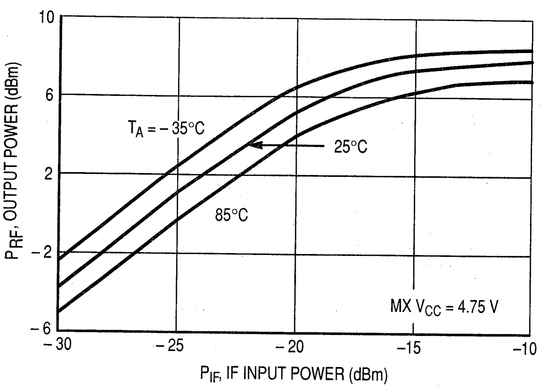


Figure 6. Mixer Output Power versus IF Input Power

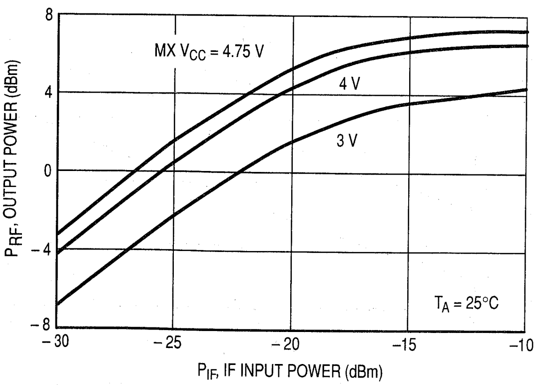


Figure 7. Mixer Output Power versus IF Input Power

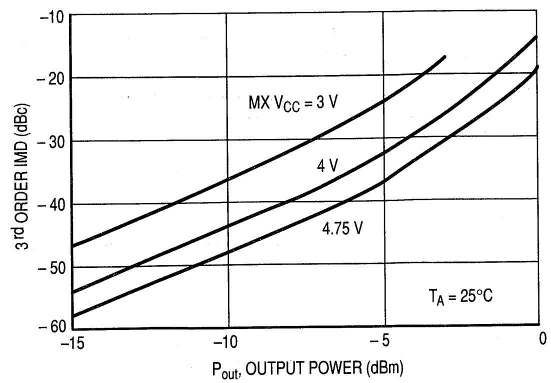


Figure 8. Mixer 3rd Order Intermodulation Distortion versus Output Power

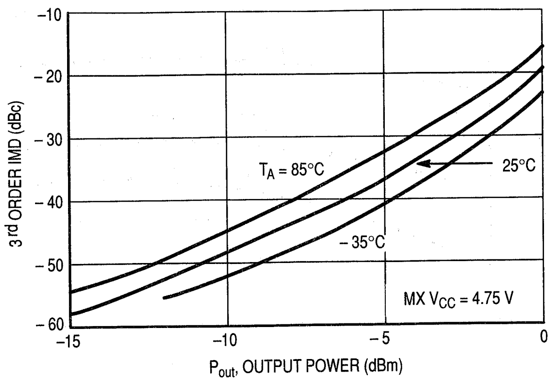


Figure 9. Mixer 3rd Order Intermodulation Distortion versus Output Power

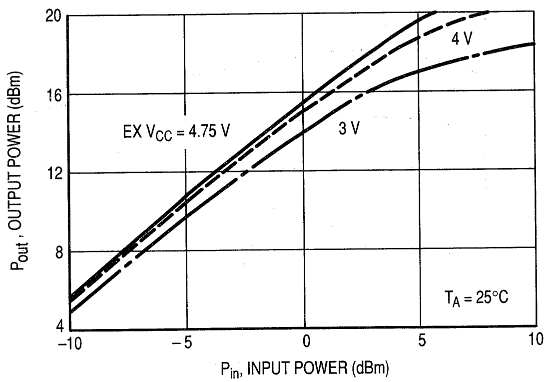


Figure 10. Exciter Output Power versus Input Power

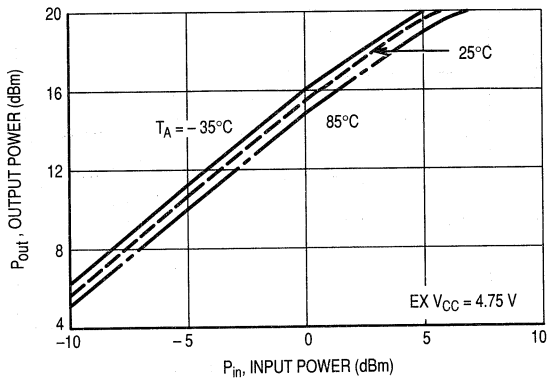


Figure 11. Exciter Output Power versus Input Power

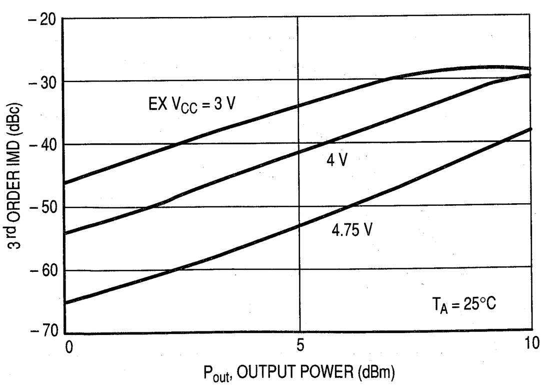


Figure 12. Exciter 3rd Order Intermodulation Distortion versus Output Power

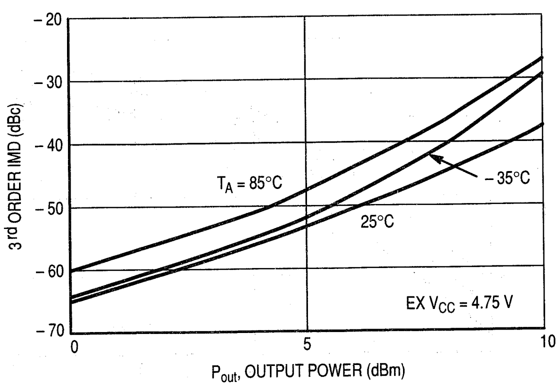


Figure 13. Exciter 3rd Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

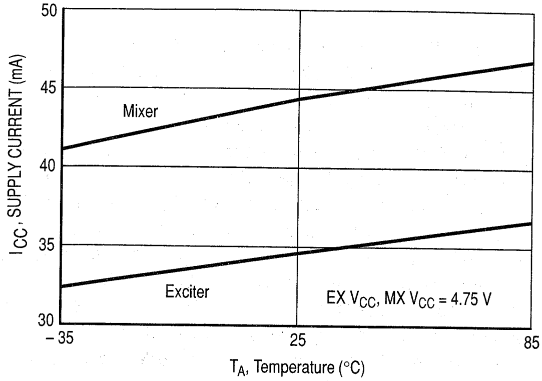


Figure 14. I_{CC} versus Temperature

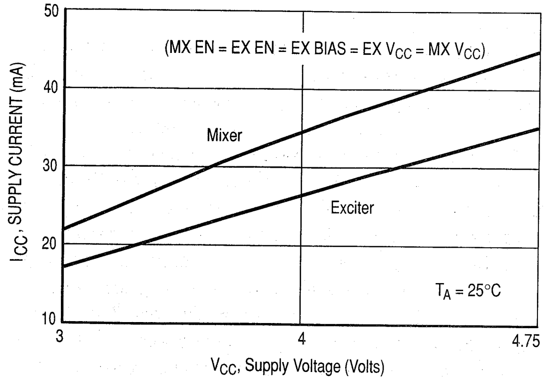


Figure 15. I_{CC} versus V_{CC}

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2101 was designed as a linear upconverter for U.S. and Japan digital cellular radios. However, it is versatile enough to be used in other applications such as analog cellular, GSM, CDMA and the 900 MHz ISM band.

The mixer is double-balanced to minimize spurious and LO emission. An external balun is required on the mixer RF output to maximize linearity and maintain good balance. An inexpensive and easy to implement balun is described below in the theory of operation. The IF and LO ports do not require baluns. The LO split is achieved on-chip with a buffer amplifier which also reduces the LO power requirement. The IF port can be driven differentially or single-ended with a decoupling capacitor on the unused IF input. Baseband signals can be applied directly to the IF inputs and the device becomes a complete low–power transmitter.

To maximize efficiency in various systems, the exciter bias current is externally adjustable. The bias current can also be ramped to reduce spectral splatter.

To minimize current drain in TDD/TDMA systems, the MRFIC2101 has separate TTL/CMOS compatible enable pins for the mixer and the exciter.

THEORY OF OPERATION

Matching the LO port to 50 ohms can be done several ways. The recommended approach is a series inductor as close to the IC as possible. The inductor value is small enough (~8 – 15 nH depending on LO frequency and distance from the IC) to be printed on the board. A DC block is required and should not be placed between the inductor and IC since the added electrical length will cause a poor match.

The IF ports are approximately 250 ohms resistive in parallel with 5.0 pF of capacitance. Matching directly into this impedance is not recommended. Series 82 nH chip inductors should first be placed as close to both IF ports as possible. This presents a high impedance to the IF ports at the LO frequency which substantially reduces the LO leakage out of the RF port. The resulting impedance then may be matched to the desired characteristic impedance. DC blocking capacitors are also required.

Both RF ports are approximately 25 ohms resistive in series with 1.5 pF of capacitance (or the parallel equivalent, 380 ohms in parallel with 1.9 pF). Best linearity is achieved by loading each port with 100 ohms resistive and resonating the 1.9 pF. Ideally, a half wavelength transmission line could be used to combine the two differential RF ports into one; however, the size of such a line would be very large. Any number of balun type network can be employed so long as the network presents 100 ohms to each port, resonates 1.9 pF capacitance at each port, and exhibits 180 degree phase difference between the two ports. The network shown in Figure 1 combines very well without a lot of added board space or complexity. Essentially, a quarter wavelength of transmission line (~1.5 inches of 50 ohms stripline in FR4) is used with additional phase shift coming from capacitors C12, C13 and C16. This network will operate anywhere from 800–1000 MHz by adjusting bias inductor L4 and C16 only.

The exciter input requires external matching and a DC block. It is best matched to 50 ohms using a short 50 ohms transmission line followed by a 5–10 pF shunt capacitor. The exciter output is approximately 50 ohms resistive in parallel with 4 pF of capacitance in the 800–1000 MHz range. It is best matched to 50 ohms using a 6–10 nH bias inductor placed as close to the IC as possible. The exciter is conditionally stable. Placing a 100-300 ohm resistor in parallel with the bias inductor, when driving large VSWR loads, may be needed to keep the exciter stable.

Supply decoupling must be done as close to the IC as possible. A 1000 pF capacitor is recommended. An additional 100 pF capacitor and an RF choke are recommended to keep the LO signal off the supply line.

Enabling/Disabling the MRFIC2101 can be done with the separate TTL/CMOS compatible enable pins for the mixer and exciter. The trip point is between 1 and 2 volts.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

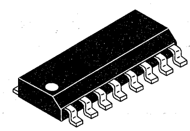
The MRFIC Line
2.4 GHz GaAs Downconverter

MRFIC2401

The MRFIC2401 is a GaAs low–noise amplifier and downmixer in a low–cost 16 lead plastic package designed for use in the 2.4 to 2.5 GHz Industrial–Scientific–Medical (ISM) band. The design is optimized for efficiency at 5.0 Volt operation at 2.45 GHz but is usable from 2.0 to 3.0 GHz in applications such as telemetry and Multichannel Multipoint Distribution System (MMDS) wireless cable TV systems. Performance is suitable for frequency hopping or direct sequence spread spectrum as well as single–frequency applications. LNA output and mixer input are available to allow image filtering.

- Single Supply Voltage = 5.0 Volts
- High Conversion Gain = 21 dB Typical Less Image Filter
- Low Supply Current = 9.5 mA Typical
- Low–Cost, Low Profile Plastic SOIC Package
- Order MRFIC2401R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2401

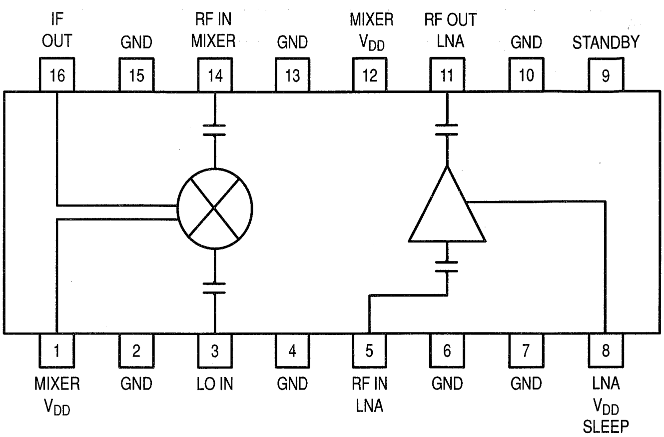
2.4 GHz
DOWNCONVERTER
GaAs MONOLITHIC
INTEGRATED CIRCUIT



CASE 751B-05
(SO-16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	Vdc
Input Power, RF IN Ports	P_{RF}	+5.0	dBm
Input Power, LO IN Port	P_{LO}	+5.0	dBm
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C
Bias Control Voltage	STANDBY	6.0	Vdc



Pin Connections and Functional Block Diagram

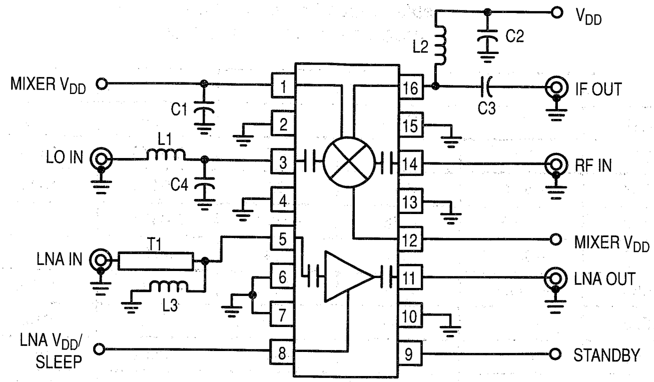
REV 3

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	4.75 to 5.25	Vdc
IF Frequency Range	f_{IF}	100 to 350	MHz
LO Drive Power Level	P_{LO}	–10 to 0	dBm
LO Frequency Range	f_{LO}	2050 to 2400	MHz
RF Frequency Range	f_{RF}	2400 to 2500	MHz
STANDBY Mode ON	STANDBY	V_{DD}	Vdc
STANDBY Mode OFF	STANDBY	0	Vdc
SLEEP Mode OFF	SLEEP	V_{DD}	Vdc
SLEEP Mode ON	SLEEP	0	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 Vdc, T_A = 25°C, RF = 2.45 GHz, LO = 2.125 GHz @ –5.0 dBm, STANDBY = 0 Vdc)

Characteristic	Min	Typ	Max	Unit
Conversion Gain – Downconverter (Less Image Filter Loss)	19	21	–	dB
Gain – LNA	–	17	–	dB
Conversion Gain – Mixer	–	4.0	–	dB
Noise Figure – LNA	–	1.9	–	dB
Noise Figure – Mixer	–	11	–	dB
Return Loss – Mixer Input, LO Input, LNA Output	–	10	–	dB
Input Third Order Intercept – Downconverter (Less Image Filter Loss)	–	–18	–	dBm
Input Third Order Intercept – LNA	–	–13	–	dBm
Input Third Order Intercept – Mixer	–	0	–	dBm
Reverse Isolation – Downconverter (Less Image Filter Loss)	–	30	–	dB
Isolation – LO to RF, LO to IF	–	20	–	dB
Supply Current – Downconverter	–	9.5	11	mA
SLEEP Mode Supply Current – Downconverter (No LO, STANDBY= 5 Vdc, V_{DD}/SLEEP = 5 Vdc)	–	600	–	µA
Turn On, Turn Off Time – LNA	–	1.0	–	µs



325 MHz IF:
C1, C2 – 100 pF
C3 – 5.6 pF
C4 – 0.5 pF
L1 – 4.7 nH
L2 – 8.2nH
L3 – 6.8 nH
T1 – 100 Ω Line, 92 MILS

240 MHz IF:
C1, C2 – 100 pF
C3 – 5.6 pF
C4 – 0.5 pF
L1 – 8.2 nH
L2 – 18 nH
L3 – 6.8 nH
T1 – 100 Ω Line, 92mils

Board Material – FR4

110 MHz IF:
C1 – 100 pF
C2 – 1000 pF
C3 – 8.2 pF
C4 – 0.3 pF
L1 – 8.2 nH
L2 – 82 nH
L3 – 6.8 nH
T1 – 100 Ω Line, 92 mils

Figure 1. Applications Circuit Configuration

f	LO Z_{in}	
Frequency (GHz)	**R**	**jX**
2.0	39.7	23.9
2.1	35.7	22.1
2.2	32.1	19.8
2.3	29.1	17.1
2.4	26.5	14.0
2.5	24.4	10.7

Table 1. Selected Port Impedances (from Conjugate Match)

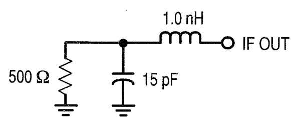


Figure 2. Equivalent IF Output Circuit

Table 2. LNA Scattering Parameters

(VDD = 5 V, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
2000	0.823	–50.8	5.35	14.3	0.0373	164.2	0.609	–64.1
2050	0.783	–62.9	6.13	–0.3	0.0425	154.3	0.558	–78.7
2100	0.752	–76.8	6.56	–18.3	0.0477	138	0.497	–94.3
2150	0.713	–89.8	6.8	–34	0.05	121	0.425	–110.7
2200	0.656	–104.2	7.14	–50.2	0.0511	106.4	0.343	–129.6
2250	0.583	–119	7.44	–66.4	0.0527	91.8	0.25	–152.3
2300	0.509	–134.1	7.8	–84.2	0.0554	78.1	0.155	176.2
2350	0.425	–148.2	7.86	–102.6	0.0579	59.89	0.088	120.7
2400	0.34	–163.6	7.84	–119.4	0.0552	42.31	0.111	43.8
2450	0.261	–177.8	7.78	–138.1	0.0528	28.27	0.191	2.2
2500	0.175	173.4	7.43	–154.6	0.0514	13.37	0.269	–21.9
2550	0.103	170.4	7.15	–170.6	0.0484	–0.842	0.338	–41.8
2600	0.056	–160.5	6.72	173	0.0455	–15.4	0.393	–59.4
2650	0.067	–130.7	6.47	159.1	0.0422	–28.11	0.436	–76.2
2700	0.102	–117.8	6.25	142.3	0.039	–41.5	0.472	–92.2
2750	0.132	–119.5	5.53	127.1	0.0353	–53.47	0.496	–107.5
2800	0.166	–125.2	5.26	117.5	0.0329	–63.28	0.513	–121.3
2850	0.19	–134.8	5.15	102.4	0.0309	–75.04	0.533	–135
2900	0.219	–144.8	4.71	87.6	0.0283	–87.86	0.547	–148.8
2950	0.235	–155.9	4.43	76.1	0.025	–95.83	0.559	–162.4
3000	0.262	–165.9	4.08	62.3	0.0235	–108.4	0.57	–175.7

TYPICAL CHARACTERISTICS

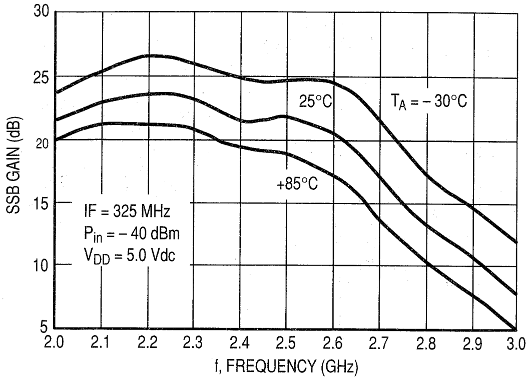


Figure 3. Downconverter Gain versus Frequency

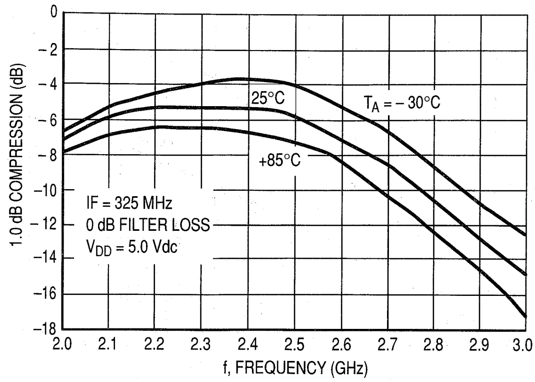


Figure 4. Downconverter 1.0 dB Compression versus Frequency

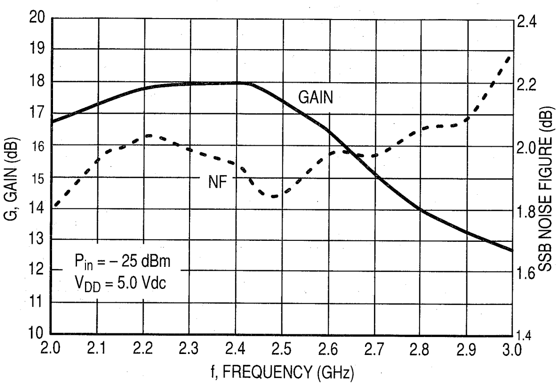


Figure 5. LNA Gain and Noise Figure versus Frequency

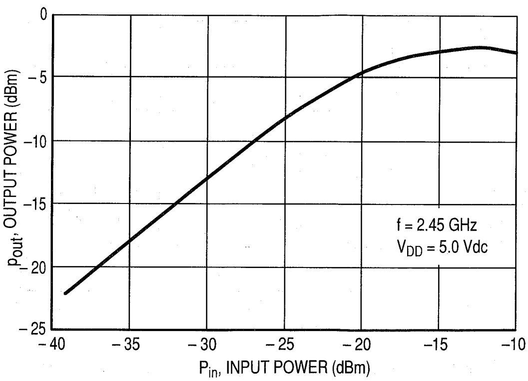


Figure 6. LNA Output Power versus Input Power

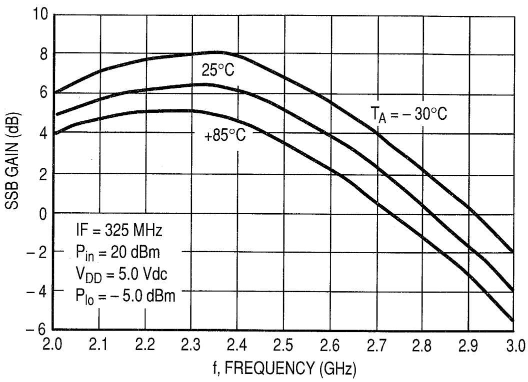


Figure 7. Mixer Conversion Gain versus Frequency

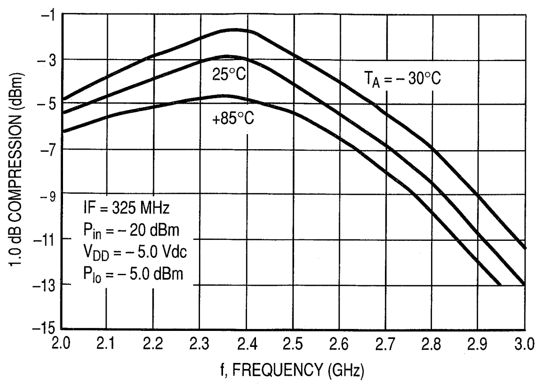


Figure 8. Mixer 1.0 dB Compression versus Frequency

TYPICAL CHARACTERISTICS

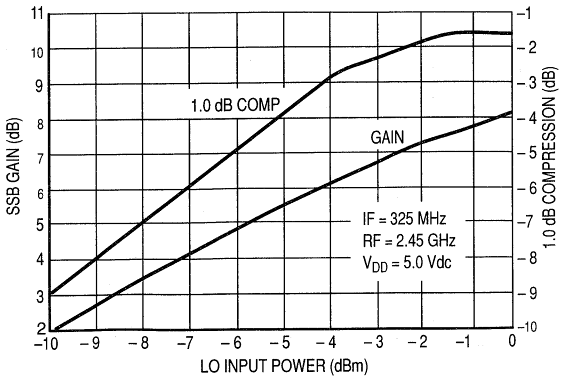


Figure 9. Mixer 1.0 dB Compression and Gain versus LO Power

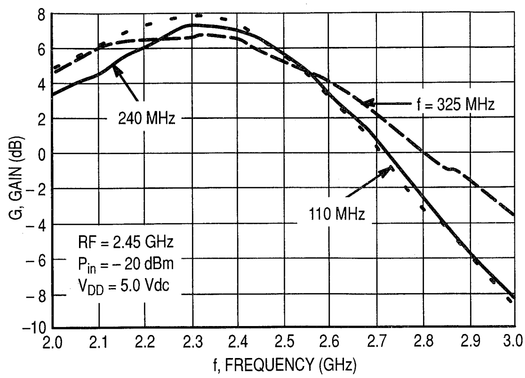


Figure 10. Mixer Gain versus Frequency

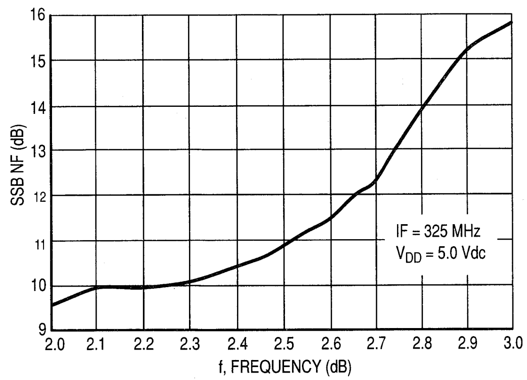


Figure 11. Mixer Noise Figure versus Frequency

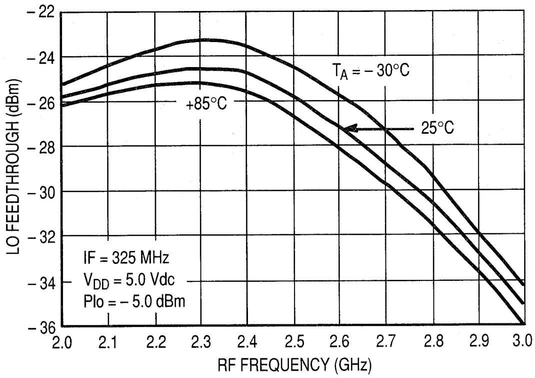


Figure 12. Mixer LO Feedthrough versus RF Frequency

DESIGN AND APPLICATIONS INFORMATION

The MRFIC2401 consists of a two–stage GaAs MESFET low noise amplifier and a single ended MESFET mixer. The LNA design conserves bias current through stacking of the two FETs, thus reusing the current. The mixer consists of a common gate stage driving a common source stage with the IF output being the drain of the common source stage shunted with 15 pF. The LNA output and mixer input have been separated to allow the addition of an external image filter. Such a filter, usually ceramic, is useful in improving the mixer noise figure and third order intercept performance. It also provides LO rejection to reduce the amount of LO power which may leak to the antenna. Alternatively, image trapping can be implemented at the LNA input or output with discrete or distributed components.

The design has been optimized for best performance from 2.4 to 2.5 GHz, but the device is usable with reduced performance from 2.0 to 3.0 GHz as shown in the performance curves. These curves were generated using the circuit shown in Figure 1 and performance above 2.5 GHz can be enhanced by rematching the LO input port. Matching circuit details are shown for IFs of 110 MHz, 240 MHz, and 325 MHz matched to 50 Ω and LO frequencies consistent with an RF frequency of 2.45 GHz. Customized IF matching can be accomplished by using the Equivalent IF Output circuit model shown in Figure 2. The best gain/noise figure tradeoff match is shown in the LNA input impedance column of Table 1. The LO input impedance is shown in the same table. These numbers are derived from conjugate match measurements of the applications circuit. The LNA output and mixer input are matched to 50 Ω.

As with all RF circuitry, layout is important. Controlled impedance lines should be used at all RF ports. RF bypassing of power supply connections as close to the part as possible, while not always shown in the applications circuit, are recommended. Additional power supply "stiffening" and digital transient bypassing should be accomplished with electrolytic or tantalum capacitors.

The device can be placed in a reduced current "standby" mode by applying 5.0 Vdc to the STANDBY pin and removing the LO drive. Further current reduction "sleep" mode, is enabled by applying 0 Vdc to V_{DD}/SLEEP. This sleep mode can also be used to disable the LNA under high signal level conditions and give higher input intercept point if V_{DD} is still applied to the mixer.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

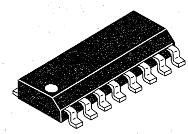
The MRFIC Line
2.4 GHz GaAs Power Amplifier

MRFIC2403

**2.4 GHz
POWER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT**

The MRFIC2403 is a two–stage class B GaAs power amplifier in a low–cost 16 lead plastic package designed for use in the 2.4 to 2.5 GHz Industrial–Scientific–Medical (ISM) band. The design is optimized for efficiency at 5.0 Volt operation at 2.5 GHz but is usable from 2.0 to 3.0 GHz in applications such as telemetry and Multichannel Multipoint Distribution System (MMDS) wireless cable TV systems. Performance is suitable for frequency hopping or direct sequence spread spectrum as well as single–frequency applications. Power control circuitry allows 20 dB dynamic range for setting the output power.

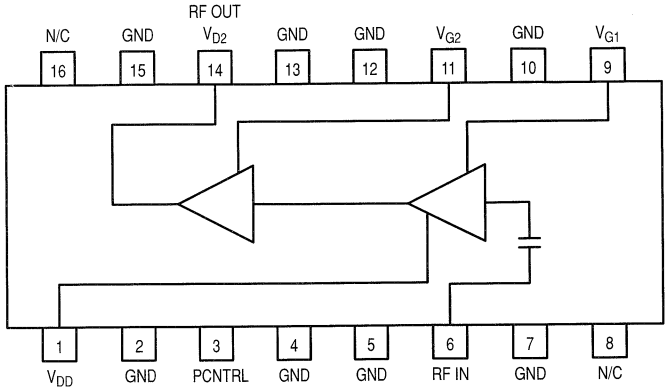
- High Output Power = +23.5 dBm Typical
- High Gain = 23 dB Typical
- Excellent Efficiency = 55% Typical
- Power Control = 20 dB Range
- Low–Cost, Low Profile Plastic SOIC Package
- Order MRFIC2403R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2403



**CASE 751B-05
(SO–16)**

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	Vdc
Power Control Voltage	V_{CONTRL}	6.0	Vdc
Gate Bias Voltage	V_{G1}, V_{G2}	–4.0	Vdc
RF Input Power	RF IN	+10	dBm
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C



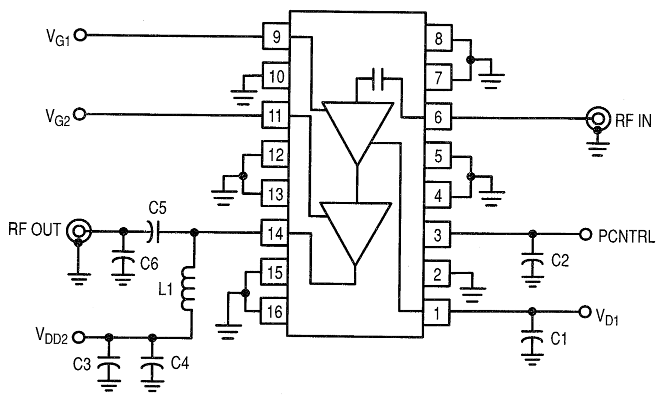
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	4.75 to 5.25	Vdc
Gate Bias Voltage, Input Stage	V_{G1}	–1.0	Vdc
Gate Bias Voltage, Output Stage	V_{G2}	–2.0	Vdc
Quiescent Drain Current, Stage One	I_{DQ1}	12	mA
Quiescent Drain Current, Stage Two	I_{DQ2}	10	mA
Operating Frequency Range	f_{OP}	2200 to 2700	MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 Vdc, T_A = 25°C, RF = 2.45 GHz @ +4.0 dBm, V_{G1} = –1.0 Vdc, V_{G2} = –2.0 Vdc, PCNTRL = 5.0 Vdc)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain (P_{in} = –6.0 dBm)	–	23	–	dB
Power Output (P_{in} = +4.0 dBm)	23	23.5	–	dBm
Power Output, Saturation	–	23.5	–	dBm
Power Output, 1.0 dB Compression	–	19	–	dBm
2nd Harmonic Output	–	–20	–	dBc
3rd Harmonic Output	–	–30	–	dBc
Third Order Intermodulation Products (P_{in} = +4.0 dBm PEP)	–	–15	–	dBc
Reverse Isolation	–	32	–	dB
Power Control Range, PCNTRL	–	20	–	dB
Reverse Isolation	–	30	–	dB
Supply Current	–	95	140	mA
SLEEP Mode Supply Current (VG1 = VG2 = –3.0 Vdc, PCNTRL = 0 Vdc)	–	150	–	μA



C1, C2, C3 – 0.01 μF
C4 – 5.1 pF
C5 – 15 pF
C6 – 1.0 pF
L1 – 6.8 nH
Board Material – 30 MIL FR4
Connectors – SMA type

Figure 1. Applications Circuit Configuration

Table 1. Class A Scattering Parameters

(VDD = 5 V, I_{DQ1} = 24 mA, I_{DQ2} = 96 mA, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
2000	0.377	–157.00	27.625	57.40	0.004	–74.70	0.740	–102.10
2050	0.218	–171.70	28.938	36.80	0.006	–101.60	0.763	–115.30
2100	0.075	–178.80	29.088	17.20	0.007	–130.70	0.724	–126.80
2150	0.049	–96.10	27.904	–0.20	0.007	–163.20	0.663	–135.80
2200	0.104	–56.60	26.930	–14.90	0.008	–169.60	0.601	–141.80
2250	0.130	–60.60	24.246	–27.80	0.009	173.50	0.550	–146.30
2300	0.125	–65.40	24.286	–39.40	0.010	165.00	0.504	–149.10
2350	0.106	–67.60	22.287	–49.60	0.010	157.70	0.471	–151.60
2400	0.083	–56.10	21.867	–59.80	0.009	140.70	0.444	–153.80
2450	0.064	–27.00	21.837	–68.90	0.011	141.40	0.422	–155.90
2500	0.072	26.20	20.113	–78.00	0.012	139.80	0.401	–158.60
2550	0.110	44.60	19.828	–86.40	0.009	140.00	0.385	–161.20
2600	0.160	44.50	18.941	–94.30	0.007	124.50	0.364	–164.50
2650	0.194	40.60	18.001	–101.90	0.012	128.30	0.350	–167.70
2700	0.237	36.60	17.268	–109.20	0.011	102.30	0.335	–171.40
2750	0.269	31.30	16.379	–116.30	0.010	110.90	0.317	–174.50
2800	0.304	25.50	15.826	–123.40	0.009	105.80	0.311	–178.60
2850	0.325	19.80	15.125	–130.40	0.010	103.60	0.292	177.50
2900	0.345	14.50	14.611	–137.50	0.008	99.70	0.279	172.80
2950	0.356	9.40	14.048	–143.60	0.009	92.80	0.271	168.90
3000	0.370	2.40	13.663	–150.40	0.011	88.20	0.259	163.80

Table 2. Class B Scattering Parameters
(VDD = 5 V, I_{DQ1} = 12 mA, I_{DQ2} = 10 mA, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
2000	0.634	–149.00	12.40	88.00	0.007	–59.00	0.893	–81.00
2050	0.554	–170.00	14.76	72.00	0.013	–81.00	0.966	–89.00
2100	0.456	163.00	17.00	53.00	0.015	–95.00	0.990	–100.00
2150	0.362	129.00	18.09	32.00	0.017	–117.00	0.955	–110.00
2200	0.310	91.00	18.81	12.00	0.020	–138.00	0.870	–119.00
2250	0.298	58.00	17.37	–5.00	0.021	–156.00	0.771	–125.00
2300	0.298	30.00	17.22	–21.00	0.021	–169.00	0.681	–128.00
2350	0.289	11.00	15.89	–34.00	0.020	179.00	0.612	–130.00
2400	0.275	0.00	14.74	–45.00	0.020	168.00	0.562	–130.00
2450	0.248	–8.00	15.35	–56.00	0.021	155.00	0.528	–131.00
2500	0.216	–10.00	13.62	–66.00	0.019	147.00	0.498	–131.00
2550	0.199	–8.00	13.46	–75.00	0.021	143.00	0.473	–132.00
2600	0.187	–2.00	12.95	–83.00	0.020	134.00	0.447	–132.00
2650	0.185	4.00	12.32	–91.00	0.020	129.00	0.426	–134.00
2700	0.202	10.00	11.78	–99.00	0.021	123.00	0.405	–135.00
2750	0.218	13.00	11.25	–107.00	0.021	115.00	0.384	–136.00
2800	0.244	14.00	10.83	–114.00	0.018	106.00	0.373	–137.00
2850	0.268	13.00	10.34	–121.00	0.019	98.00	0.353	–139.00
2900	0.285	10.00	10.05	–129.00	0.019	99.00	0.332	–140.00
2950	0.301	7.00	9.61	–135.00	0.018	102.00	0.316	–143.00
3000	0.317	3.00	9.46	–142.00	0.018	90.00	0.302	–145.00

TYPICAL CHARACTERISTICS

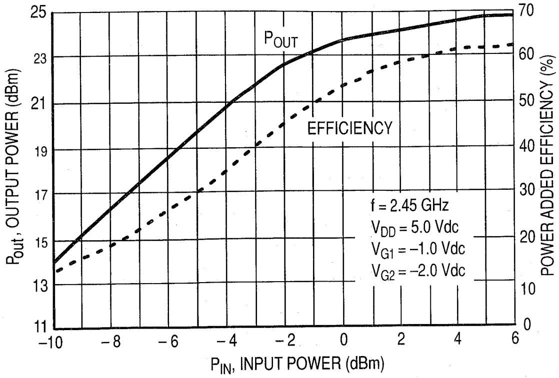


Figure 2. Output Power and Efficiency versus Input Power

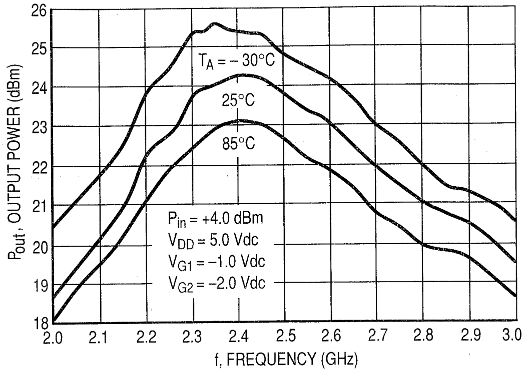


Figure 3. Output Power versus Frequency

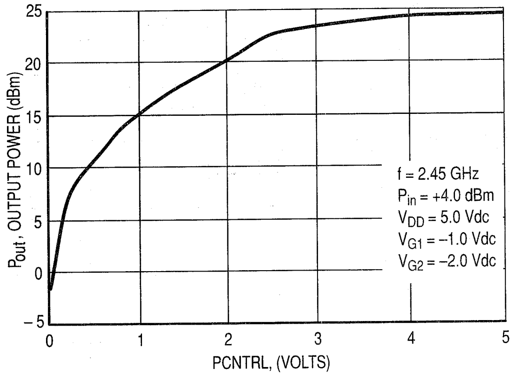


Figure 4. Output Power versus PCNTRL Voltage

DESIGN AND APPLICATIONS INFORMATION

The MRFIC2403 is a two–stage power amplifier designed using Motorola's MAFET planar, refractory gate MESFET IC process. The RF MESFETs are power, depletion mode devices and, therefore, require negative bias on the MESFET gates. For class B operation, –1.0 Vdc is applied to V_{G1} and –2.0 Vdc is applied to V_{G2}. Class A biasing will yield slightly higher gain and 1.0 dB compression point and can be accomplished by adjusting the bias on VG1 for I_{DQ1} = 24 mA and V_{G2} for I_{DQ2} = 96 mA. Where negative voltages are not already available, Motorola's MC33128 Power Management IC can produce –2.5 Vdc from a single positive supply.

The device is capable of better than +23 dBm saturated output power in the 2.4 to 2.5 GHz ISM band with the output matching circuit shown in Figure 1. The device can be operated at other frequencies in the 2.0 GHz to 3.0 GHz range with this circuit but performance can be improved with tuning for the specific frequency of use. Input matching is provided on chip. This circuit provides the best gain, saturated output power and efficiency tradeoff. Saturated operation has the advantage of best efficiency with less variation in performance over frequency and temperature. Operation in saturation is acceptable for constant envelope modulation schemes such as 2 and 4 level FM as specified for frequency hopping (FHSS) radios in the proposed IEEE 802.11 PHY layer specification. For direct sequence (DSSS) IEEE 802.11 operation, where differential binary phase shift keying (DBPSK) and differential quadrature phase shift keying (DQPSK) are specified, the amplifier will have to be "backed off" from saturation by 5.0 dB or more to avoid spectral regrowth. Care must be taken in the layout of the circuit and controlled impedance lines must be used at the RF pins. Capacitive bypassing as shown in the Applications Circuit must be implemented as close to the chip as possible to avoid amplifier instability. Additionally, the supply voltage should be supported by sufficient "stiffening" capacitance, typically electrolytic or tantalum bypass capacitors, to eliminate noise from digital circuits.

Output power control is accomplished by varying the voltage on the PCNTRL pin. 0 Vdc gives minimum output and reduces the current drawn by the amplifier to the quiescent value. The amplifier can be put into "sleep" mode by decreasing the voltage on the gate bias pins to –3.0 Vdc and the current drain is reduced to a few hundred microamps.

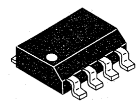
EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

The MRFIC Line
2.4 GHz GaAs Exciter Amplifier

MRFIC2404

**2.4 GHz
EXCITER AMPLIFIER
GaAs MONOLITHIC
INTEGRATED CIRCUIT**



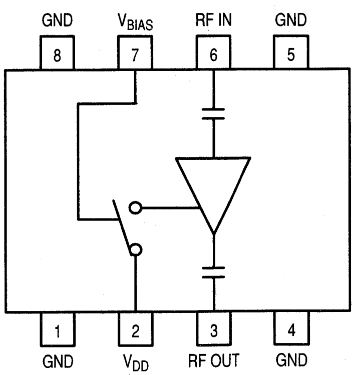
**CASE 751-05
(SO-8)**

The MRFIC2404 is a single–stage class A GaAs amplifier in a low–cost 8 lead plastic package designed to drive the MRFIC2403 power amplifier for use in the 2.4 to 2.5 GHz Industrial–Scientific–Medical (ISM) band. The design is optimized for 5.0 Volt operation at 2.45 GHz but is usable from 2.0 to 3.0 GHz in applications such as telemetry and Multichannel Multipoint Distribution System (MMDS) wireless cable TV systems. Performance is suitable for frequency hopping or direct sequence spread spectrum as well as single–frequency applications.

- High Output Capability = +5.0 dBm Typical
- High Gain = 17 dB Typical
- Low Current Drain = 9.0 mA Typical
- Single Supply Voltage = 5.0 Volts
- Good Noise Figure = 4.3 dB Typical
- Low–Cost, Low Profile Plastic SOIC Package
- Order MRFIC2404R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 12 mm, 13 inch Reel.
- Device Marking = M2404

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	12	Vdc
RF Input Power	RF IN	+10	dBm
Bias Enable Voltage	V_{bias}	6.0	Vdc
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C



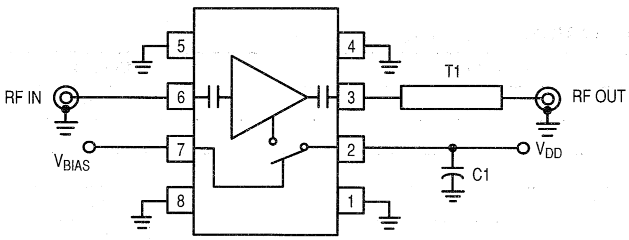
Pin Connections and Functional Block Diagram

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	4.75 to 5.25	Vdc
Bias Enable Voltage – ON	V_{bias}	0	Vdc
Bias Enable Voltage – OFF	V_{bias}	5.0	Vdc
Operating Frequency Range	f_{OP}	2000 to 3000	MHz

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 Vdc, T_A= 25°C, RF = 2.45 GHz, V_{bias} = 0 Vdc)

Characteristic	Min	Typ	Max	Unit
Small Signal Gain	16	17	–	dB
Power Output, 1.0 dB Compression	–	+5.0	–	dBm
Power Output (P_{in} = –11 dBm)	4.0	5.0	–	dBm
Third Order Intercept Point	–	+15	–	dBm
Noise Figure	–	4.3	–	dB
Reverse Isolation	–	25	–	dB
Turn On Time	–	1.0	–	μs
Supply Current	–	9.0	12	mA
SLEEP Mode Supply Current (V_{bias} = 5.0 Vdc)	–	800	–	μA



C1 – 15 pF
T1 – 100 Ω Line, 185 MILs (3.3 nH)
Board Material – 30 MIL FR4
Connectors – SMA Type

Figure 1. Applications Circuit Configuration

Table 1. Scattering Parameters
(VDD = 5 V, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	∠ ϕ	$\|S_{21}\|$	∠ ϕ	$\|S_{12}\|$	∠ ϕ	$\|S_{22}\|$	∠ ϕ
2000	0.232	–92.34	6.290	165.97	0.024	–51.08	0.483	–123.13
2050	0.174	–90.78	7.049	147.75	0.029	–66.26	0.383	–125.77
2100	0.122	–76.88	7.563	127.95	0.032	–78.38	0.281	–124.34
2150	0.102	–48.38	7.803	109.02	0.035	–97.84	0.191	–109.23
2200	0.128	–19.45	8.046	91.04	0.037	–105.62	0.159	–80.33
2250	0.185	–6.60	8.144	72.36	0.039	–123.88	0.196	–53.35
2300	0.244	–5.52	7.977	55.31	0.038	–135.36	0.273	–42.38
2350	0.300	–8.04	7.979	39.91	0.043	–144.83	0.350	–41.15
2400	0.343	–12.42	8.147	23.40	0.044	–160.94	0.423	–43.39
2450	0.379	–17.11	8.020	5.27	0.045	–173.09	0.477	–47.05
2500	0.403	–21.90	7.550	–10.93	0.041	173.83	0.522	–50.67
2550	0.424	–26.32	7.245	–25.36	0.043	165.85	0.556	–54.67
2600	0.436	–30.95	6.911	–39.88	0.042	154.14	0.582	–58.35
2650	0.443	–34.94	6.631	–52.32	0.041	145.35	0.600	–62.23
2700	0.447	–39.48	6.566	–65.57	0.044	135.12	0.610	–65.41
2750	0.445	–43.12	6.338	–79.97	0.043	123.72	0.622	–68.57
2800	0.446	–46.68	6.009	–93.15	0.042	114.52	0.624	–72.06
2850	0.441	–50.42	5.733	–105.10	0.043	107.18	0.620	–74.86
2900	0.439	–53.14	5.565	–116.69	0.041	98.95	0.617	–77.74
2950	0.437	–57.27	5.393	–129.54	0.042	90.72	0.608	–80.01
3000	0.409	–61.28	4.938	–142.70	0.043	81.68	0.611	–81.12

Typical Characteristics

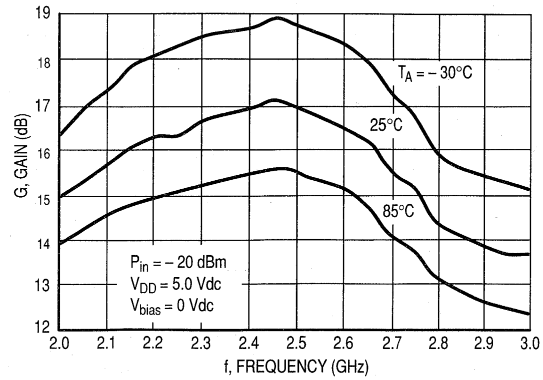


Figure 2. Gain versus Frequency

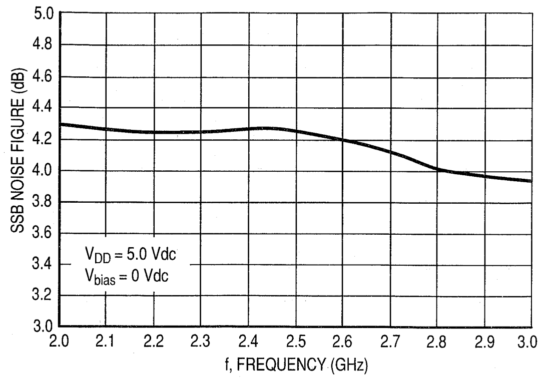


Figure 3. Noise Figure versus Frequency

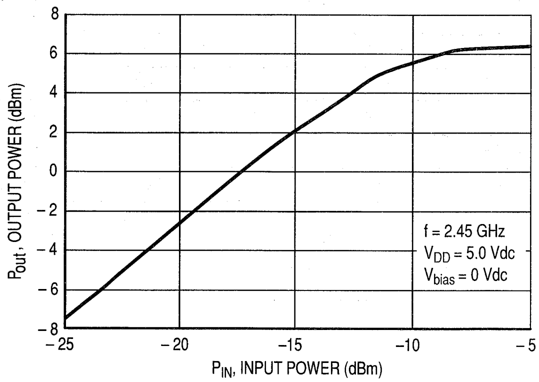


Figure 4. Output Power versus Input Power

DESIGN AND APPLICATIONS INFORMATION

The MRFIC2404 is a single–stage GaAs amplifier designed for exciter applications such as driving the MRFIC2403 power amplifier. The 4.3 dB noise figure, 17 dB gain and +5.0 dBm power output at 1.0 dB gain compression make the MRFIC2404 suitable for high–performance receiver IF application, Multichannel Multipoint Distribution System (MMDS) applications, telemetry and other applications in the 2.0 to 3.0 GHz range.

The characterization curves show typical performance in the 2.0 to 3.0 GHz range in the circuit shown in Figure 1. This circuit was also used to derive the device impedance shown in Table 1. The amplifier input is matched to 50 Ω while the output requires about 3.3 nH series inductance for best match at 2.45 GHz. The V_{DD} supply line should be bypassed as close to the chip as possible to avoid low frequency oscillations. Power supply "stiffening" and digital transient bypassing in the form of electrolytic of tantalum capacitors should be added.

The device can be put into a reduced current "sleep" mode by 5.0 Vdc to the V_{bias} pin.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

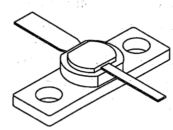
The RF Line
Microwave Power Transistors

MRW2001
MRW2003

Designed primarily for large–signal output and driver amplifier stages in the 1.0 to 2.3 GHz frequency range.

- Designed for Class B or C, Common Base Power Amplifiers
- Specified 28 Volt, 2.0 GHz Characteristics:
  Output Power — 1.0 to 20 Watts
  Power Gain — 5.2 to 9.0 dB, Min
  Collector Efficiency — 40%, Min
- Gold Metallization for Improved Reliability
- Diffused Ballast Resistors
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

5.2–9.0 dB
1.0–2.3 GHz
1.0 – 20 W
MICROWAVE
POWER TRANSISTORS



CASE 328A–03, STYLE 1
(GP–13)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CES}	50	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous MRW2001 MRW2003	I_C	 0.25 0.5	Adc
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, RF, Junction to Case MRW2001 MRW2003	$R_{\theta JC}$	 25 15	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{BE} = 0) MRW2001 (I_C = 20 mA, V_{BE} = 0) MRW2003	$V_{(BR)CES}$	 50 50	 — —	 — —	Vdc

(continued)

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ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (continued)						
Emitter–Base Breakdown Voltage		$V_{(BR)EBO}$				Vdc
(I_E = 0.2 mA, I_C = 0)	MRW2001		3.5	—	—	
(I_E = 0.25 mA, I_C = 0)	MRW2003		3.5	—	—	
Collector Cutoff Current	MRW2001	I_{CBO}	—	—	0.5	mAdc
(V_{CB} = 28 V, I_E = 0)	MRW2003		—	—	0.5	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				—
(I_C = 100 mA, V_{CE} = 5.0 V)	MRW2001		10	—	120	
(I_C = 100 mA, V_{CE} = 5.0 V)	MRW2003		10	—	100	
DYNAMIC CHARACTERISTICS						
Output Capacitance	MRW2001	C_{ob}	—	—	4.0	pF
(V_{CB} = 28 V, I_E = 0, f = 1.0 MHz)	MRW2003		—	—	5.0	
FUNCTIONAL TESTS						
Common–Base Amplifier Power Gain (V_{CE} = 28 V, P_{out} = 1.0 W, f = 2.0 GHz)	MRW2001	G_{PB}	9.0	—	—	dB
Common–Base Amplifier Power Gain (V_{CE} = 28 V, P_{out} = 3.0 W, f = 2.0 GHz)	MRW2003	G_{PB}	8.0	—	—	dB
Collector Efficiency		η	40	—	—	%
(V_{CE} = 28 V, P_{out} = 1.0 W, f = 2.0 GHz)	MRW2001					
(V_{CE} = 28 V, P_{out} = 3.0 W, f = 2.0 GHz)	MRW2003					
Load Mismatch (V_{CE} = 28 V, f = 2.0 GHz, Load VSWR = ∞:1, All Phase Angles)		ψ	No Degradation in Output Power			
P_{out} = 1.0 W	MRW2001					
P_{out} = 3.0 W	MRW2003					
Saturated Output Power						W
(V_{CE} = 28 V, f = 2.3 GHz)	MRW2001	$P_{sat\,1}$	—	1.0	—	
(V_{CE} = 28 V, f = 1.5 GHz)		$P_{sat\,2}$	—	1.2	—	
(V_{CE} = 28 V, f = 1.0 GHz)		$P_{sat\,3}$	—	1.3	—	
(V_{CE} = 28 V, f = 2.3 GHz)	MRW2003		—	3.0	—	
(V_{CE} = 28 V, f = 1.5 GHz)			—	3.7	—	
(V_{CE} = 28 V, f = 1.0 GHz)			—	4.0	—	

TYPICAL CHARACTERISTICS

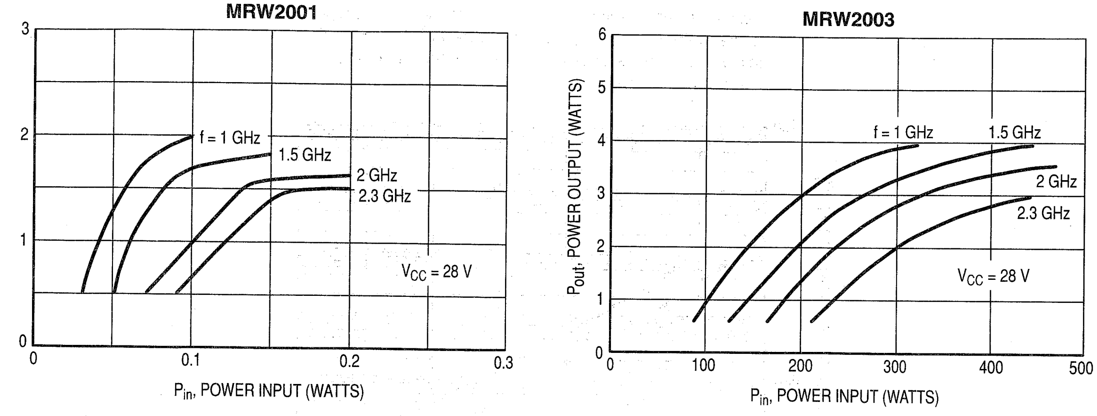


Figure 1. Output Power versus Input Power

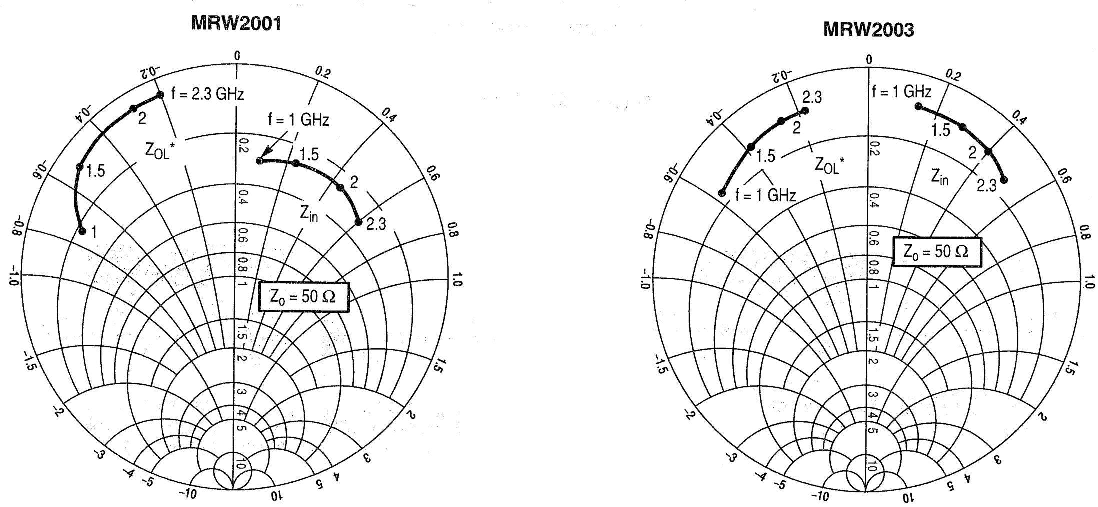


Figure 2. Series Equivalent Input/Output Impedance
V_{CC} = 28 V

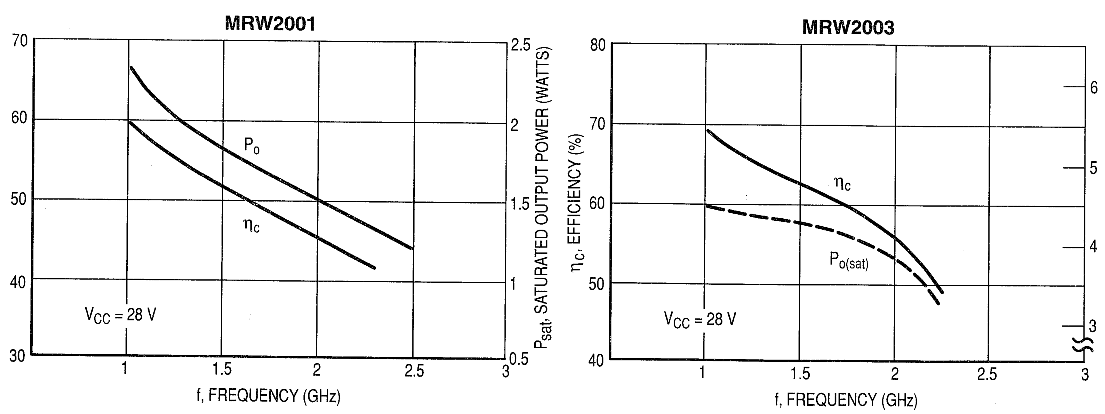


Figure 3. Power Output and Efficiency versus Frequency

The graph shown below displays MTTF in hours x ampere^2 emitter current for each of the "Super 2.0 GHz" devices. Life tests at elevated temperatures have correlated to better than ±10% to the theoretical prediction for metal failure. Sample MTTF calculations based on operating conditions are included on the graph.

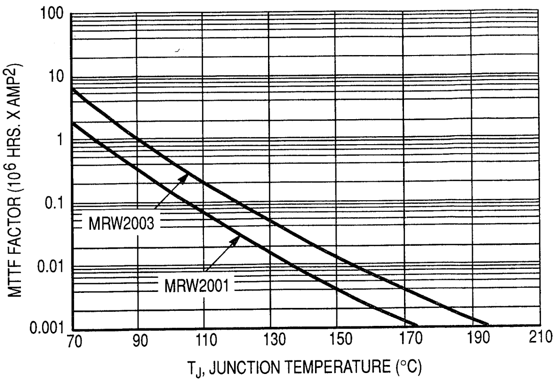


Figure 4. MTTF Factor

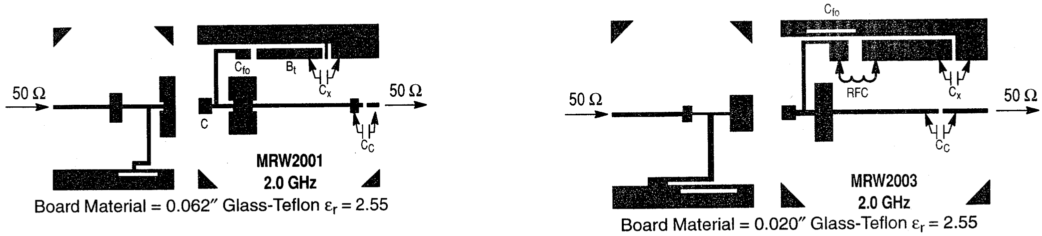


Figure 5. PC Board Layouts

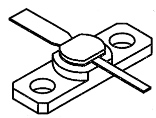
The RF Line
Microwave Power Transistors

MRW3001
MRW3003
MRW3005

. . . designed primarily for large–signal output and driver amplifier stages in the 1.5 to 3.0 GHz frequency range.

- Designed for Class B or C, Common Base Linear Power Amplifiers
- Specified 28 Volt, 3.0 GHz Characteristics:
  Output Power — 1.0 to 5.0 Watts
  Power Gain — 5.0 to 7.0 dB Min
  Collector Efficiency — 30% Min
- Gold Metallization for Improved Reliability
- Diffused Ballast Resistors
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

5.0–7.0 dB
1.5–3.0 GHz
1.0–5.0 WATTS
MICROWAVE
POWER TRANSISTORS



CASE 328A–03, STYLE 1
(GP–13)
MRW3001, 3003, 3005

MAXIMUM RATINGS

Rating	Symbol	3001	3003	3005	Unit
Collector–Base Voltage	V_{CBO}	45			Vdc
Emitter–Base Voltage	V_{EBO}	3.5			Vdc
Operating Junction Temperature	T_J	200			°C
Storage Temperature Range	T_{stg}	−65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max			Unit
Thermal Resistance, RF, Junction to Case	$R_{\theta JC}$	35	17	8.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage		$V_{(BR)CES}$				Vdc
(I_C = 10 mA, V_{BE} = 0)	MRW3001		50	—	—	
(I_C = 30 mA, V_{BE} = 0)	MRW3003		50	—	—	
(I_C = 50 mA, V_{BE} = 0)	MRW3005		50	—	—	
Collector–Base Breakdown Voltage		$V_{(BR)CBO}$				Vdc
(I_C = 1.0 mA, I_E = 0)	MRW3001		45	—	—	
(I_C = 3.0 mA, I_E = 0)	MRW3003		45	—	—	
(I_C = 5.0 mA, I_E = 0)	MRW3005		45	—	—	
Emitter–Base Breakdown Voltage (I_E = 1.0 mA, I_C = 0)		$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 V, I_E = 0)	MRW3001	I_{CBO}	—	—	0.5	mAdc
	MRW3003		—	—	0.75	
	MRW3005		—	—	1.25	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				—
(I_C = 100 mA, V_{CE} = 5.0 V)	MRW3001		10	—	120	
(I_C = 300 mA, V_{CE} = 5.0 V)	MRW3003		10	—	120	
(I_C = 500 mA, V_{CE} = 5.0 V)	MRW3005		10	—	120	

(continued)

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ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 28 V, I_E = 0, f = 1.0 MHz)	MRW3001	C_{ob}	—	3.5	4.0	pF
	MRW3003		—	5.7	7.0	
	MRW3005		—	8.4	10	
FUNCTIONAL TESTS						
Common–Base Amplifier Power Gain		G_{PB}				dB
(V_{CE} = 28 V, P_{out} = 1.0 W, f = 3.0 GHz)	MRW3001		7.0	—	—	
(V_{CE} = 28 V, P_{out} = 3.0 W, f = 3.0 GHz)	MRW3003		6.0	—	—	
(V_{CE} = 28 V, P_{out} = 5.0 W, f = 3.0 GHz)	MRW3005		5.0	—	—	
Collector Efficiency		η_c				%
(V_{CE} = 28 V, P_{out} = 1.0 W, f = 3.0 GHz)	MRW3001		30	—	—	
(V_{CE} = 28 V, P_{out} = 3.0 W, f = 3.0 GHz)	MRW3003		30	—	—	
(V_{CE} = 28 V, P_{out} = 5.0 W, f = 3.0 GHz)	MRW3005		30	—	—	
Load Mismatch (V_{CE} = 28 V, f = 3.0 GHz, Load VSWR = ∞:1, All Phase Angles)		ψ	No Degradation in Output Power			
P_{out} = 1.0 W	MRW3001					
P_{out} = 3.0 W	MRW3003					
P_{out} = 5.0 W	MRW3005					

MRW3001
TYPICAL CHARACTERISTICS

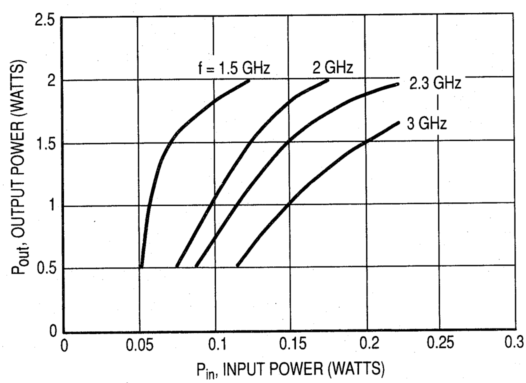


Figure 1. Output Power versus Input Power

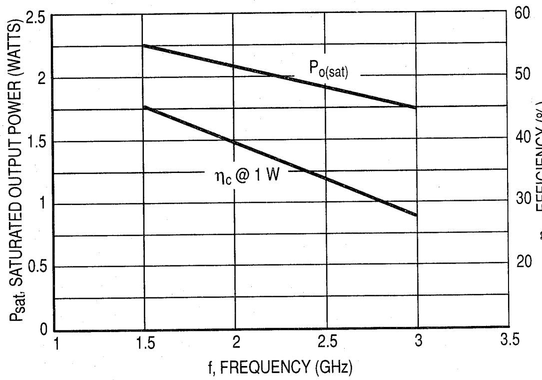


Figure 2. P_{sat} and η versus Frequency

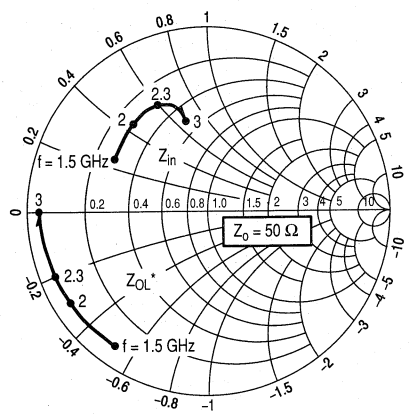


Figure 3. Series Equivalent Input/Output Impedance

TYPICAL CHARACTERISTICS

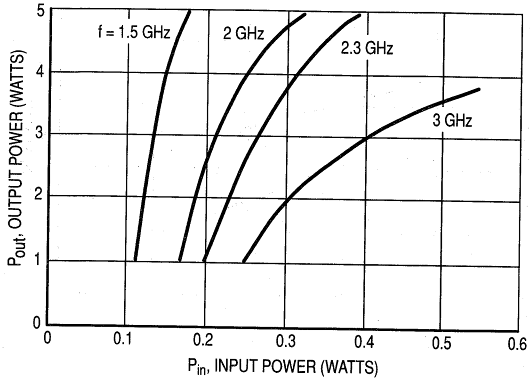


Figure 4. Output Power versus Input Power

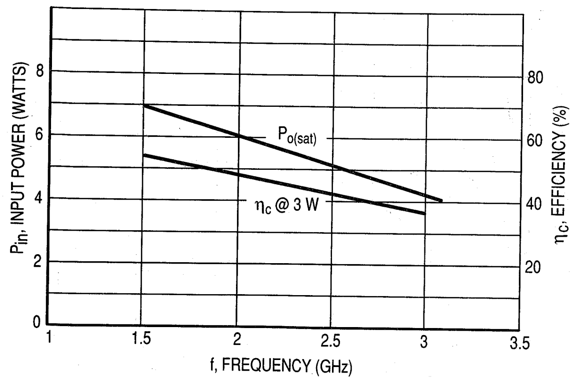


Figure 5. P_{sat} and η versus Frequency

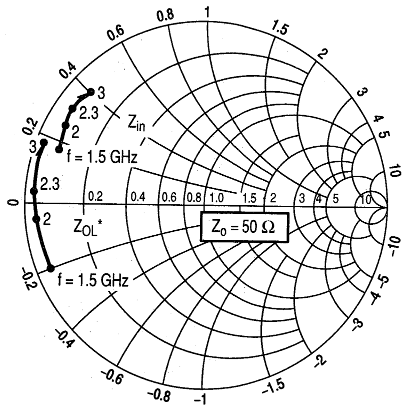


Figure 6. Series Equivalent Input/Output Impedance

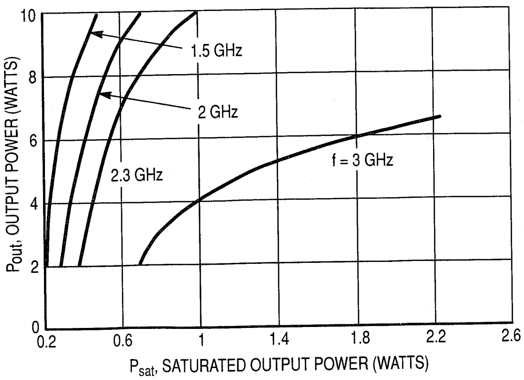


Figure 7. Output Power versus Input Power

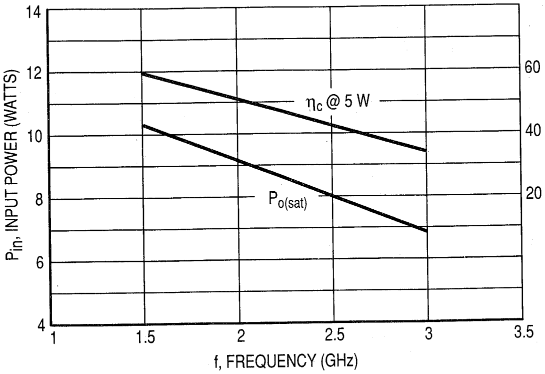


Figure 8. P_{sat} and η versus Frequency

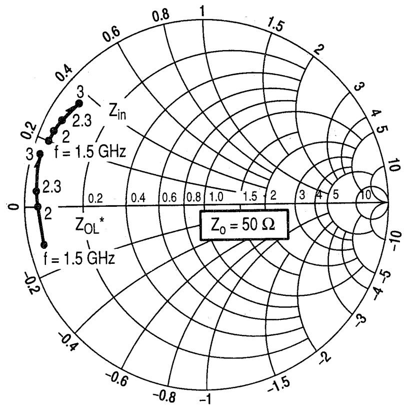


Figure 9. Series Equivalent Input/Output Impedance

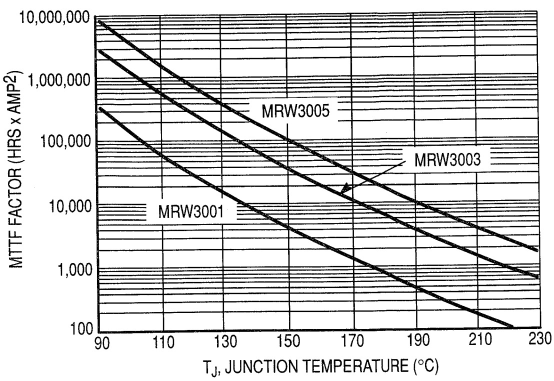


Figure 10. MTTF Factor versus Junction Temperature

MTTF Factor
(Normalized to 1.0 ampere² Continuous Duty)

The graph shown displays MTTF in hours x ampere² emitter current for each of the 3.0 GHz devices. Life tests at elevated temperatures have correlated to better than ±10% to the theoretical prediction for metal failure. **CAUTION** — A calculation is required to obtain actual metal life. Sample MTTF calculations based on operating conditions are shown below.

Junction Temperature — °C

To calculate metal lifetime under any set of conditions, obtain actual data or estimate from typical performance curves. Solve for T_J (°C):

$$(1)\ T_J = \theta_{JF}\left(\frac{P_{out} \times 100}{\eta_C\ \%} + P_{in} - P_{out}\right) + T_{FLANGE}$$

Enter graph of MTF factor versus T_J. Obtain MTF factor. Calculate metal life by:

$$(2)\ \text{Metal Life in Hours} = \frac{\text{MTF Factor}}{I_C^2\ (\text{Amps})}$$

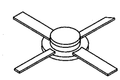
The RF Line
Microwave Linear Power Transistors

MRW54001

. . . designed primarily for large–signal output and driver amplifier stages in the 1.0 to 4.0 GHz frequency range.

- Designed for Class A or AB, Common–Emitter Linear Power Amplifiers
- Specified 20 Volt, 2.0 GHz Characteristics:
  Output Power — 0.5 Watt
  Power Gain — 10 to 11 dB
- 100% Tested for Load Mismatch at All Phase Angles with ∞:1 VSWR
- Gold Metallization for Improved Reliability
- Diffused Ballast Resistors

10–11 dB
1.0–4.0 GHz
0.5 WATT
MICROWAVE LINEAR
POWER TRANSISTORS



CASE 400–01, STYLE 1
(TW200)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	22	Vdc
Collector–Base Voltage	V_{CES}	50	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	40	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mA, I_B = 0)	$V_{(BR)CEO}$	22	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 10 mA, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 1.0 mA, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 0.25 mA, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 V, I_E = 0)	I_{CBO}	—	—	0.25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mA, V_{CE} = 5.0 V)	h_{FE}	20	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 V, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	3.5	pF

(continued)

REV 1

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CE} = 20 V, P_{out} = 0.5 W, f = 2.0 GHz, I_E = 120 mA)	G_{PE}	10	—	—	dB
Load Mismatch (V_{CE} = 20 V, I_E = 120 mA, P_{out} = 0.5 W, f = 2.0 GHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No Degradation in Output Power			
Cutoff Frequency (V_{CE} = 20 V, I_E = 120 mA)	f_τ	4.0	4.5	—	GHz
Gain Linearity (V_{CE} = 20 V, I_E = 120 mA, f = 2.0 GHz, P_{o1} = 0.5 W, P_{o2} = 0.5 mW)	L_G	— —	— —	−0.2 +1.0	dB
Intermodulation Distortion, 3rd Order (V_{CE} = 20 V, I_E = 120 mA, P_o (PEP) = 0.5 W, Tones at 2.0 GHz and 2.005 GHz)	IMD	—	−30	—	dB

TYPICAL CHARACTERISTICS

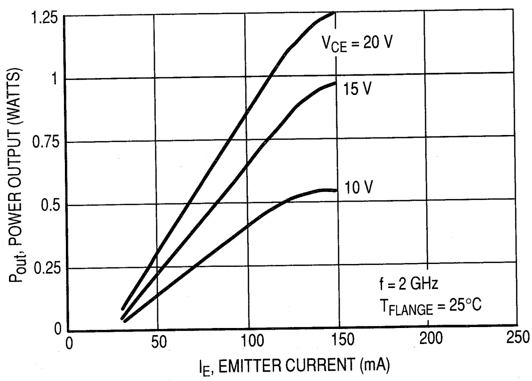


Figure 1. 1.0 dB Compression Point versus Emitter Current

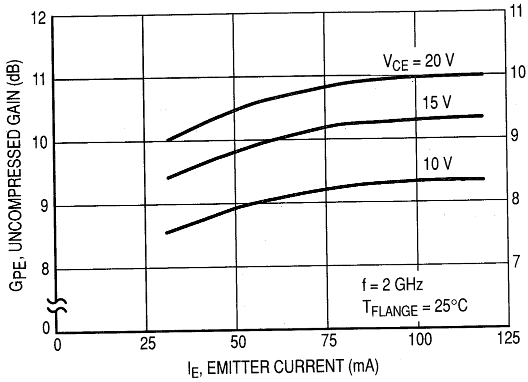


Figure 2. Gain versus Emitter Current

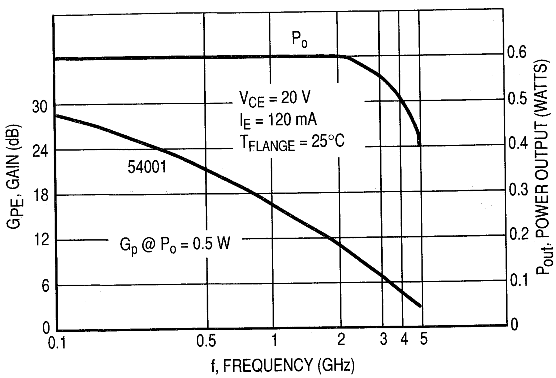


Figure 3. Gain and 1.0 dB Compressed Power versus Frequency

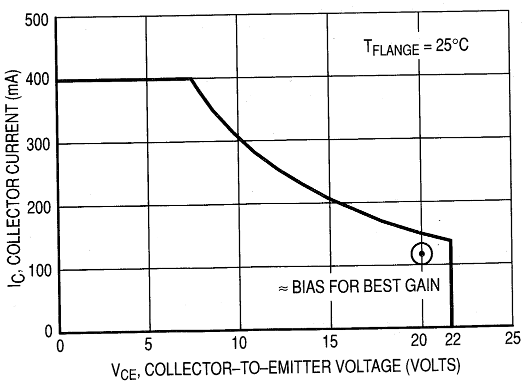


Figure 4. DC Safe Operating Area

V_{CE} (Volts)	I_C (mA)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	∠ φ	Mag	∠ φ	Mag	∠ φ	Mag	∠ φ
20	100	0.5	0.76	−177	6.65	74	0.03	20	0.43	−73
		1.0	0.76	159	3.24	39	0.03	24	0.50	−104
		1.3	0.76	148	2.46	21	0.04	25	0.56	−120
		1.5	0.75	141	2.07	9.0	0.04	24	0.60	−130
		1.7	0.76	134	1.80	−1.0	0.05	24	0.64	−140
		2.0	0.76	124	1.51	−14	0.06	22	0.68	−152
		2.3	0.74	113	1.27	−33	0.06	13	0.74	−167
		2.5	0.73	106	1.15	−43	0.07	9.0	0.76	−173
		2.7	0.72	98	1.06	−52	0.07	5.0	0.77	179
		32	0.69	85	0.95	−67	0.08	−4.0	0.82	170
		3.3	0.64	71	0.86	−81	0.09	−14	0.85	161
		3.5	0.61	60	0.81	−94	0.10	−22	0.87	155
		3.7	0.57	47	0.77	−103	0.10	−30	0.80	149
		4.0	0.51	24	0.70	−119	0.11	−44	0.92	141

Table 1. MRW54001 Common Emitter S–Parameters

The graph shown below displays MTTF in hours x ampere^2 emitter current for each of the devices. Life tests at elevated temperatures have correlated to better than ±10% to the theoretical prediction for metal failure. Divide MTTF by I_C^2 for MTTF in a particular application.

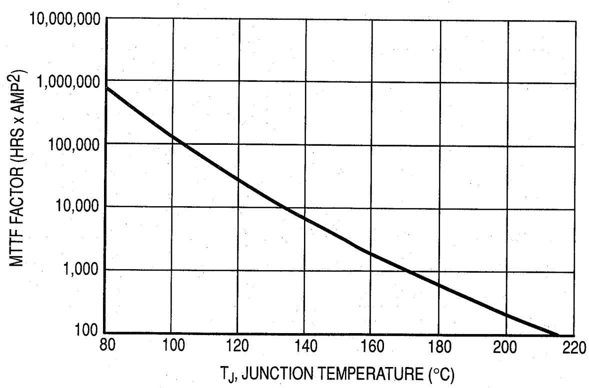


Figure 5. MTTF Factor versus Junction Temperature

Advance Information

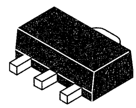
The RF Small Signal Line

Silicon Lateral FET

N–Channel Enhancement–Mode MOSFET

MXR9745T1
MXR9745RT1

31.5 dBm, 850 MHz
HIGH FREQUENCY
POWER TRANSISTOR
LDMOS FET



CASE 345–03
(MXR9745RT1, STYLE 8)
(MXR9745T1, STYLE 9)
(SOT–89)

Designed for use in low voltage, moderate power amplifiers such as portable analog and digital cellular radios and PC RF modems.

- Performance Specifications at 6 Volt, 850 MHz:
  Output Power = 31.5 dBm Min
  Power Gain = 8.5 dB Typ
  Efficiency = 60% Min
- Guaranteed Ruggedness at Load VSWR = 20:1
- Available in Tape and Reel Packaging Options:
  T1 Suffix = 1,000 Units per Reel
- MXR9745RT1 is Gate–Drain Pin Out Reversed.
  All Electricals Same as MXR9745T1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	35	Vdc
Drain–Gate Voltage (R_{GS} = 1 MΩ)	V_{DGO}	25	Vdc
Gate–Source Voltage	V_{GS}	±10	Vdc
Drain Current – Continuous	I_D	2	Adc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	10 100	W mW/°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Leakage Current (V_{DS} = 35 V, V_{GS} = 0)	I_{DSS}	–	–	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 V, V_{DS} = 0)	I_{GSS}	–	–	1	μAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 1

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 6 V, I_D = 500 μA)	$V_{GS(th)}$	1	1.3	2	Vdc
Forward Transconductance (V_{DS} = 6 V, I_D = 400 mA)	g_{fs}	–	550	–	mmhos
Resistance Drain–Source (V_{GS} = 4 V, I_D = 100 mA)	$R_{DS(on)}$	–	1	2.5	Ω
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 6 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	–	14	–	pF
Output Capacitance (V_{DS} = 6 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	–	11	–	pF
Feedback Capacitance (V_{DS} = 6 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	–	1.8	–	pF
FUNCTIONAL CHARACTERISTICS					
Power Gain (V_{DD} = 6 Vdc, P_{in} = 23 dBm, I_{DQ} = 250 mA, f = 850 MHz)	G_{ps}	8	8.5	–	dB
Drain Efficiency (V_{DD} = 6 Vdc, P_{in} = 23 dBm, I_{DQ} = 250 mA, f = 850 MHz)	η_D	55	60	–	%
Ruggedness Test (V_{DD} = 6 Vdc, P_{in} = 23 dBm, I_{DQ} = 250 mA, f = 850 MHz, Load VSWR = 20:1, All Phase Angles at Frequency Test)	Ψ	No Degradation in Output Power after Test			

Table 1. Large Signal Impedance
V_{DD} = 6 V, P_{in} = 23 dBm, I_{DQ} = 250 mA

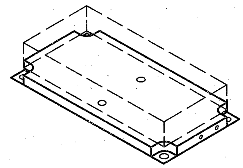
f MHz	Z_{in} Ohms	Z_{OL}* Ohms
850	4.8 – j6.4	6 – j7.5

Z_{OL}* is the conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

The RF Line
Broadband RF Array for TV Transmitter

RFA8090B

140 W, 470–860 MHz
CLASS AB
RF POWER AMPLIFIER



CASE 429E–01, STYLE 1

The RFA8090B is a solid state class AB amplifier and is specifically designed for TV transposers and transmitters. This amplifier incorporates microstrip technology and reliable Motorola push–pull transistors.

- Specified 28 Volts, 470–860 MHz Characteristics
  Output Power — 95 Watts (CW)
  Output Power — 140 Watts (peak)
  Gain — 8 dB min (@ 95 Watts)
- 50 Ω Input and Output Impedance

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	32	Vdc
Quiescent Current	I_{CQ}	2 x 300	mAdc
Input Power	P_{in}	20	Watts
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Temperature (1)	T_{op}	–20 to +70	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V, I_{CQ} = 200 mA, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Instantaneous Bandwidth	BW	470	860	MHz

FUNCTIONAL TESTS IN CW (SOUND) (T_C = 25°C, V_{CC} = 28 V, I_{CQ} = 200 mA, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Power Gain (P_{out} = 95 W)	G_p	8	—	dB
Gain Ripple (P_{out} = 95 W)	G_{rple}	—	±0.7	dB
Output Power @ 1 dB Compression	P_{out}	95	—	Watts
Mismatch Tolerance (P_{out} = 95 W)	VSWR	3:1	—	—
Efficiency (P_{out} = 95 W)	η	50	—	%

FUNCTIONAL TESTS IN VIDEO (standard black level)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Output Power (synch.) (V_{CC} = 28 Vdc, I_{CQ} = 200 mA, f = 860 MHz)	P_{out}	120	—	—	Watts
Peak Output Power (synch.) (V_{CC} = 32 Vdc, I_{CQ} = 100 mA, f = 860 MHz)	P_{out}	140	—	—	Watts

NOTE:
1. Temperature is measured at temperature test point (on the flange of the transistor).

REV 1

TYPICAL CHARACTERISTICS

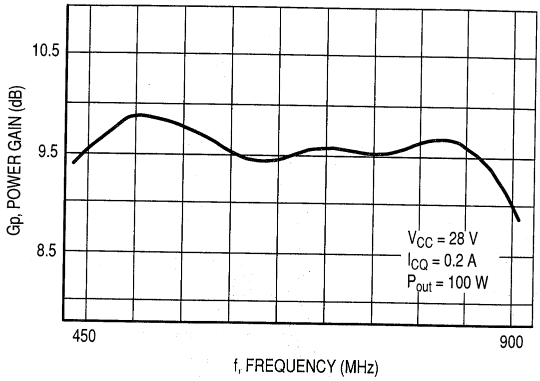


Figure 1. Power Gain versus Frequency

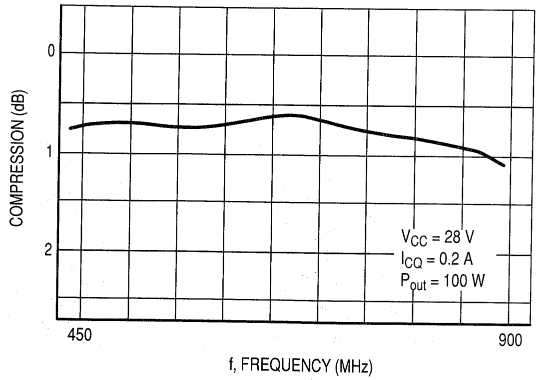


Figure 2. Gain Compression versus Frequency

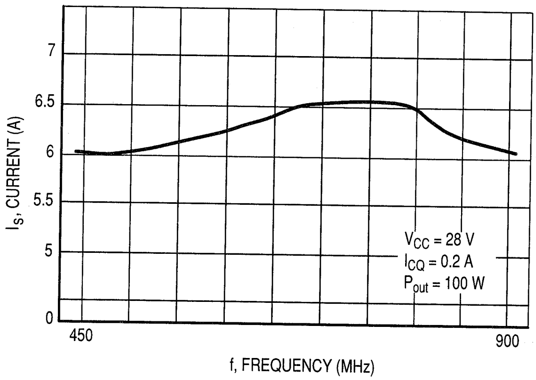


Figure 3. Supply Current versus Frequency

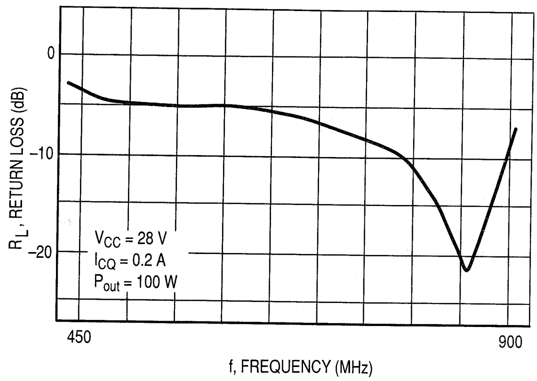


Figure 4. Input Return Loss versus Frequency

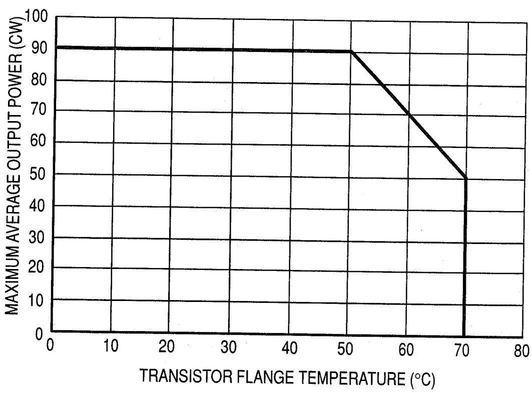


Figure 5. Maximum Average Output Power versus Temperature

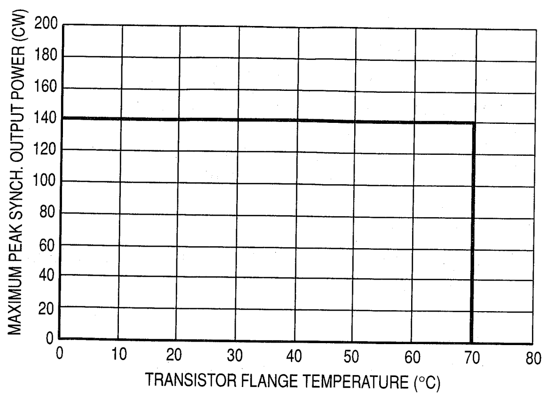


Figure 6. Maximum Peak Synch. Output Power (B/G Standard) versus Temperature

TYPICAL VIDEO CHARACTERISTICS

TEST CONDITIONS:
DIFF. Gain, 10 Steps
Channel 61, 10% rest carrier
V_{CE} = 28 V
I_Q = 0.2 A

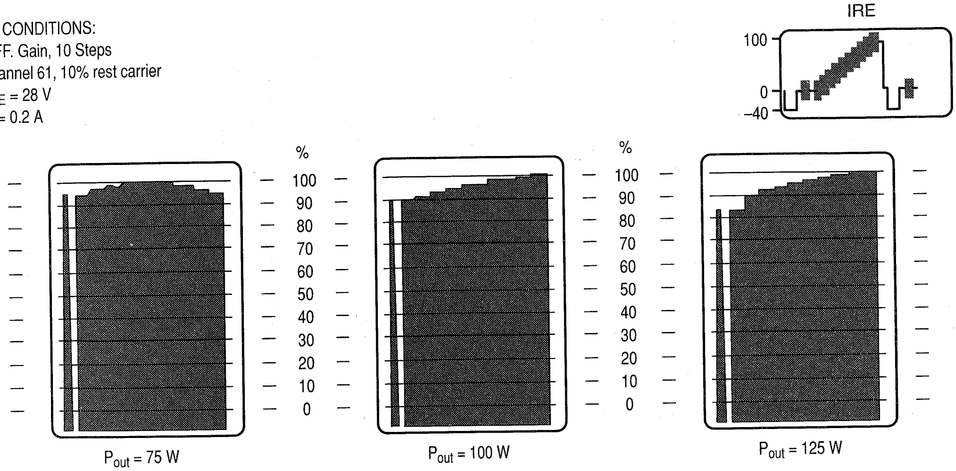
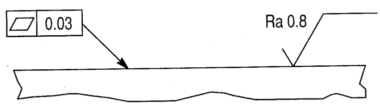


Figure 7. Differential Gain

MOUNTING RECOMMENDATIONS

HEATSINK TOOLING

- Planarity: Better than 0.03 mm
- Roughness: Typical value 0.8
- 6 fixing holes M3



THERMAL COMPOUND

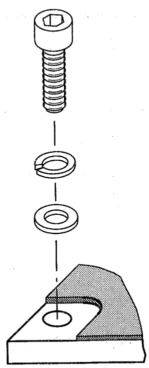
- Paste with silicones: SICERONT KF Ref. 1201 Recommended.
- Thickness: Optimum between 0.06 mm and 0.15 mm, on the whole back surface of the amplifier.
  (Typical volume: 215 mm 3 for 0.1 mm thickness)
  (Equivalent weight: 0.5g for 2.2 density paste).

SCREWS

- Socket head cap screws: CHC M3 x 10 for Copper/Aluminum Heatsink.
- Material: Nickel plated steel.

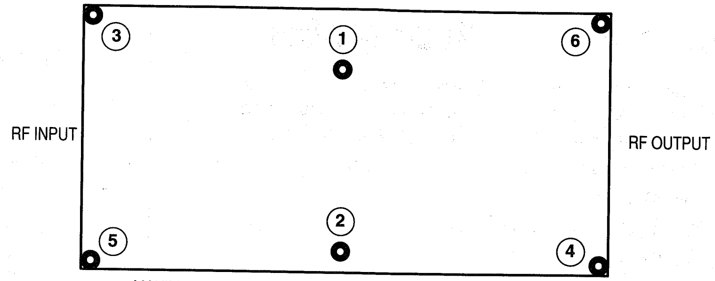
WASHERS

- Split lock washers WZ ∅3 + Flat washers ZU ∅3.



MOUNTING RECOMMENDATIONS (continued)

TIGHTENING ORDER



MAXIMUM RECOMMENDED TORQUE: 12 Kg.cm (10.5 in. lbs)

CLEANING

Some components of the RFA8090B are not qualified for every kind of cleaning solvent; do not clean the amplifier in a solvent bath. Local cleaning is recommended.

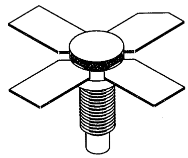
The RF Line
UHF Linear Power Transistor

. . . designed for very high output 1.5 V MATV amplifiers up to 860 MHz and 500 mW Band V TV transposer stages. Gold metallization and diffused emitter ballast resistors are used to enhanced reliability, ruggedness and linearity.

- Band IV and V (470–860 MHz)
- 0.5 W — P_{ref} @ –58 dB IMD
- High Gain — 12 dB Typ, Class A, f = 860 MHz
- Gold Metallization for Reliability

TPV596A

0.5 W, 470–860 MHz
UHF LINEAR
POWER TRANSISTOR



CASE 244–04, STYLE 1
(.280 SOE)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	24	Vdc
Collector–Base Voltage	V_{CBO}	45	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous	I_C	0.7	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	8.75 0.05	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (T_C = 70°C)	$R_{\theta JC}$	20	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mA, I_B = 0)	$V_{(BR)CEO}$	24	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 1.0 mA, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 4.0 mA, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Emitter–Base Leakage Current (V_{EB} = 2.0 V)	I_{EBO}	—	—	0.25	mA
Collector Cutoff Current (V_{CB} = 28 V, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
Collector–Emitter Breakdown Voltage (I_C = 20 mA, R_{BE} = 10 Ω)	$V_{(BR)CER}$	50	—	—	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mA, V_{CE} = 5.0 V)	h_{FE}	15	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 V, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	5.0	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CE} = 20 V, P_{out} = 0.5 W, f = 860 MHz, I_E = 0.22 A)	G_{PE}	11.5	12	—	dB
Load Mismatch (V_{CE} = 20 V, P_{out} = 1.0 W, I_E = 0.22 A, f = 860 MHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No Degradation in Output Power			
Intermodulation Distortion, 3 Tone (f = 860 MHz, V_{CE} = 20 V, I_E = 0.22 A, P_{ref} = 1.0 W, Vision Carrier = –8.0 dB, Sound Carrier = –7.0 dB, Sideband Signal = –16 dB, Specification TV05001)	IMD_1	—	—	–50	dB
Intermodulation Distortion (IDEM) (f = 860 MHz, V_{CE} = 20 V, I_E = 0.22 A, P_{ref} = 0.5 W, Vision Carrier = –8.0 dB, Sound Carrier = –10 dB, Sideband Signal = –16 dB)	IMD_2	—	–60	–58	dB

TYPICAL CHARACTERISTICS

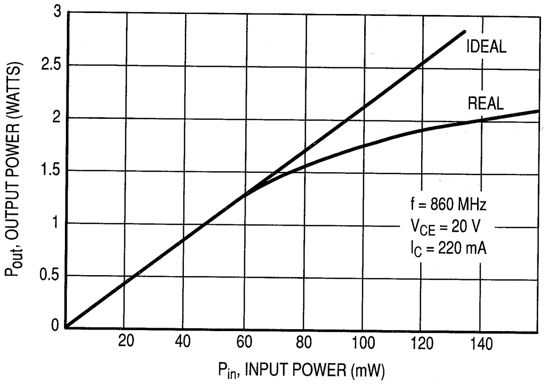


Figure 1. Power Output versus Power Input

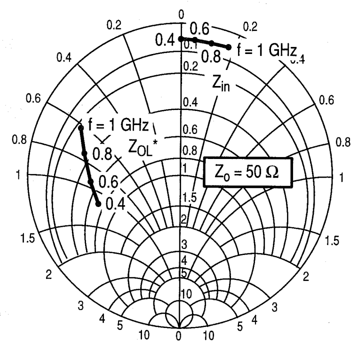


Figure 2. Large Signal Impedances
V_{CE} = 20 V — I_C = 220 mA

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

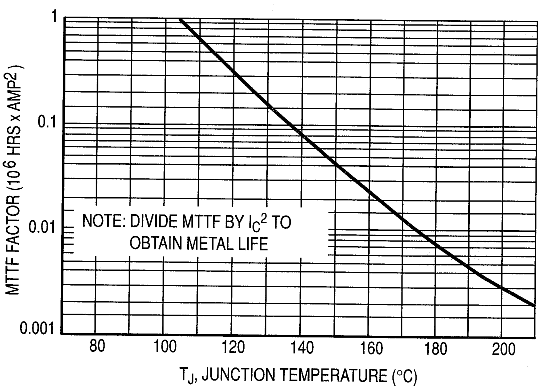


Figure 3. MTTF Factor versus Junction Temperature

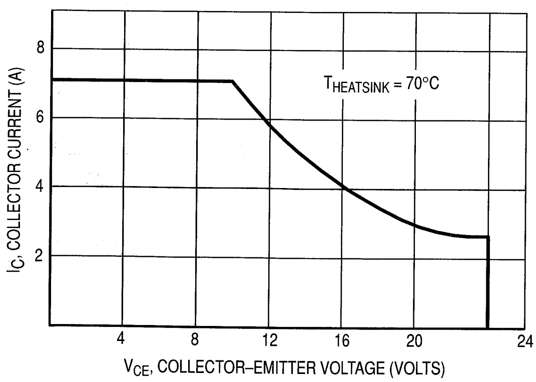
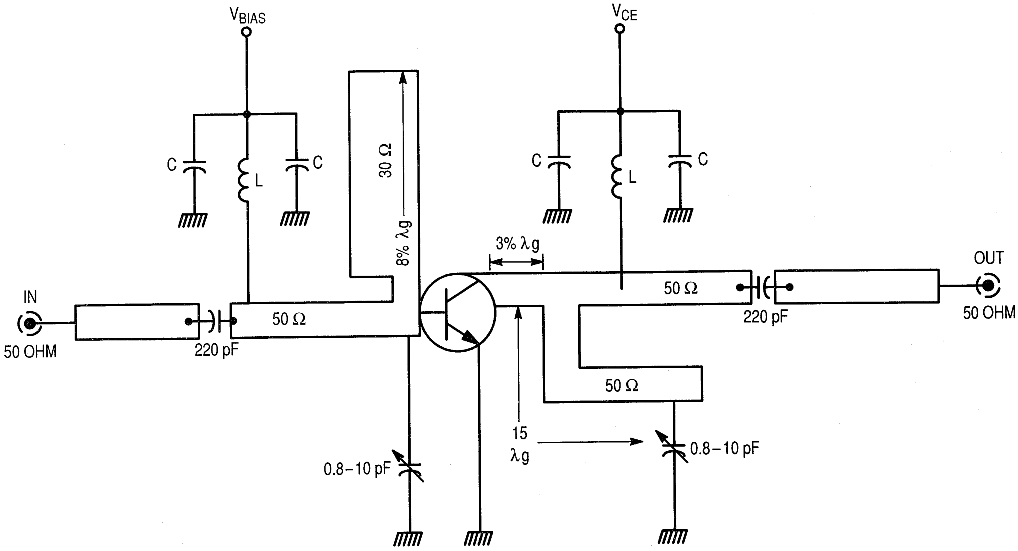


Figure 4. DC Safe Operating Area



NOTE: λg is the wave length in the microstrip circuit

Figure 5. 860 MHz Test Circuit

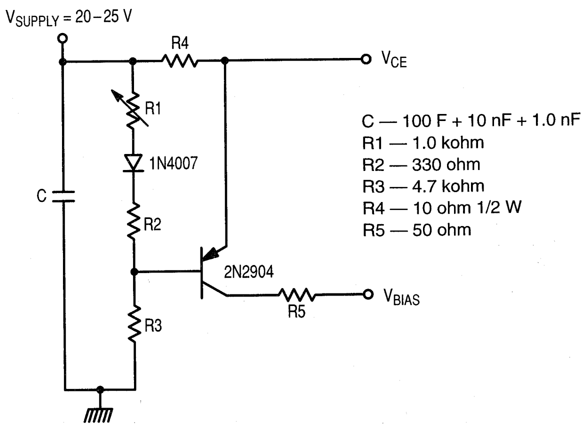


Figure 6. Class A Bias Circuit

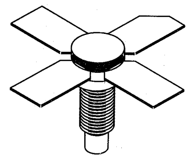
The RF Line
UHF Linear Power Transistor

TPV597

. . . designed for 1.0 watt stages in Band V TV transposer amplifiers. Gold metallized dice and diffused emitter ballast resistors are used to enhance reliability, ruggedness and linearity.

- Band IV and V (470–860 MHz)
- 1.0 W — P_{ref} @ −58 dB IMD
- 20 V — V_{CC}
- High Gain — 11 dB Typ, Class A @ f = 860 MHz
- Gold Metallization for Reliability

1.0 W, 470–860 MHz
UHF LINEAR
POWER TRANSISTOR



CASE 244–04, STYLE 1
(.280 SOE)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	24	Vdc
Collector–Base Voltage	V_{CBO}	45	Vdc
Emitter–Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous	I_C	1.4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	19 0.11	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	9.0	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 40 mA, I_B = 0)	$V_{(BR)CEO}$	24	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 2.0 mA, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 4.0 mA, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Emitter–Base Leakage Current (V_{EB} = 2.0 V)	I_{EBO}	—	—	0.5	mA
Collector–Emitter Breakdown Voltage (I_C = 40 mA, R_{BE} = 10 Ω)	$V_{(BR)CER}$	50	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 V, I_E = 0)	I_{CBO}	—	—	1.2	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mA, V_{CE} = 5.0 V)	h_{FE}	15	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 V, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	7.0	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CE} = 20 V, P_{out} = 1.0 W, f = 860 MHz, I_E = 0.44 A)	G_{PE}	10.5	11	—	dB
Load Mismatch (V_{CE} = 20 V, P_{out} = 2.0 W, I_E = 0.44 A, f = 860 MHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No Degradation in Output Power			

(continued)

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (continued)					
Intermodulation Distortion, 3 Tone (f = 860 MHz, V_{CE} = 20 V, I_E = 0.44 A, P_{ref} = 1.0 W, Vision Carrier = –8.0 dB, Sound Carrier = –7.0 dB, Sideband Signal = –16 dB, Specification TV05001)	IMD_1	—	–60	–58	dB
Cutoff Frequency (V_{CE} = 20 V, I_E = 0.44 A)	f_τ	2.2	2.5	—	GHz
Intermodulation Distortion (IDEM) (f = 860 MHz, V_{CE} = 20 V, I_E = 0.44 A, P_{ref} = 2.0 W, Vision Carrier = –8.0 dB, Sound Carrier = –10 dB, Sideband Signal = –16 dB)	IMD_2	—	—	–51	dB

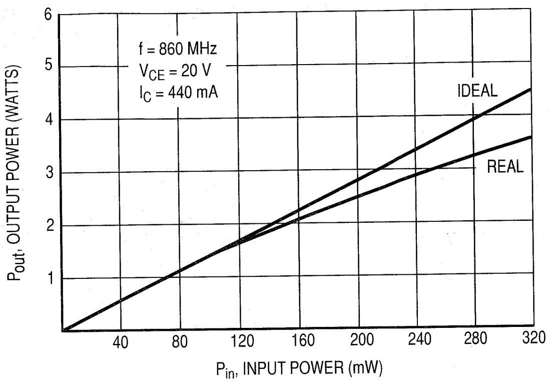


Figure 1. Power Output versus Power Input

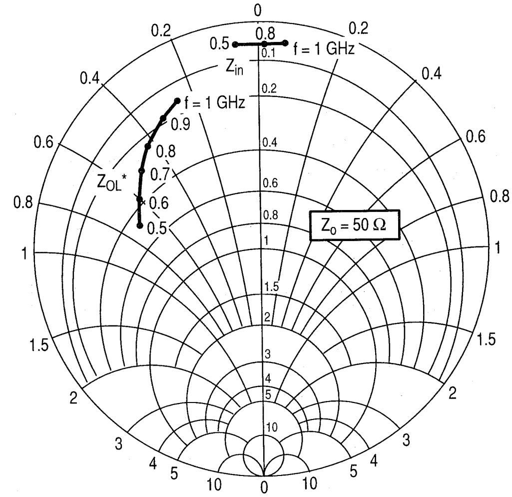


Figure 2. Large Signal Impedances
V_{CE} = 20 V — I_C = 440 mA

Z_{OL}* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

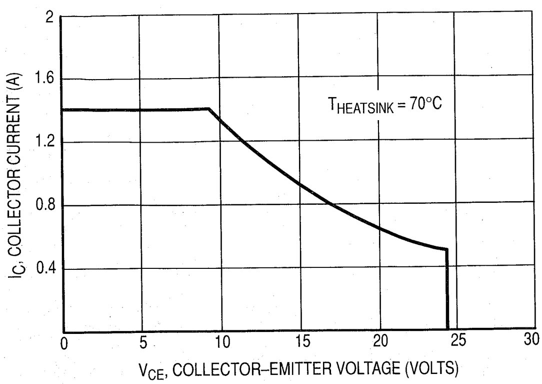


Figure 3. Safe Operating Area

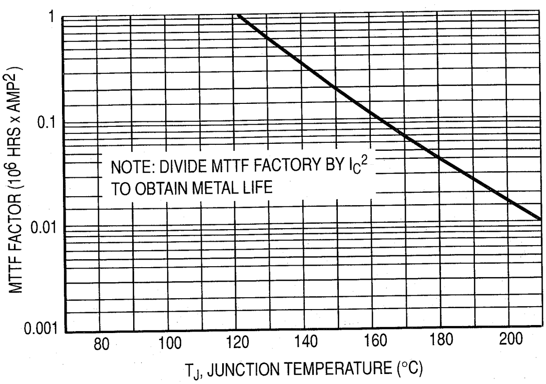
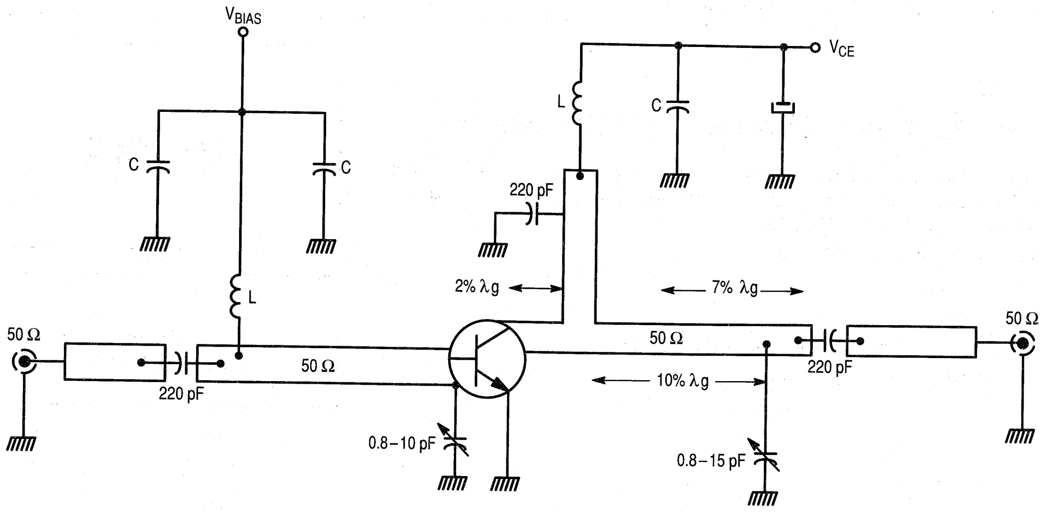


Figure 4. MTTF Factor versus Junction Temperature



L = 6 turns ID = 1 mm Wire diameter = 0.6 mm
The lengths are given for f = 860 MHz

NOTE: λg is the wave length in the microstrip circuit

Figure 5. 860 MHz Test Circuit

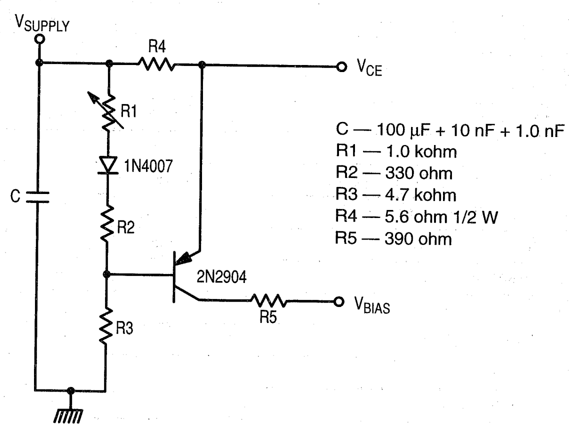


Figure 6. Class A Bias Circuit

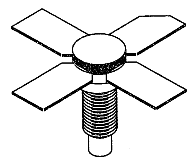
The RF Line
UHF Linear Power Transistor

TPV598

Designed for 4.0 watt stages in Band V TV transposer amplifiers. Gold metallized dice and diffused emitter ballast resistors are used to enhance reliability, ruggedness and linearity.

- Band IV and V (470–860 MHz)
- 4.0 W — P_{ref} @ −60 dB IMD
- 25 V — V_{CC}
- High Gain — 7.0 dB Min, Class A @ f = 860 MHz
- Gold Metallization for Reliability

4.0 W, 470–860 MHz
UHF LINEAR
POWER TRANSISTOR



CASE 244–04, STYLE 1
(.280 SOE)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	27	Vdc
Collector–Base Voltage	V_{CBO}	45	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

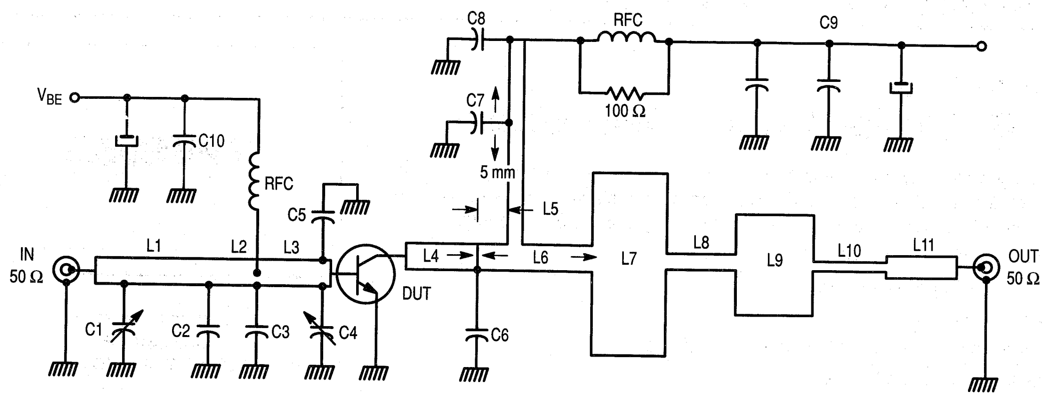
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (T_C = 70°C)	$R_{\theta JC}$	6.2	°C/W
Thermal Resistance, Case to Heatsink	$R_{\theta CH}$	0.4 Typ	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 60 mA, I_B = 0)	$V_{(BR)CEO}$	27	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 10 mA, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 3.0 mA, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector–Emitter Leakage Current (V_{CE} = 20 V)	I_{CEO}	—	—	5.0	mA
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mA, V_{CE} = 20 V)	h_{FE}	10	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 25 V, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	20	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CE} = 25 V, P_{out} = 4.0 W, f = 860 MHz, I_C = 850 mA)	G_{PE}	7.0	—	—	dB
Intermodulation Distortion, 3 Tone (f = 860 MHz, V_{CE} = 25 V, I_E = 850 mA, P_{ref} = 4.0 W, Vision Carrier = −8.0 dB, Sound Carrier = −7.0 dB, Sideband Signal = −16 dB, Specification TV05001)	IMD_1	—	—	−58	dB
Cutoff Frequency (V_{CE} = 25 V, I_C = 850 mA)	f_τ	—	2.0	—	GHz

REV 1



C1 — Variable 0.5–4.7 pF Airtronic
C2, C3 — ATC 4.7 pF
C4 — ATC 10 pF + Variable 0.5–4.7 pF Airtronic
C5 — ATC 10 pF + ATC 5.6 pF
C6 — ATC 18 pF + 0.5–4.7 pF Variable Airtronic
C7 — 470 pF Chip Capacitor
C8 — 1.0 nF + 10 nF Decoupling
C9 — 1.0 nF + 10 nF + 0.1 μF + 10 μF
C10 — 10 nF + 1.0 μF + 10 μF
RFC = 8 turns, ID 2.5 mm, Wire = 0.5 mm

L1 — 50 Ω line 6.2% λg at 860 MHz
L2 — 50 Ω line 4.2% λg at 760 MHz
L3 — 50 Ω line 4.9% λg at 860 MHz
L4 — 20 Ω line 6.5% λg at 860 MHz
L5 — 50 Ω line 5% λg at 860 MHz
L6 — 20 Ω line 9.5% λg at 860 MHz
L7 — 4.0 Ω line 8% λg at 860 MHz
L8 — 55 Ω line 7.5% λg at 860 MHz
L9 — 7.5 Ω line 8% λg at 860 MHz
L10 — 100 Ω line 8% λg at 860 MHz
L11 — 20 Ω line 8% λg at 860 MHz
Note: λg is the wavelength in the microstrip circuit

Figure 1. Broadband Test Circuit

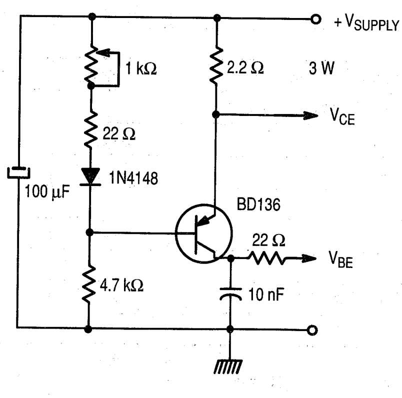


Figure 2. Class A Bias Circuit

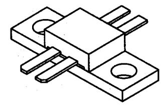
The RF Line
UHF Linear Power Transistor

TPV695A

Designed for driver and output stages in band IV and V TV transposers and transmitter amplifiers. The TPV695A uses gold metallized die with diffused emitter ballast resistors to enhance reliability, ruggedness and linearity.

- Band IV and V (470–860 MHz)
- 14 W — P_{ref} @ –47 dB IMD
- 25 V — V_{CC}
- High Gain — 10 dB Min, Class A, f = 860 MHz
- Gold Metallization for Reliability
- Push–Pull Package

**14 W, 470–860 MHz
UHF LINEAR
POWER TRANSISTOR**



**CASE 395B–01, STYLE 1
BMA2**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	28	Vdc
Collector–Base Voltage	V_{CES}	50	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–50 to +200	°C
Operating Case Temperature Range	T_C	–15 to +70	°C

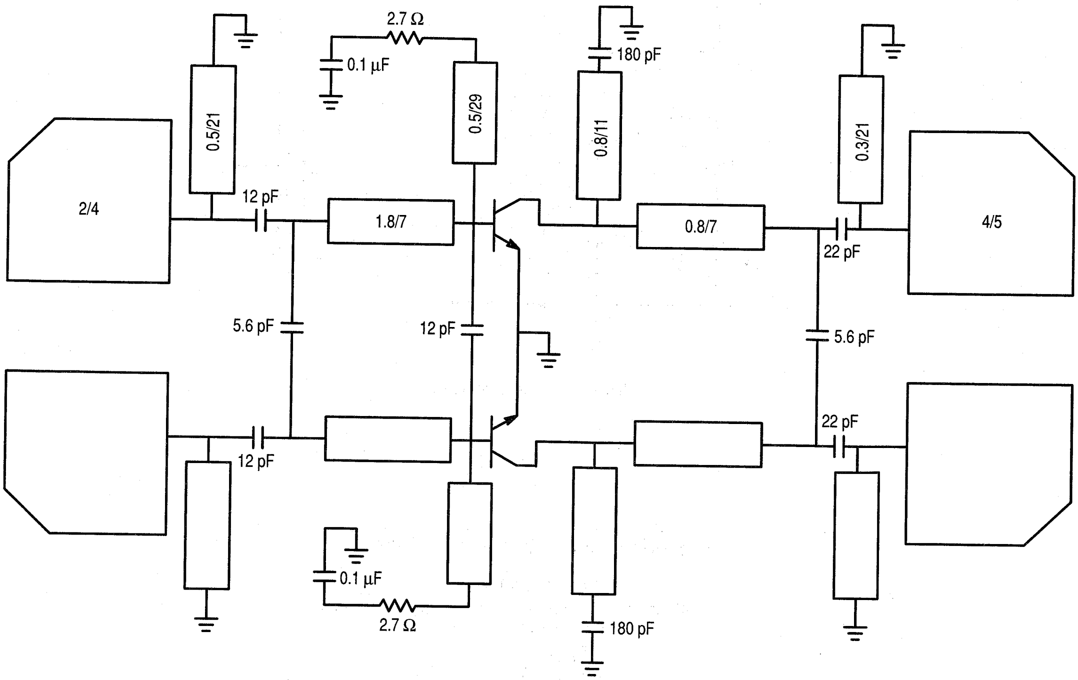
THERMAL CHARACTERISTICS

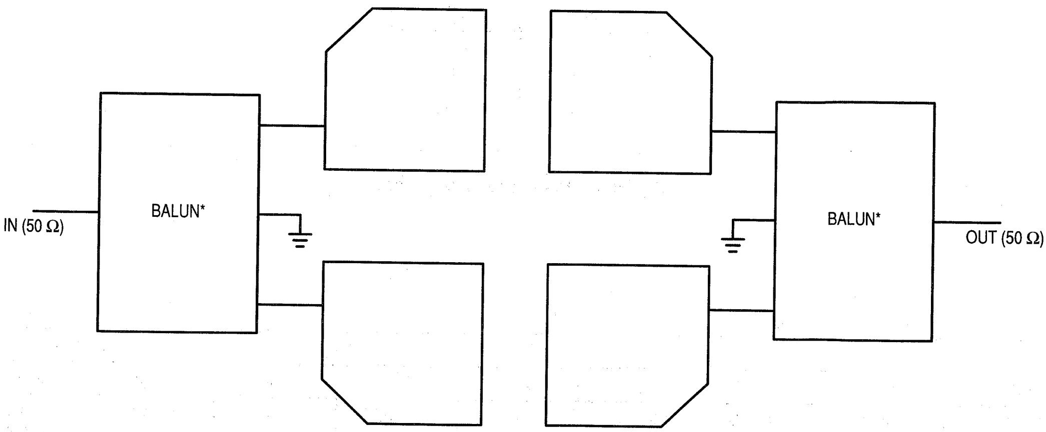
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 20 mA, I_B = 0)	$V_{(BR)CEO}$	28	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 20 mA, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 5.0 mA, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 19 V, I_E = 0)	I_{CBO}	—	—	15	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 A, V_{CE} = 10 V)	h_{FE}	20	—	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 V, I_E = 0, f = 1.0 MHz)	C_{ob}	—	18	20	pF
FUNCTIONAL TESTS					
Common–Emitter Amplifier Power Gain (V_{CE} = 25 V, P_{out} = 14 W, f = 860 MHz, I_C = 2.0 x 900 mA)	G_{PE}	10	—	—	dB
Overdrive (no degradation) (f = 470 MHz, V_{CE} = 25 V, I_C = 2.0 x 900 mA)	$P_{in_{over}}$	12.5	—	—	W
Intermodulation Distortion, 3 Tone (f = 860 MHz, V_{CE} = 25 V, I_E = 2.0 x 900 mA, P_{ref} = 14 W, Vision Carrier = –7.0 dB, Sound Carrier = –8.0 dB, Sideband Signal = –16 dB, Specification TV05001)	IMD_1	—	–47	–46	dB

Dimension: width/length mm
Board Material — 1/50″, Teflon Glass, $\varepsilon_r = 2.55$





— Balun is 50 Ω unbalanced to 2 x 25 Ω balanced

Figure 1. 470–860 MHz Test Circuit

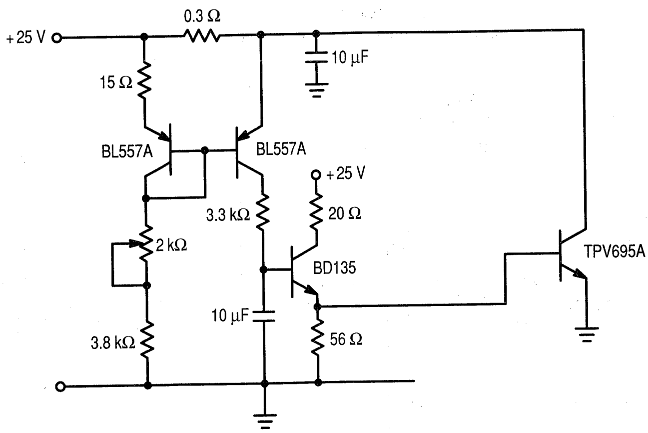


Figure 2. Bias Network

Intermodulation Distortion, 3 Tone

Test Conditions:
@ −8 dB Ref. Vision Carrier, −7 dB Ref. Sound Carrier,
−16 dB Ref. Sideband Signal
P_{ref} = 14 Watts
V_{CB} = 25 Volts & I_{CS} = 2 x 900 mA

Frequency MHz	IMD dB
860	−47
760	−47
660	−47
560	−47
470	−48

Figure 3. IMD versus Frequency

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
400	0.918	176.6	0.605	58.3	$2.75 \cdot 10^{-4}$	−8.2	0.449	−173.1
450	0.908	175.6	1.44	53.1	$3.01 \cdot 10^{-4}$	−11.8	0.452	−172.4
500	0.877	176.1	1.28	48.3	$3.10 \cdot 10^{-4}$	−12.8	0.438	−171.7
550	0.889	174.5	1.21	42.3	$3.72 \cdot 10^{-4}$	−16.3	0.452	−170.1
600	0.891	174.0	1.16	36.3	$4.31 \cdot 10^{-4}$	−18.5	0.466	−168.9
650	0.863	173.6	1.15	29.9	$6.11 \cdot 10^{-4}$	−25	0.469	−167.2
700	0.839	173.1	1.15	21.9	$6.03 \cdot 10^{-4}$	−34.3	0.500	−165.5
750	0.805	172.8	1.15	13.8	$6.55 \cdot 10^{-4}$	−39.9	0.541	−164.2
800	0.800	172.6	1.15	4.7	$7.29 \cdot 10^{-4}$	−46.6	0.583	−163.5
850	0.771	172.3	1.20	−8.2	$8.39 \cdot 10^{-4}$	−57.4	0.673	−163.1
900	0.762	172.2	1.11	−21.1	$8.55 \cdot 10^{-4}$	−67.6	0.759	−164.3

Table 1. S–Parameters

The RF Line
UHF Linear Power Transistor

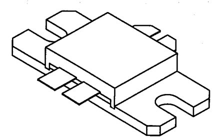
. . . designed for output stages in Band IV & V TV transmitter amplifiers. Internal matching of both input and output along with use of a push–pull package configuration aids broadband amplifier designs.

Gold metallized dice with diffused emitter ballast resistors enhances reliability, ruggedness and linearity.

- Band IV & V (470–860 MHz)
- 25 W — P_{ref} @ −45 dB IMD
- 25 V — V_{CC}
- Push–Pull Package
- Gold Metallization for Reliability

TPV7025

25 W, 470–860 MHz
UHF LINEAR
POWER TRANSISTOR



CASE 398–03, STYLE 1
(BMA–4)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	28	Vdc
Collector–Base Voltage	V_{CBO}	45	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	−50 to +200	°C
Operating Case Temperature	T_C	70	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (T_C = 70°C)	$R_{\theta JC}$	1.5	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Breakdown Voltage (I_C = 120 mA, I_B = 0)	$V_{(BR)CEO}$	28	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 20 mA, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 6.0 mA, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 A, V_{CE} = 20 V)	h_{FE}	10	—	60	—
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance (V_{CB} = 28 V, I_E = 0, f = 1.0 MHz)	C_{ob}	64	—	80	pF

NOTE:
1. Each transistor chip measured separately.

(continued)

ELECTRICAL CHARACTERISTICS — continued

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (2)					
Common–Emitter Amplifier Power Gain (V_{CE} = 25 V, P_{out} = 25 W, f = 860 MHz, I_{CQ} = 3.2 A)	G_{PE}	9.0	—	10.5	dB
Load Mismatch (V_{CE} = 25 V, P_{out} = 24 W, f = 860 MHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No Degradation in Output Power			
Overdrive (f = 470 MHz, 2 tones, V_{CE} = 25 V, I_C = 3.2 A) (No Degradation)	$P_{in_{over}}$	24	—	—	W
Intermodulation Distortion, 3 Tone (f = 860 MHz, V_{CE} = 25 V, I_E = 3.2 A, P_{ref} = 25 W, Vision Carrier = –8.0 dB, Sound Carrier = –7.0 dB, Sideband Signal = –16 dB, Specification TV05001)	IMD_1	—	—	–45	dB
Cross Modulation Distortion (P_{ref} = 25 W, f = 860 MHz, Δ% Sound = (–7.0 dB), Vision 0 – Peak)	X_{MOD}	—	—	20	%

NOTE:
2. Both transistor chips operating in push–pull amplifier.

TYPICAL CHARACTERISTICS

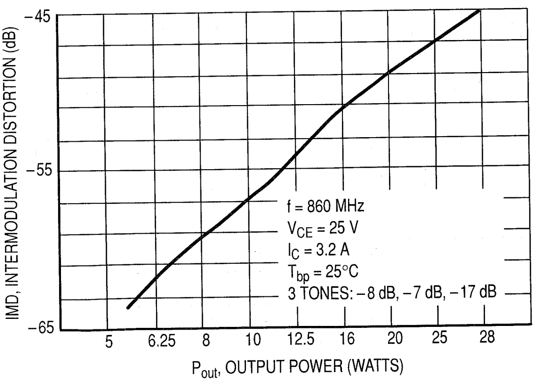


Figure 1. IMD versus Output Power

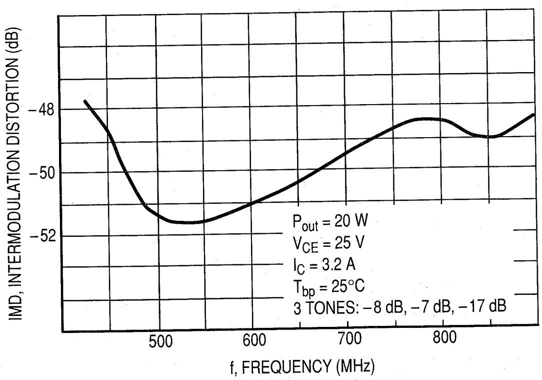
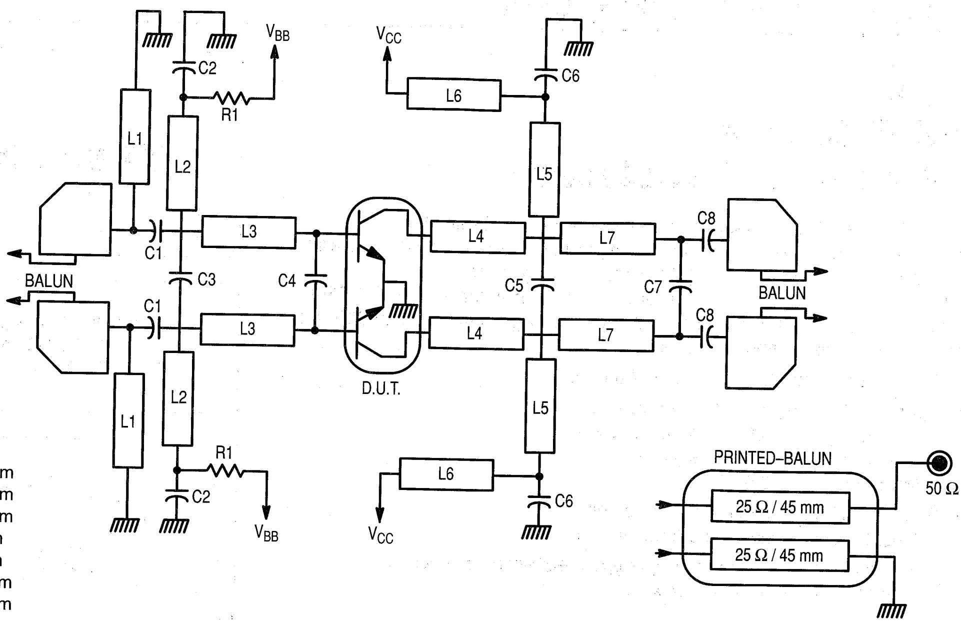


Figure 2. IMD versus Frequency



C1 — 15 pF
C2 — 180 pF
C3 — 10 pF
C4 — 15 pF
C5 — 15 pF
C6 — 180 pF
C7 — 4.7 pF
C8 — 100 pF
L1 — 90 / 16 mm
L2 — 90 / 16 mm
L3 — 35 / 10 mm
L4 — 25 / 7 mm
L5 — 70 / 6 mm
L6 — 70 / 26 mm
L7 — 60 / 16 mm
R1 — 3.3 Ω

Board Material: Teflon Glass Substrate .020 In.

Note: L1 to L7 dimension given in length/width.

Figure 3. 470–860 MHz Broadband Test Circuit

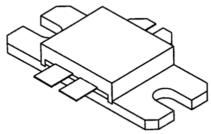
V_{CE} (Volts)	I_C (A)	f (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			Mag	∠ φ	Mag	∠ φ	Mag	∠ φ	Mag	∠ φ
25	2 x 1.8	0.44	1.0	178	1.25	80	0.02	29	0.89	156
		0.46	1.0	176	1.25	84	0.02	31	0.78	151
		0.48	1.0	174	1.30	81	0.02	30	0.70	148
		0.50	0.99	173	1.39	75	0.02	29	0.65	145
		0.52	0.98	171	1.42	70	0.03	26	0.59	142
		0.54	0.97	173	1.52	65	0.03	17	0.53	140
		0.56	0.97	171	1.67	67	0.03	12	0.46	139
		0.58	0.94	169	1.77	49	0.03	8.0	0.39	138
		0.60	0.92	164	1.93	40	0.04	0	0.31	142
		0.62	0.89	163	2.05	30	0.04	−9.0	0.23	157
		0.64	0.86	163	2.19	18	0.05	−19	0.21	−173
		0.66	0.82	164	2.29	4.0	0.05	−30	0.30	−150
		0.68	0.79	166	2.29	−11	0.05	−42	0.43	−147
		0.70	0.79	169	2.16	−26	0.05	−55	0.57	−150
		0.72	0.79	171	1.99	−40	0.05	−66	0.68	−155
		0.74	0.82	172	1.80	−52	0.05	−76	0.77	−161
		0.76	0.84	172	1.59	−63	0.04	−87	0.83	−168
		0.78	0.86	172	1.38	−74	0.04	−96	0.86	−173
		0.80	0.88	171	1.23	−82	0.03	−102	0.88	−178
		0.82	0.89	170	1.10	−88	0.03	−106	0.88	178
		0.84	0.90	170	0.99	−94	0.03	−110	0.89	175
		0.86	0.90	169	0.89	−100	0.03	−115	0.88	172
		0.88	0.90	168	0.80	−107	0.03	−119	0.87	170

Table 1. Common Emitter S–Parameters

The RF Line
NPN Silicon RF Power Transistor

TPV8100B

**150 W, 470–860 MHz
NPN SILICON
RF POWER TRANSISTOR**



CASE 398–03, STYLE 1

The TPV8100B is designed for output stages in band IV and V TV transmitter amplifiers. It incorporates high value emitter ballast resistors, gold metallizations and offers a high degree of reliability and ruggedness.

Including double input and output matching networks, the TPV8100B features high impedances. It can easily operate in a full 470 MHz to 860 MHz bandwidth in a single and simple circuit.

- To be used class AB for TV band IV and V.
- Specified 28 Volts, 860 MHz Characteristics
  Output Power = 125 Watts (peak sync.)
  Output Power = 100 Watts (CW)
  Minimum Gain = 8.5 dB
- Specified 32 Volts, 860 MHz Characteristics
  Output Power = 150 Watts (peak sync.)
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CER}	40	Vdc
Collector–Base Voltage	V_{CBO}	65	Vdc
Emitter–Base Voltage	V_{EBO}	4	Vdc
Collector–Current — Continuous	I_C	12	Adc
Total Device Dissipation @ 25°C Case Derate above 25°C	P_D	215 1.25	Watts W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1)	$R_{\theta JC}$	0.8	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 10 mA, R_{be} = 75 Ω)	$V_{(BR)CER}$	30	—	—	Vdc
Collector–Emitter Breakdown Voltage (I_C = 10 mAdc)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector–Base Breakdown Voltage (I_E = 20 mAdc)	$V_{(BR)CBO}$	65	—	—	Vdc
Collector–Emitter Leakage (V_{CE} = 28 V, R_{be} = 75 Ω)	I_{CER}	—	—	10	mA

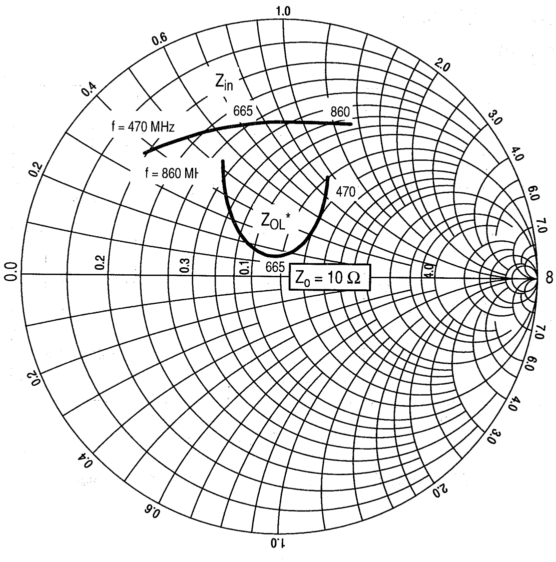
(continued)

NOTE:
1. Thermal resistance is determined under specified RF operating condition.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 2 Adc, V_{CE} = 10 Vdc)	h_{FE}	30	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (each side) (2) (V_{CB} = 28 V, I_E = 0, f = 1 MHz)	C_{ob}	—	44	—	pF
FUNCTIONAL TESTS IN CW (SOUND)					
Common–Emitter Amplifier Power Gain (V_{CC} = 28 V, P_{out} = 100 W, I_{CQ} = 2 x 50 mA, f = 860 MHz)	G_p	8.5	9.5	—	dB
Collector Efficiency (V_{CC} = 28 V, P_{out} = 100 W, I_Q = 2 x 50 mA, f = 860 MHz)	η	55	58	—	%
Output Power @ 1 dB Compression (P_{ref} = 25 W) (V_{CC} = 28 V, I_{CQ} = 2 x 50 mA, f = 860 MHz)	P_{out}	100	110	—	W
FUNCTIONAL TESTS IN VIDEO (STANDARD BLACK LEVEL)					
Peak Output Power (synch.) (V_{CC} = 28 V, I_{CQ} = 2 x 50 mA, f = 860 MHz)	P_{out}	125	135	—	W
Peak Output Power (synch.) (V_{CC} = 32 V, I_{CQ} = 2 x 25 mA, f = 860 MHz)	P_{out}	150	160	—	W
Recommended Quiescent Current	I_{CQ}	—	—	2 x 0.3	A

NOTE:
2. Value of "C_{ob}" is that of die only. It is not measurable in TPV8100B because of internal matching network.



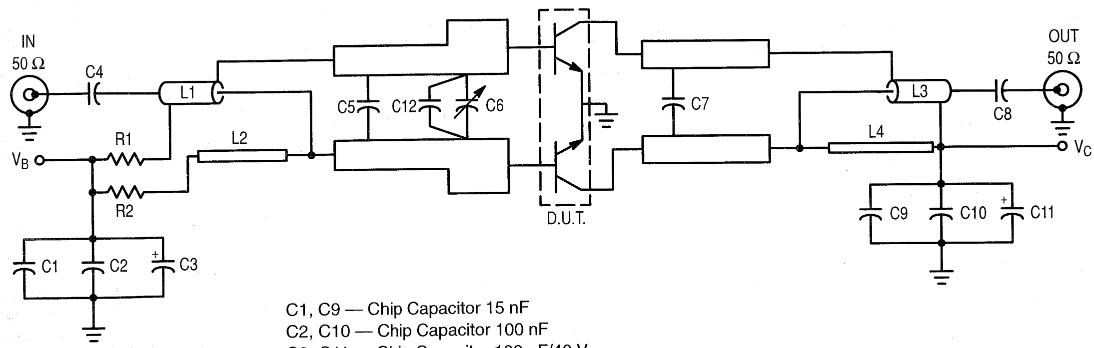
f (MHz)	Z_{in} (Ohms)	Z_{OL}* (Ohms)
470	1.95 + j3.67	10.0 + j9.50
665	3.65 + j6.82	9.23 + j1.30
860	6.66 + j13.8	4.45 + j5.22

Z_{OL}* = Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

NOTE: Z_{in} & Z_{OL}* are given from base–to–base and collector–to–collector respectively.

Input and Output impedances with circuit tuned for maximum linearity @ V_{CC} = 28 V / I_{CQ} = 2 x 50 mA / P_{out} = 100 W

Figure 1. Series Equivalent Input/Output Impedances



C1, C9 — Chip Capacitor 15 nF
C2, C10 — Chip Capacitor 100 nF
C3, C11 — Chip Capacitor 100 μF/40 V
C4 — Chip Capacitor 15 pF ATC 100A
C5 — Chip Capacitor 5.6 pF ATC 100A
C6 — Trimmer Capacitor 1–4 pF
C7 — Chip Capacitor 12 pF ATC 100B
C8 — Chip Capacitor 15 pF ATC 100A
C12 — Chip Capacitor 12 pF ATC 100A
L1, L3 — Coaxial Wire 25 Ω/85 Mils/40 mm
L2, L4 — Printed Board Inductance
R1, R2 — Chip Resistor 1 Ω 0805 5%

Figure 2. Test Circuit

TYPICAL CHARACTERISTICS

CW — WIDEBAND

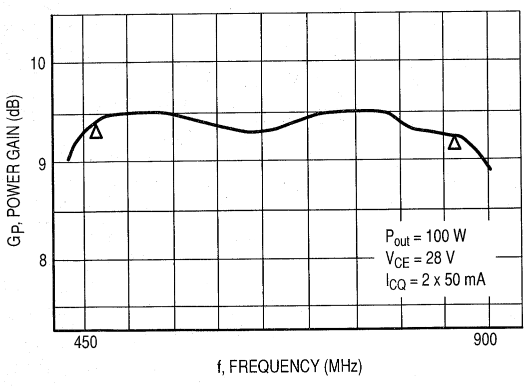


Figure 3. Power Gain versus Frequency

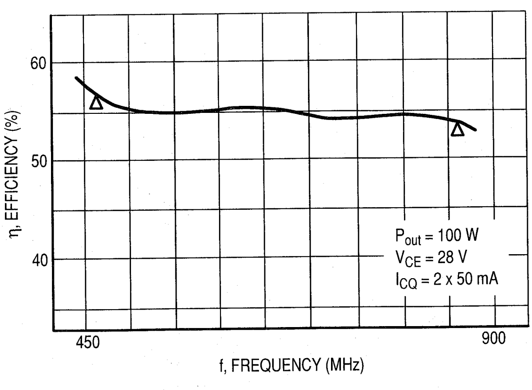
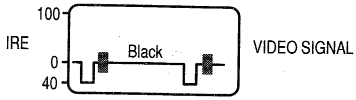


Figure 4. Collector Efficiency versus Frequency

TYPICAL VIDEO CHARACTERISTICS @ f = 800 MHz
V_{CE} = 28 V



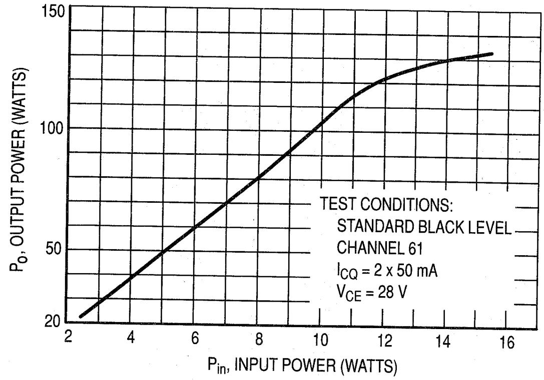


Figure 5. Peak Output Power versus Peak Input Power

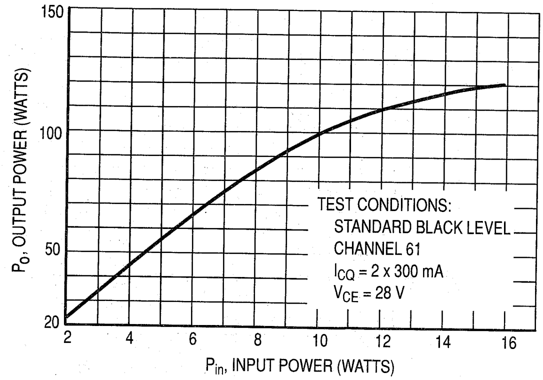


Figure 6. Peak Output Power versus Peak Input Power

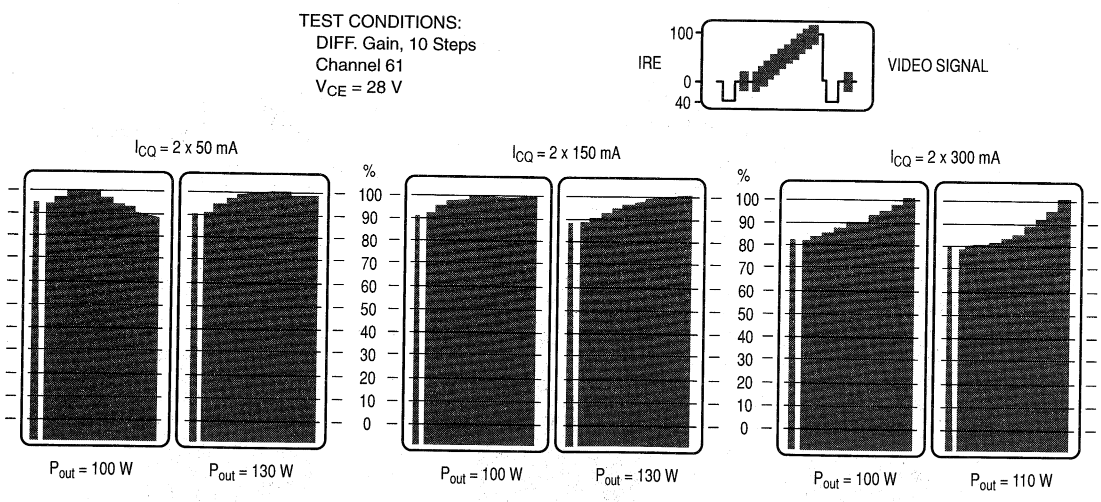
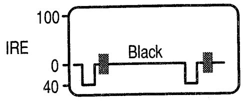


Figure 7. Gain versus Output Power

TYPICAL VIDEO CHARACTERISTICS @ f = 800 MHz
V_{CE} = 32 V



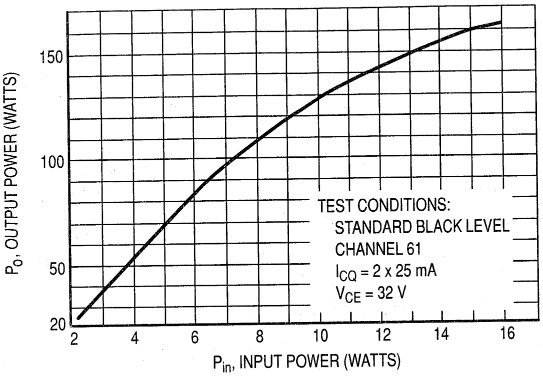


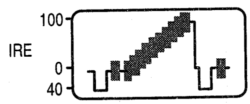
Figure 8. Peak Output Power versus Peak Input Power

V_{CE} = 32 V, I_{CQ} = 2 x 25 mA

P_{out}	Gain
25 W	10.6 dB
50 W	11.1 dB
100 W	11.3 dB
120 W	11.1 dB
130 W	11.0 dB
140 W	10.7 dB
150 W	10.5 dB
160 W	10.2 dB

(see curve on left)

TEST CONDITIONS:
DIFF. Gain, 10 Steps
Channel 61
V_{CE} = 32 V
I_{CQ} = 2 x 25 mA



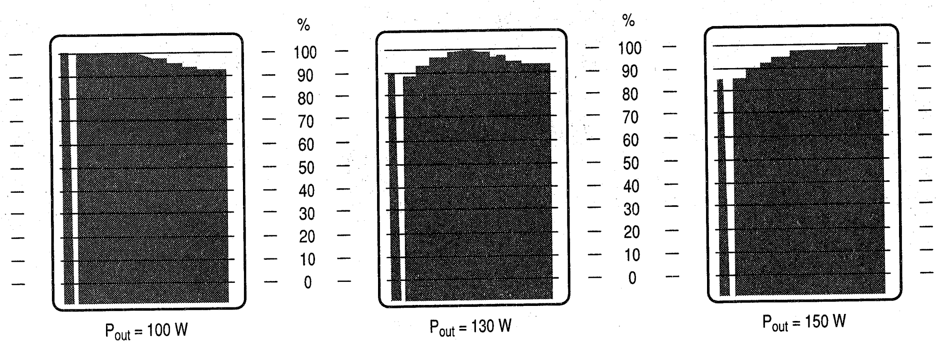


Figure 9. Differential Gain

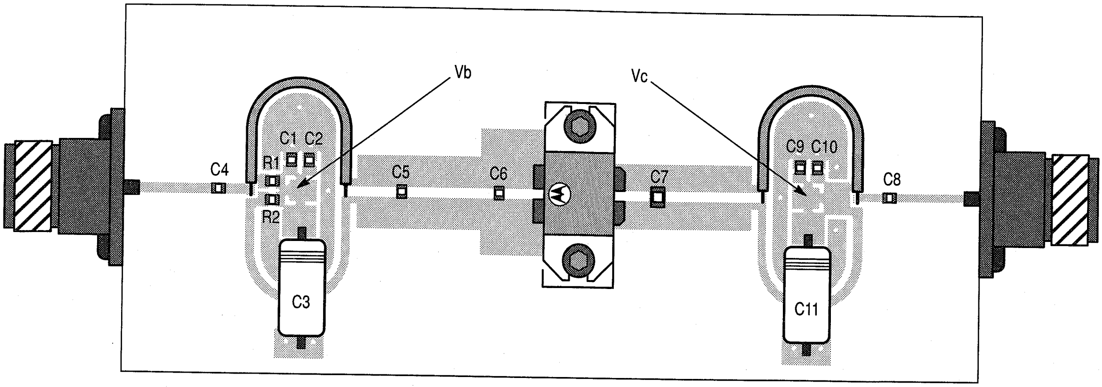


Figure 10. Components View

Section Three

Tape and Reel Specifications

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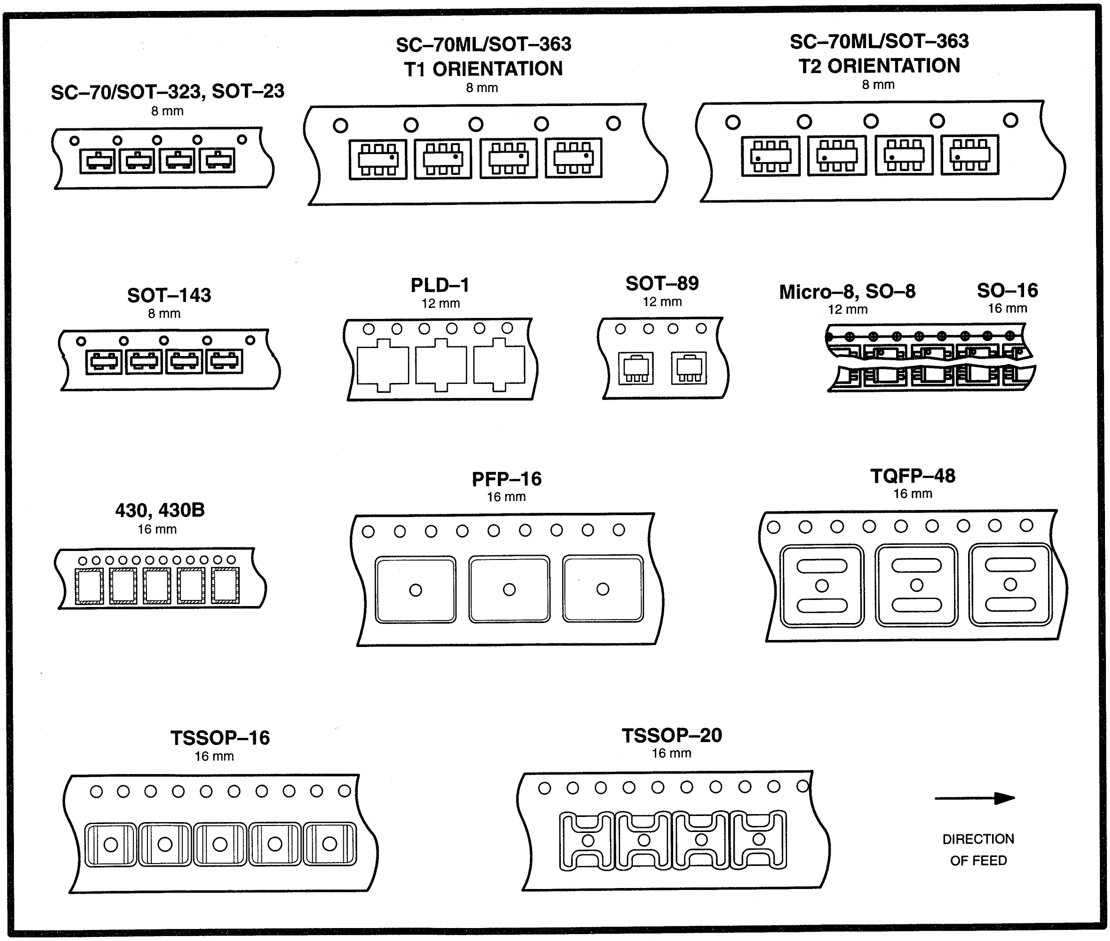
Tape and Reel Specifications

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the "peel–back" cover tape.

- Two Reel Sizes Available (7″ and 13″)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, –1, –2
- SC–70/SOT–323, SC–70ML/SOT–323, SOT–23, SOT–143 in 8 mm Tape
- Micro–8, PLD–1, SO–8, SOT–89 in 12 mm Tape
- SO–16, TQFP–48, TSSOP–16, TSSOP–20, 430 and 430B in 16 mm Tape

Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

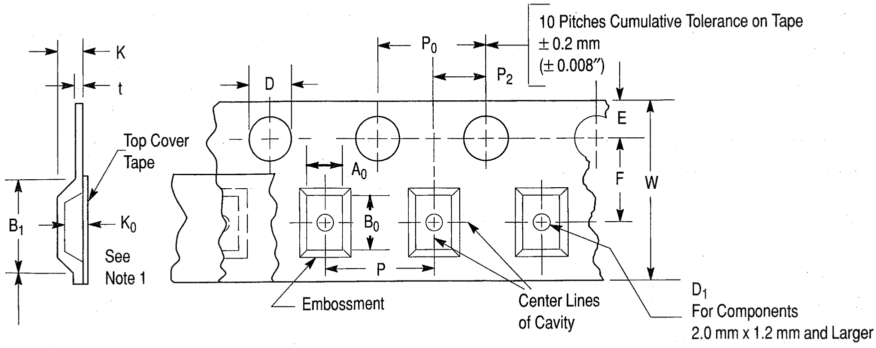


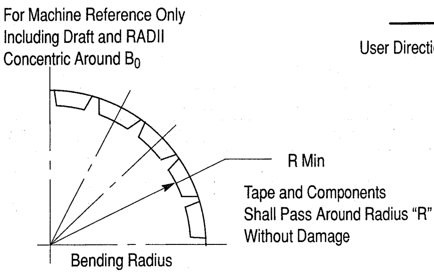
EMBOSSED TAPE AND REEL ORDERING INFORMATION

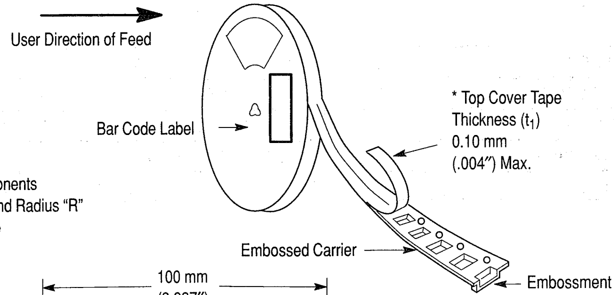
Package	Tape Width (mm)	Pitch mm (inch)	Reel Size mm (inch)	Devices Per Reel and Minimum Order Quantity	Device Suffix
SC–70/SOT–323	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
SC–70ML/SOT–323	8	4.0 ± 0.1 (.157 ± .004)	178 (7)	3,000 3,000	T1 T2
Micro–8	12	8.0 ± 0.1 (.315 ± .003)	330 (13)	4,000	R2
PLD–1	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
SO–8	12 12	8.0 ± 0.1 (.315 ± .004)	178 (7) 330 (13)	500 2,500	R1 R2
SOT–89	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
SO–16	16 16	8.0 ± 0.1 (.315 ± .004)	178 (7) 330 (13)	500 2,500	R1 R2
SOT–23	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
SOT–143	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
TQFP–48	16	12.0 ± 0.1 (.471 ± .004)	330 (13)	1,500	R2
TSSOP–16	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
TSSOP–20	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,000	R2
430, 430B	16	8.0 ± 0.1 (.315 ± .004)	178 (7)	500	R1
PFP–16	16	12.0 ± 0.1 (.471 ± .004)	330 (13)	1,500	R2

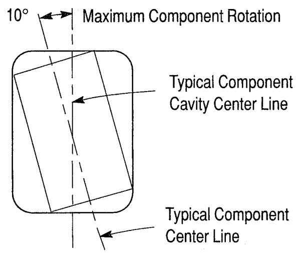
EMBOSSED TAPE AND REEL DATA FOR DISCRETES

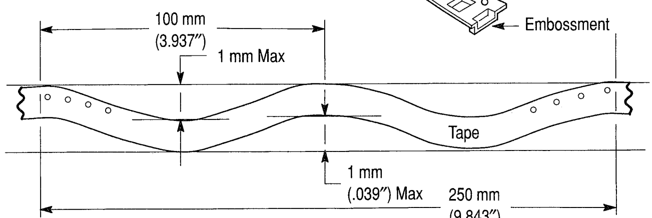
CARRIER TAPE SPECIFICATIONS











Camber (Top View)

Allowable Camber To Be 1 mm/100 mm Nonaccumulative Over 250 mm

DIMENSIONS

Tape Size	B_1 Max	D	D_1	E	F	K	P_0	P_2	R Min	T Max	W Max
8 mm	4.55 mm (.179″)	1.5 + 0.1 mm − 0.0 (.059 + .004″ − 0.0)	1.0 Min (.039″)	1.75 ± 0.1 mm (.069 ± .004″)	3.5 ± 0.05 mm (.138 ± .002″)	2.4 mm Max (.094″)	4.0 ± 0.1 mm (.157 ± .004″)	2.0 ± 0.1 mm (.079 ± .002″)	25 mm (.98″)	0.6 mm (.024″)	8.3 mm (.327″)
12 mm	8.2 mm (.323″)		1.5 mm Min (.060″)		5.5 ± 0.05 mm (.217 ± .002″)	6.4 mm Max (.252″)			30 mm (1.18″)		12 ± .30 mm (.470 ± .012″)
16 mm	12.1 mm (.476″)				7.5 ± 0.10 mm (.295 ± .004″)	7.9 mm Max (.311″)					16.3 mm (.642″)

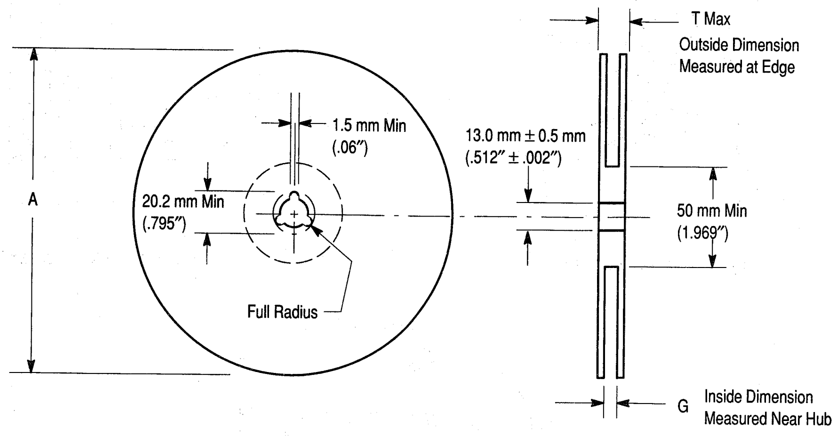
Metric dimensions govern — English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within .05 mm min. to .50 mm max., the component cannot rotate more than 10° within the determined cavity.

NOTE 2: If B_1 exceeds 4.2 mm (.165) for 8 mm embossed tape, the tape may not feed through all tape feeders.

NOTE 3: Pitch information is contained in the Embossed Tape and Reel Ordering Information on pg. 3–3.

EMBOSSED TAPE AND REEL DATA FOR DISCRETES



Size	A Max	G	T Max
8 mm	330 mm (12.992″)	8.4 mm + 1.5 mm, –0.0 (.33″ + .059″, –0.00)	14.4 mm (.56″)
12 mm	330 mm (12.992″)	12.4 mm + 2.0 mm, –0.0 (.49″ + .079″, –0.00)	18.4 mm (.72″)
16 mm	360 mm (14.173″)	16.4 mm + 2.0 mm, –0.0 (.646″ + .078″, –0.00)	22.4 mm (.882″)

Reel Dimensions

Metric Dimensions Govern — English are in parentheses for reference only

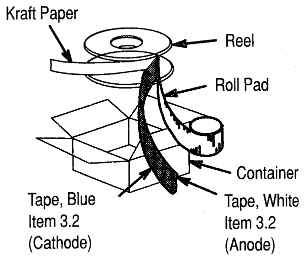


Figure 1. Reel Packing

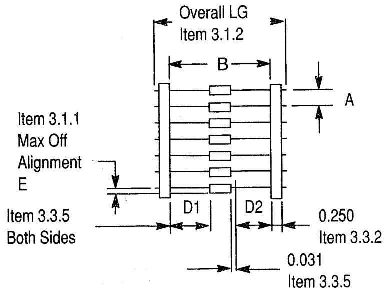


Figure 2. Component Spacing

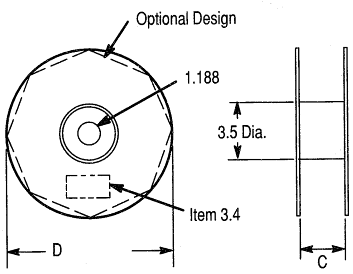


Figure 3. Reel Dimensions

Section Four

Surface Mount Information

In Brief . . .

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the state–of–the–art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that is common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

Table of Contents

INFORMATION FOR USING SURFACE MOUNT PACKAGES

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For example, for an SO–8 device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{100°C/W} = 1.25 \text{ Watts}$$

The 100°C/W for the SO–8 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.25 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the collector pad. By increasing the area of the collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–70/SOT–323, SOT–23, SOT–143 and the SO–8, the stencil opening should be the same as the pad size or a 1:1 registration.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 1 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

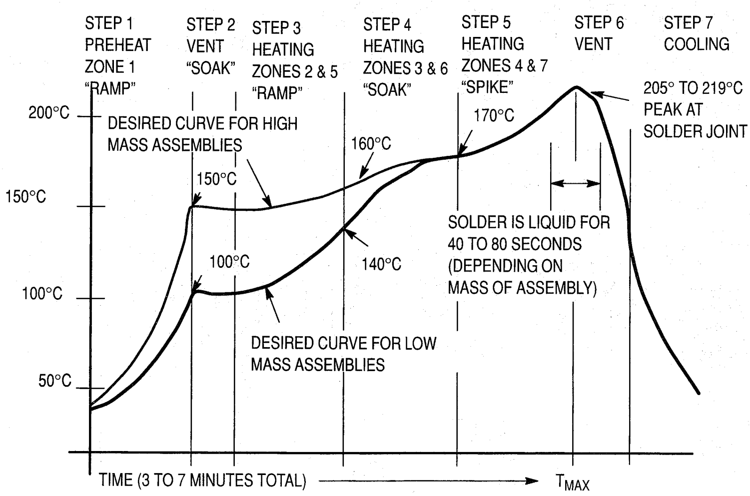
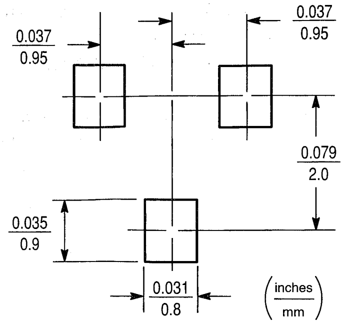
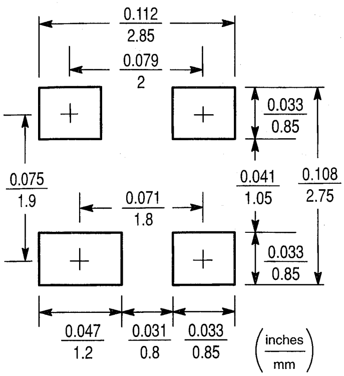


Figure 1. Typical Solder Heating Profile

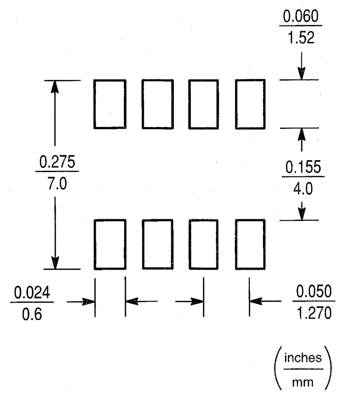
Footprints for Soldering



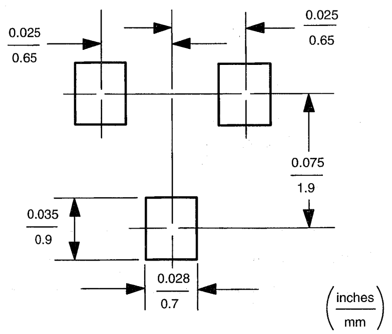
SOT–23



SOT–143



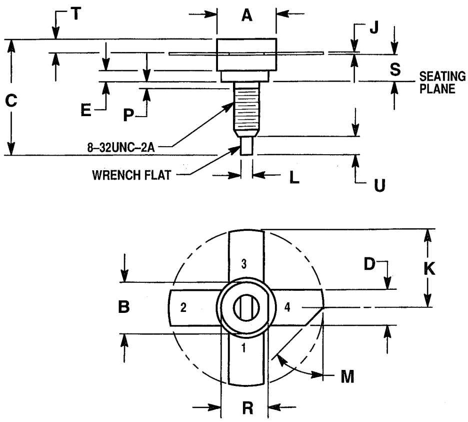
SO–8



SC–70/SOT–323

Section Five
Case Dimensions

Case Dimensions

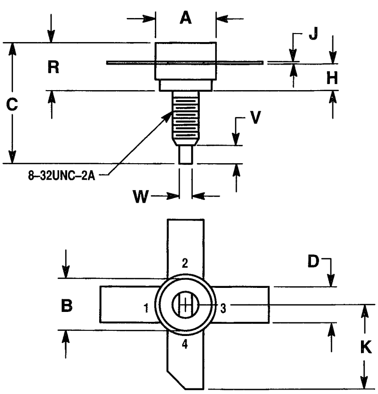


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.370	0.385	9.40	9.78
B	0.320	0.330	8.13	8.38
C	0.670	0.790	17.02	20.07
D	0.215	0.235	5.46	5.97
E	0.070	—	1.78	—
J	0.003	0.007	0.08	0.18
K	0.490	—	12.45	—
L	0.055	0.070	1.40	1.78
M	45°NOM		45°NOM	
P	—	0.050	—	1.27
R	0.299	0.307	7.59	7.80
S	0.158	0.178	4.01	4.52
T	0.083	0.100	2.11	2.54
U	0.098	0.132	2.49	3.35

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 145A–09
ISSUE M
(.380″ STUD)

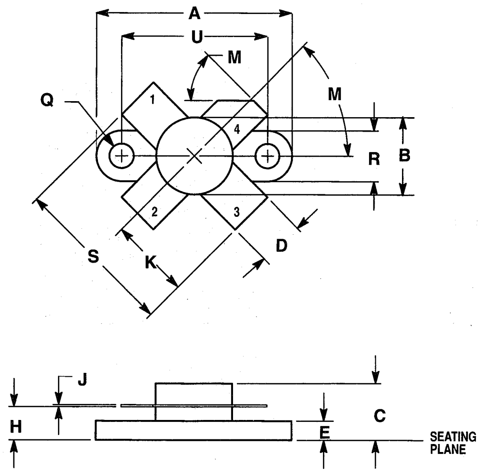


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.385	9.28	9.77
B	0.320	0.330	8.13	8.38
C	0.700	0.778	17.78	19.76
D	0.220	0.230	5.59	5.84
H	0.160	0.170	4.07	4.31
J	0.003	0.006	0.08	0.15
K	0.490	0.520	12.45	13.20
R	0.248	0.275	6.30	7.23
V	0.100	0.130	2.54	3.30
W	0.055	0.065	1.40	1.65

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 145D–02
ISSUE A
(.380″ SOE)



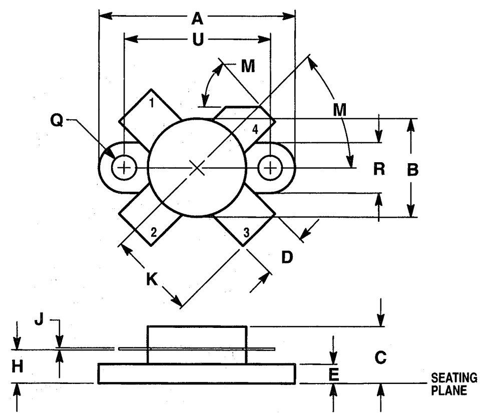
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.960	0.990	24.39	25.14
B	0.370	0.390	9.40	9.90
C	0.229	0.281	5.82	7.13
D	0.215	0.235	5.47	5.96
E	0.085	0.105	2.16	2.66
H	0.150	0.108	3.81	4.57
J	0.004	0.006	0.11	0.15
K	0.395	0.405	10.04	10.28
M	40°	50°	40°	50°
Q	0.113	0.130	2.88	3.30
R	0.245	0.255	6.23	6.47
S	0.790	0.810	20.07	20.57
U	0.720	0.730	18.29	18.54

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 211–07
ISSUE N
(.380″ FLANGE)



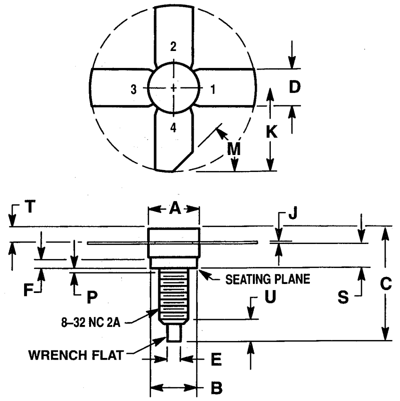
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.960	0.990	24.39	25.14
B	0.465	0.510	11.82	12.95
C	0.229	0.275	5.82	6.98
D	0.216	0.235	5.49	5.96
E	0.084	0.110	2.14	2.79
H	0.144	0.178	3.66	4.52
J	0.003	0.007	0.08	0.17
K	0.435	—	11.05	—
M	45°NOM		45°NOM	
Q	0.115	0.130	2.93	3.30
R	0.246	0.255	6.25	6.47
U	0.720	0.730	18.29	18.54

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

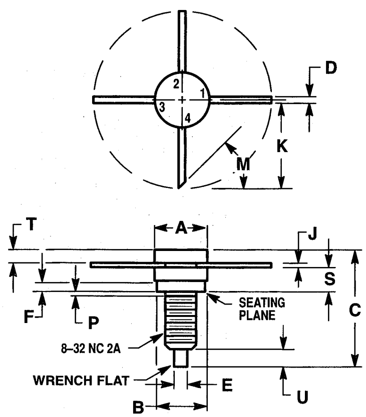
CASE 211–11
ISSUE N
(.500″ FLANGE)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
G	1.52	—	0.060	—
J	0.08	0.17	0.003	0.007
K	11.05	—	0.435	—
M	45°NOM		45°NOM	
P	—	1.27	—	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.77	0.055	0.070
U	2.92	3.68	0.115	0.145

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 244–04
ISSUE J
(.280″ STUD)

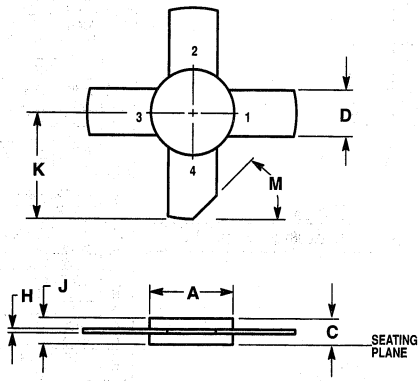


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	15.24	16.51	0.600	0.650
D	0.66	0.86	0.026	0.034
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.10	0.15	0.004	0.006
K	11.17	—	0.440	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	2.74	3.35	0.108	0.132
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

STYLE 3:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

CASE 244A–01
ISSUE A



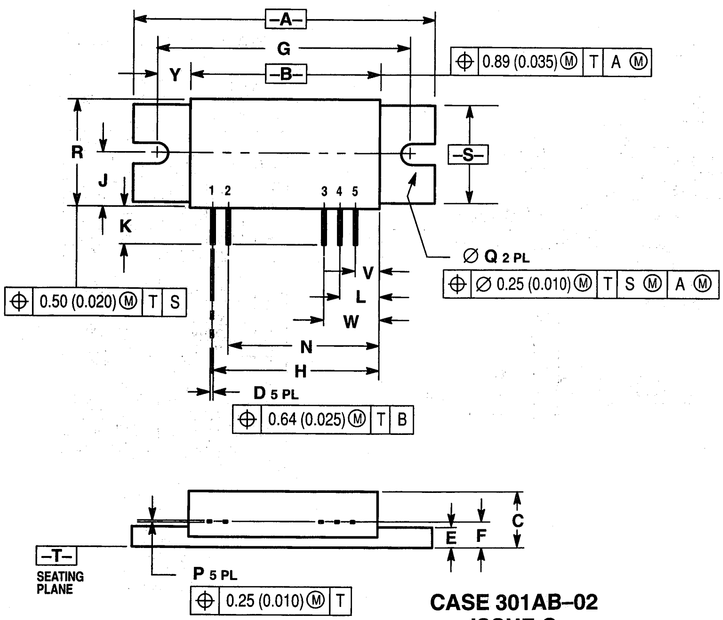
NOTES:
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.
5. SEATING PLANE = GROUND AND IS CONNECTED TO PIN 1 AND 3.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.271	0.286	6.88	7.26
C	0.112	0.136	2.84	3.45
D	0.215	0.235	5.46	5.97
H	0.055	0.065	1.40	1.65
J	0.003	0.007	0.08	0.18
K	0.435	—	11.05	—
M	45° REF		45° REF	

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

STYLE 3:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 249–06
ISSUE H
(.280″ PILL)

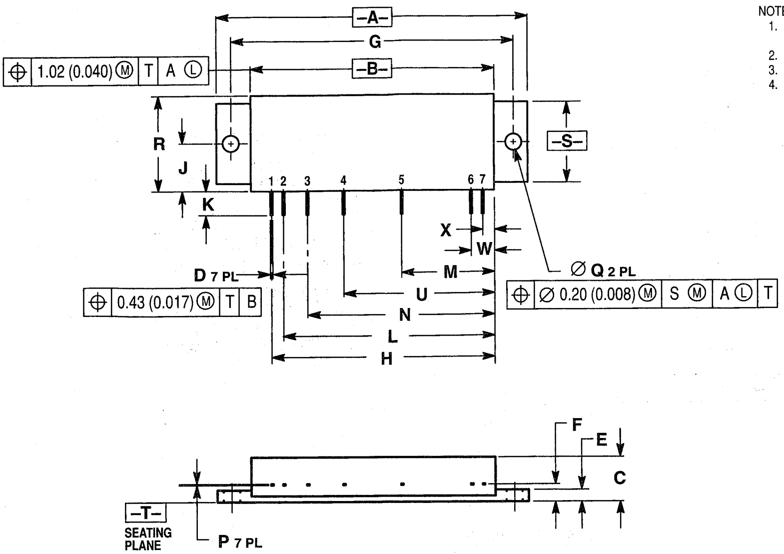


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.
4. REF INDICATES NON–CONTROLLED DIMENSION FOR REFERENCE USE ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.890	1.910	48.01	48.51
B	1.170	1.190	29.72	30.23
C	0.350	0.376	8.89	9.55
D	0.018	0.022	0.46	0.56
E	0.120	0.135	3.05	3.43
F	0.165 BSC		4.19 BSC	
G	1.600 BSC		40.64 BSC	
H	1.055 BSC		26.80 BSC	
J	0.336	0.360	8.53	9.14
K	0.225	—	5.72	—
L	0.255 BSC		6.48 BSC	
N	0.955 BSC		24.26 BSC	
P	0.008	0.012	0.20	0.31
Q	0.151	0.161	3.84	4.09
R	0.685	0.705	17.40	17.91
S	0.598	0.612	15.19	15.55
V	0.155 BSC		3.94 BSC	
W	0.355 BSC		9.02 BSC	
Y	0.210 REF		5.33 REF	

STYLE 1:
PIN 1. RF INPUT
2. +DC (BIAS)
3. +DC (SUPPLY)
4. +DC (SUPPLY)
5. RF OUTPUT
CASE: GROUND

CASE 301AB–02
ISSUE G

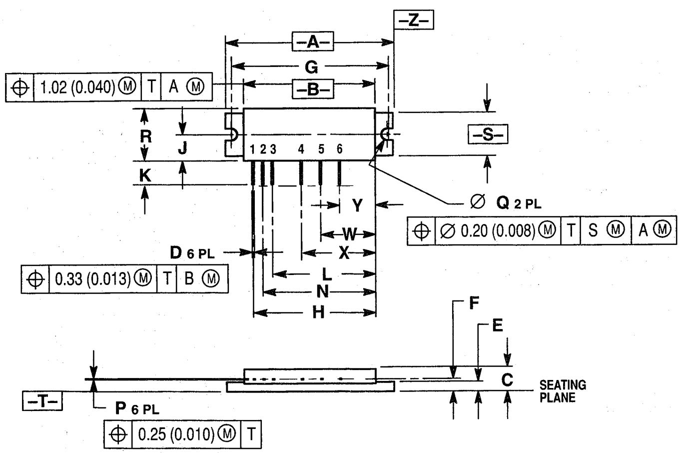


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.
4. REF INDICATES NON–CONTROLLED DIMENSION FOR REFERENCE USE ONLY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.638	2.662	67.01	67.61
B	2.075 REF		52.71 REF	
C	—	0.375	—	9.53
D	0.017	0.023	0.43	0.58
E	0.098	0.114	2.49	2.90
F	0.134	0.156	3.40	3.96
G	2.405 BSC REF		61.09 BSC REF	
H	1.900 BSC		48.26 BSC	
J	0.390	0.430	9.91	10.92
K	0.175	0.217	4.45	5.51
L	1.800 BSC		45.72 BSC	
M	0.800 BSC		20.32 BSC	
N	1.600 BSC		40.64 BSC	
P	0.010 REF		0.25 REF	
Q	0.133	0.147	3.38	3.73
R	0.800	0.820	20.32	20.83
S	0.668	0.692	16.97	17.58
U	1.300 BSC		33.02 BSC	
W	0.200 BSC		5.08 BSC	
X	0.100 BSC		2.54 BSC	

STYLE 1:
PIN 1. RF INPUT
2. DC TERMINAL, Vs1
3. DC TERMINAL, Vs2
4. DC TERMINAL, Vb
5. DC TERMINAL, Vs3
6. DC TERMINAL, Vs4
7. RF OUTPUT

CASE 301AK–01
ISSUE B

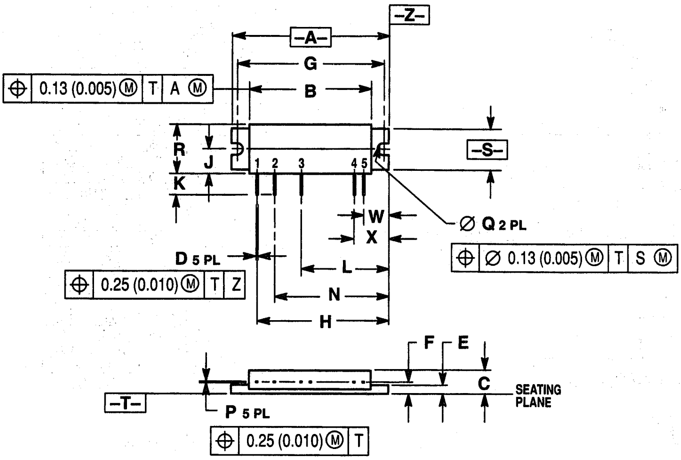


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.
4. REF INDICATES NON–CONTROLLED DIMENSION FOR REFERENCE USE ONLY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.132 BSC		3.35 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.230	0.300	5.84	7.62
L	1.090 BSC		27.69 BSC	
N	1.190 BSC		30.25 BSC	
P	0.010 REF		0.25 REF	
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
V	0.590 BSC		14.99 BSC	
X	0.790 BSC		20.07 BSC	
X	0.390 BSC		9.91 BSC	

STYLE 1:
PIN 1. RF INPUT
2. VDD1
3. VCONT
4. VDD2
5. VDD3
6. RF OUTPUT
CASE: GROUND

CASE 301AL–01
ISSUE O

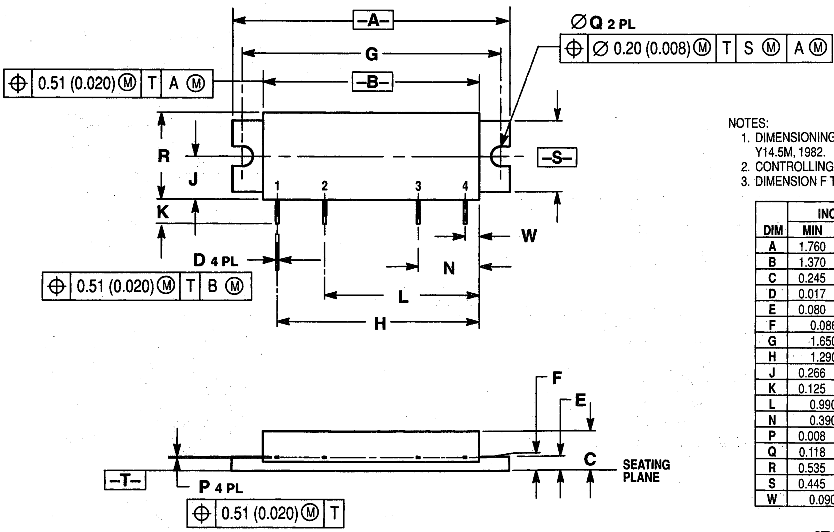


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.760	1.780	44.71	45.21
B	1.370	1.390	34.80	35.31
C	0.240	0.270	6.10	6.86
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.132 BSC		3.35 BSC	
G	1.655 BSC		42.04 BSC	
H	1.490 BSC		37.85 BSC	
J	0.266	0.280	6.76	7.11
K	0.230	0.300	5.85	7.62
L	0.990 BSC		25.15 BSC	
N	1.290 BSC		32.77 BSC	
P	0.008	0.013	0.21	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.09
S	0.445	0.465	11.31	11.81
W	0.285 BSC		7.24 BSC	
X	0.390 BSC		9.91 BSC	

STYLE 1:
PIN 1. RF INPUT
2. VD1, VD2
3. VCONT
4. VD3
5. RF OUTPUT
CASE: GROUND

CASE 301AN–02
ISSUE B

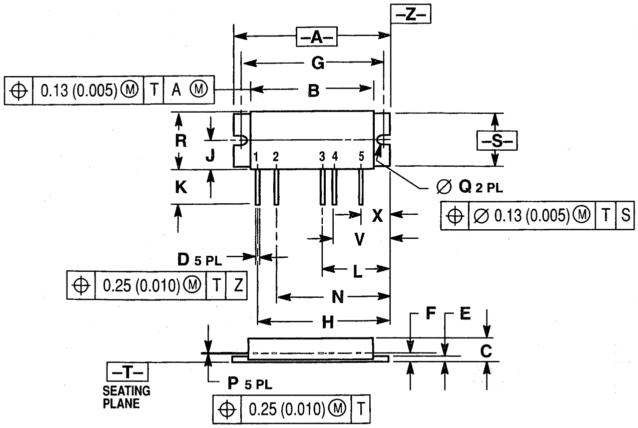


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.086 BSC		2.18 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.125	0.165	3.18	4.19
L	0.990 BSC		25.15 BSC	
N	0.390 BSC		9.91 BSC	
P	0.008	0.013	0.20	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
W	0.090 BSC		2.29 BSC	

STYLE 1:
PIN 1. RF INPUT
2. VDD1
3. VDD2
4. RF OUTPUT
CASE: GROUND

CASE 301AP–01
ISSUE A

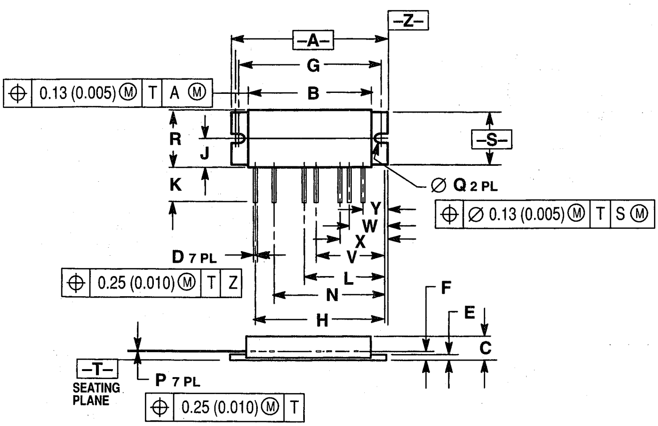


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.760	1.780	44.71	45.21
B	1.370	1.390	34.80	35.30
C	0.245	0.265	6.23	6.73
D	0.018	0.022	0.46	0.55
E	0.080	0.100	2.04	2.54
F	0.130 BSC		3.30 BSC	
G	1.650 BSC		41.91 BSC	
H	1.485 BSC		37.72 BSC	
J	0.267	0.278	6.79	7.06
K	0.230	0.300	5.85	7.62
L	0.785 BSC		19.94 BSC	
N	1.285 BSC		32.64 BSC	
P	0.008	0.012	0.21	0.30
Q	0.120	0.130	3.05	3.30
R	0.535	0.555	13.59	14.09
S	0.445	0.465	11.31	11.81
V	0.685 BSC		17.40 BSC	
X	0.385 BSC		9.78 BSC	

STYLE 1:
PIN 1. RF INPUT/V CONT
2. VS1
3. VS2
4. VS3
5. RF OUTPUT
CASE: GROUND

CASE 301E–04
ISSUE F



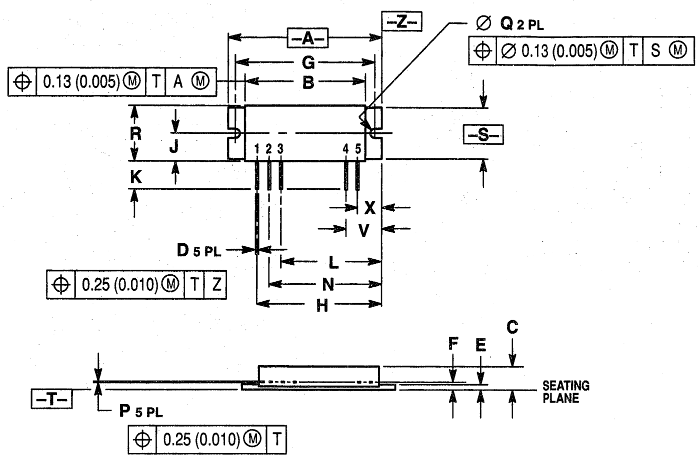
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.380	2.395	60.46	6.083
B	1.970	1.990	50.04	50.54
C	0.250	0.265	6.35	6.73
D	0.018	0.022	0.46	0.55
E	0.085	0.100	2.16	2.54
F	0.132 BSC		3.35 BSC	
G	2.260 BSC		57.40 BSC	
H	2.042 BSC		51.87 BSC	
J	0.267	0.278	6.78	7.06
K	0.230	0.300	5.85	7.62
L	1.242 BSC		31.55 BSC	
N	1.742 BSC		44.25 BSC	
P	0.008	0.012	0.21	0.30
Q	0.120	0.130	3.05	3.30
R	0.535	0.555	13.59	14.09
S	0.445	0.465	11.31	11.81
V	1.142 BSC		29.01 BSC	
W	0.542 BSC		13.77 BSC	
X	0.642 BSC		16.31 BSC	
Y	0.342 BSC		8.69 BSC	

STYLE 1:
PIN 1. RF INPUT/V CONT
2. VS1
3. VS2
4. VS3
5. VS4
6. VS5
7. RF OUTPUT
CASE: GROUND

CASE 301F–03
ISSUE C

CASE DIMENSIONS (continued)

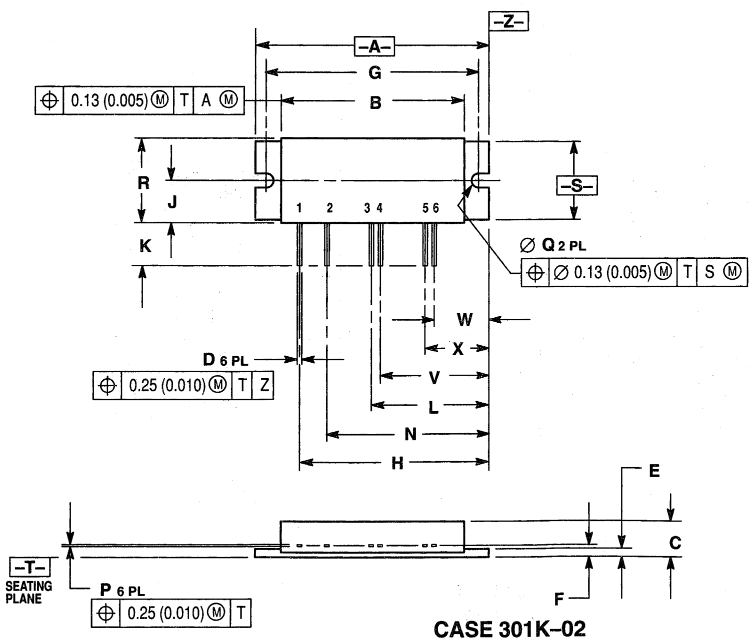


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.190	2.210	55.63	56.13
B	1.395	1.415	35.44	35.94
C	0.350	0.376	8.89	9.55
D	0.018	0.022	0.46	0.55
E	0.120	0.135	3.05	3.42
F	0.160 BSC		4.06 BSC	
G	1.900 BSC		48.26 BSC	
H	1.600 BSC		40.64 BSC	
J	0.345	0.385	8.77	9.77
K	0.225	—	5.72	—
L	1.400 BSC		35.56 BSC	
N	1.500 BSC		38.10 BSC	
P	0.008	0.012	0.21	0.30
Q	0.150	0.160	3.81	4.06
R	0.690	0.770	17.53	19.55
S	0.595	0.610	15.12	15.49
V	0.700 BSC		17.78 BSC	
X	0.500 BSC		12.70 BSC	

STYLE 1:
PIN 1. RF INPUT
2. +DC
3. +DC
4. +DC
5. RF OUTPUT
CASE: GROUND

CASE 301G–03
ISSUE C



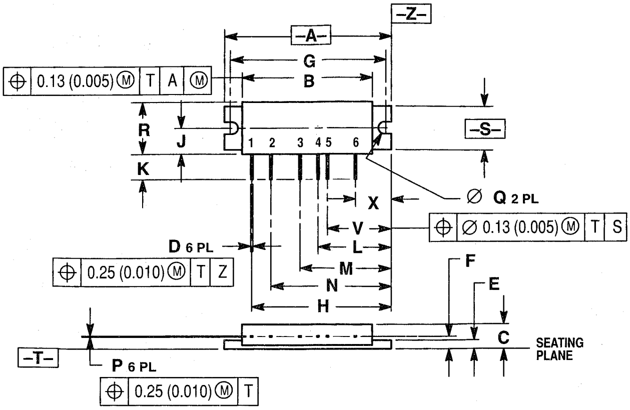
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.770	1.785	44.96	45.35
B	1.370	1.390	34.80	35.31
C	0.250	0.265	6.35	6.73
D	0.018	0.022	0.46	0.55
E	0.085	0.100	2.16	2.54
F	0.132 BSC		3.35 BSC	
G	1.655 BSC		42.04 BSC	
H	1.490 BSC		37.85 BSC	
J	0.267	0.278	6.78	7.06
K	0.230	0.300	5.85	7.62
L	0.990 BSC		25.15 BSC	
N	1.290 BSC		32.77 BSC	
P	0.008	0.012	0.21	0.30
Q	0.120	0.130	3.05	3.30
R	0.535	0.555	13.59	14.09
S	0.445	0.465	11.31	11.81
V	0.890 BSC		22.61 BSC	
W	0.285 BSC		7.24 BSC	
X	0.390 BSC		9.91 BSC	

STYLE 3:
PIN 1. RF INPUT
2. VS1
3. VCONT
4. VS2
5. VS3
6. RF OUTPUT
CASE: GROUND

CASE 301K–02
ISSUE G

CASE DIMENSIONS (continued)

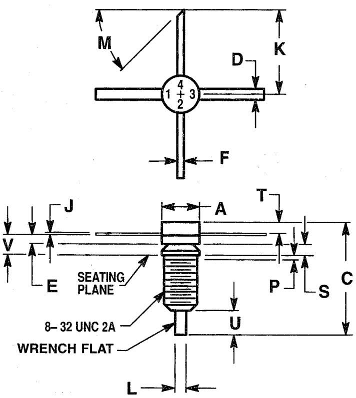


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.760	1.780	44.71	45.21
B	1.370	1.390	34.80	35.30
C	0.245	0.265	6.23	6.73
D	0.018	0.022	0.46	0.55
E	0.080	0.100	2.04	2.54
F	0.130 BSC		3.30 BSC	
G	1.650 BSC		41.91 BSC	
H	1.485 BSC		37.72 BSC	
J	0.267	0.278	6.79	7.09
K	0.177	0.217	4.50	5.51
L	0.785 BSC		19.94 BSC	
M	0.985 BSC		25.02 BSC	
N	1.285 BSC		32.64 BSC	
P	0.008	0.012	0.21	0.30
Q	0.120	0.130	3.05	3.30
R	0.535	0.555	13.59	14.09
S	0.445	0.465	11.31	11.81
V	0.685 BSC		17.40 BSC	
X	0.385 BSC		9.78 BSC	

STYLE 1:
PIN 1. RF INPUT/V CONT
2. VS1
3. Vb
4. VS2
5. VS3
6. RF OUTPUT
CASE: GROUND

CASE 301V–02
ISSUE D

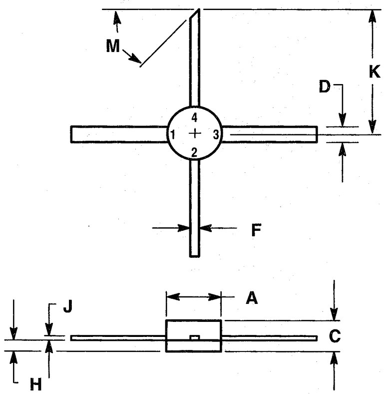


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.200	0.220	5.08	5.59
C	0.550	0.640	13.97	16.26
D	0.055	0.065	1.40	1.65
E	0.040	0.050	1.02	1.27
F	0.025	0.035	0.64	0.89
J	0.003	0.007	0.08	0.18
K	0.435	—	11.05	—
L	0.055	0.065	1.40	1.65
M	45°NOM		45°NOM	
P	—	0.050	—	1.27
S	0.055	0.065	1.40	1.65
T	0.055	0.070	1.40	1.78
U	0.110	0.150	2.79	3.81
V	0.095	0.115	2.41	2.92

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 305–01
ISSUE O
(.204″ STUD)

CASE DIMENSIONS (continued)



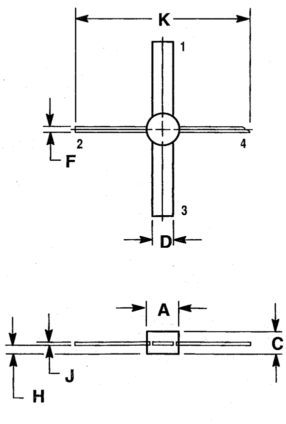
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.200	0.220	5.08	5.59
C	0.095	0.130	2.41	3.30
D	0.055	0.065	1.40	1.65
F	0.025	0.035	0.64	0.89
H	0.040	0.050	1.02	1.27
J	0.003	0.007	0.08	0.18
K	0.435	—	11.05	—
M	45 °REF		45 °REF	

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 305A–01
ISSUE A
(.204″ PILL)



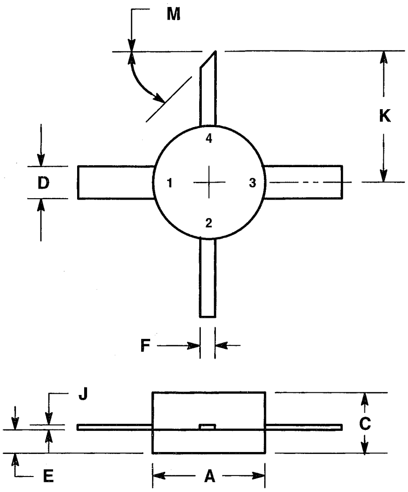
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.200	0.210	5.08	5.33
C	—	0.125	—	3.17
D	0.120	0.130	3.05	3.30
F	0.025	0.035	0.64	0.88
H	0.035	0.045	0.88	1.14
J	0.004	0.006	0.11	0.15
K	0.970	1.030	24.64	26.16

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 305C–02
ISSUE A

CASE DIMENSIONS (continued)

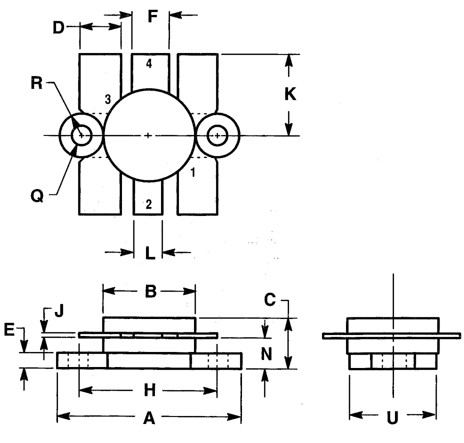


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.200	0.220	5.08	5.59
C	0.095	0.130	2.41	3.30
D	0.055	0.065	1.40	1.65
E	0.040	0.050	1.02	1.27
F	0.025	0.035	0.64	0.89
J	0.003	0.007	0.08	0.18
K	0.235	0.265	5.97	6.73
M	45° NOM		45° NOM	

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 305D–01
ISSUE O



NOTES:
1. FLANGE IS ISOLATED IN ALL STYLES.

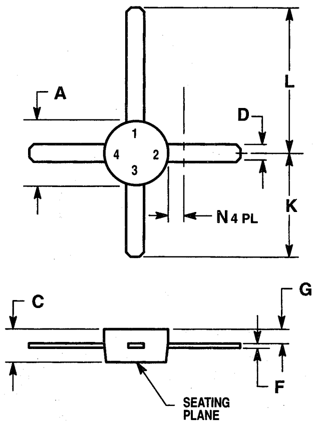
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	24.38	25.14	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.58	0.210	0.220
E	2.16	3.04	0.085	0.120
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.17	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.31	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130
U	11.94	12.57	0.470	0.495

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

STYLE 3:
PIN 1. SOURCE
2. DRAIN
3. SOURCE
4. GATE

CASE 316–01
ISSUE D
(.500″ CQ)

CASE DIMENSIONS (continued)



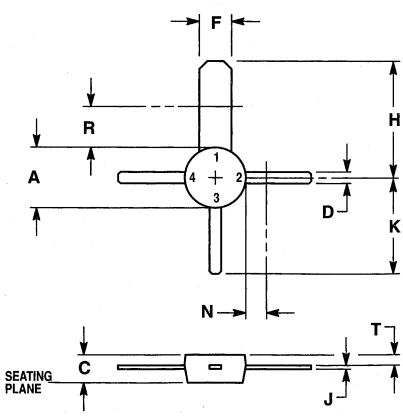
NOTES:
1. DIMENSION D NOT APPLICABLE IN ZONE N.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.080	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

STYLE 1:
PIN 1. DRAIN
2. SOURCE
3. GATE 1
4. GATE 2

STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 317–01
ISSUE E
(MACRO–X)

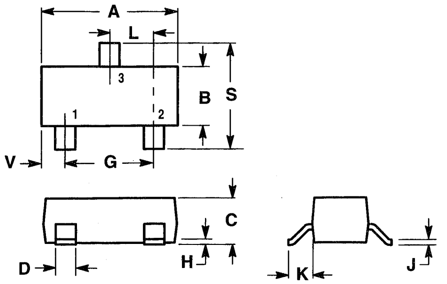


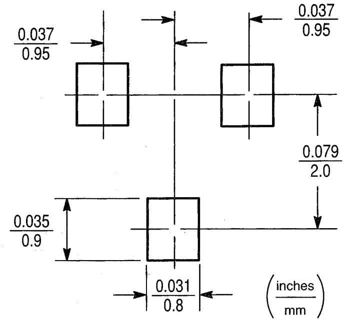
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. LEAD DIMENSIONS UNCONTROLLED WITHIN DIMENSION N AND R.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.175	0.205	4.45	5.20
C	0.075	0.100	1.91	2.54
D	0.033	0.039	0.84	0.99
F	0.097	0.104	2.46	2.64
H	0.348	0.383	8.84	9.72
J	0.008	0.012	0.24	0.30
K	0.285	0.320	7.24	8.12
N	—	0.065	—	1.65
R	—	0.128	—	3.25
T	0.025	0.040	0.64	1.01

STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 317D–02
ISSUE C
(POWER MACRO)





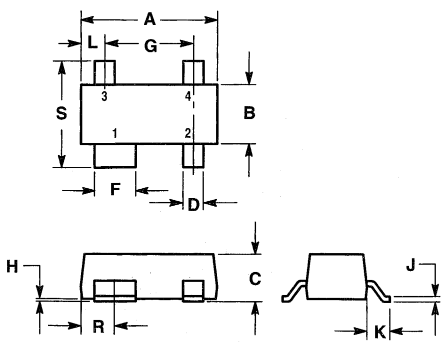
SOT–23 FOOTPRINT

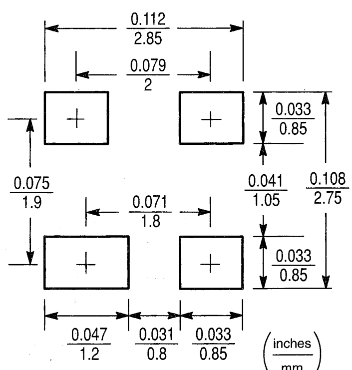
STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

CASE 318–08
ISSUE AF
(TO–236AB)





SOT–143 FOOTPRINT

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. EMITTER
4. BASE

STYLE 7:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SOURCE

STYLE 8:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. N/C

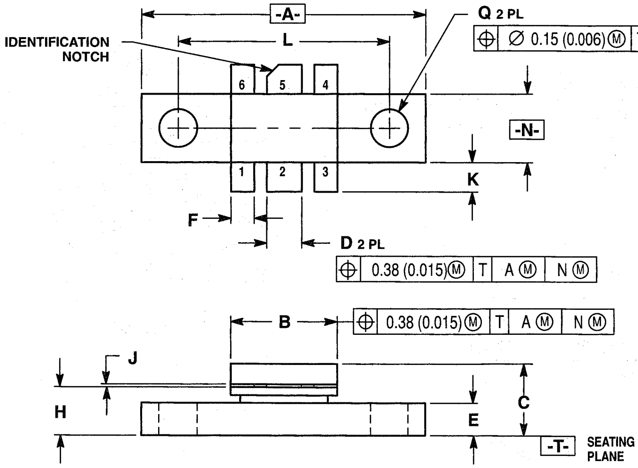
STYLE 11:
PIN 1. SOURCE
2. GATE 1
3. GATE 2
4. DRAIN

NOTES:
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.110	0.120
B	1.20	1.39	0.047	0.055
C	0.84	1.14	0.033	0.045
D	0.39	0.50	0.015	0.020
F	0.79	0.93	0.031	0.037
G	1.78	2.03	0.070	0.080
H	0.013	0.10	0.0005	0.004
J	0.08	0.15	0.003	0.006
K	0.46	0.60	0.018	0.024
L	0.445	0.60	0.0175	0.024
R	0.72	0.83	0.028	0.033
S	2.11	2.48	0.083	0.098

CASE 318A–05
ISSUE R

CASE DIMENSIONS (continued)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

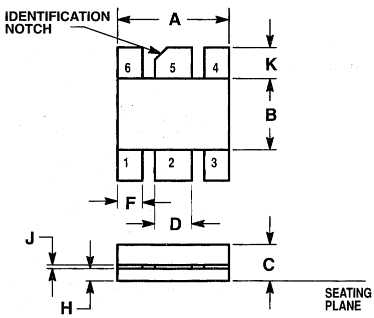
DIM	INCHES MIN	INCHES MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.965	0.985	24.52	25.01
B	0.355	0.375	9.02	9.52
C	0.230	0.260	5.85	6.60
D	0.115	0.125	2.93	3.17
E	0.102	0.114	2.59	2.90
F	0.075	0.085	1.91	2.15
H	0.160	0.170	4.07	4.31
J	0.004	0.006	0.11	0.15
K	0.090	0.110	2.29	2.79
L	0.725 BSC		18.42 BSC	
N	0.225	0.241	5.72	6.12
Q	0.125	0.135	3.18	3.42

STYLE 1:
PIN 1. BASE (COMMON)
2. EMITTER (INPUT)
3. BASE (COMMON)
4. BASE (COMMON)
5. COLLECTOR (OUTPUT)
6. BASE (COMMON)

STYLE 2:
PIN 1. EMITTER (COMMON)
2. BASE (INPUT)
3. EMITTER (COMMON)
4. EMITTER (COMMON)
5. COLLECTOR (OUTPUT)
6. EMITTER (COMMON)

STYLE 3:
PIN 1. SOURCE (COMMON)
2. GATE (INPUT)
3. SOURCE (COMMON)
4. SOURCE (COMMON)
5. DRAIN (OUTPUT)
6. SOURCE (COMMON)

CASE 319–07
ISSUE M
(CS–12)

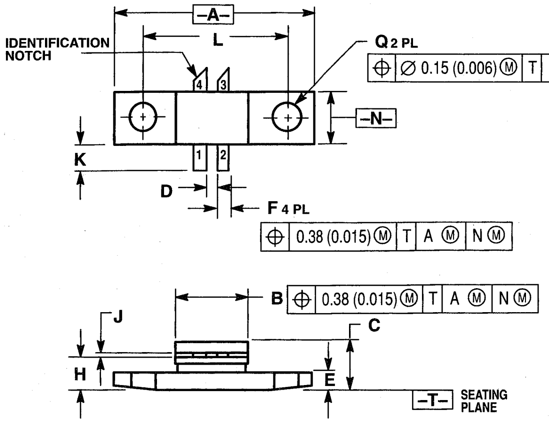


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.355	0.365	9.02	9.27
B	0.225	0.235	5.72	5.96
C	0.110	0.125	2.80	3.17
D	0.115	0.125	2.93	3.17
F	0.075	0.085	1.91	2.15
H	0.035	0.045	0.89	1.14
J	0.004	0.006	0.11	0.15
K	0.090	0.110	2.29	2.79

STYLE 2:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. EMITTER
5. COLLECTOR
6. EMITTER

CASE 319A–02
ISSUE B

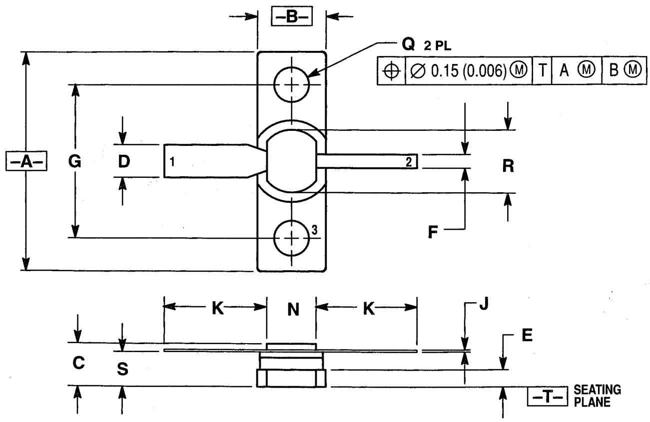


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.965	0.985	24.51	25.02
B	0.355	0.375	9.02	9.52
C	0.230	0.260	5.84	6.60
D	0.055	0.065	1.40	1.65
E	0.102	0.114	2.59	2.90
F	0.055	0.065	1.40	1.65
H	0.160	0.170	4.06	4.31
J	0.004	0.006	0.10	0.15
K	0.120	0.140	3.05	3.55
L	0.725 BSC		18.42 BSC	
N	0.225	0.241	5.72	6.12
Q	0.125	0.135	3.18	3.42

STYLE 1:
PIN 1. GATE (INPUT)
2. GATE (INPUT)
3. DRAIN (OUTPUT)
4. DRAIN (OUTPUT)
SOURCE IS FLANGE

CASE 319B–02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M. 1982.
2. CONTROLLING DIMENSION: INCH.

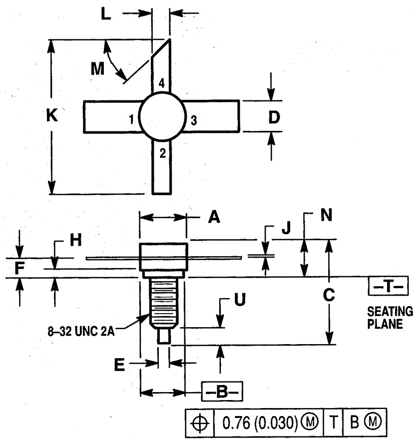
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.795	0.805	20.20	20.45
B	0.245	0.255	6.23	6.47
C	0.145	0.170	3.69	4.31
D	0.115	0.125	2.93	3.17
E	0.055	0.065	1.40	1.65
F	0.045	0.055	1.15	1.39
G	0.562 BSC		14.27 BSC	
J	0.003	0.006	0.08	0.15
K	0.260	0.375	6.60	9.52
N	0.175	0.185	4.45	4.69
Q	0.120	0.135	3.05	3.42
R	0.225	0.235	5.72	5.97
S	0.120	0.130	3.05	3.30

STYLE 1:
1. EMITTER
2. COLLECTOR
3. BASE

STYLE 2:
1. BASE
2. COLLECTOR
3. EMITTER

CASE 328A–03
ISSUE E

CASE DIMENSIONS (continued)



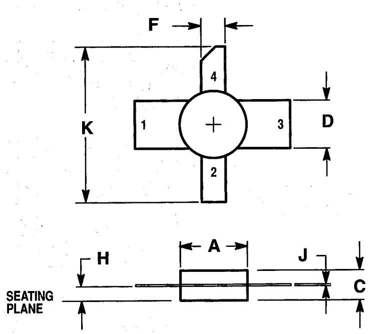
NOTES:
1. DIMENSION K APPLIES TWO PLACES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.86	7.62	0.270	0.300
B	6.10	6.60	0.240	0.260
C	16.26	16.76	0.640	0.660
D	4.95	5.21	0.195	0.205
E	1.40	1.65	0.055	0.065
F	2.67	4.32	0.105	0.170
H	1.40	1.65	0.055	0.065
J	0.08	0.18	0.003	0.007
K	15.24	—	0.600	—
L	2.41	2.67	0.095	0.105
M	45° NOM		45° NOM	
N	4.97	6.22	0.180	0.245
U	2.92	3.68	0.115	0.145

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 332–04
ISSUE D
(.280″ STUD)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

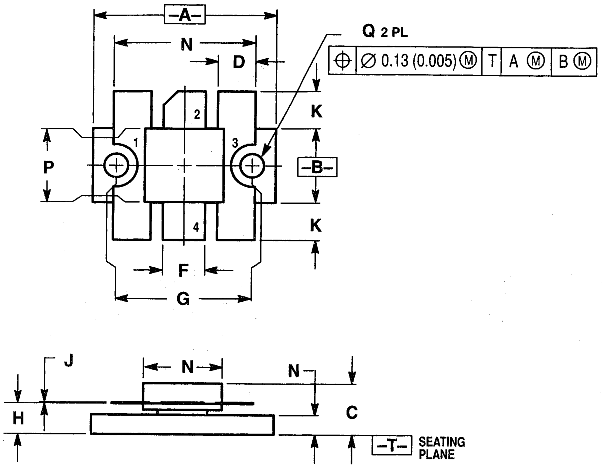
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.270	0.290	6.86	7.36
C	0.115	0.135	2.93	3.42
D	0.195	0.205	4.96	5.20
F	0.095	0.105	2.42	2.66
H	0.050	0.070	1.27	1.77
J	0.003	0.007	0.08	0.17
K	0.600	—	15.24	—

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 332A–03
ISSUE D
(.280″ PILL)

CASE DIMENSIONS (continued)



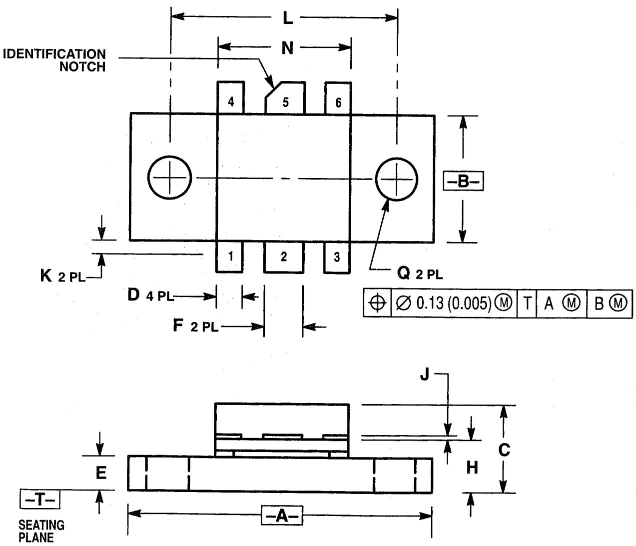
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.965	0.985	24.51	25.02
B	0.390	0.410	9.91	10.41
C	0.250	0.290	6.73	7.36
D	0.190	0.210	4.83	5.33
E	0.095	0.115	2.42	2.92
F	0.215	0.235	5.47	5.96
G	0.725 BSC		18.42 BSC	
H	0.155	0.175	3.94	4.44
J	0.004	0.006	0.10	0.15
K	0.195	0.205	4.95	5.21
L	0.740	0.770	18.80	19.55
N	0.415	0.425	10.54	10.80
P	0.390	0.400	9.91	10.16
Q	0.120	0.135	3.05	3.42

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

STYLE 2:
PIN 1. SOURCE
2. DRAIN
3. SOURCE
4. GATE

CASE 333–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

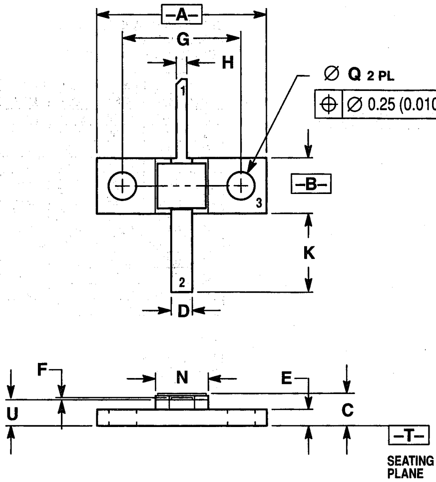
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.965	0.985	24.52	25.01
B	0.390	0.410	9.91	10.41
C	0.250	0.290	6.35	7.36
D	0.075	0.090	1.91	2.28
E	0.095	0.115	2.42	2.92
F	0.110	0.130	2.80	3.30
H	0.155	0.175	3.94	4.44
J	0.004	0.006	0.11	0.15
K	0.090	0.116	2.29	2.94
L	0.725 BSC		18.41 BSC	
N	0.415	0.435	10.55	11.04
Q	0.120	0.135	3.05	3.42

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. BASE
5. COLLECTOR
6. BASE

STYLE 2:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. EMITTER
5. COLLECTOR
6. EMITTER

CASE 333A–02
ISSUE C
(MAAC PAC)

CASE DIMENSIONS (continued)

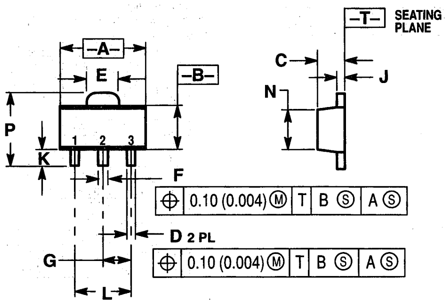


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.790	0.810	20.07	20.57
B	0.253	0.267	6.43	6.78
C	0.144	0.160	3.66	4.06
D	0.093	0.107	2.37	2.71
E	0.074	0.080	1.88	2.03
F	0.002	0.006	0.06	0.15
G	0.560 BSC		14.22 BSC	
H	0.043	0.057	1.10	1.44
K	0.346	0.394	8.79	10.10
N	0.243	0.257	6.18	6.52
Q	0.125	0.135	3.18	3.42
U	0.117	0.128	2.98	3.25

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 336E–02
ISSUE B



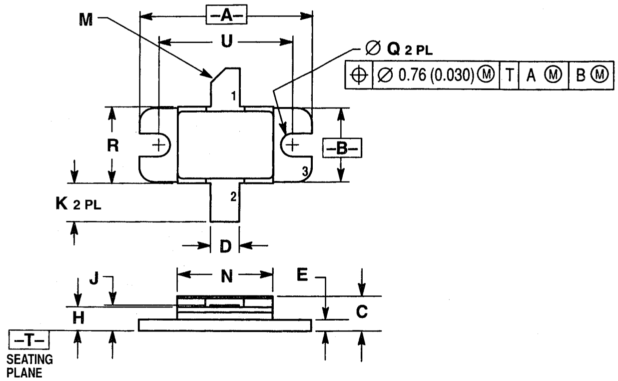
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.40	4.60	0.174	0.181
B	2.29	2.60	0.091	0.102
C	1.40	1.60	0.056	0.062
D	0.36	0.48	0.015	0.018
E	1.62	1.80	0.064	0.070
F	0.44	0.55	0.018	0.021
G	1.50 BSC		0.059 BSC	
J	0.35	0.44	0.014	0.017
K	0.89	1.20	0.035	0.047
L	3.00 BSC		0.118 BSC	
N	2.14	2.28	0.084	0.089
P	3.94	4.25	0.156	0.167

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. DRAIN
2. SOURCE
3. GATE

CASE 345–03
ISSUE H

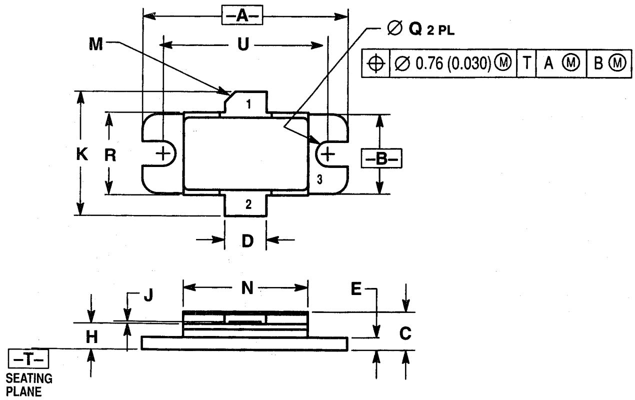


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.890	0.910	22.61	23.11
B	0.375	0.395	9.53	10.03
C	0.150	0.165	3.81	4.19
D	0.145	0.155	3.69	3.93
E	0.055	0.065	1.40	1.65
H	0.120	0.130	3.05	3.30
J	0.003	0.006	0.08	0.15
K	0.185	0.215	4.70	5.46
M	45° REF		45° REF	
N	0.490	0.510	12.45	12.95
Q	0.115	0.125	2.93	3.17
R	0.395	0.405	10.04	10.28
U	0.700 BSC		17.78 BSC	

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 355C–02
ISSUE C



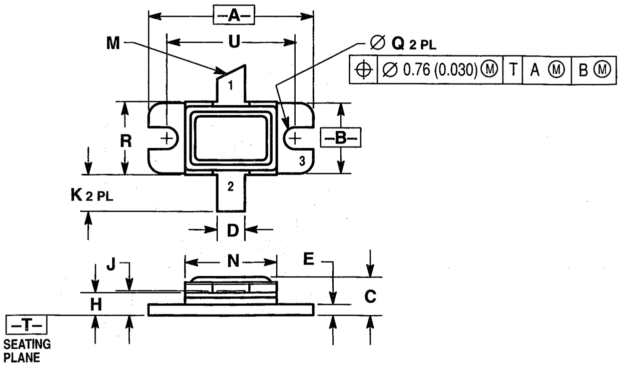
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.990	1.010	25.15	25.65
B	0.375	0.395	9.53	10.03
C	0.150	0.165	3.81	4.19
D	0.195	0.205	4.95	5.21
E	0.055	0.065	1.40	1.65
H	0.120	0.130	3.05	3.30
J	0.003	0.006	0.08	0.15
K	0.570	0.630	14.48	16.00
M	45° REF		45° REF	
N	0.590	0.610	14.99	15.49
Q	0.115	0.125	2.92	3.18
R	0.395	0.405	10.03	10.29
U	0.800 BSC		20.32 BSC	

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 355D–02
ISSUE B

CASE DIMENSIONS (continued)

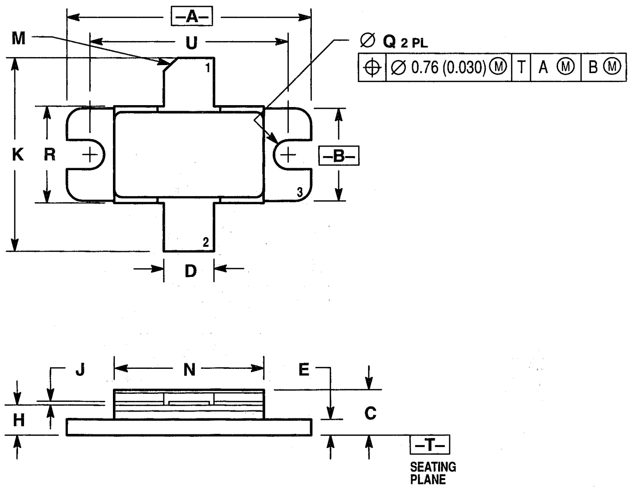


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.890	0.910	22.61	23.11
B	0.375	0.395	9.53	10.03
C	0.190	0.210	4.83	5.33
D	0.145	0.155	3.69	3.93
E	0.055	0.065	1.40	1.65
H	0.120	0.130	3.05	3.30
J	0.003	0.006	0.08	0.15
K	0.185	0.215	4.70	5.46
M	45° REF		45° REF	
N	0.490	0.510	12.45	12.95
Q	0.115	0.125	2.93	3.17
R	0.395	0.405	10.04	10.28
U	0.700 BSC		17.78 BSC	

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 355E–01
ISSUE B

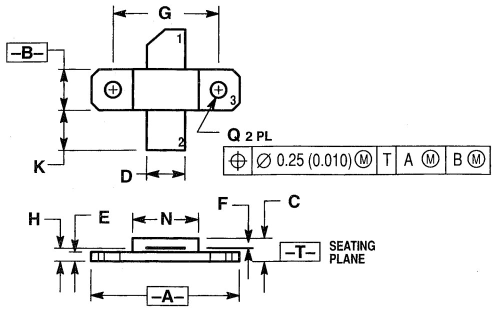


NOTES:
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
7. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.990	1.010	25.15	25.65
B	0.375	0.395	9.53	10.03
C	0.150	0.165	3.81	4.19
D	0.195	0.205	4.95	5.21
E	0.055	0.065	1.40	1.65
H	0.120	0.130	3.05	3.30
J	0.003	0.006	0.08	0.15
K	0.780	0.820	19.81	20.83
M	45° REF		45° REF	
N	0.590	0.610	14.99	15.49
Q	0.115	0.125	2.92	3.18
R	0.395	0.405	10.03	10.29
U	0.800 BSC		20.32 BSC	

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 355H–01
ISSUE A

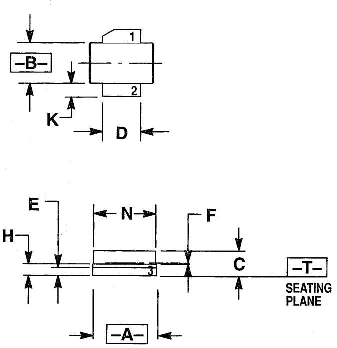


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.790	0.810	20.07	20.57
B	0.220	0.240	5.59	6.09
C	0.125	0.175	3.18	4.45
D	0.205	0.225	5.21	5.71
E	0.050	0.070	1.27	1.77
F	0.004	0.006	0.11	0.15
G	0.562 BSC		14.27 BSC	
H	0.070	0.090	1.78	2.29
K	0.215	0.255	5.47	6.47
N	0.350	0.370	8.89	9.39
Q	0.120	0.140	3.05	3.55

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 360B–01
ISSUE O

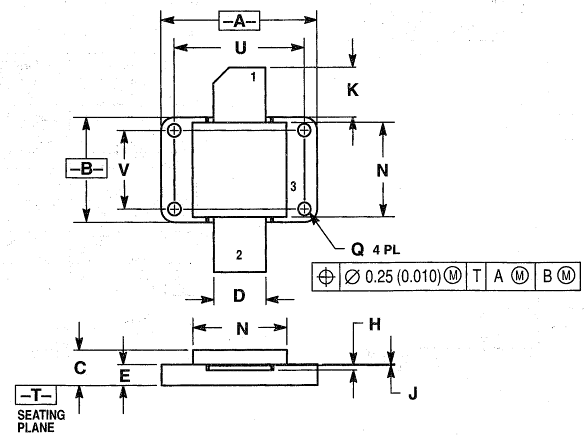


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.370	0.390	9.40	9.91
B	0.220	0.240	5.59	6.09
C	0.105	0.155	2.67	3.94
D	0.205	0.225	5.21	5.71
E	0.035	0.045	0.89	1.14
F	0.004	0.006	0.11	0.15
H	0.057	0.067	1.45	1.70
K	0.085	0.115	2.16	2.92
N	0.350	0.370	8.89	9.39

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 360C–03
ISSUE B

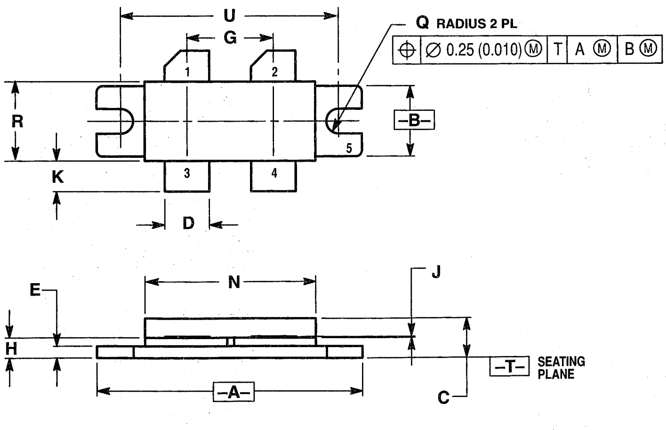


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.490	1.510	37.85	38.35
B	0.990	1.010	25.15	25.65
C	0.330	0.365	8.38	9.27
D	0.490	0.510	12.45	12.95
E	0.195	0.205	4.95	5.21
H	0.045	0.055	1.14	1.39
J	0.004	0.006	0.10	0.15
K	0.425	0.500	10.80	12.70
N	0.890	0.910	22.87	23.11
Q	0.120	0.130	3.05	3.30
U	1.250 BSC		31.75 BSC	
V	0.750 BSC		19.05 BSC	

STYLE 2:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 368–03
ISSUE C
(HOG PAC)

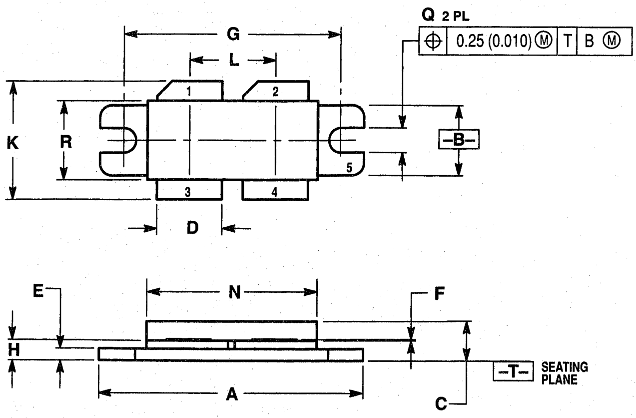


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.370	0.410	9.40	10.41
C	0.190	0.230	4.83	5.84
D	0.215	0.235	5.47	5.96
E	0.050	0.070	1.27	1.77
G	0.430	0.440	10.92	11.18
H	0.102	0.112	2.59	2.84
J	0.004	0.006	0.11	0.15
K	0.185	0.215	4.83	5.33
N	0.845	0.875	21.46	22.23
Q	0.060	0.070	1.52	1.78
R	0.390	0.410	9.91	10.41
U	1.100 BSC		27.94 BSC	

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375–04
ISSUE D

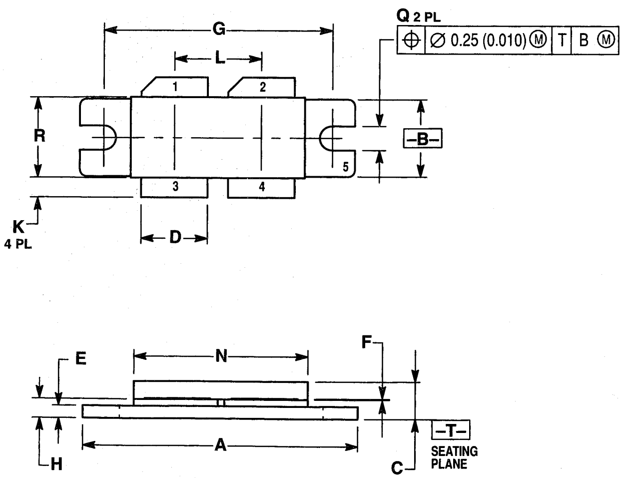


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.330	1.350	33.79	34.29
B	0.375	0.395	9.52	10.03
C	0.180	0.205	4.57	5.21
D	0.320	0.340	8.13	8.64
E	0.060	0.070	1.52	1.77
F	0.004	0.006	0.11	0.15
G	1.100 BSC		27.94 BSC	
H	0.082	0.097	2.08	2.46
K	0.580	0.620	14.73	15.75
L	0.435 BSC		11.05 BSC	
N	0.845	0.875	21.46	22.23
Q	0.118	0.130	3.00	3.30
R	0.390	0.410	9.91	10.41

STYLE 1:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. BASE
5. EMITTER

CASE 375A–01
ISSUE O



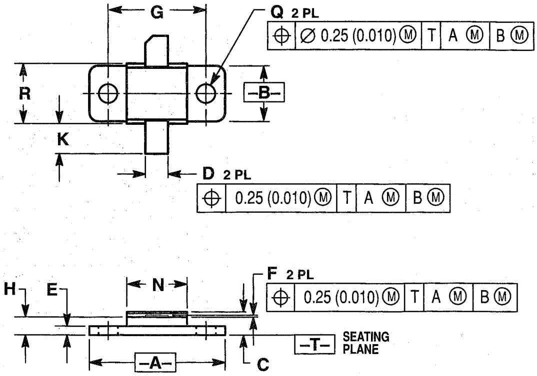
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.330	1.350	33.79	34.29
B	0.375	0.395	9.52	10.03
C	0.180	0.210	4.57	5.33
D	0.320	0.340	8.13	8.64
E	0.060	0.070	1.52	1.77
F	0.004	0.006	0.11	0.15
G	1.100 BSC		27.94 BSC	
H	0.093	0.108	2.36	2.74
K	0.085	0.115	2.16	2.92
L	0.425 BSC		10.80 BSC	
N	0.845	0.875	21.46	22.23
Q	0.118	0.130	3.00	3.30
R	0.390	0.410	9.91	10.41

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375B–02
ISSUE A

CASE DIMENSIONS (continued)

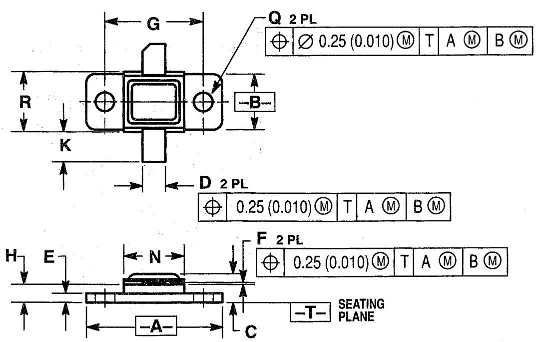


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.890	0.910	22.61	23.11
B	0.370	0.400	9.40	10.16
C	0.145	0.160	3.69	4.06
D	0.140	0.160	3.56	4.06
E	0.055	0.065	1.40	1.65
F	0.003	0.006	0.08	0.15
G	0.650 BSC		16.51 BSC	
H	0.110	0.130	2.80	3.30
K	0.180	0.220	4.57	5.59
N	0.390	0.410	9.91	10.41
Q	0.115	0.135	2.93	3.42
R	0.390	0.140	9.91	10.41

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 376B–02
ISSUE B

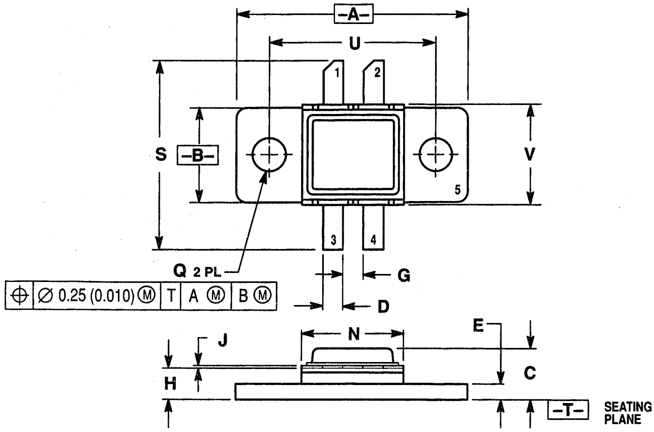


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.890	0.910	22.61	23.11
B	0.370	0.400	9.40	10.16
C	0.190	0.210	4.83	5.33
D	0.140	0.160	3.56	4.06
E	0.055	0.065	1.40	1.65
F	0.003	0.006	0.08	0.15
G	0.650 BSC		16.51 BSC	
H	0.110	0.130	2.80	3.30
K	0.180	0.220	4.57	5.59
N	0.390	0.410	9.91	10.41
Q	0.115	0.135	2.93	3.42
R	0.390	0.140	9.91	10.41

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 376C–01
ISSUE O

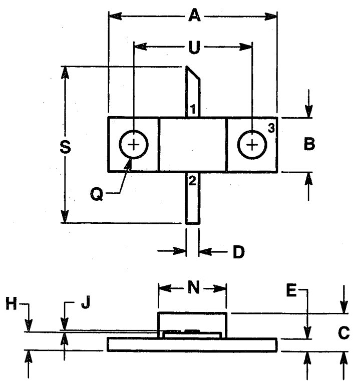


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.895	0.905	22.73	22.99
B	0.380	0.390	9.65	9.91
C	0.172	0.208	4.37	5.28
D	0.075	0.085	1.91	2.16
E	0.055	0.065	1.40	1.65
G	0.075	0.085	1.91	2.16
H	0.115	0.125	2.92	3.18
J	0.003	0.006	0.08	0.15
N	0.393	0.403	9.98	10.24
Q	0.123	0.133	3.13	3.38
S	0.705	0.745	17.91	18.92
U	0.650 BSC		16.51 BSC	
V	0.393	0.403	9.98	10.24

STYLE 1:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. BASE
5. EMITTER

CASE 391–03
ISSUE C

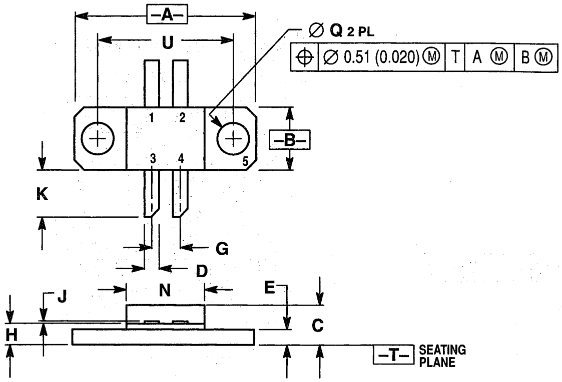


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.795	0.805	20.19	20.45
B	0.255	0.265	6.48	6.73
C	0.156	0.176	3.96	4.47
D	0.055	0.065	1.40	1.65
E	0.057	0.063	1.45	1.60
H	0.081	0.089	1.98	2.34
J	0.002	0.006	0.05	0.15
N	0.316	0.326	8.03	8.28
Q	0.125	0.135	3.18	3.43
S	0.620	0.680	15.75	17.27
U	0.552	0.572	14.02	14.53

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 394–03
ISSUE B

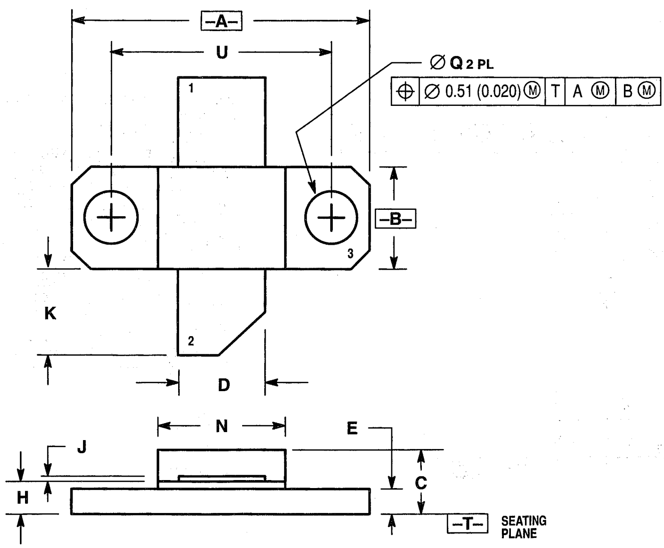


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.739	0.750	18.77	19.05
B	0.240	0.260	6.10	6.60
C	0.165	0.198	4.19	5.03
D	0.055	0.065	1.40	1.65
E	0.055	0.070	1.40	1.78
G	0.110	0.130	2.79	3.30
H	0.079	0.091	2.01	2.31
J	0.003	0.005	0.08	0.13
K	0.180	0.220	4.57	5.59
N	0.315	0.330	8.00	8.38
Q	0.125	0.135	3.18	3.42
U	0.560 BSC		14.22 BSC	

STYLE 1:
PIN 1. BASE
2. BASE
3. COLLECTOR
4. COLLECTOR
5. EMITTER

CASE 395B–01
ISSUE A



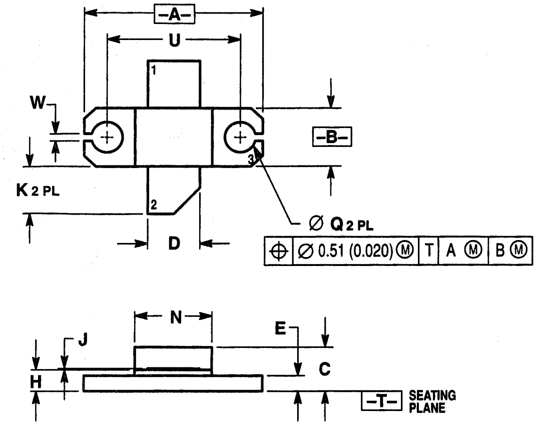
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.739	0.750	18.77	19.05
B	0.240	0.260	6.10	6.60
C	0.165	0.198	4.19	5.03
D	0.215	0.225	5.46	5.72
E	0.055	0.070	1.40	1.78
H	0.079	0.091	2.01	2.31
J	0.004	0.006	0.10	0.15
K	0.210	0.240	5.33	6.10
N	0.315	0.330	8.00	8.38
Q	0.125	0.135	3.18	3.42
U	0.560 BSC		14.23 BSC	

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

CASE 395C–01
ISSUE A

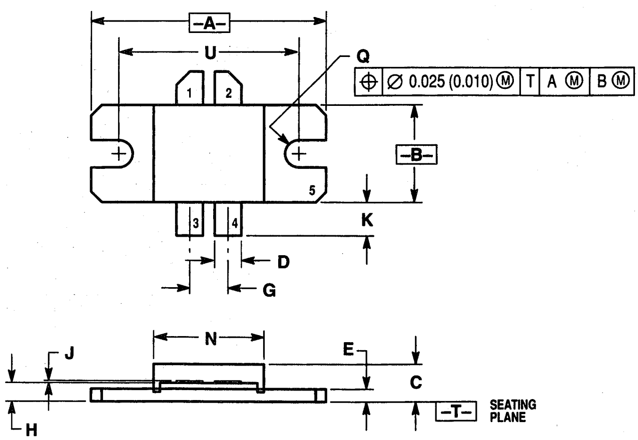


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.739	0.750	18.77	19.05
B	0.240	0.260	6.10	6.60
C	0.165	0.198	4.19	5.03
D	0.215	0.225	5.46	5.72
E	0.060	0.070	1.52	1.78
H	0.084	0.096	2.13	2.44
J	0.004	0.006	0.10	0.15
K	0.178	0.208	4.52	5.28
N	0.315	0.330	8.00	8.38
Q	0.125	0.135	3.18	3.42
U	0.560 BSC		14.23 BSC	
W	0.035	0.045	0.89	1.14

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

CASE 395D–03
ISSUE B

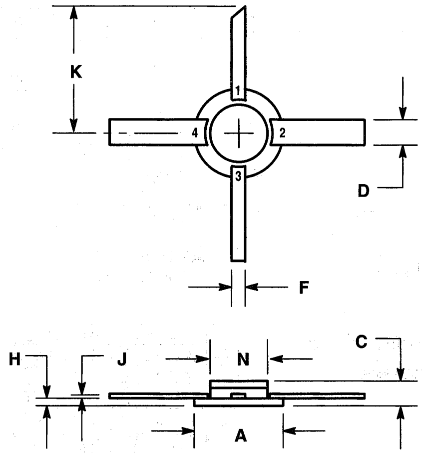


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.094	1.110	27.79	28.19
B	0.457	0.465	11.61	11.81
C	0.165	0.182	4.25	4.62
D	0.121	0.131	3.08	3.32
E	0.055	0.065	1.40	1.65
G	0.177	0.185	4.50	4.69
H	0.081	0.091	2.06	2.31
J	0.002	0.004	0.06	0.10
K	0.142	0.163	3.60	4.14
N	0.510	0.520	12.95	13.21
Q	0.125	0.135	3.18	3.42
U	0.844 BSC		21.44 BSC	

STYLE 1:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. BASE
5. EMITTER

CASE 398–03
ISSUE C

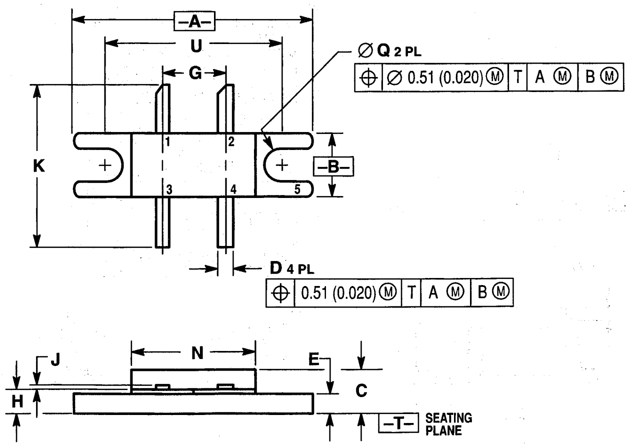


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.203	0.207	5.16	5.25
C	0.049	0.065	1.25	1.65
D	0.055	0.065	1.40	1.65
F	0.025	0.035	0.64	0.88
H	0.017	0.023	0.44	0.58
J	0.002	0.004	0.06	0.10
K	0.280	0.320	7.12	8.12
N	0.123	0.133	3.13	3.37

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 400–01
ISSUE B

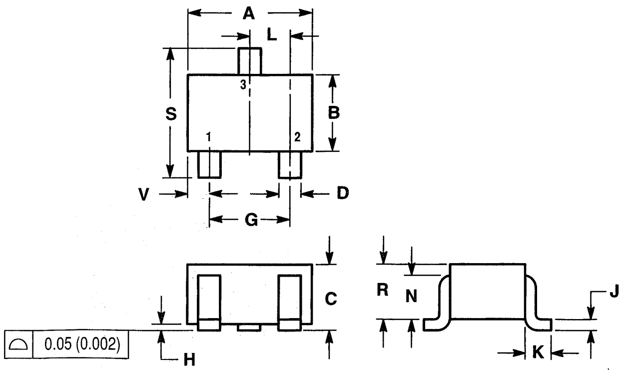


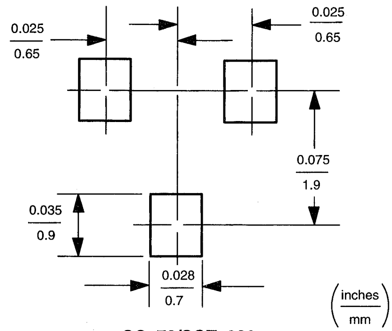
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.965	0.985	24.52	25.01
B	0.245	0.265	6.23	6.73
C	0.165	0.185	4.20	4.69
D	0.050	0.070	1.27	1.77
E	0.070	0.080	1.78	2.03
G	0.254 BSC		6.45 BSC	
H	0.095	0.105	2.42	2.66
J	0.003	0.006	0.08	0.15
K	0.625	0.675	15.88	17.14
N	0.495	0.520	12.58	13.20
Q	0.120	0.140	3.05	3.55
U	0.725 BSC		18.42 BSC	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 412–01
ISSUE O





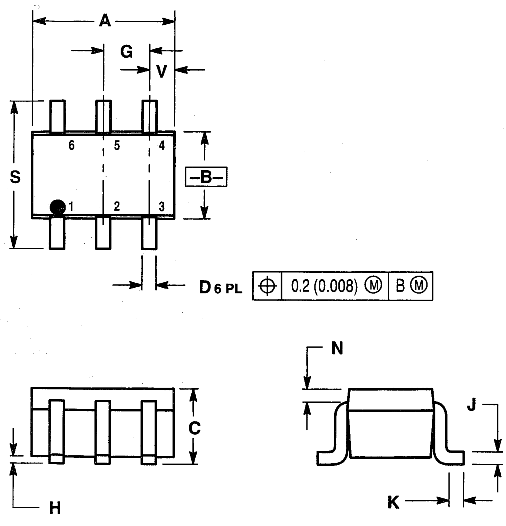
SC–70/SOT–323 FOOTPRINT

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.035	0.049	0.90	1.25
D	0.012	0.016	0.30	0.40
G	0.047	0.055	1.20	1.40
H	0.000	0.004	0.00	0.10
J	0.004	0.010	0.10	0.25
K	0.017 REF		0.425 REF	
L	0.026 BSC		0.650 BSC	
N	0.028 REF		0.700 REF	
R	0.031	0.039	0.80	1.00
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

CASE 419–02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

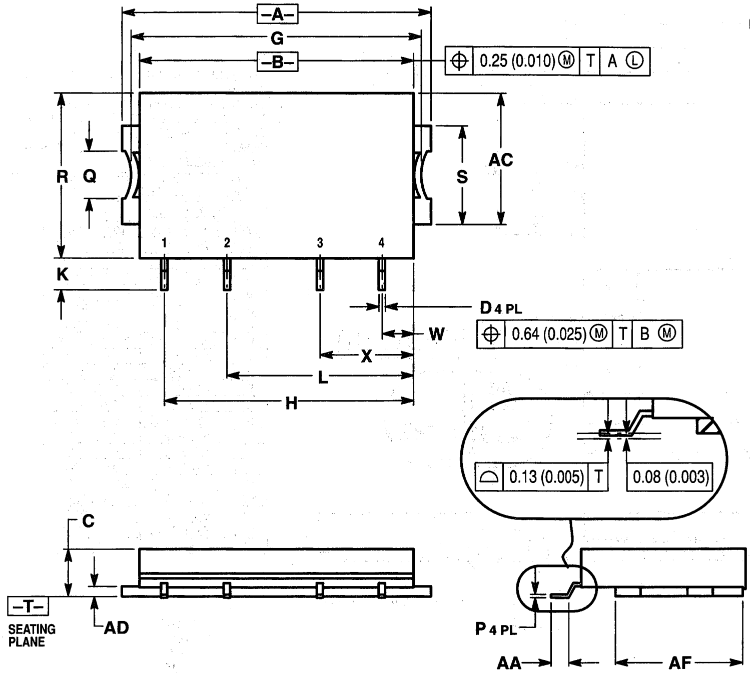
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	—	0.004	—	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

CASE 419B–01
ISSUE G

CASE DIMENSIONS (continued)



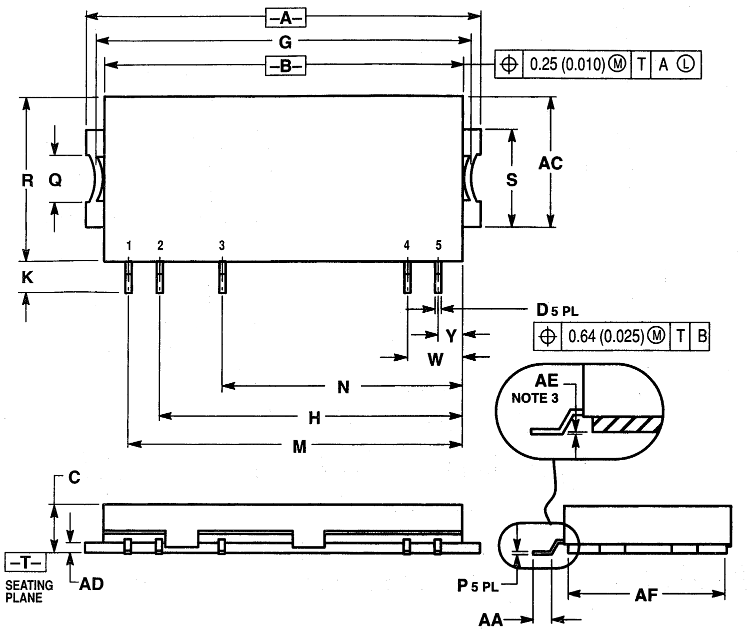
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION AE (PACKAGE COPLANARITY): THE BOTTOM OF THE DEVICE LEADS AND THE REFERENCE PLANE -T- MUST BE COPLANAR WITHIN DIMENSION AE.
4. REF INDICATES NON-CONTROLLED DIMENSION FOR REFERENCE USE ONLY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.68	24.99	0.972	0.984
B	21.84	22.15	0.860	0.872
C	3.63	4.14	0.143	0.163
D	0.43	0.58	0.017	0.023
G	22.48 REF		0.885 REF	
H	20.10 BSC		0.791 BSC	
K	2.11	2.62	0.083	0.103
L	15.10 BSC		0.594 BSC	
P	0.25 REF		0.010 REF	
Q	3.78 REF		0.149 REF	
R	13.06	13.36	0.514	0.526
S	7.95 REF		0.313 REF	
W	2.60 BSC		0.102 BSC	
X	7.60 BSC		0.299 BSC	
AA	1.35	1.70	0.053	0.067
AC	10.49 REF		0.413 REF	
AD	0.81 REF		0.032 REF	
AF	10.24 REF		0.403 REF	

STYLE 1:
PIN 1. P IN
2. VBIAS
3. VDD1, 2, 3
4. P OUT

CASE 420AB–02
ISSUE A

CASE DIMENSIONS (continued)

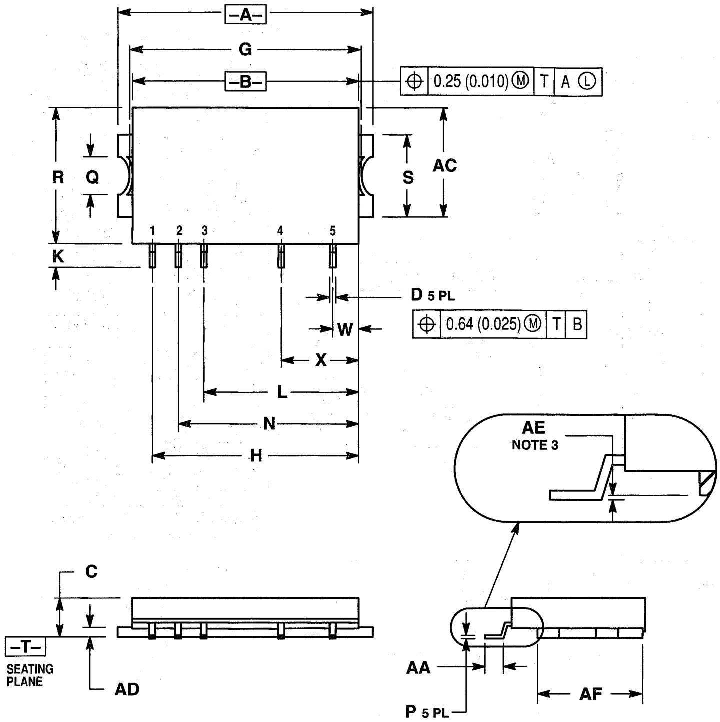


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION AE (PACKAGE COPLANARITY): THE BOTTOM OF THE DEVICE LEADS AND THE REFERENCE PLANE –T– MUST BE COPLANAR WITHIN DIMENSION AE.
4. REF INDICATES NON–CONTROLLED DIMENSION FOR REFERENCE USE ONLY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.75	32.05	1.250	1.262
B	28.85	29.10	1.136	1.146
C	3.70	4.00	0.146	0.157
D	0.43	0.58	0.017	0.023
G	29.60 REF		1.165 REF	
H	24.51 BSC		0.965 BSC	
K	2.10	2.62	0.083	0.103
M	27.00 BSC		1.063 BSC	
N	19.51 BSC		0.768 BSC	
P	0.25 REF		0.010 REF	
Q	3.78 REF		0.149 REF	
R	13.15	13.45	0.518	0.530
S	8.00 REF		0.315 REF	
W	4.50 BSC		0.177 BSC	
Y	1.98 BSC		0.078 BSC	
AA	1.35	1.70	0.053	0.067
AC	10.50 REF		0.413 REF	
AD	0.81 REF		0.032 REF	
AE	+0.050	–0.076	+0.002	–0.003
AF	12.80 REF		0.504 REF	

STYLE 1:
PIN 1. P IN
2. VCONT
3. VDD1
4. VDD2
5. POUT

CASE 420AC–01
ISSUE A

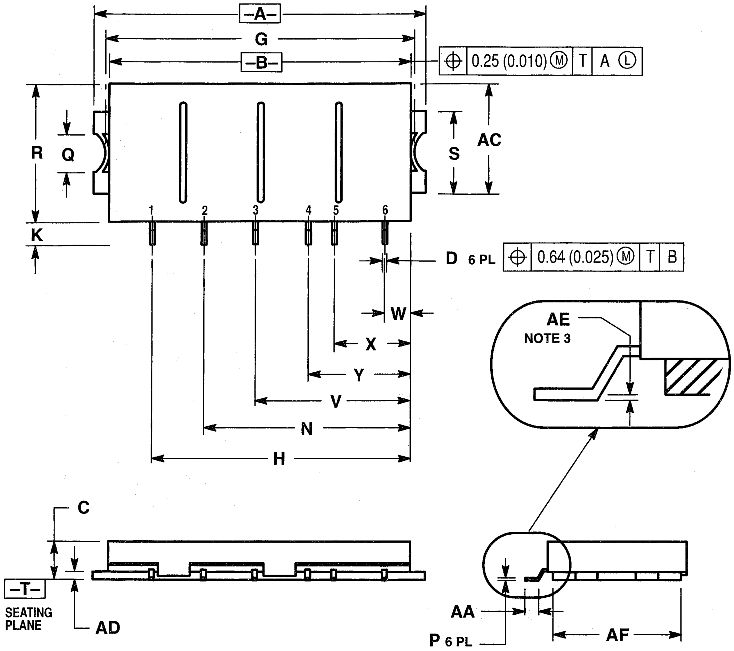


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION AE (PACKAGE COPLANARITY): THE BOTTOM OF THE DEVICE LEADS AND THE REFERENCE PLANE –T– MUST BE COPLANAR WITHIN DIMENSION AE.
4. REF INDICATES NON–CONTROLLED DIMENSION FOR REFERENCE USE ONLY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.68	24.99	0.972	0.984
B	21.87	22.12	0.861	0.871
C	3.63	4.00	0.143	0.157
D	0.43	0.58	0.017	0.023
G	22.48 REF		0.885 REF	
H	20.10 BSC		0.791 BSC	
K	2.11	2.62	0.083	0.103
L	15.10 BSC		0.594 BSC	
N	19.00 BSC		0.748 BSC	
P	0.25 REF		0.010 REF	
Q	3.78 REF		0.149 REF	
R	13.06	13.36	0.514	0.526
S	7.95 REF		0.313 REF	
W	2.60 BSC		0.102 BSC	
X	7.60 BSC		0.299 BSC	
AA	1.35	1.70	0.053	0.067
AC	10.49 REF		0.413 REF	
AD	0.81 REF		0.032 REF	
AE	+0.051	–0.076	+0.002	–0.003
AF	10.24 REF		0.403 REF	

STYLE 1:
PIN 1. P IN
2. VGG1, 2
3. VDD1
4. VDD2
5. P OUT

CASE 420J–03
ISSUE C



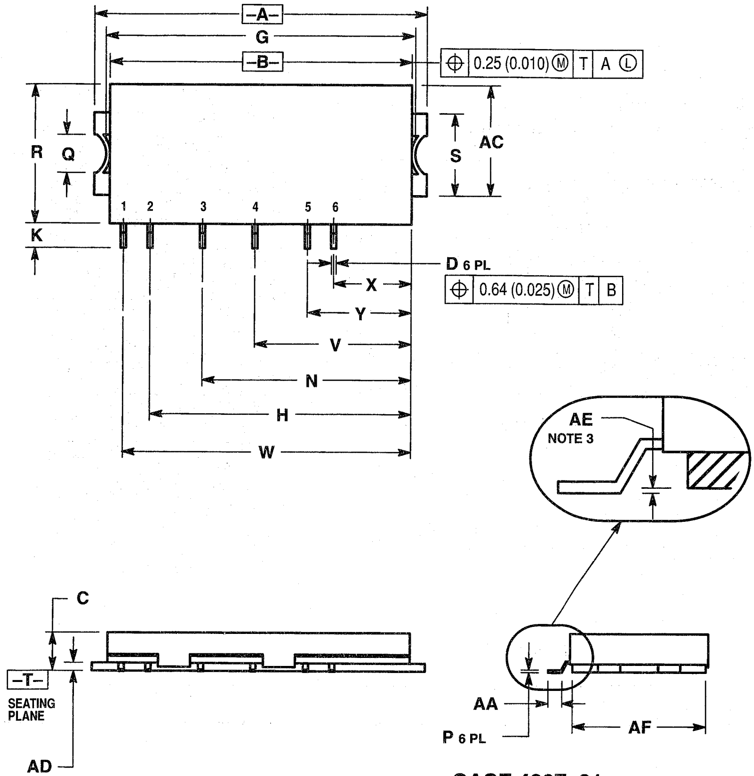
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION AE (PACKAGE COPLANARITY): THE BOTTOM OF THE DEVICE LEADS AND THE REFERENCE PLANE –T– MUST BE COPLANAR WITHIN DIMENSION AE.
4. REF INDICATES NON–CONTROLLED DIMENSION FOR REFERENCE USE ONLY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.75	32.05	1.250	1.262
B	28.85	29.10	1.136	1.146
C	3.70	4.00	0.146	0.157
D	0.43	0.58	0.017	0.023
G	29.60 REF		1.165 REF	
H	25.03 BSC		0.985 BSC	
K	2.10	2.62	0.083	0.103
N	20.03 BSC		0.789 BSC	
P	0.25 REF		0.010 REF	
Q	3.78 REF		0.149 REF	
R	13.15	13.45	0.518	0.530
S	8.00 REF		0.315 REF	
V	15.03 BSC		0.595 BSC	
W	2.53 BSC		0.100 BSC	
X	7.53 BSC		0.297 BSC	
Y	10.03 BSC		0.395 BSC	
AA	1.35	1.70	0.053	0.067
AC	10.50 REF		0.413 REF	
AD	0.81 REF		0.032 REF	
AE	+0.050	–0.076	+0.002	–0.003
AF	12.80 REF		0.504 REF	

STYLE 1:
PIN 1. RF INPUT POWER /V_{CONT}
2. VDD1
3. V_{BIAS}
4. VDD2
5. VDD3
6. RF OUTPUT
CASE: GROUND

CASE 420L–03
ISSUE C

CASE DIMENSIONS (continued)



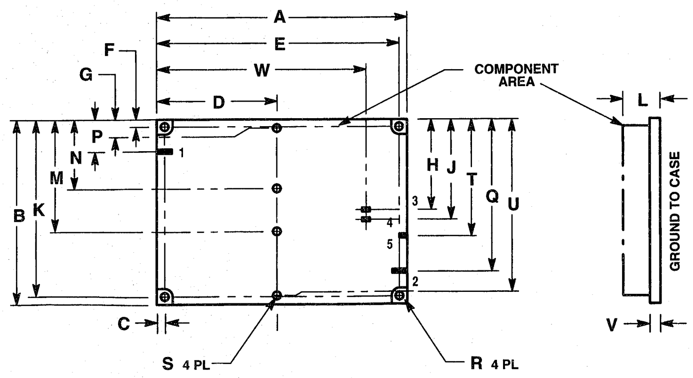
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION AE (PACKAGE COPLANARITY): THE BOTTOM OF THE DEVICE LEADS AND THE REFERENCE PLANE –T– MUST BE COPLANAR WITHIN DIMENSION AE.
4. REF INDICATES NON–CONTROLLED DIMENSION FOR REFERENCE USE ONLY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.75	32.05	1.250	1.262
B	28.85	29.10	1.136	1.146
C	3.70	4.00	0.146	0.157
D	0.43	0.58	0.017	0.023
G	29.60 REF		1.165 REF	
H	25.03 BSC		0.985 BSC	
K	2.10	2.62	0.083	0.103
N	20.03 BSC		0.789 BSC	
P	0.25 REF		0.010 REF	
Q	3.78 REF		0.149 REF	
R	13.15	13.45	0.518	0.530
S	8.00 REF		0.315 REF	
V	15.03 BSC		0.592 BSC	
W	27.53 BSC		1.084 BSC	
X	7.53 BSC		0.297 BSC	
Y	10.03 BSC		0.395 BSC	
AA	1.35	1.70	0.053	0.067
AC	10.50 REF		0.413 REF	
AD	0.81 REF		0.032 REF	
AE	+0.050	–0.076	+0.002	–0.003
AF	12.80 REF		0.504 REF	

STYLE 1:
PIN 1. RF INPUT POWER
2. VDD1
3. Vbias
4. VDD2
5. VDD3
6. RF OUTPUT
CASE: GROUND

CASE 420Z–01
ISSUE O

CASE DIMENSIONS (continued)

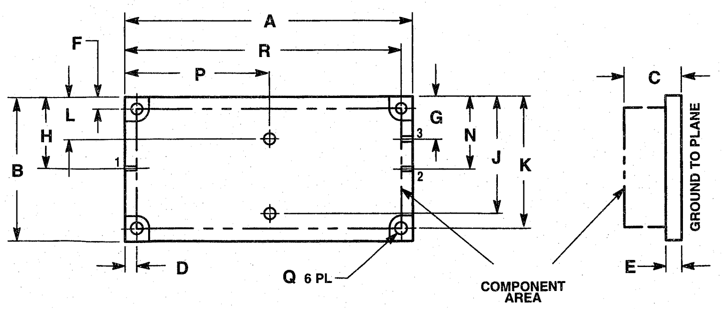


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	114.88	115.12	4.523	4.532
B	84.88	85.12	3.342	3.351
C	3.40	3.60	0.134	0.142
D	54.70	54.90	2.154	2.161
E	111.40	111.60	4.386	4.394
F	3.40	3.60	0.134	0.142
G	4.00	4.20	0.157	0.165
H	39.90	40.70	1.571	1.602
J	44.30	45.10	1.744	1.776
K	81.40	81.60	3.205	3.213
L	—	17.00	—	0.669
M	51.80	52.00	2.039	2.047
N	33.00	33.20	1.229	1.307
P	14.60	15.40	0.575	0.606
Q	69.60	70.40	2.740	2.772
R	3.40	3.70	0.134	0.146
S	3.00	3.30	0.118	0.130
T	53.50	54.30	2.106	2.138
U	80.80	81.00	3.181	3.189
V	4.50	4.90	0.177	0.193
W	95.80	96.60	3.772	3.803

STYLE 1:
PIN 1. RF INPUT
2. RF OUTPUT
3. $+V_{CC}1$
4. $+V_{CC}2$
5. RF DETECTION GROUND TO CASE

CASE 429C–03
ISSUE B

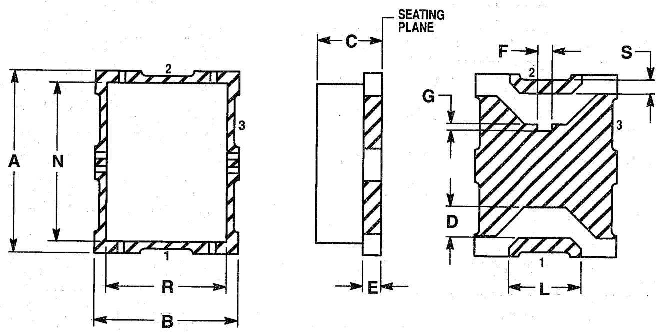


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	3.342	3.351	84.88	85.12
B	1.669	1.678	42.38	42.62
C	—	0.669	—	17.00
D	0.124	0.132	3.15	3.35
E	0.177	0.193	4.50	4.90
F	0.124	0.132	3.15	3.35
G	0.476	0.508	12.10	12.90
H	0.909	0.941	23.10	23.90
J	1.354	1.362	34.40	34.60
K	1.541	1.549	39.15	39.35
L	0.488	0.496	12.40	12.60
N	0.909	0.941	23.10	23.90
P	1.569	1.577	39.85	40.05
Q	0.122	0.134	3.10	3.40
R	3.215	3.222	81.65	81.85

STYLE 1:
PIN 1. RF INPUT
2. RF OUTPUT
3. $+V_{CC}$
GROUND TO CASE

CASE 429E–01
ISSUE O

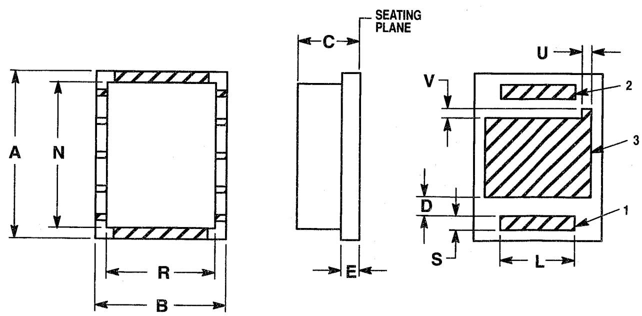


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.260	0.270	6.60	6.86
B	0.200	0.210	5.08	5.33
C	0.090	0.104	2.29	2.64
D	0.040	0.050	1.02	1.27
E	0.022	0.028	0.56	0.71
F	0.015	0.025	0.38	0.64
G	0.005	0.015	0.13	0.38
L	0.100	0.110	2.54	2.79
N	0.226	0.236	5.74	5.99
R	0.166	0.176	4.22	4.47
S	0.025	0.035	0.64	0.89

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE

CASE 430–01
ISSUE O

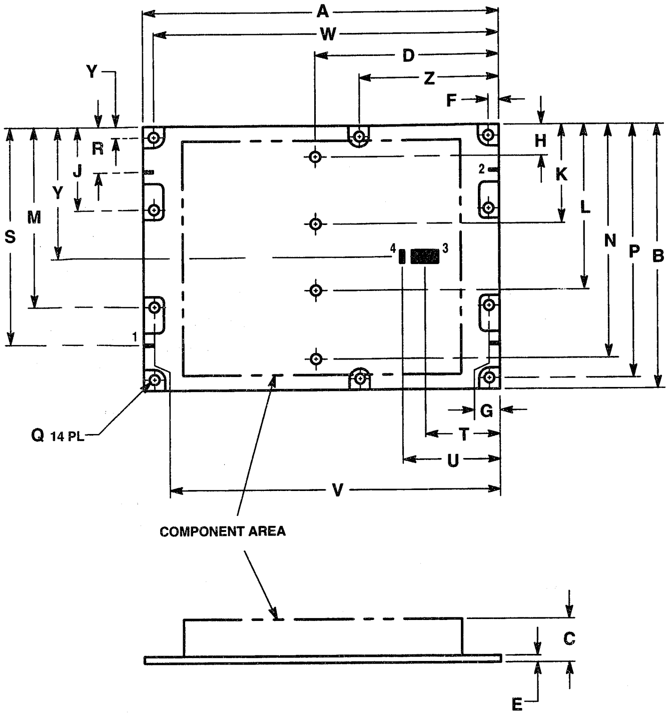


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.260	0.270	6.60	6.86
B	0.200	0.210	5.08	5.33
C	0.090	0.104	2.29	2.64
D	0.020	0.040	0.51	1.02
E	0.022	0.028	0.56	0.71
L	0.115	0.125	2.92	3.18
N	0.226	0.236	5.74	5.99
R	0.166	0.176	4.22	4.47
S	0.019	0.029	0.48	0.74
U	0.010	0.020	0.25	0.51
V	0.010	0.020	0.25	0.51

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

CASE 430B–02
ISSUE A



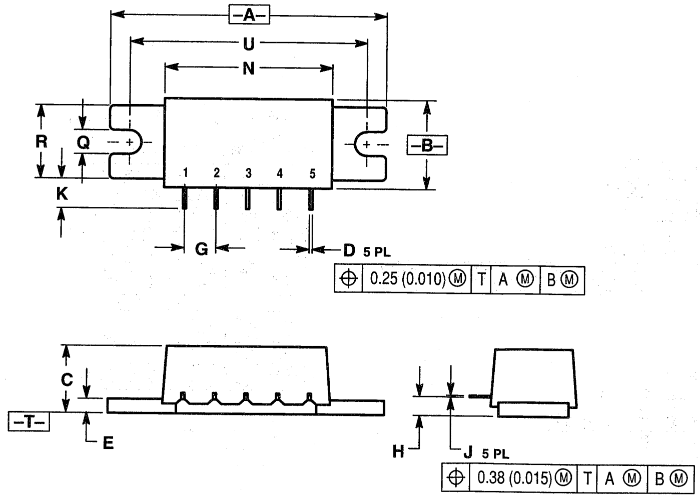
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	114.88	115.12	4.523	4.532
B	84.88	85.12	3.342	3.351
C	—	14.0	—	0.551
D	59.9	60.01	2.358	2.366
E	2.0	2.4	0.079	0.094
F	3.4	3.6	0.134	0.142
G	3.15	3.35	0.124	0.132
H	9.9	10.1	0.390	0.398
J	26.8	27.0	1.055	1.063
K	31.9	32.1	1.256	1.264
L	52.9	53.1	2.083	2.091
M	58.0	58.2	2.283	2.291
N	74.9	75.1	2.949	2.957
P	81.4	81.6	3.205	3.213
Q	3.1	3.4	0.122	0.134
R	14.6	15.4	0.575	0.606
S	69.6	70.4	2.740	2.772
T	24.0	24.8	0.945	0.976
U	31.6	32.4	1.244	1.276
V	111.65	111.85	4.396	4.404
W	111.4	111.6	4.386	4.394
X	3.4	3.6	0.134	0.142
Y	42.1	42.9	1.657	1.689
Z	45.9	46.1	1.807	1.815

STYLE 1:
PIN 1. RF INPUT
2. RF OUTPUT
3. DC VOLTAGE
4. CORRECTION
GROUND TO PLANE

CASE 439–01
ISSUE O

CASE DIMENSIONS (continued)



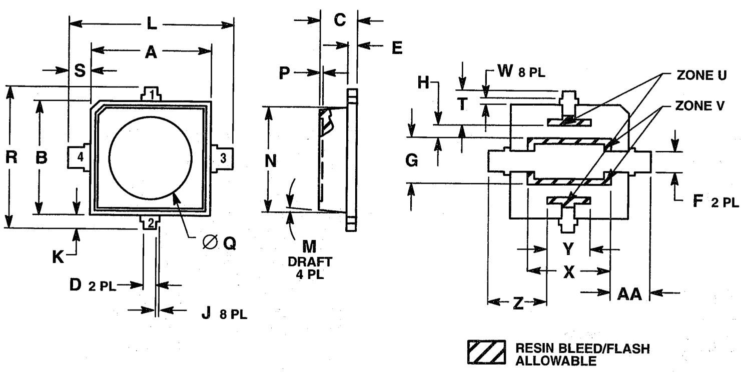
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.740	1.760	44.20	44.70
B	0.550	0.570	13.97	14.49
C	0.405	0.445	10.29	11.30
D	0.018	0.022	0.46	0.55
E	0.085	0.095	2.16	2.41
G	0.200 BSC		5.08 BSC	
H	0.120 BSC		3.05 BSC	
J	0.009	0.011	0.23	0.28
K	0.180	0.220	4.57	5.59
N	1.045	1.075	26.54	27.30
Q	0.145	0.155	3.68	3.94
R	0.455	0.465	11.56	11.81
U	1.490	1.510	37.85	38.35

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. RESISTOR–GROUND
4. VCC
5. RF OUTPUT

STYLE 2:
PIN 1. RF INPUT
2. GROUND
3. VCC1
4. VCC2
5. RF OUTPUT

CASE 448–02
ISSUE A

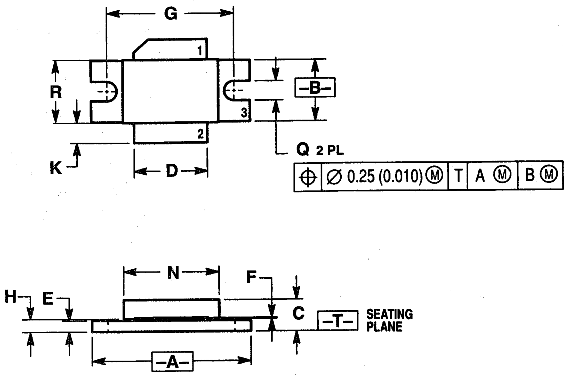


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.185	0.195	4.70	4.95
B	0.175	0.185	4.44	4.70
C	0.058	0.064	1.47	1.63
D	0.017	0.023	0.43	0.58
E	0.014	0.017	0.36	0.43
F	0.027	0.033	0.69	0.84
G	0.071	0.077	1.80	1.96
H	0.017	0.023	0.43	0.58
J	0.000	0.007	0.00	0.18
K	0.018	0.026	0.46	0.66
L	0.253	0.263	6.43	6.68
M	5 °REF		5 °REF	
N	1.75 REF		4.44 REF	
P	0.000	0.006	0.00	0.15
Q	0.120	0.130	3.05	3.30
R	0.220	0.230	5.59	5.84
S	0.030	0.038	0.76	0.97
T	0.050	0.060	1.27	1.52
U	0.000	0.018	0.00	0.46
V	0.000	0.014	0.00	0.36
W	0.004	0.016	0.10	0.41
X	0.131	0.141	3.33	3.58
Y	0.065	0.075	1.65	1.90
Z	0.089	0.099	2.26	2.51
AA	0.056	0.066	1.42	1.67

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. SOURCE

CASE 449–02
ISSUE A

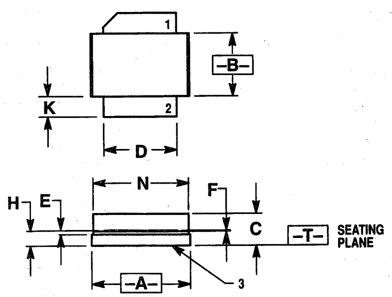


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.995	1.005	25.27	25.53
B	0.380	0.390	9.65	9.91
C	0.170	0.205	4.32	5.21
D	0.455	0.465	11.56	11.81
E	0.060	0.075	1.52	1.91
F	0.004	0.006	0.10	0.15
G	0.800 BSC		20.32 BSC	
H	0.078	0.090	1.98	2.29
K	0.117	0.137	2.97	3.48
N	0.595	0.605	15.11	15.37
Q	0.120	0.130	3.05	3.30
R	0.395	0.410	10.03	10.41

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

CASE 451–04
ISSUE D

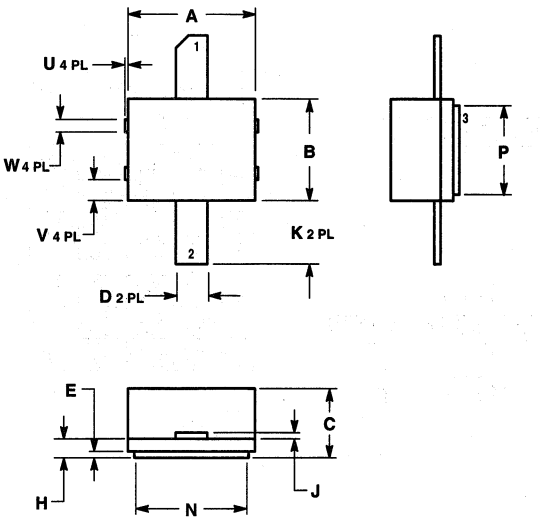


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.615	0.625	15.62	15.88
B	0.395	0.410	10.03	10.41
C	0.170	0.205	4.32	5.21
D	0.455	0.465	11.56	11.81
E	0.060	0.075	1.52	1.91
F	0.004	0.006	0.10	0.15
H	0.078	0.090	1.98	2.29
K	0.117	0.137	2.97	3.48
N	0.595	0.605	15.11	15.37

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

CASE 451A–01
ISSUE O

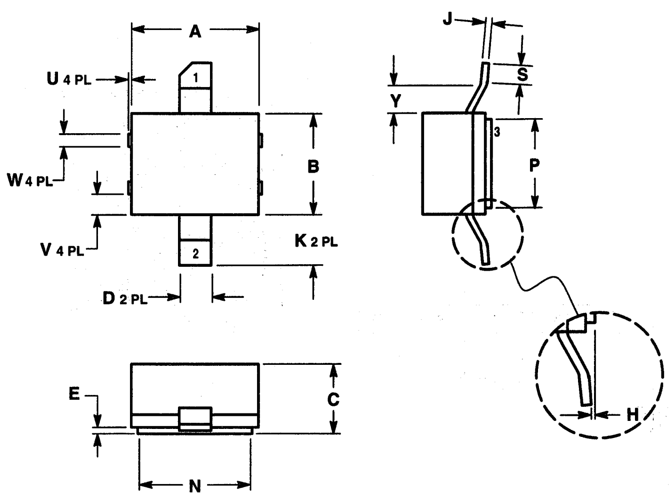


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.197	0.203	5.00	5.16
B	0.157	0.163	3.99	4.14
C	0.085	0.110	2.16	2.79
D	0.047	0.053	1.19	1.35
E	0.006	0.010	0.15	0.25
H	0.025	0.031	0.64	0.79
J	0.006	0.010	0.15	0.25
K	0.060	0.100	1.52	2.54
N	0.177	0.183	4.50	4.65
P	0.137	0.143	3.48	3.63
U	0.000	0.005	0.00	0.13
V	0.030	0.040	0.76	1.02
W	0.017	0.023	0.43	0.58

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 458–03
ISSUE C

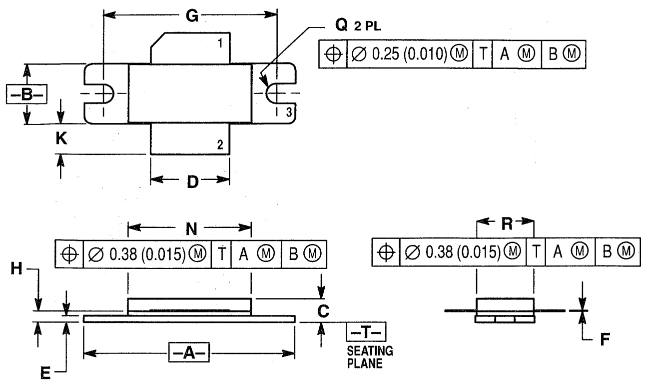


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION –H– (PACKAGE COPLANARITY): THE BOTTOM OF THE LEADS AND REFERENCE PLANE –T– MUST BE COPLANAR WITHIN DIMENSION –H–.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.197	0.203	5.00	5.16
B	0.157	0.163	3.99	4.14
C	0.085	0.110	2.16	2.79
D	0.047	0.053	1.19	1.35
E	0.006	0.010	0.15	0.25
H	0.000	0.004	0.00	0.10
J	0.006	0.010	0.15	0.25
K	0.050	0.080	1.27	2.03
N	0.177	0.183	4.50	4.65
P	0.137	0.143	3.48	3.63
S	0.020	0.040	0.51	1.02
U	0.000	0.005	0.00	0.13
V	0.030	0.040	0.76	1.02
W	0.017	0.023	0.43	0.58
Y	0.030	0.040	0.76	1.02

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 458A–01
ISSUE O

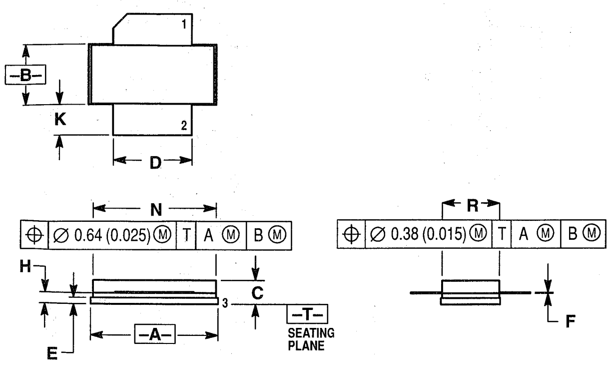


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.050	0.070	1.27	1.78
K	0.170	0.210	4.32	5.33
N	0.775	0.785	19.69	19.94
Q	0.118	0.138	3.00	3.51
R	0.365	0.375	9.27	9.53

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465–01
ISSUE O



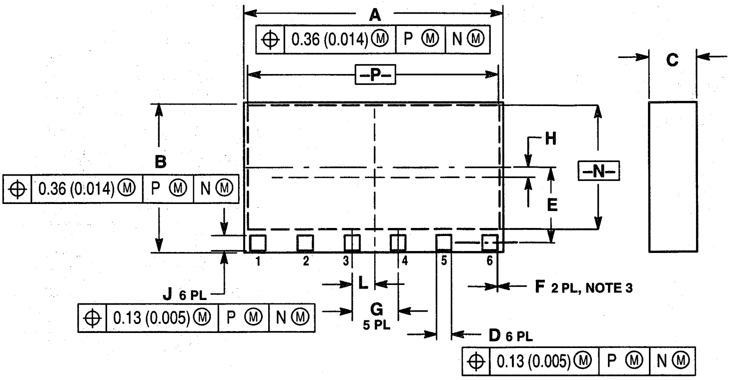
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.050	0.070	1.27	1.78
K	0.170	0.210	4.32	5.33
N	0.775	0.785	19.69	19.94
R	0.365	0.375	9.27	9.53

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465A–01
ISSUE O

CASE DIMENSIONS (continued)

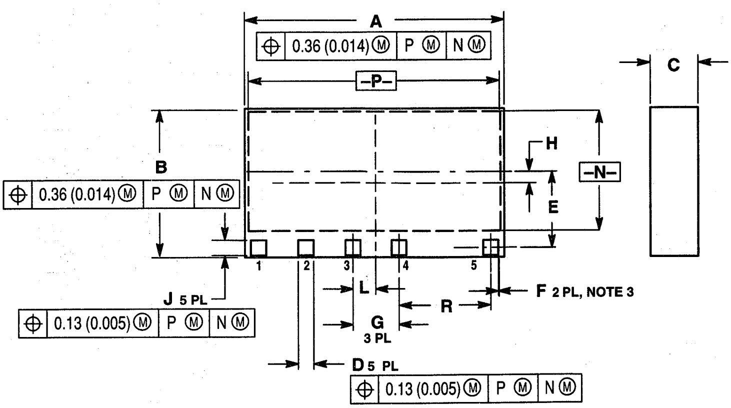


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. PADS 1 AND 6 HAVE EXTENDED METAL ON THE OUTER EDGES ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.545	0.555	13.84	14.10
B	0.310	0.320	7.87	8.13
C	0.088	0.108	2.25	2.75
D	0.033	0.037	0.84	0.94
E	0.159 BSC		4.04 BSC	
F	0.004 REF		0.10 REF	
G	0.0984 BSC		2.50 BSC	
H	0.0215 BSC		0.55 BSC	
J	0.028	0.032	0.71	0.81
L	0.0492 BSC		1.25 BSC	
N	0.256	0.260	6.50	6.60
P	0.534	0.538	13.56	13.66

STYLE 1:
PIN 1. RFin
2. Vcont
3. Vdd1
4. Vbias
5. Vdd2
6. RFout

CASE 467–03
ISSUE D

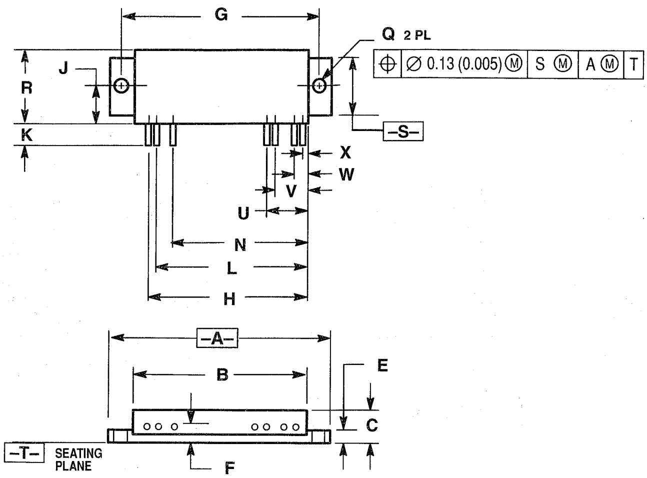


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. PADS 1 AND 5 HAVE EXTENDED METAL ON THE OUTER EDGES ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.545	0.555	13.84	14.10
B	0.310	0.320	7.87	8.13
C	0.083	0.113	2.10	2.87
D	0.033	0.037	0.84	0.94
E	0.161 BSC		4.09 BSC	
F	0.004 REF		0.10 REF	
G	0.0984 BSC		2.50 BSC	
H	0.0238 BSC		0.60 BSC	
J	0.028	0.032	0.71	0.81
L	0.0492 BSC		1.25 BSC	
N	0.250	0.254	6.35	6.45
P	0.534	0.538	13.56	13.66
R	0.1968 BSC		5.00 BSC	

STYLE 1:
PIN 1. RFin
2. Vcont
3. Vdd
4. Vbias
5. RFout

CASE 467A–03
ISSUE C

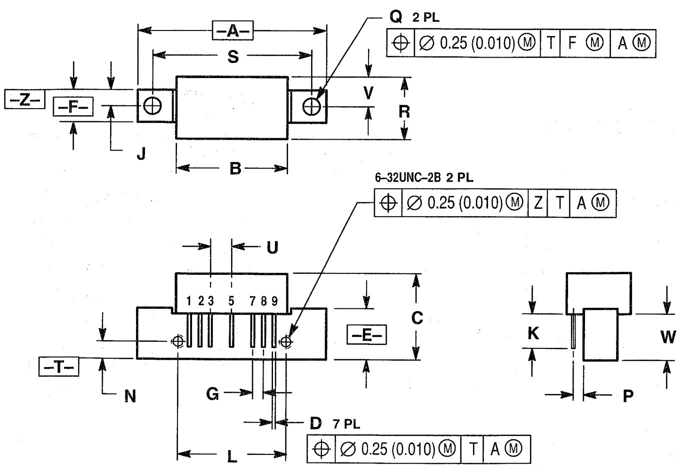


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.640	2.660	67.06	67.56
B	2.040	2.085	51.82	52.95
C	0.335	0.360	8.51	9.14
E	0.100	0.115	2.54	2.92
F	0.085	0.115	2.16	2.92
G	2.405 BSC		61.09 BSC	
H	1.885	1.915	47.88	48.64
J	0.400	0.440	10.16	11.18
K	0.230	0.300	5.85	7.62
L	1.785	1.815	45.34	46.10
N	1.585	1.615	40.26	41.02
Q	0.136	0.146	3.46	3.70
R	0.800	0.820	20.32	20.82
S	0.670	0.690	17.02	17.52
U	0.485	0.515	12.32	13.08
V	0.385	0.415	9.78	10.54
W	0.185	0.215	4.70	5.46
X	0.085	0.115	2.16	2.92

STYLE 2:
PIN 1. RF OUTPUT
2. GROUND
3. Vs 2
4. GROUND
5. Vs 1
6. GROUND
7. RF INPUT

CASE 700–04
ISSUE F



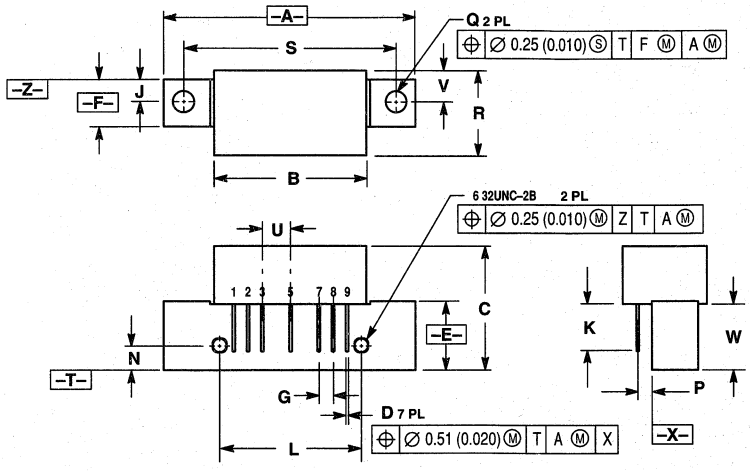
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	1.775	—	45.08
B	—	1.085	—	27.56
C	—	0.840	—	21.34
D	0.018	0.022	0.46	0.56
E	0.465	0.510	11.81	12.95
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.315	0.355	8.00	8.50
L	1.00 BSC		25.40 BSC	
N	0.165 BSC		4.10 BSC	
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	—	0.595	—	15.11
S	1.500 BSC		38.10 BSC	
U	0.200 BSC		5.08 BSC	
V	0.280 BSC		7.11 BSC	
W	0.435	0.450	11.05	11.43

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 714–06
ISSUE K

CASE DIMENSIONS (continued)

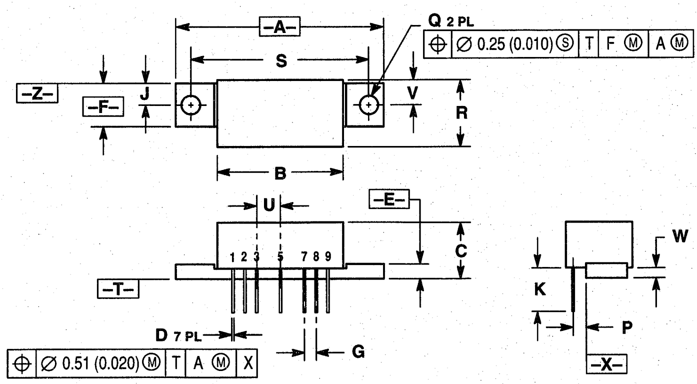


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	1.775	—	45.08
B	—	1.085	—	27.56
C	—	0.870	—	22.10
D	0.018	0.022	0.46	0.56
E	0.465	0.510	11.81	12.95
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.330	0.370	8.38	9.40
L	1.000 BSC		25.40 BSC	
N	0.165 BSC		4.19 BSC	
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	—	0.595	—	15.11
S	1.500 BSC		38.10 BSC	
U	0.200 BSC		5.08 BSC	
V	0.209	0.239	5.31	6.07
W	0.425	—	10.80	—

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
5. $+V_{CC}$
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 714F–03
ISSUE C



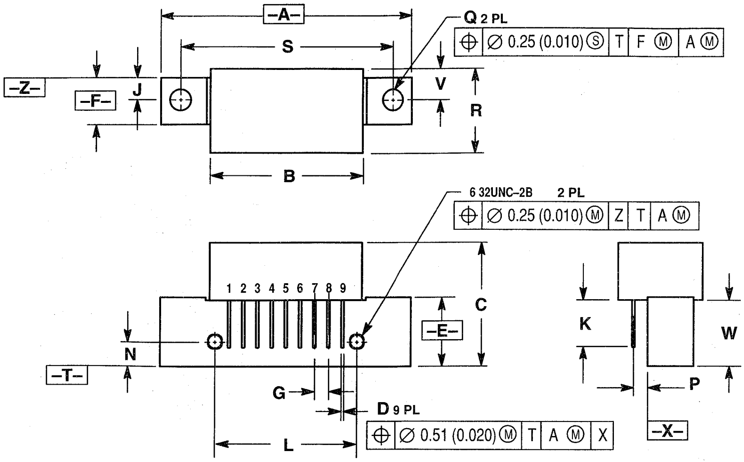
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	1.775	—	45.08
B	—	1.085	—	27.56
C	—	0.495	—	12.57
D	0.018	0.022	0.46	0.56
E	0.120	0.130	3.05	3.30
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.330	0.370	8.38	9.40
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	—	0.595	—	15.11
S	1.500 BSC		38.10 BSC	
U	0.200 BSC		5.08 BSC	
V	0.209	0.239	5.31	6.07
W	0.050	—	1.27	—

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
5. +VCC
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 714G–03
ISSUE D

CASE DIMENSIONS (continued)



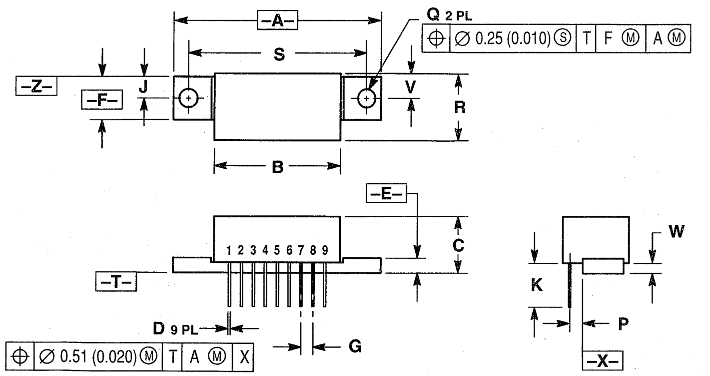
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	1.775	—	45.08
B	—	1.085	—	27.56
C	—	0.870	—	22.10
D	0.018	0.022	0.46	0.56
E	0.465	0.510	11.81	12.95
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.330	0.370	8.38	9.40
L	1.000 BSC		25.40 BSC	
N	0.165 BSC		4.19 BSC	
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	—	0.595	—	15.11
S	1.500 BSC		38.10 BSC	
V	0.209	0.239	5.31	6.07
W	0.425	—	10.80	—

STYLE 2:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. RESISTOR-GROUND
5. GROUND
6. GROUND
7. GROUND
8. V_{CC} 1
9. RF OUTPUT

STYLE 3:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. V_{CC} 1
5. GROUND
6. GROUND
7. GROUND
8. V_{CC} 2
9. RF OUTPUT

CASE 714P–03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

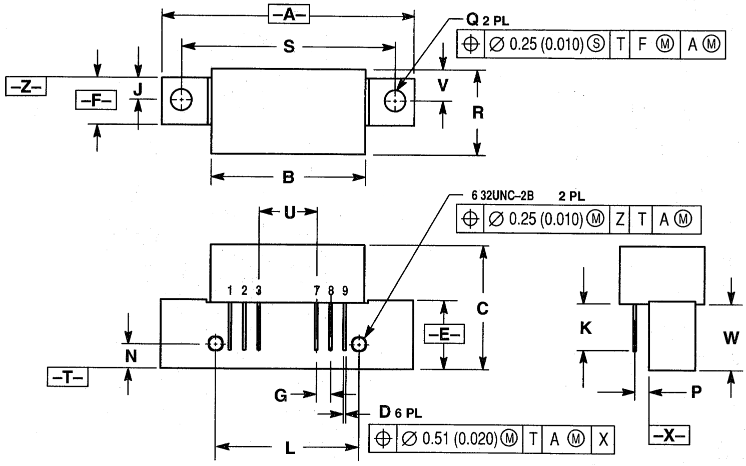
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	—	1.775	—	45.08
B	—	1.085	—	27.56
C	—	0.495	—	12.57
D	0.018	0.022	0.46	0.56
E	0.120	0.130	3.05	3.30
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.330	0.370	8.38	9.40
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	—	0.595	—	15.11
S	1.500 BSC		38.10 BSC	
V	0.209	0.239	5.31	6.07
W	0.050	—	1.27	—

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. RESISTOR-GROUND
5. GROUND
6. GROUND
7. GROUND
8. V_{CC} 1
9. RF OUTPUT

STYLE 2:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. V_{CC} 1
5. GROUND
6. GROUND
7. GROUND
8. V_{CC} 2
9. RF OUTPUT

CASE 714T–03
ISSUE B

CASE DIMENSIONS (continued)

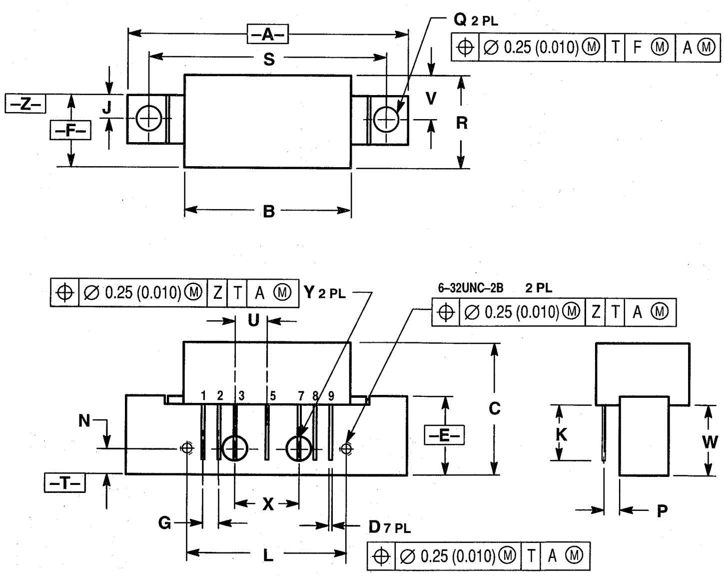


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	—	1.775	—	45.08
B	—	1.085	—	27.56
C	—	0.870	—	22.10
D	0.018	0.022	0.46	0.56
E	0.465	0.510	11.81	12.95
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.330	0.370	8.38	9.40
L	1.000 BSC		25.40 BSC	
N	0.165 BSC		4.19 BSC	
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	—	0.595	—	15.11
S	1.500 BSC		38.10 BSC	
R	0.400 BSC		10.16 BSC	
V	0.209	0.239	5.31	6.07
W	0.425	—	10.80	—

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 714V–01
ISSUE O



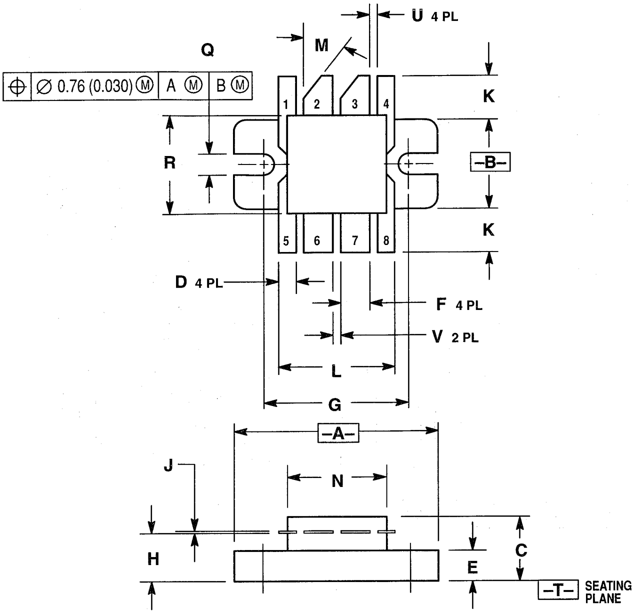
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	—	1.775	—	45.08
B	—	1.085	—	27.56
C	—	0.840	—	21.34
D	0.018	0.022	0.46	0.56
E	0.465	0.510	11.81	12.95
F	0.300	0.325	7.62	8.25
G	0.100 BSC		2.54 BSC	
J	0.156 BSC		3.96 BSC	
K	0.315	0.355	8.00	8.50
L	1.00 BSC		25.40 BSC	
N	0.165 BSC		4.19 BSC	
P	0.100 BSC		2.54 BSC	
Q	0.148	0.168	3.76	4.27
R	—	0.600	—	15.24
S	1.500 BSC		38.10 BSC	
U	0.200 BSC		5.08 BSC	
V	—	0.250	—	6.35
W	0.435	0.450	11.05	11.43
X	0.400 BSC		10.16 BSC	
Y	0.152	0.163	3.85	4.15

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 714Y–02
ISSUE B

CASE DIMENSIONS (continued)



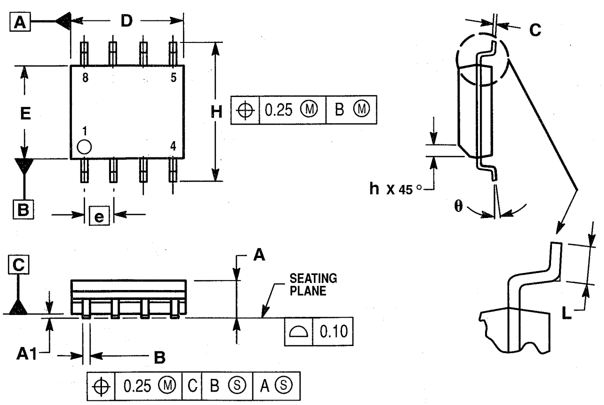
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

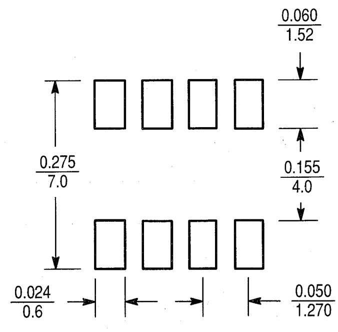
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.60	23.11	0.890	0.910
B	9.52	10.03	0.375	0.395
C	6.65	7.16	0.262	0.282
D	1.60	1.95	0.063	0.077
E	2.94	3.40	0.116	0.134
F	2.87	3.22	0.113	0.127
G	16.51 BSC		0.650 BSC	
H	4.01	4.36	0.158	0.172
J	0.07	0.15	0.003	0.006
K	4.34	4.90	0.171	0.193
L	12.45	12.95	0.490	0.510
M	45° NOM		45° NOM	
N	1.051	11.02	0.414	0.434
Q	3.04	3.35	0.120	0.132
R	9.90	10.41	0.390	0.410
U	1.02	1.27	0.040	0.050
V	0.64	0.89	0.025	0.035

STYLE 1:
PIN 1. EMITTER (COMMON)
2. COLLECTOR
3. COLLECTOR
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE
7. BASE
8. EMITTER (COMMON)

STYLE 2:
PIN 1. SOURCE (COMMON)
2. DRAIN
3. DRAIN
4. SOURCE (COMMON)
5. SOURCE (COMMON)
6. GATE
7. GATE
8. SOURCE (COMMON)

CASE 744A–01
ISSUE C





SO–8 FOOTPRINT (inches / mm)

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

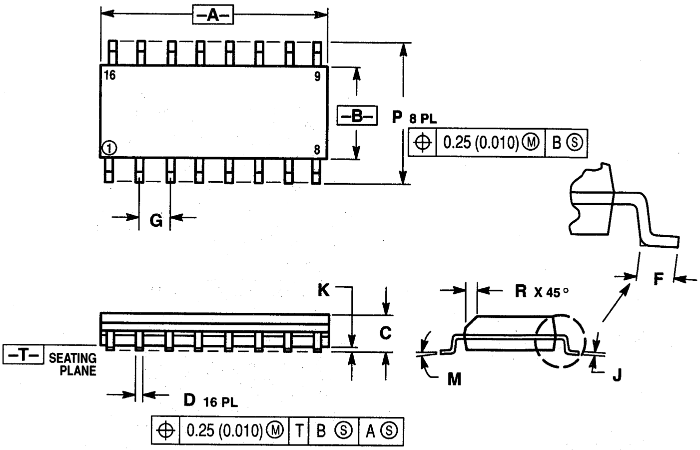
STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

CASE 751–05
ISSUE S

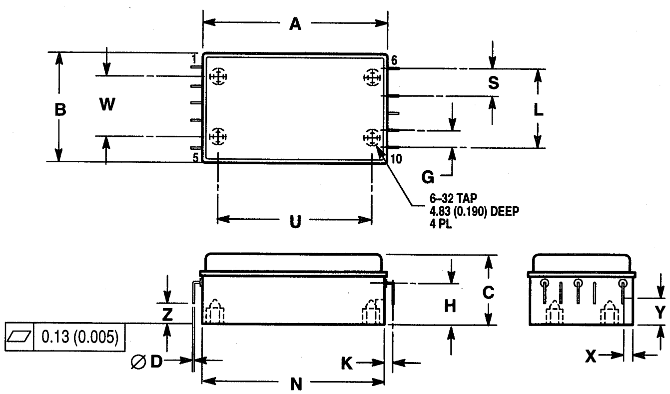
CASE DIMENSIONS (continued)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751B–05
ISSUE J

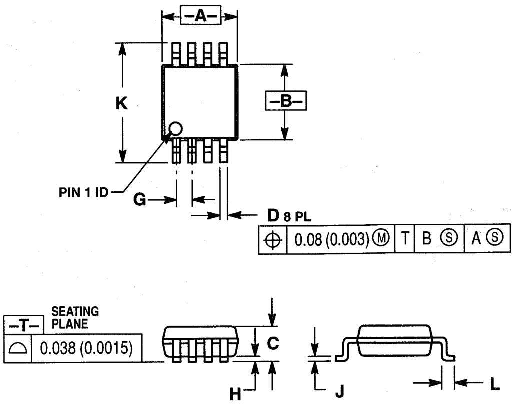


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.107	2.165	53.52	55.00
B	1.225	1.265	31.12	32.13
C	0.805	0.845	20.45	21.46
D	0.018	0.022	0.46	0.56
G	0.190	0.210	4.83	5.33
H	0.490	0.510	12.45	12.95
K	0.100	0.120	2.54	3.05
L	0.910	0.930	23.12	23.62
N	2.053	2.083	52.15	52.90
S	0.310	0.330	7.87	8.38
U	1.785	1.815	45.34	46.10
W	0.690	0.710	17.53	18.03
X	0.090	0.110	2.29	2.79
Y	0.290	0.310	7.37	7.87
Z	0.230	0.270	5.84	6.86

STYLE 2:
PIN 1. 24 V
2. GROUND
3. INPUT
4. GROUND
5. N/C
6. N/C
7. GROUND
8. OUTPUT
9. GROUND
10. 24 V

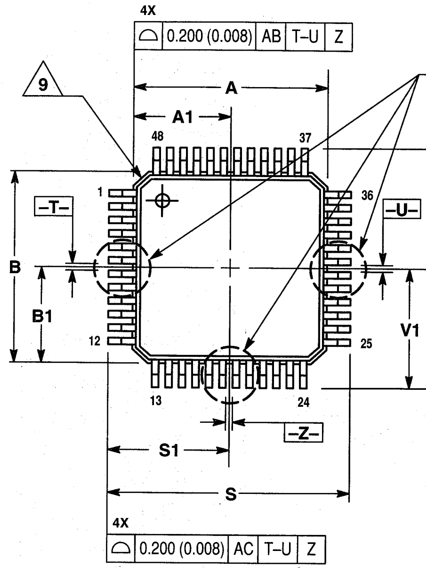
CASE 825A–03
ISSUE C

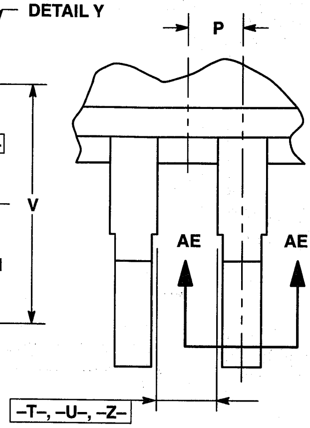


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

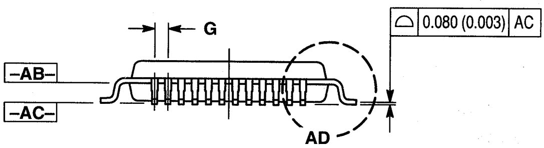
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	—	1.10	—	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

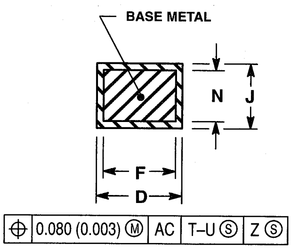
CASE 846A–02
ISSUE D
(Micro–8)



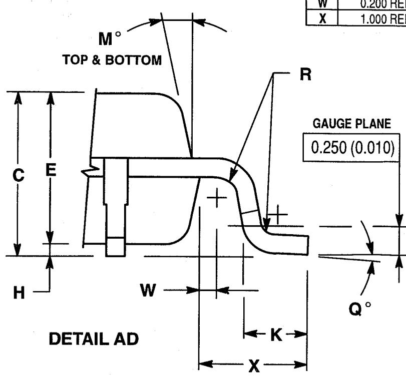


DETAIL Y





SECTION AE–AE

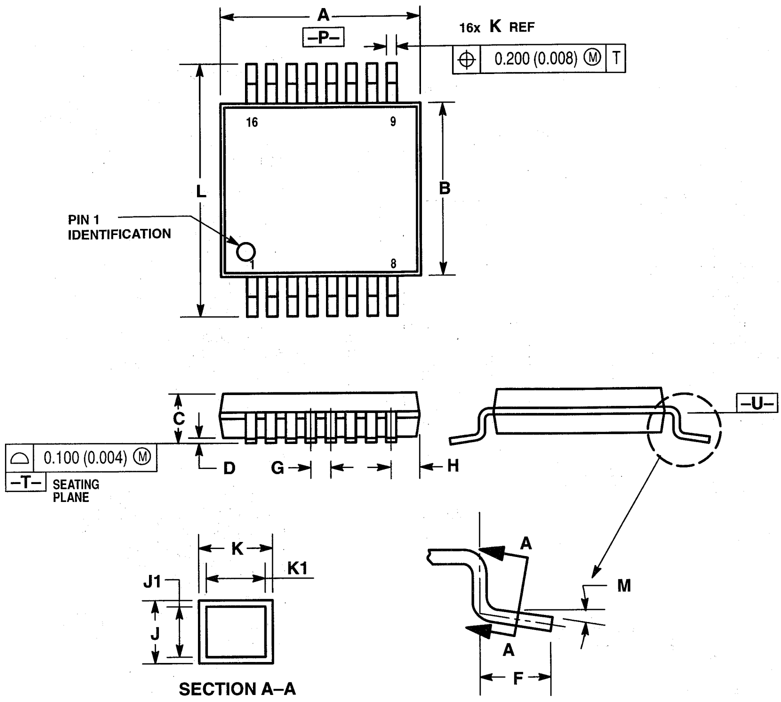


DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12 °REF		12 °REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

CASE 932–02
ISSUE D
(TQFP–48)

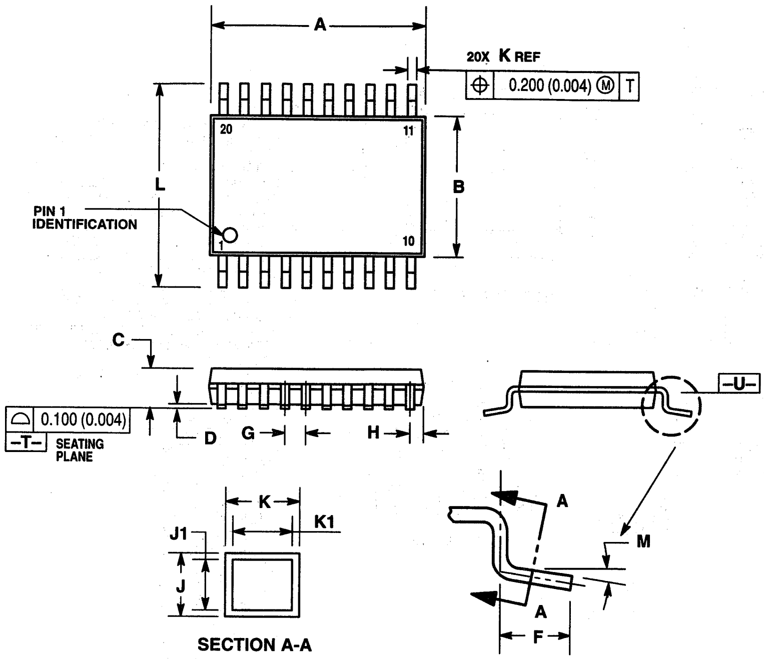


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –U–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	5.10	—	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.22	0.23	0.009	0.010
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

CASE 948C–03
ISSUE B
(TSSOP–16)

CASE DIMENSIONS (continued)

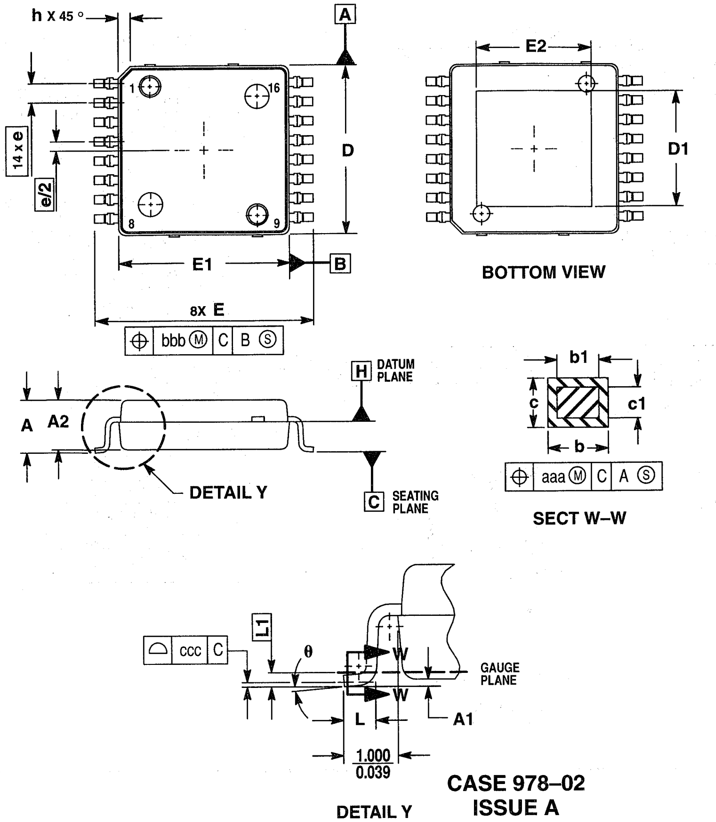


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –U–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	6.60	—	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.275	0.375	0.011	0.015
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

CASE 948D–03
ISSUE B
(TSSOP–20)

CASE DIMENSIONS (continued)



CASE 978–02
ISSUE A
(PFP–16)

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.350
A1	0.025	0.152
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	—	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

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